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Virtual Variable Sampling Repetitive Control of Single-phase DC/AC PWM Converters

Zhichao Liu, *Student Member*, *IEEE*, Bin Zhang, *Senior Member*, *IEEE*, Keliang Zhou, *Senior Member*, *IEEE*, Yongheng Yang, *Senior Member*, *IEEE* and Jingcheng Wang

***Abstract*—Repetitive control (RC) presents an attractive solution to achieve low steady-state tracking error and total harmonic distortion (THD) for periodic signals. For conventional RC (CRC), it requires that the ratio of reference signal period to the fixed sampling period to be an integer. Therefore, the reference signal with variable frequency or a fractional period ratio will lead to severe performance degradation. Although existing hardware variable sampling rate methods enable CRC to be frequency adaptive, the variable sampling frequency will also influence the overall system stability, and they need that the CPU has variable sampling frequency ability. In this paper, a flexible and easy-to-implement method, virtual variable sampling (VVS), is proposed to enable RC to be frequency adaptive. The proposed VVS method, which creates a virtual delay unit to approximate each variable sampling delay, achieves a flexible variable sampling as similar as hardware-based variable sampling, but it does not influence overall system sampling frequency and stability. Experimental results of a single phase DC/AC converter system are presented to show the effectiveness of the proposed VVS-RC.**

***Index Terms*—Virtual variable sampling, repetitive control, phase lead compensation, fractional delay length, DC/AC converter, total harmonic distortion**

I. Introduction

Repetitive control is widely used in dealing with periodic signals including tracking periodic references and rejecting periodic disturbances. The periodic nature of power source signals makes RC an effective approach to maintain and improve the quality of power supplies with excellent waveform and low THD [1]–[6]. Therefore, RC has been effectively used in the applications of power converters [7]–[12], active power filters [13]–[15], and other industry facilities [16], [17].

For CRC, it requires the unit z^{-N} to provide a time delay that equals to one period of the reference signal. Therefore the delay length N should equal to the ratio of reference period to sampling period [18]. However, an integer delay length N cannot be guaranteed in most existing RC works especially when the reference signal is under the influence of frequency fluctuation. Some examples are listed as follows: (1) The reference period is not an integral multiple of sampling period [19]. When a 60 Hz reference AC voltage signal is sampled with a sampling frequency of 10 kHz, the ratio equals to 166.67; (2) For renewable energy based micro-grid system, the unstable energy output from wind or photo-voltaic generator can easily lead to a sudden power imbalance or a large frequency fluctuation [20]. For example, 1 Hz frequency fluctuation for a 60 Hz micro-grid system will result in the ratio changes from 163.9 to 169.5 accordingly. (3) New generation aircraft power systems require a variable-frequency supply, generally in the range of 360-900 Hz [21], [22]. The reference frequency of the bus-connected converters and active filters varies with the frequency of the power system. The RC cannot maintain a fixed delay length N when the reference frequency is changing. Inaccurate delay length N will deviate the peak gains of digital RC away from the fundamental and harmonic frequencies, which will reduce harmonics suppression and deteriorate the tracking performance.

Variable sampling/switching period techniques were developed to maintain fixed integer samples per reference period for wind and aircraft power systems [23], [24]. However, it requires that the digital control system has the capability of the variable sampling frequency. In addition, variable sampling frequency method also compromises the overall closed-loop stability [25]. Some other approaches were also proposed to solve similar questions. A parallel structure fractional RC scheme was developed [26] in which a correction factor in complex number is inserted to adjust the poles for each parallel RC controller. Fractional-order delay z^{-N_f} ($N_f \in [0, n]$) is approximated by an n^{th}-order finite impluse response (FIR) filter in [27]–[29]. A linear-phase-lag low-pass filter was designed to compensate the fractional delay length [30]. Although these methods show improvements, novel and generic solutions are needed since the complex correction factor in [26] is difficult to be implemented, the compensation methods in [27]–[29] are only designed to approximate the fractional delay part of the ratio of sampling frequency to reference frequency. If the variable reference frequency leads to fractional-order delay length N_f beyond the range $[0, n]$, the fractional delay method is not able to provide an accurate compensation.

To achieve a generic solution to this problem, this paper proposes a virtual variable sampling RC (VVS-RC) scheme. The VVS approximates a variable sampling period under

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fixed sampling frequency. By setting this flexible VVS period, digital RC is able to maintain an integer delay length N_v under different situations mentioned above by adjusting coefficients in VVS. In this way, VVS method provides a flexible and fundamental solution to the non-integral delay length and frequency adaptive problem for digital RC.

The remainder of this paper is organized as follows: Section II states the frequency sensitivity of CRC, the detail of VVS construction, and VVS-RC structure and its stability analysis; Section III studies the modeling and parameter setting for VVS-RC. Experimental results are presented in Section IV to verify the effectiveness of the VVS-RC method, which is followed by concluding remarks in Section V.

II. Virtual Variable Sampling RC

A. Frequency sensitivity of CRC

Fig. 1 shows a typical digital control system with plug-in CRC controller for a periodic signal reference [31], where $R(z)$ is the periodic reference input with reference fundamental frequency f_r and reference period $T_r = 1/f_r$, $G_c(z)$ is the conventional feedback controller, $G_p(z)$ is the plant model, $D(z)$ is the disturbance, $Y(z)$ is the system output, and system sampling frequency is f_s. Plug-in CRC controller is a feed-forward controller that consists of RC gain K_r, low pass filter $Q(z)$, phase lead filter $G_f(z)$, and period delay z^{-N} in which integral delay length $N = \lfloor T_r/T_s \rceil$ is the nearest integer to the ratio of reference period T_r to the sampling period $T_s = 1/f_s$.

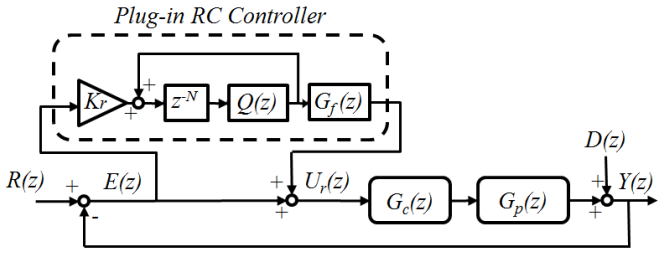

Fig. 1. Control system with plug-in RC controller

The transfer function of the CRC $G_{rc}(z)$ in Fig. 1 is:

$$G_{rc}(z) = \frac{U_r(z)}{E(z)} = K_r \frac{z^{-N}Q(z)}{1 - z^{-N}Q(z)} G_f(z) \qquad (1)$$

where $E(z) = R(z) - Y(z)$ is the system tracking error.

In the frequency domain, RC transfer function in Eq. (1) has infinity magnitude gain at the fundamental and all harmonic frequencies of the reference signal without concerning the low pass filter $Q(z)$. Therefore, RC is able to achieve zero tracking error on the desired frequency and eliminate 2nd and higher order harmonic components to realize zero THD.

However, traditional CRC is very sensitive to reference frequency fluctuation. Even a small frequency fluctuation will lead to severe magnitude decline on the fundamental and all harmonic frequencies. Based on Euler's equation, the magnitude response of RC transfer function Eq. (1) without concerning low pass filter $Q(s)$ is:

$$|G_{rc}(z)| = \frac{K_r}{\sqrt{2 - 2\cos[2\pi h(1 + \Delta f_r/f_r)]}} \qquad (2)$$

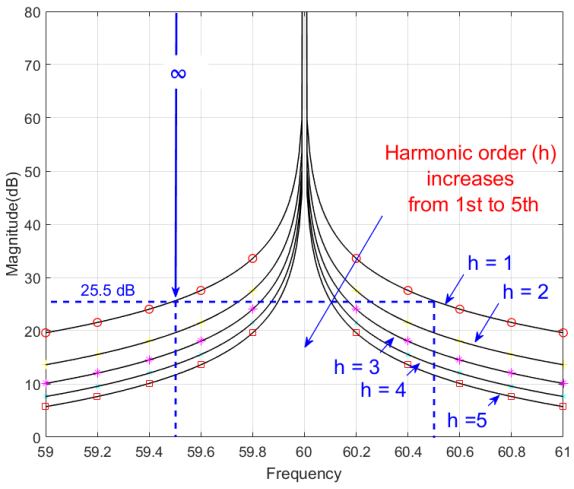

Fig. 2. Sensitivity of RC magnitude to delay length deviation

Note that phase lead compensation $G_f(z) = z^{\gamma}$ with γ being the lead step has been ignored in Eq. (2) because of its unit magnitude. Fig. 2 shows the magnitudes around the first 5th order harmonics ($h = 1, 2, ..., 5$) of the CRC designed for a 60 Hz system. From the figure, the RC magnitude on first harmonic frequency will decrease from infinity to 25.5 dB when the reference frequency deviates 0.5 Hz away from the desired frequency, and this magnitude drop is more obvious for higher order harmonics frequencies. The capabilities of CRC periodic signal tracking and THD elimination will severely degrade under reference frequency fluctuation.

B. Virtual variable sampling

In CRC, delay length N in z^{-N} is assumed to be an integer. However, it's difficult or even impossible to have a constant integral ratio T_r/T_s especially when the reference fundamental frequency f_r is varying or under certain disturbance. A generic way to address this problem is to use a varying sampling frequency scheme [23], [24]. However, the limitations of these varying frequency schemes are their high requirement of CPU processing capacity and the influence on overall system stability.

To overcome the limitations of hardware based variable sampling methods, an easy-to-implement solution based on software signal processing, virtual variable sampling, is proposed in this section. In VVS method, the variable delay period, T_v, is approximated by an nth-order FIR filter, while the overall system sampling period is still a constant value. The Lagrange interpolation polynomial method is applied to make variable delay period approximation:

$$z_v^{-1} = \sum_{i=1}^{n} a_i z^{-i}, \text{with} \quad a_i = \prod_{j=1, j\neq i}^{n} \frac{T_v - iT_s}{jT_s - iT_s} \qquad (3)$$

where T_s is the overall system sampling period. The VVS delay period T_v is able to approximate a variable sampling time delay from T_s to nT_s. Higher order of VVS period provides more approximation accuracy and a larger range, while it also brings more computational cost. With the development

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of CPU computational ability, the computational cost is not the significant restriction for VVS application.

In this paper, the VVS delay order n is selected as 3, which makes T_v is able to approximate the period from T_s to $3T_s$.

$$z_v^{-1} = a_1 z^{-1} + a_2 z^{-2} + a_3 z^{-3} \tag{4}$$

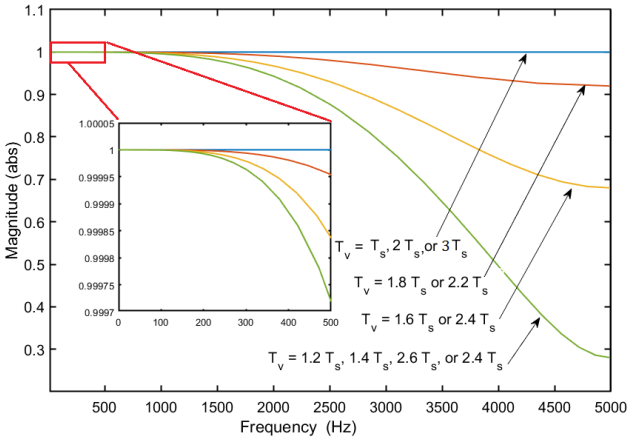

Fig. 3. Magnitude performance of VVS delay unit z_v^{-1} when variable sampling period T_v changes from T_s to $3T_s$

Fig. 3 shows the magnitude of 3rd order VVS delay unit z_v^{-1} when variable sampling period T_v changes from T_s to $3T_s$ under 10 kHz sampling frequency. The unity magnitude means the zero approximation error. Based on Eq. (3), VVS delay unit $z_v^{-1} = z^{-1}, z^{-2}$, or z^{-3} when $T_v = T_s, 2T_s$, or $3T_s$. It is obvious that there is no approximation error when $T_v = T_s, 2T_s$, or $3T_s$. The VVS delay unit performs as a low pass filter property below Nyquist frequency. For the signal with frequency from 0 to 500 Hz, VVS delay unit has the approximation accuracy above 99.97%.

C. Virtual variable sampling RC

To make RC frequency adaptive, VVS method is applied to RC scheme. First, the constant delay length needs to be selected. Suppose the variable reference period $\widetilde{T}_r$ has the range between T_{r_min} and T_{r_max}, and virtual sampling period T_v is between T_s and $3T_s$ when 3rd order VVS method is applied. The delay length N_v should be:

$$\frac{T_{r\_min}}{3T_s} < N_v < \frac{T_{r\_max}}{T_s} \tag{5}$$

Normally, the constant delay length N_v chooses an integer near the middle of the range in Eq. (5) to make VVS RC have the largest frequency adaptability range.

After the delay length N_v is selected, the virtual sampling period T_v under variable reference period $\widetilde{T}_r$ is set as:

$$T_v = \frac{\widetilde{T}_r}{N_v} \tag{6}$$

When reference period $\widetilde{T}_r$ changes or fluctuates, the virtual sampling period T_v needs to be adjusted. The VVS delay unit z_v^{-1} can be determined by Eq. (3) accordingly.

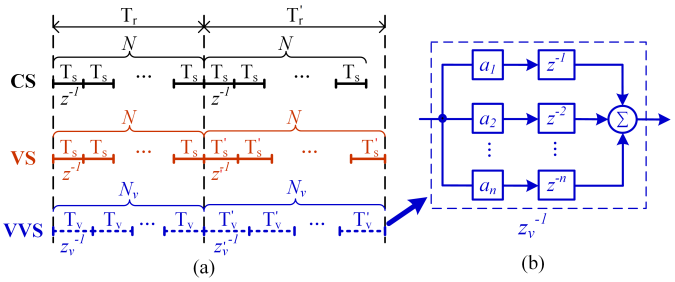

Fig. 4. The sampling comparison among constant sampling, variable sampling, and VVS under a sudden reference period change

The comparison among constant sampling (CS), variable sampling (VS), and VVS are presented in Fig. 4. Repetitive control requires constant sampling points in one reference period, but CS is not able to maintain fixed sampling points when the reference period is changing. When the reference period changes from T_r to T_r', CS cannot provide fixed integer number of delay periods T_s for both periods. By changing sampling periods T_s and T_v, VS and VVS can easily keep the sampling points as a constant number N or N_v. The difference is that the sampling period T_v of VVS is approximated by an FIR filter, which does not require to adjust the physical system sampling frequency.

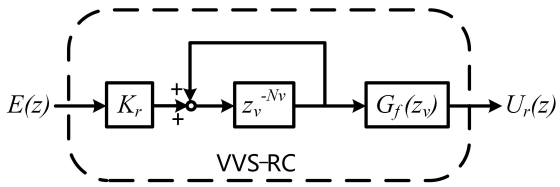

Fig. 5. Virtual variable sampling RC

With the form of VVS delay unit z_v^{-1}, the VVS-RC is shown in Fig. 5 and has the transfer function as:

$$G_{VVS-RC}(z_v) = K_r \frac{z_v^{-N_v}}{1 - z_v^{-N_v}} G_f(z_v) \tag{7}$$

where K_r is the VVS-RC gain and $G_f(z)$ is a phase lead filter to be designed based on the VVS frequency.

Comparing with CRC [31], $z_v^{-N_v}$ has a low pass filter performance as shown in Fig. 3, thus the filter $Q(z)$ in Fig. 1 is no longer needed. In contrast to fractional-order RC [27]–[29], VVS-RC is able to deal with a signal with larger frequency variation range. For instance, a 3rd-order FIR filter in [27]–[29] is able to approximate the fractional delay z^{-N_f} from z^0 to z^{-3}. For a 10 kHz sampling frequency system, it can deal with the reference signal with the frequency from 59.17 Hz to 60.24 Hz when the overall delay range is set from z^{-166} to z^{-169}. On the contrary, for a 10 kHz sampling frequency system, a 3rd-order VVS is able to adjust virtual sampling frequency from 3.33 kHz to 10 kHz, which can deal with the reference signal with the frequency from 41.66 Hz to 125 Hz under a fixed delay z_v^{-80} in RC. The cost of the VVS-RC is that it needs more memory unit than CRC and fractional-order RC. In the case of the prior example, a third order VVS-RC

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takes 50% more computational cost than CRC or fractional-order RC.

Furthermore, the sampling period of input and output is still the system sampling period T_s, while all RC analyses are conducted under the virtual sampling period T_v. Different from multi-rate sampling [8], aliasing and imaging do not exist in VVS. Therefore, there is no need adding anti-aliasing and anti-imaging filters between VVS-based RC with virtual sampling period T_v and digital control system with system sampling period T_s.

D. Fractional-order phase lead compensation

The phase lead compensation is designed to improve the system stability by providing a phase lead to cancel out the system phase lag mainly resulting from system model $G_p(z)$ in Fig. 1 and digital controller computation delay [18]. Theoretically, it can be implemented as the inverse of the closed-loop system model. In practice, it is difficult to obtain the inverse of the closed-loop system model accurately due to various model uncertainties [32], [33].

For accurate phase compensation, a fractional order phase lead (FOPL) filter $G_f(z_v) = z_v^{\gamma}$ is applied, where $\gamma \in \mathbb{R}^+$ can be a fractional number. The FOPL can be approximated by a nth-order filter [34], [35] as:

$$z_v^{\gamma} \approx z_v^{n_i} + \sum_{k=0}^{n} A_k z_v^k \tag{8}$$

where n_i is the nearest integer of $(\gamma - n/2)$. The Lagrange interpolation coefficients A_k which is similar as VVS approximation in Eq. (3) can be calculated as:

$$A_k = \prod_{i=0, i\neq k}^{n} \frac{\gamma - i}{k - i} \tag{9}$$

In practice, the order of phase lead compensation is also selected as $n = 3$ based on the tradeoff between approximation accuracy and computation complication.

With the form of Eq. (8), the FOPL filter produces a linear phase lead:

$$\theta_f = \gamma \times \frac{\omega}{\omega_N} 180^{\circ} \tag{10}$$

for input signal at angular frequency ω, where ω_N is the system Nyquist frequency given by πf_s. Therefore, the FOPL filter can produce higher compensation resolution than an integral-order filter.

E. Stability analysis of VVS-RC

For overall system in Fig. (1) replacing the CRC with VVS-RC of Eq. (7), the error transfer function can be expressed as:

$$E(z) = \frac{(1 - z_v^{-N_v})(1 - G(z))}{1 - z_v^{-N_v}(1 - K_r G_f(z_v) G(z))} \times [R(z) - D(z)] \tag{11}$$

where $G(z) = G_c(z)G_p(z)/[1 + G_c(z)G_p(z)]$ is the closed-loop system transfer function without VVS-RC. The VVS delay $z_v^{-N_v}$ can be approximated as z^{-vN_v}, where the real number v is selected to make $vN_v = T_r/T_s$. Then, the VVS-RC transfer function can be presented as:

$$E(z) = \frac{(1 - z^{-vN_v})(1 - G(z))}{1 - z^{-vN_v}(1 - K_r G_f(z_v) G(z))} \times [R(z) - D(z)] \tag{12}$$

If the frequency of reference $r(t)$ and disturbance $d(t)$ approaches $\omega_l = 2\pi l f_r$ with $l = 0, 1, 2, ...$ and less than the system Nyquist frequency, then $z^{-vN_v} = 1$. The system gets zero tracking error:

$$\lim_{\omega \to \omega_l} \|E(z)\| = 0 \tag{13}$$

Equation (13) indicates that this scheme can suppress all harmonics of the periodic error signal, even in the presence of un-modeled dynamics. The advantage of VVS-RC is that it does not require the sampling frequency to be an integral multiple of the fundamental frequency of the reference signal.

The overall system holds the stability conditions: the closed-loop feedback system $G(z)$ is stable [36], [37], and

$$| 1 - K_r G_f(z) G(z) | < 1 \tag{14}$$

Obviously, stability criteria for the VVS-RC system above is compatible to those of a RC system. The design of control gain K_r and compensation filter $G_f(z_v)$ for the proposed VVS-RC are the same as that for a CRC with fractional-order phase lead [34]:

$$0 < K_r \leq \frac{2cos[(\theta_g(e^{j\omega}) + \gamma\omega]}{N_g(e^{j\omega})} \tag{15}$$

$$| \theta_g(e^{j\omega}) + \gamma\omega | < 90^{\circ} - \varepsilon \tag{16}$$

where N_g and θ_g represent magnitude and phase response of closed-loop transfer function $G(z)$, ε is a small positive constant to enhance the system robustness [18].

III. VVS-RC for Single-phase DC/AC Converter

A. Modeling of the DC/AC PWM converter

Fig. 6 shows a plug-in VVS-RC controlled single-phase DC/AC converter system, where E_n is the DC bus voltage; L and C are inductor-capacitor (LC) filter; R is linear load; C_r, L_r, and R_r are capacitor, inductor, and resistor in rectifier load, respectively. The output voltage V_{out} and inductor current I_L are two system states for state feedback controller (SFC); V_{in} is the input PWM voltage.

With a sampling interval $T_s = 1/f_s$, the discrete-time state space of the single-phase DC/AC converter system in Fig. 6 can be written as [38]:

$$\begin{bmatrix} v(k+1) \\ i(k+1) \end{bmatrix} = \begin{pmatrix} \varphi_{11} & \varphi_{12} \\ \varphi_{21} & \varphi_{22} \end{pmatrix} \begin{bmatrix} v(k) \\ i(k) \end{bmatrix} + \begin{pmatrix} g_1 \\ g_2 \end{pmatrix} u(k) \tag{17}$$

where $\varphi_{11} = 1 - T_s/(RC) + T_s^2/(2R^2C^2) - T_s^2/(2LC)$, $\varphi_{12} = T_s/C - T_s^2/(2RC^2)$, $\varphi_{21} = -T_s/L + T_s^2/(2RLC)$, $\varphi_{22} = 1 - T_s^2/(2LC)$, $g_1 = E_n T_s^2/(2LC)$, $g_2 = E_n T_s/L$.

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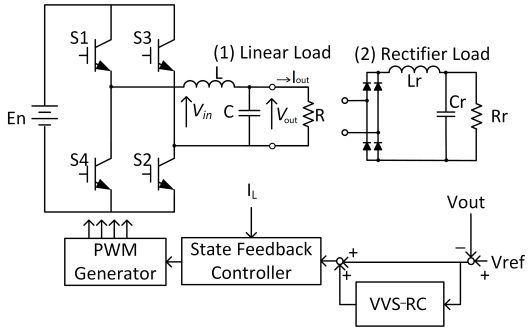

Fig. 6. Plug-in VVS-RC controlled DC/AC converter system

TABLE I
SINGLE-PHASE PWM SYSTEM PARAMETERS

Parameter	Value	Parameter	Value
DC bus voltage E_n	200 V	Linear load R	200 Ω
Inductor filter L_f	3 mH	Capacitor filter C_f	60 μF
Rectifier capacitor C_r	60 μF	rectifier inductor L_r	3 mH
Rectifier resistance R_r	200 Ω	PWM frequency	10 kHz
Sampling frequency f_s	10 kHz		

B. State feedback controller design

The state feedback controller for system (17) has the form as:

$$u = -K\begin{bmatrix} v(k) \\ i(k) \end{bmatrix} + gv_r(k) = -k_1 v(k) - k_2 i(k) + gv_r(k) \tag{18}$$

where k_1, k_2, and g are controller parameters, v_r is the reference sinusoidal voltage.

With the state feedback controller (18), the closed-loop system becomes:

$$\begin{bmatrix} v(k+1) \\ i(k+1) \end{bmatrix} = \begin{bmatrix} \varphi_{11} - g_1 k_1 & \varphi_{12} - g_1 k_2 \\ \varphi_{21} - g_2 k_1 & \varphi_{22} - g_2 k_2 \end{bmatrix} \begin{bmatrix} v(k) \\ i(k) \end{bmatrix} + \begin{pmatrix} g_1 g \\ g_2 g \end{pmatrix} v_r(k) \tag{19}$$

The poles of the feedback control system can be assigned by adjusting coefficients k_1 and k_2. The transfer function can be rewritten as [39]:

$$H(z) = \frac{m_1 z + m_2}{z^2 + p_1 z + p_2} \tag{20}$$

where $p_1 = -(\varphi_{22} - g_2 k_2) - (\varphi_{11} - g_1 k_1)$, $p_2 = (\varphi_{11} - g_1 k_1)(\varphi_{22} - g_2 k_2) - (\varphi_{12} - g_1 k_2)(\varphi_{21} - g_2 k_1)$, $m_1 = g_1 k$, $m_2 = g_2 k - g_1 k(\varphi_{22} - g_2 k_2)$.

With the parameters in Table I and state feedback controller $k_1 = 0.5$, $k_2 = 7$, and $g = 1.5$, the closed-loop transfer function for 60 Hz single-phase 110V DC/AC converter is derived as:

$$G(z) = \frac{0.623z + 0.01}{z^2 - 0.773z} \tag{21}$$

The feedback control system is stable with the poles $p_1 = 0$, $p_2 = 0.773$ in the unit circle. With only feedback controller, a severe phase lag in tracking and high THD in waveform distortion influence output performance under no load, linear load and rectifier load conditions which are shown in the first row of Fig. 11. The major distortion components appear on the $3rd$ and $5th$ harmonic frequencies.

C. Plug-in VVS-RC design

For CRC, the delay length chooses the closest integer of the ratio of Tr/Ts, $N = \lfloor T_r/T_s \rceil = \lfloor 166.67 \rceil = 167$. For VVS-RC, the delay length N_v is selected as 80, which meets the requirement of Eq. (5). With this setting, VVS-RC is able to check the signal from 41.67 Hz to 125 Hz. The VVS delay unit for 60 Hz reference signal is:

$$z_v^{-1} = 0.038z^{-1} + 0.993z^{-2} + 0.045z^{-3} \tag{22}$$

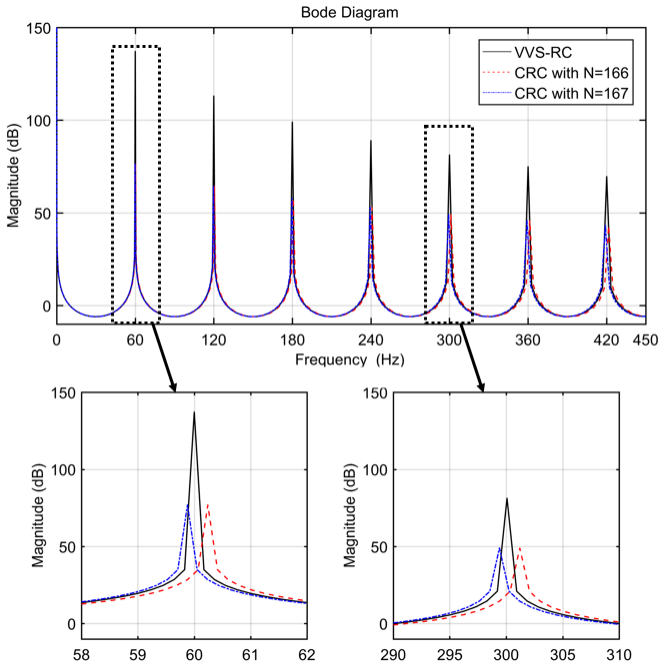

Fig. 7. Magnitude response of VVS-RC and CRC

The next step is to choose the RC gain K_r and to build the linear phase lead filter $G_f(z_v)$. In order to achieve fast transient response after applying VVS-RC, K_r is selected as 1, which also meets the requirement of Eq. (15). The phase lead of $G_f(z_v)$ is designed by following the analysis in [18] and measuring the actual system phase lag. The final phase lead is selected as

$$G_f(z_v) = z_v^{2.5} \approx -0.06z_v^1 + 0.56z_v^2 + 0.56z_v^3 - 0.06z_v^4 \tag{23}$$

To compare the performance of CRC and VVS-RC, CRC is designed based on regular CRC design procedure. For CRC, the delay length N is selected as the closest integer 167 because the ratio $T_r/T_s = 166.67$, and the low pass filter is selected as $Q(z) = 0.1z^{-1} + 0.8 + 0.1z^1$. Fig. 7 shows the magnitude response comparison of VVS-RC and CRCs. For CRC, the frequency resolution for magnitude peak is $f_s \times h/N$, where h is the harmonic order. In this case, because the ratio of the sampling frequency to the reference frequency is not an integer, the magnitude peaks of CRC shift away from the fundamental frequency and its harmonic frequencies. On

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the contrary, VVS RC does not have the limit on frequency resolution. Therefore, the magnitude peak is easy to be set at the desired frequency. Another different aspect is the peak magnitude. VVS RC achieves larger magnitude than CRC at the low frequency. As a result, it is able to have better harmonic distortion elimination ability at these harmonics.

IV. Experimental Validation

A. System setup

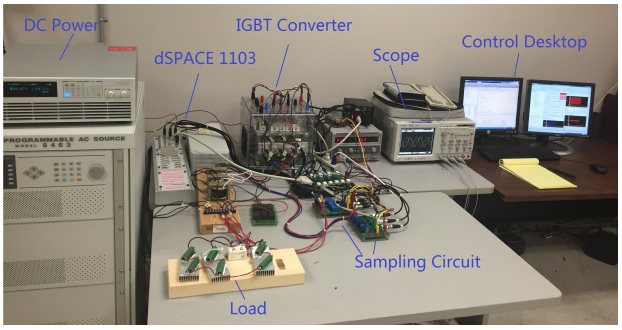

Fig. 8. Experiment setups

Fig. 8 shows the experimental setup, which consists of a dSPACE-controlled PWM IGBT H-bridge device, LC filter, DC power source, loads, and signal collection circuits.

In the experiments, the plug-in VVS-RC and state feedback controller are generated in MATLAB Simulink and implemented by dSPACE DS1103 board to control the H-bridge IGBT converter. The output voltage and current waveform are recorded via ControlDesk for system control and performance analysis.

B. Experimental results and comparison

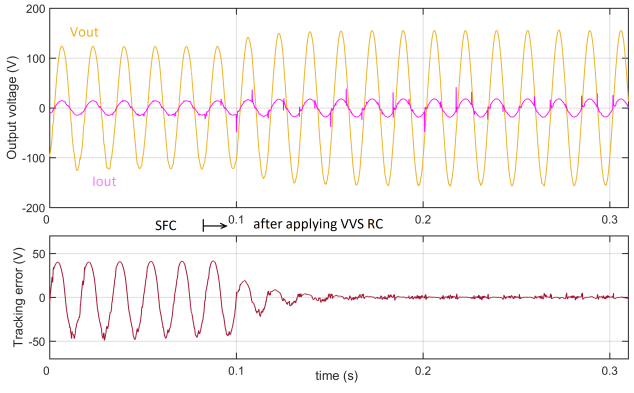

Fig. 9. Transient response on linear load after applying VVS-RC

The transient responses and tracking errors after applying VVS-RC under linear load and rectifier load are presented in Figs. 9 and 10. Under only SFC, the output has large tracking error because of the magnitude and phase error. After applying VVS-RC, tracking error converges to a very limited value after about three cycles.

Fig. 11 shows the steady-state performance comparison between SFC, CRC, and VVS-RC under linear and rectifier

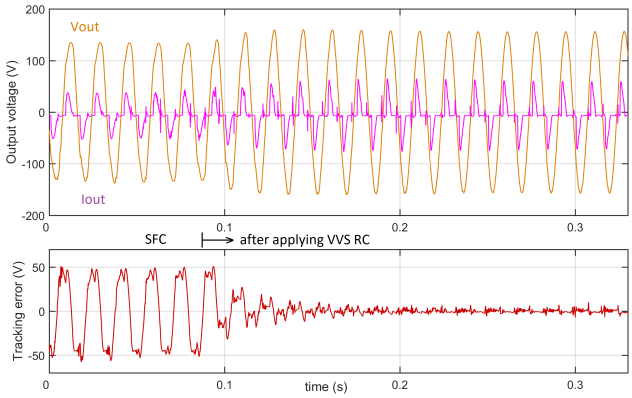

Fig. 10. Transient response on rectifier load after applying VVS-RC

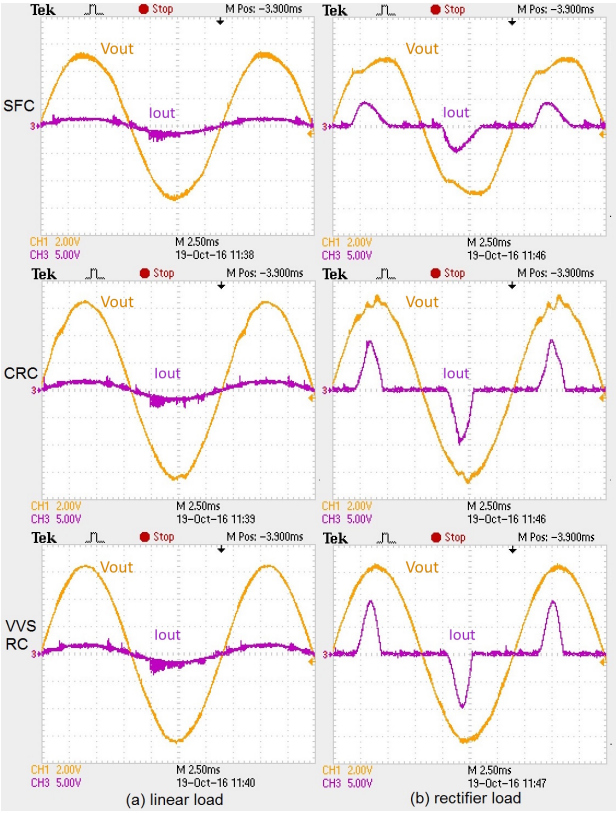

Fig. 11. Experiment results comparison for SFC, CRC, and VVS-RC under linear load (left column) and rectifier load (right column)

load for 60 Hz reference signal. It is clear that VVS-RC has the waveform with the least distortion under the condition of the fractional ratio of T_r to T_s. For SFC, there are large magnitude error and phase lag, and severe distortion under rectifier load. Although not too much magnitude error and phase lag for CRC, certain distortion still happens because of inaccurate delay length N.

Tables II shows the result comparisons for Fig. 11 in terms of tracking error in root mean square (RMS) value and THD under linear load (LL), no load (NL), and rectifier load (RL). From the table, SFC shows an unsatisfied response with large magnitude error and phase lag. Both CRC and VVS-RC show significant improvement on tracking error and THD. Because

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TABLE II
STEADY-STATE PERFORMANCE COMPARISON IN TERMS OF TRACKING ERROR AND THD

	Tracking Error (V)			THD		
	LL	NL	RL	LL	NL	RL
SFC	30.35	27.18	34.79	2.33%	2.72%	8.04%
CRC	1.73	1.78	2.5	1.73%	1.18%	2.18%
VVS-RC	1.05	1.19	1.18	0.72%	0.69%	0.71%

of the accurate delay design by $z_v^{-N_v}$, VVS-RC shows the best performance under different load conditions with 39.3%, 33.2%, and 52.8% improvement on tracking error and 58.4%, 41.5%, and 67.4% on THD compared with CRC.

C. VVS-RC under sudden load change

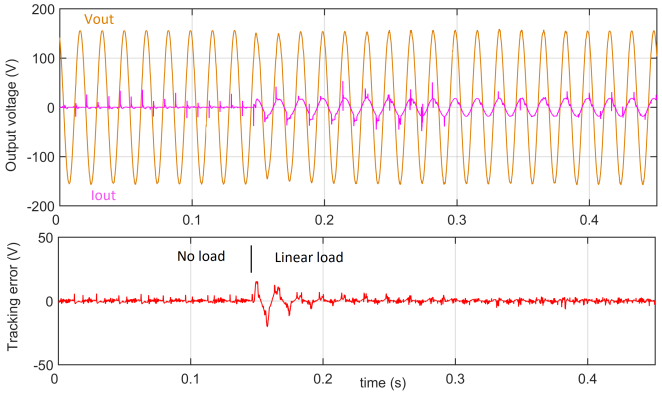

Fig. 12. VVS-RC with linear load under sudden load change

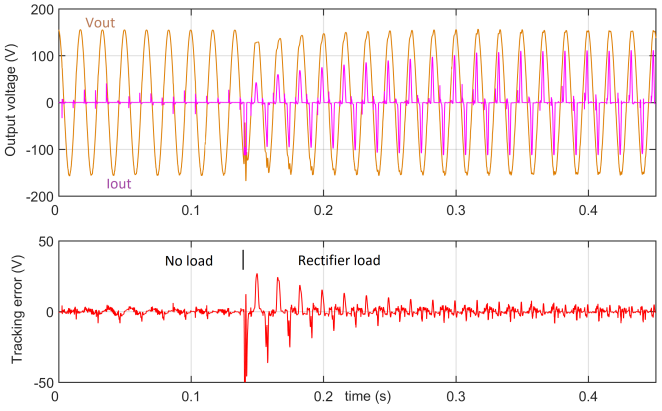

Fig. 13. VVS-RC with rectifier load under sudden load change

Figs. 12 and 13 show that the VVS-RC operates under sudden step load switches from no load to linear load and rectifier load, respectively. It is clear that output voltages do not vary too much and recover from the sudden step load changes within about four cycles for linear load condition and seven cycles for rectifier load condition. The experiments prove that VVS-RC is robust to sudden load changes.

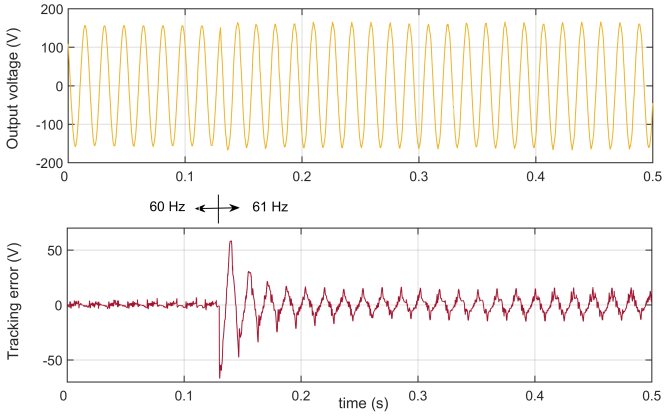

Fig. 14. Output response of CRC when reference frequency changes from 60Hz to 61Hz

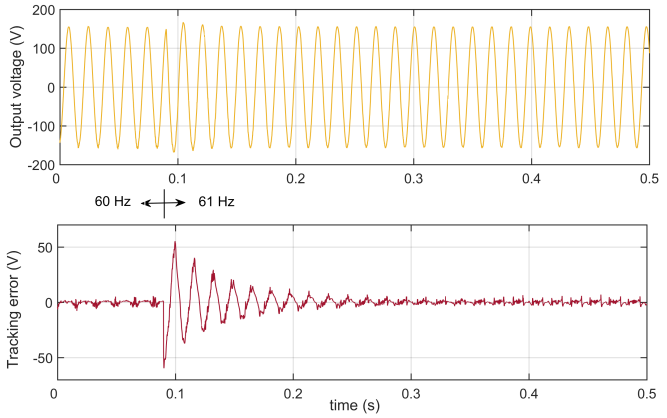

Fig. 15. Output response of VVS-RC when reference frequency changes from 60Hz to 61Hz

D. Frequency adaptability comparison between CRC and VVS-RC

Figs. 14 and 15 show the transient response of CRC and VVS-RC under reference frequency sudden change from 60 Hz to 61 Hz. By adjusting the VVS delay unit flexibly, the tracking error of VVS-RC converges back to a very limited value after about 10 cycles transient process. Without the frequency adaptability, the steady-state tracking error of CRC increases under such frequency fluctuation. The proposed VVS method enables RC with excellent frequency adaptability.

V. CONCLUSION

In this paper, a flexible, generic, and easy-to-implement virtual variable sampling RC is proposed to address the performance degradation caused by the fractional ratio of reference period to sampling period. With fixed system sampling period, a virtual variable sampling period is achieved by building an approximated virtual unit delay. Based on this, RC can be implemented with a virtual variable sampling period that is different from the system sampling period. Comparing with variable sampling period methods that are achieved in hardware, the virtual variable sampling period is approximated by software and, therefore, is simpler and more economical.

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In contrast to fractional-order RC in previous work, this method is more flexible and can deal with signals with larger frequency variation range. The cost of VVS-RC is that it will take more computational memories than conventional RC or fractional-order RC. Theoretical analysis shows that the proposed RC scheme is able to make the infinity gain appears on the fundamental and harmonic frequencies of the periodic signal, which guarantees the tracking performance. Experimental results also show that virtual variable sampling RC offers transient performance as fast as CRC, and better tracking performance than CRC under fractional frequency ratio. The proposed RC scheme can also be used for solving the fractional delay length problem when digital RC is applied in grid-connected device, especially when the grid frequency fluctuates under disturbance.

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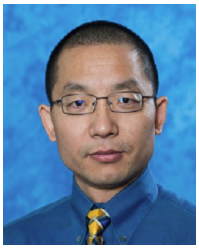

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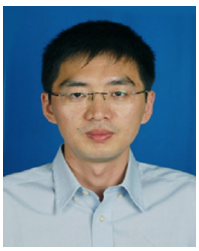

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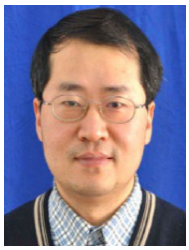

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