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Balanced Conduction Loss Distribution among SMs in Modular Multilevel Converters

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***Abstract*—Due to the parameter mismatch, the unbalanced power loss distribution among SMs in the modular multilevel converter (MMC) can be introduced and further deteriorated by the low-frequency asynchronous switching transients related to no-carrier modulation techniques. The unbalanced thermal stress can reduce the reliability of the MMC and increase the complexity of cooling system design. Nevertheless, an internal balance mechanism exists in the MMC thanks to the capacitor voltage balancing. It contributes to an even conduction loss dissipation among SMs, which is studied and revealed in this paper. Moreover, a computationally light conduction loss estimation method is proposed correspondingly relying on the characteristics of semiconductors and the arm current only. Simulations and experiments are conducted to verify the effectiveness the proposed method.**

***Index Terms*—Modular multilevel converter (MMC), balanced conduction loss distribution, conduction loss estimation, semiconductor.**

I. Introduction

The modular multilevel converter is an emerging and attractive voltage-source converter (VSC) topology for high-voltage direct current (HVDC) transmission systems due to its modularity, scalability to different voltage levels, high output quality and no high voltage dc-link capacitor [1]–[3].

Reliability is one of the major concerns for the MMC because of the large cost investment and the large number of semiconductors, which are the weakest components in power converters [4]. Thus, it is necessary to fulfill the full potential of submodules (SMs) by posing even thermal stress on the devices. However, unbalanced power loss behavior (component-level and submodule-level) in the MMC can lead to various thermal stresses, which brings a challenge to the cooling system design and the converter reliability. The component-level unbalance is caused by a dc bias in the arm current when the active power is transferred through the MMC. The four semiconductors (taking the half bridge SM for example) undertake different thermal stress [5]. Submodule-level uneven power loss dissipation mainly results from the parameter mismatch among SMs and the low switching frequency for the MMC based on nearest level modulation (NLM) [6].

To address above problems, some research efforts have been made. An explanation about the loss unbalance for both conduction loss and the switching loss is detailed, and a two-dimension sorting method is proposed for a balanced junction temperature behavior [7]. Experiment validations and reliability assessment are further conducted on a down-scale bench [6]. Various active thermal balancing methods based on the circulating current are explored for component-level power loss balancing, but the effectiveness is limited [8]. [4] focuses on the submodule-level power loss balancing integrated with the capacitor voltage balancing, but the loss model for MMC with a large number of SMs is computationally burdened.

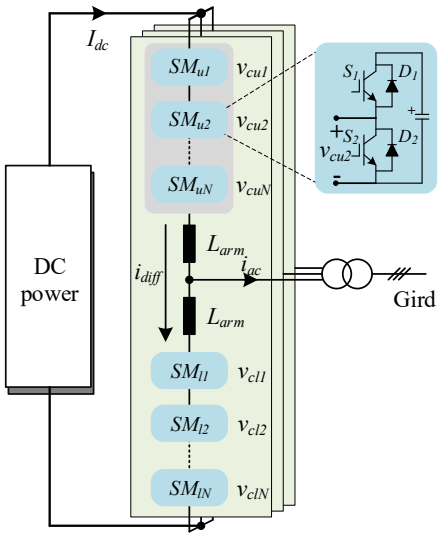

Fig. 1. Circuit configuration of a typical three-phase MMC. (I_{dc} is the dc-bus current, i_{ac} is the ac output current, and i_{diff} is the differential current.)

In fact, an internal power loss balancing mechanism already exists in the MMC thanks to the capacitor voltage balancing as mentioned in [6]. However, no detailed explanation has been given to the phenomenon until now, to which the attention will be paid in this paper. An analytical derivation will be given to confirm this. In addition, a very computationally light conduction loss estimation method is proposed and verified through simulations and experiments.

The rest of this paper is organized as follows: Section II gives the introduction of the basic operation principles of the MMC. In Section III, the proposed submodule-level conduction loss estimation method is introduced followed by the full-scale simulation validation in Section IV. Experimental validation based on a down-scale test bench is conducted and describes in Section V. Section VI gives the conclusions.

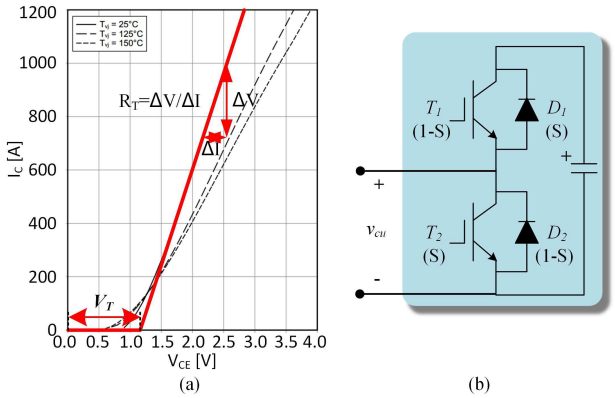

Fig. 2. (a). Curve fitting of IGBT datasheet, and (b). Gate signal relationship between four different semiconductors in a half-bridge SM.

II. Operating Principle of MMC

A typical circuit configuration of three-phase MMCS is presented in Fig.1. The MMC is composed of three phases, which can be divided into the upper arm and the lower arm. Each arm includes N series-connected SMs, and an arm inductor to restrain the circulating current within the phase leg. Half-bridge SM with four semiconductors is adopted in this paper. Generally, the arm current can be divided into two parts, namely the common component i_{comm} and the differential component i_{diff} [9]. A dc bias is an essential part of the differential component for the active power transfer, and to maintain the SM's voltage at the rated value. In addition, harmonic currents can be injected into the differential current to achieve certain objectives as well [10]. If the dc bias differential current is only considered here neglecting other harmonics, the upper arm current i_{up} of phase A can be expressed as

$$i_{up} = \frac{I_{dc}}{3} + \frac{I_{ac}}{2}\cos(\omega t + \varphi_1), \tag{1}$$

where I_{dc} and I_{ac} are the amplitude of dc-bus current and ac output current; φ_1 is the power factor angle, and ω is the angular frequency.

Assuming a lossless MMC system, the relationship between I_{dc} and I_{ac} can be derived [11] as

$$I_{ac} = \frac{4I_{dc}}{3m\cos(\varphi_1)}. \tag{2}$$

III. Submodule-level Balanced Conduction Loss Distribution

A. Submodule-level Conduction Loss Calculation

Considering the equivalence among the six arms in three-phase MMC system, the analysis in the following will only take the upper arm of phase A for example. The upper arm current i_{up} is first divided into the positive part i_p and the negative part i_n respectively for an easy loss calculation.

$$i_p = \frac{|i_{up}| + i_{up}}{2}, \quad i_n = \frac{|i_{up}| - i_{up}}{2}. \tag{3}$$

The conduction loss averaged in one fundamental period of IGBT and diode can be calculated by

$$\begin{aligned} P_{con\_T2/D1} &= \frac{1}{T}\int_0^T \left(V_{T/D} i_p + R_{T/D} i_p^2\right) S_{T2/D1} dt \\ P_{con\_T1/D2} &= \frac{1}{T}\int_0^T \left(V_{T/D} i_n + R_{T/D} i_n^2\right) S_{T1/D2} dt \end{aligned} \tag{4}$$

where P_{con_x} is the average conduction loss of device x in one fundamental period T; V_T, V_D, R_T and R_D are the on-state voltage and the on-state resistance of IGBT and diode obtained by curve fitting of the data-sheet as shown in Fig. 2; S_i is the time-dependent gate signal of the i^{th} SM, equal to 1 or 0, where $S_{T2} = S_{D1} = S_i$, $S_{T1} = S_{D2} = (1 - S_i)$.

Adding up the equations in (4) and combining with (3), the total conduction loss of one SM can be derived as

$$\begin{aligned} P_{total} &= \frac{1}{T}\int_0^T (V_D i_p + R_D i_p^2 + V_T i_n + R_T i_n^2) dt \\ &+ \frac{1}{T}\int_0^T \Delta V i_{up} S_i dt + \frac{1}{T}\int_0^T \Delta R i_{up} |i_{up}| S_i dt \end{aligned} \tag{5}$$

where $\Delta V = V_T - V_D$ and $\Delta R = R_T - R_D$, are the parameter differences between IGBT and diode.

In the normal operation of the MMC, the capacitor voltages among SMs are balanced in the steady-state, which can be achieved by various voltage balancing control methods [12], [13]. Therefore, it is reasonable to assume that the increase and decrease of the SM's capacitor voltage (charged by D_2 and discharged by T_1) are equal during one fundamental period, and the relationship can be expressed as

$$\Delta U^+ = \int_0^T \frac{i_p(1-S_i)}{TC_i} dt = \Delta U^- = \int_0^T \frac{i_n(1-S_i)}{TC_i} dt \tag{6}$$

where $\Delta U^{+/-}$ is the voltage increase/decrease during one fundamental period; C_i is the capacitance of the i^{th} SM.

The relationship in (6) can be further simplified as

$$\int_0^T i_{up} S_i dt = \int_0^T i_{up} dt. \tag{7}$$

Substituting (7) into (5), the total conduction loss per SM can be re-expressed as

$$\begin{aligned} P_{total} &= \underbrace{\frac{1}{T}\int_0^T (V_D i_p + R_D i_p^2 + V_T i_n + R_T i_n^2) dt}_{P_{com1}} \\ &+ \underbrace{\frac{1}{T}\int_0^T (\Delta V + \Delta R k) dt}_{P_{com2}} + \underbrace{\frac{\Delta R}{T}\int_0^T i_{up}(|i_{up}| - k) S_i dt}_{\Delta P_i} \end{aligned} \tag{8}$$

where P_{com1} and P_{com2} are the common conduction loss components for all SMs , they are unrelated to the switching actions; ΔP_i is the specific conduction loss component of the i^{th} SM; k is a constant related to the arm current.

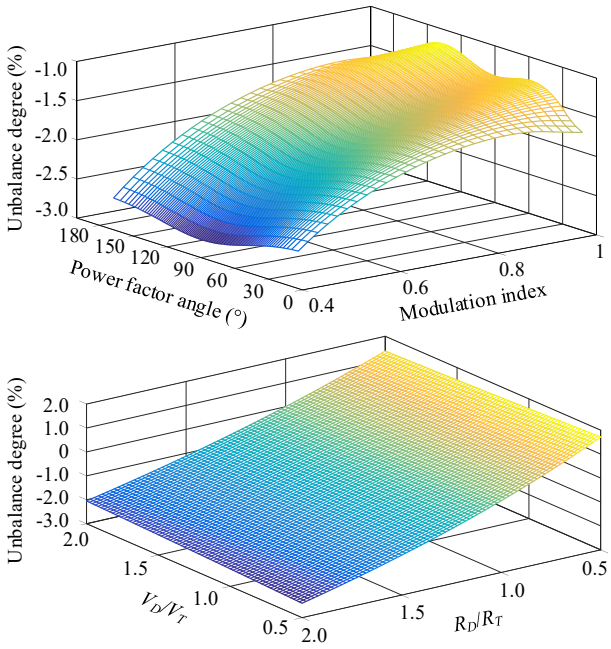

Fig. 3. Unbalance degree regarding different modulation index, power factor and semiconductor parameters.

ΔP_i can be estimated by $P(k)$, whose minimum value can be achieved when (10) holds.

$$|\Delta P_i| \leq \left| \frac{\Delta R}{T} \int_0^T |i_{up}(|i_{up}| - k)| dt \right| = P(k) \tag{9}$$

$$k = \frac{\int_0^T |i_{up}|^2 dt}{\int_0^T |i_{up}| \, dt}. \tag{10}$$

B. Conduction Loss variation

The conduction loss variation among SMs is cause by ΔP_i, which is dependent on the switching actions. Its impact on the total conduction loss of one SM can be evaluated by a defined parameter, unbalance degree $e_{SM} = P(k)/P_{total}$. It can be affected by several parameters, such as the MMC operation conditions (modulation index and power factor) and the semiconductor on-state characteristics. Their effects are illustrated by full-scale simulation results in the following based on the IGBT module 5SNA-1200G450350 from ABB, whose on-state parameters are listed in Table I.

Fig. 3 shows the unbalance degree under different power factor, modulation index, and power device characteristics. It can be seen that e_{SM} is always within $\pm 4\%$ when the modulation index ranges from 1 to 0.4, which covers the normal operating range of MMC system. The impact of parameter differences between IGBT and diode are also evaluated in Fig. 3, and the unbalance degree within 3% can be achieved as well. Note that the unbalance degree here is overestimated, and its actual value should be less than that in Fig. 3. Based on the results above, two preliminary conclusions which will be validated in the following sections can be achieved:

TABLE I
SIMULATION PARAMETERS FOR FULL-SCALE AND DOWN-SCALE MMC

Parameter	Fullscale	Downscale
Power rating	30 MVA	24 kVA
Dc-link voltage V_{dc}	50 kV	2 kV
SM number N	20	20
Arm inductor L_{arm}	13 mH	20 mH
Arm capacitor C_{arm}	3 mF	0.22-0.26 mF
V_T	1.5 V	1.9 V
V_D	2.5 V	1.36 V
R_T	0.52 mΩ	31.6 mΩ
R_D	0.94 mΩ	13.8 mΩ

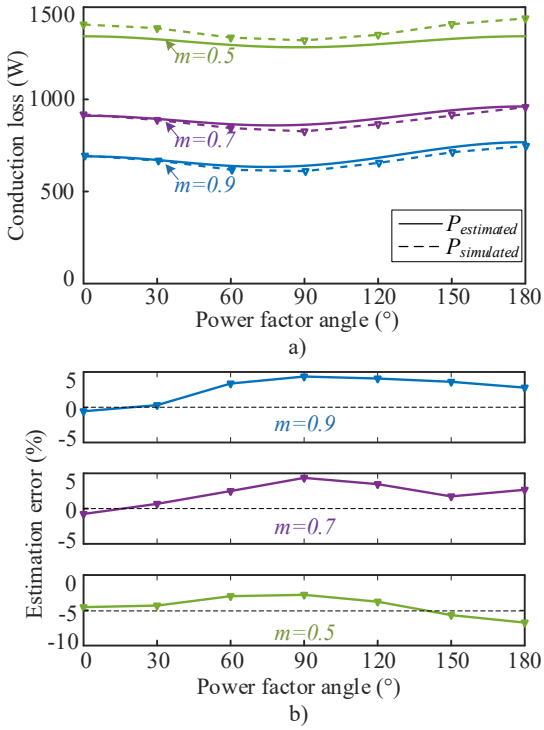

Fig. 4. Conduction loss per SM during one fundamental period regarding different power factor angles. a) Conduction loss, and b) conduction loss estimation error.

1). The total conduction loss of one SM can be estimated by P_{total}. This method is independent on the gate signal, and is computationally light with the need of on-state semiconductor characteristics and the arm current information only.

2). Different SMs share a balanced submodule level conduction loss regardless of the switching transient or the modulation strategies when the capacitor voltage of SMs are well balanced.

IV. Full-scale Simulation Validation

To validate the proposed conduction loss estimation approach, and the balanced SM-level conduction loss distribution, simulations based on a three-phase MMC as shown in Fig. 1 are conducted. IGBT module 5SNA-1200G450350 from ABB is used in this paper. Other system parameters are listed in Table I. Fig. 4 and Fig. 5 illustrate the conduction loss of

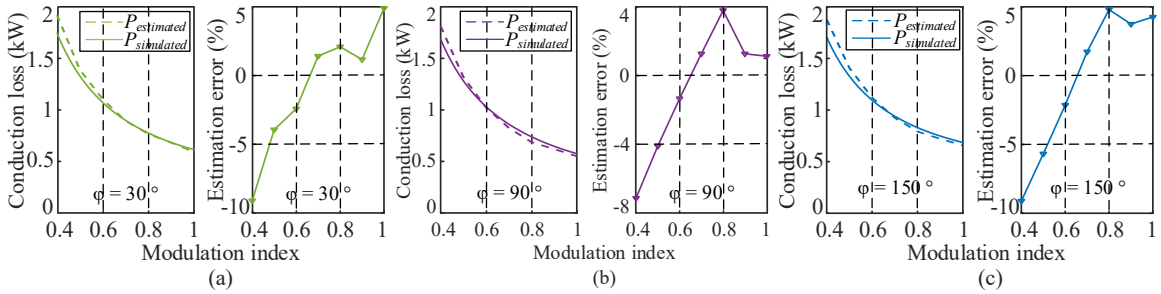

Fig. 5. The total conduction loss and the estimation error of an SM during one fundamental period regarding different modulation indexes. a) $\varphi = 30°$, b) $\varphi = 90°$, and c) $\varphi = 150°$.

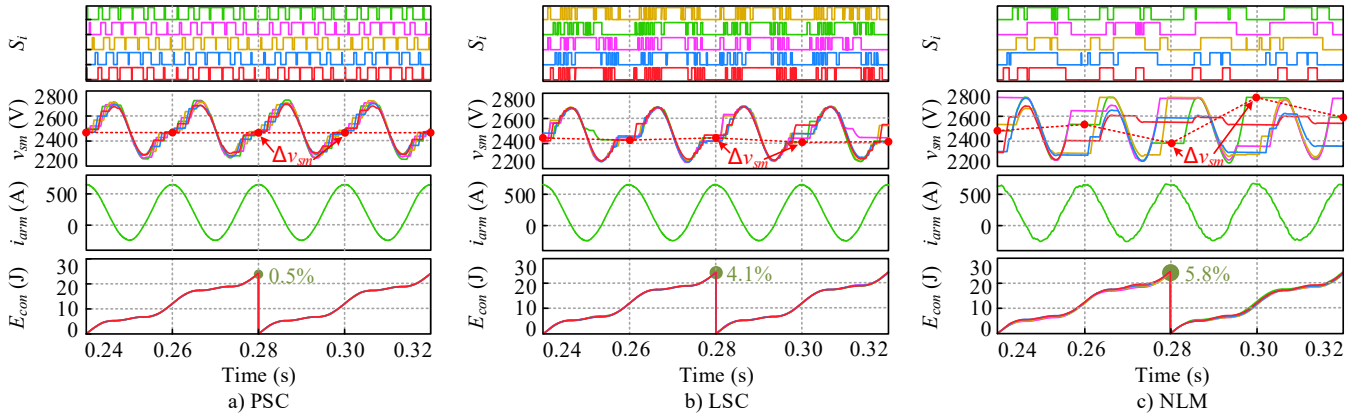

Fig. 6. Conduction loss of five SMs in the upper arm of phase A with modulation index $m = 0.8$ and power factor angle $\varphi = 30°$: a) PSC, b) LSC and c) NLM. (Sub-graphs from top to bottom are: the gate signal, the arm current, the SM capacitor voltage, and the conduction loss per SM averaged in 0.02 s.)

one SM under different power factor angles and different modulation indexes. It can be seen that conduction loss increases greatly with the decrease of the modulation index, and, in contrast, the power factor has a small impact on the conduction loss. The estimation error remains acceptable with the value being around 5% when the modulation index is larger than 0.5. However, it increases sharply for the modulation index less than 0.5. Nevertheless, the proposed method is still valid since MMCs operate in a high modulation index (e.g., around 0.9) condition in most cases.

To illustrate the balanced conduction loss distribution, a series of simulations are done with regards to different modulation strategies and different SM capacitances based on the scaled-down three-phase MMC in Fig. 1. Three commonly-used modulation methods, namely phase-shifted Carrier (PSC) modulation, level-shifted carrier (LSC) modulation and nearest level modulation (NLM) are validated respectively. The capacitance mismatch introduced by manufacturing process, degradation and maintenance of a broken SM [7] is taken into account by evenly setting its value from 2.2 mF to 2.6 mF for SM1 to SM20 with the variation of 18%.

Fig. 6 shows the simulation waveforms of 5 SMs (SM1, SM5, SM10, SM15 and SM20) in the same arm in two fundamental periods with the modulation index and power factor being 0.9 and 1 respectively. Different switching patterns for the three modulation methods can be clearly observed. The capacitor voltages are well regulated averaging at 2500 V. The current waveform for NLM contains more harmonic components compared with that of PSC due to the lower switching frequency. The average accumulated conduction losses are 23.9 J, 24.2 J, and 24.2 J for PSC, LSC and NLM respectively, and it can be seen that the loss unbalance degree increases from 0.5%, 4.1% to 5.8%. The reason, as mentioned in Section III, is that the capacitor voltage balancing performance gets worse as shown in Fig. 6. Δv_{sm} gets larger and larger, and equations (6) and (7) are not hold perfectly. Nevertheless, the small loss difference can still confirm that the modulation method and capacitance mismatch have a negligible effect on the balanced conduction loss of one SM.

V. Down-scale Simulation and Experiment Validation

In addition to the full-scale simulation validation, a three-phase MMC with scaled down system parameters is simulated as well. The arm current contains dc and ac components with the peak value being 4 A and 10 A respectively. Unity power factor is used, and the modulation index is set at 0.8. Moreover, the same IGBT module F4_50R12KS4 from Infineon with the experiment is used in the simulation. Thermal profiles of both IGBT and diode in the simulation are tested through Curve Tracer B1506A under various temperatures ranging from $25°C$ to $125°C$. Meanwhile, a down-scale experiment with the same

Fig. 7. Scaled down experiment test bench.

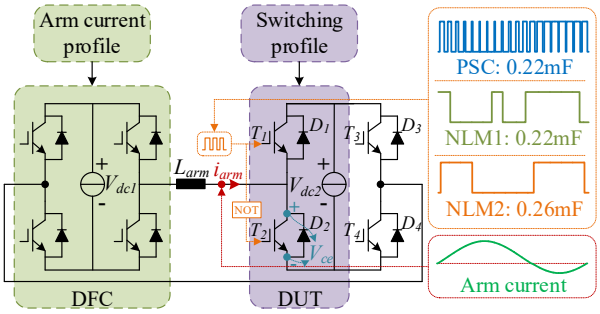

Fig. 8. Circuit topology of the down-scaled experimental bench.

system parameters in the simulation is conducted based on the prototype in Fig. 7. Fig. 8 shows the circuit scheme where two full bridge converters are used. One is used as the device for control (DFC) regulating the inductor current to track the current profile from simulation. Another one is divided into the DUT and the auxiliary half bridge. The DUT is controlled by the switching profile. Besides, two capacitors (0.22 mF and 0.26 mF) and two modulation methods (PSC and NLM) are used in this paper for validation. Other parameters are listed in Table I.

Fig. 9 shows the experiment waveforms of the arm current, the on-state voltages of both IGBT and diode, and the gate signals under the condition of NLM. It can be seen that the arm current is well regulated, and the on-state voltages of both IGBT and diode are sampled in two fundamental periods. By using the waveform data exported from the oscilloscope, the accumulated conduction loss of the four semiconductors can be calculated in Matlab. The experimental results are compared with the simulation as shown in Fig. 10. The simulated total conduction losses of one SM in one fundamental period are 0.2332 J, 0.2333 J and 0.2316 J for PSC, NLM1 and NLM2 respectively with the variation of 0.7%. The average accumulated conduction losses from the experiment are around 0.2464 J with the variation as low as 0.3%. In addition, the conduction loss calculated by the proposed method is 0.2296 J with the error of 1.4% and 6.8% compared with the simulation and experiment results respectively.

The small errors between the simulations, the experiments

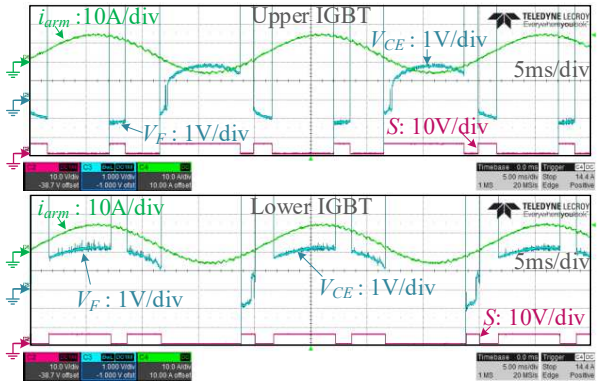

Fig. 9. Experiment waveforms of the arm current, the on-state voltage and the gate signal of upper and lower IGBTs under the unity power factor and the modulation index of 0.8.

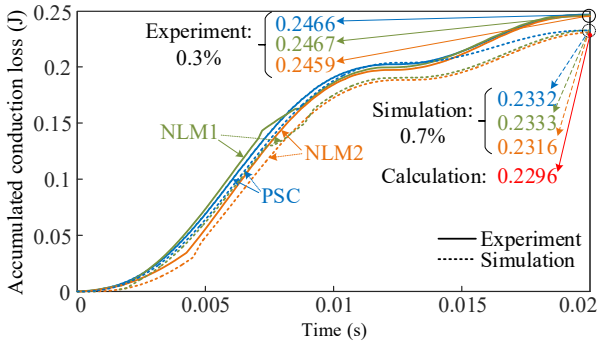

Fig. 10. Simulation and experiment results of the accumulated conduction loss of one SM under three different modulation methods.

and the calculation confirm the balanced conduction loss distribution and validate the effectiveness of the proposed conduction loss estimation method.

VI. Conclusion and Future Work

Different SMs share a balanced conduction loss regardless of the operation condition, the modulation techniques and the parameter mismatch related to the capacitor and the semiconductor when the SM capacitor voltages are well balanced. The conclusion is helpful to guide the practical cooling design and the active thermal balanced control of the MMC system, where more attention should be paid to the switching loss. Moreover, a computationally light conduction loss estimation method is proposed correspondingly, which depends on the on-state characteristics of the semiconductors and the arm current only without considering the switching transients. The validity of the conclusion is verified through both full-scale and down-scale simulation and experiment.

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