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Submodule Level Power Loss Balancing Control for Modular Multilevel Converters

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***Abstract*—This paper investigates the power loss imbalance in Modular Multilevel Converters (MMCs) with Nearest Level Modulation (NLM) resulting from the low switching frequency operation and the parameter mismatch. The imbalance might pose a challenge to the cooling system design as well as the reliability of the MMC. To address this problem, a submodule-level power loss balancing control (PLBC) is proposed. Compared with the normal control strategy without the thermal balancing, this method is able to decrease the degree of power loss imbalance among submodules (SMs) to at least half without deteriorating the performance of the converter efficiency and the capacitor voltage ripple. The effectiveness of the proposed control is validated by simulations.**

***Index Terms*—Power loss balancing, modular multilevel converter, power semiconductors.**

I. Introduction

The modular multilevel converter (MMC) is one of the most attractive topologies for high-voltage and high-power applications. The multilevel configuration greatly improves the output harmonic performance, which reduces or eliminates the output filters [1]. Moreover, low-voltage power devices available on the market can be directly applied in different voltage level situations by altering the number of series connected SMs per arm [2].

Moreover, MMC has to meet high reliability requirement to secure a continuous operation in most of its applications. To achieve this objective, much attention is paid to the power device, which is assumed as one of the weakest components in the MMC system [3]. To increase the reliability, one widely-used method for the MMC is redundancy design, where redundant SM functions to replace the failed one when failure occurs [4]. In addition, it is also attractive to improve the reliability through control method prior to failures. For example, the active thermal control utilizing existing signals only might be a promising candidate. It aims to regulate the thermal stress, especially the most stressed devices, such as the junction temperature swing and the mean junction temperature, to extend the power module lifetime [5].

Examples from conventional two-level or three-level converters in wind power applications can be found in [6]. Similar research on the MMC can be found in [7], where circulating current generated from a look-up table according to the output power is injected into the arm current to relieve the thermal stress of the power devices. It is also possible is to distribute the power loss evenly and to fulfill the potential lifetime of all devices. An inherent component-level power loss imbalance exists in the MMC due to the dc component in the circulating current. The worst case is under the scenario of a pure active or pure reactive power transfer [8] [9]. The impact of a series of control freedoms, including the circulating current and the arm voltage reference, on the power loss redistribution has been investigated [10]. Simulation results illustrate that when functioning alone, all of them have a negligible impact on the most stressed components, like the bottom IGBT in each SM under unity power factor condition. The multi-objective optimization control proposed in [11] introduces the third-order output common-mode voltage and the SM capacitor voltage as another two freedoms to obtain the optimal operating parameters for the MMC. Simulations and experiments show an impressive temperature reduction resulting primarily from the switching loss reduction.

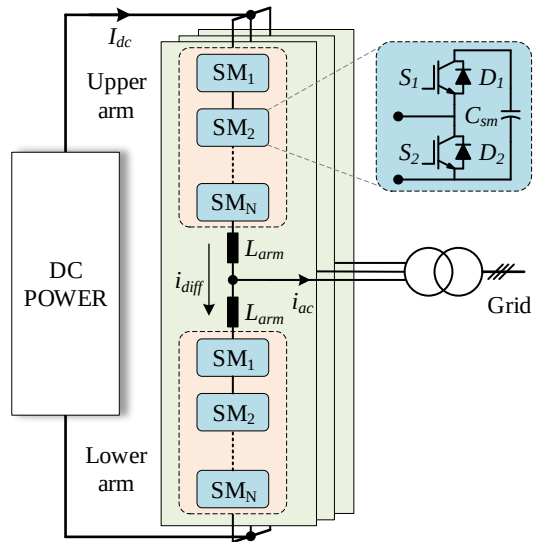

Fig. 1. Circuit configuration of a three-phase MMC. I_{dc} is the dc-bus current, i_{ac} is the ac output current, and i_{diff} is the differential current.

In addition to the component-level thermal imbalance in the MMC, uneven power loss distribution in the submodule-level due to the low switching frequency and the parameter mismatch (reasons are given in Section II) is also challenging

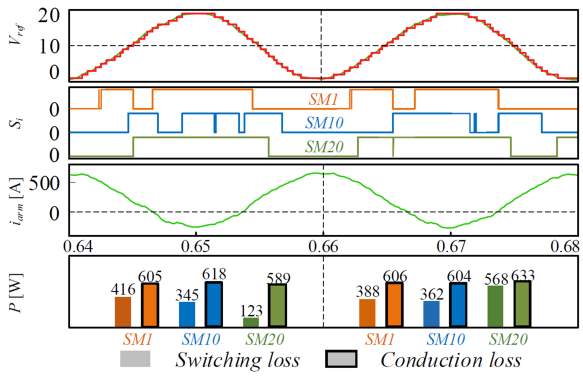

Fig. 2. Voltage references for the upper arm, the gate signals for SM [1], SM [10] and SM [20], the arm current, and the power losses including the switching losses and the conduction losses.

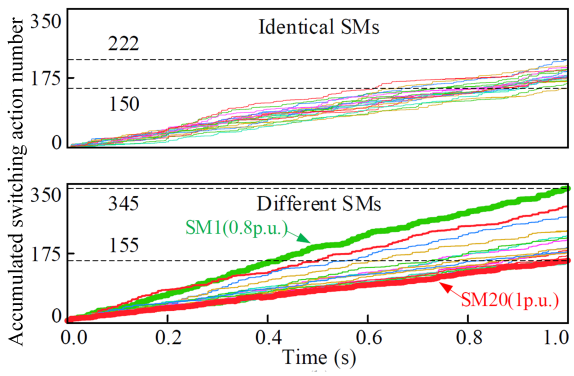

Fig. 3. Accumulated switching action number within one second among 20 SMs under the NLM. (Upper sub-figure shows the results of identical SMs, and lower sub-figure shows the results of SMs with different capacitance)

in terms of the reliability and cooling design for the SM. A two-dimension sorting and selection algorithm is proposed by taking the temperature into consideration in addition to the capacitor voltage with decreased thermal spread among SMs and without deterioration of system performance [12]. The method is further extended and validated by experiments [13]. Besides the temperature, regulating power losses is also an alternative for thermal balancing control [14]. However, as revealed in [15], the submodule-level conduction losses among SMs are well balanced regardless of the operation condition, the modulation techniques and the parameter mismatch under the circumstance of balanced SM capacitor voltages. It can be readily achieved by various voltage balancing control (VBC) strategies. Therefore, this paper proposes a simplified method with respect to the one presented in [14] by excluding the need for IGBT conduction loss estimation, resulting in reduced computation requirements and less parameters to be adjusted. Moreover, the trade-off between the capacitor voltage balancing and the power loss balancing is studied.

The remainder of this paper is organized as follows. Section II describes the power loss imbalance in the MMC followed by the proposed control strategy in Section III. Section IV provides the simulation results. Section V gives the conclusion.

TABLE I
MAIN SYSTEM PARAMETERS OF THE MMC FOR CASE STUDY.

Item	Value	Item	Value
Power rating	30 MW	DC bus voltage	50 kV
SM number	20	SM capacitor C_{sm}	2 mF
Arm inductor L_{arm}	13 mH	Modulation index	0.8

II. Power Loss Imbalance in the MMC

A. Low Switching Frequency

MMC can be controlled by the nearest level modulation (NLM) technology, where the equivalent switching frequency could be as low as several times of the fundamental frequency. In this case, different switching time matters regarding the switching losses since it corresponds to different arm current value and various switching loss. As shown in Fig. 2, a three-phase 30 MW MMC model with 20 identical SMs per arm is simulated with an equivalent switching frequency being 150 Hz. Other main system parameters are listed in Table I. It can be seen, taking three SMs for example, that the switching losses averaged in one fundamental period vary from 123 W to 416 W, and it is from 362 W to 568 W in two consecutive fundamental periods. However, the averaged conduction loss difference among SMs are under 5%. The results indicate that an internal balancing mechanism exists for the conduction loss of one SM, but it is not the case for the switching losses.

B. Parameter Mismatch

Identical SM is normally assumed in most existing studies on the performance analysis of the MMC. However, in practice, the capacitance for different SMs varies with each other due to its tolerance and different degree of degradation with the deviation being as large as 20% of the ideal value [12]. This deteriorates the power loss imbalance in the MMC. Fig. 3 shows the number of the accumulated switching action of SMs with the identical and different capacitance respectively. It can be seen that the maximum switching frequency difference is 72 Hz for identical SMs. However, It increases to 190 Hz for SMs with uneven capacitances from 1.6 mF to 2.0 mF. This validates the effect of the capacitance mismatch on the switching frequency spread and uneven switching loss distribution. Other parameter mismatch related to the characteristic of semiconductors (e.g., on-state voltage drop) and the Thermal Interface Materials (TIM) (e.g., the mounting pressure, the thickness, and the degradation) [16] can introduce different thermal behavior to the SMs as well. However, the part is not considered in this paper.

III. Active Power Loss Balancing Control of the MMC

As mentioned in the introduction, the conduction loss among SMs are well balanced in the MMC. Thus, this paper focuses on the switching loss imbalance only in the submodule level. The capacitor voltage sorting algorithm determines the actual switching action of one SM, thus modifying the voltage

TABLE II
PLBC OPERATING MECHANISM REGARDING THE ARM CURRENT DIRECTION, THE SM STATUS AND THE SWITCHING LOSS INFORMATION

Arm current	Principle of sorting algorithm	Previous SM status	Switching loss	Expected SM status	Output of PLBC
Positive	Insert/bypass SM with lower/higher voltage	Insert	Higher/lower than the average accumulated switching loss	Insert/bypass	Decrease/increase v_{sm}
		Bypass		Bypass/insert	Increase/decrease v_{sm}
Negative	Insert/bypass SM with higher/lower voltage	Insert		Insert/bypass	Increase/decrease v_{sm}
		Bypass		Bypass/insert	Decrease/increase v_{sm}

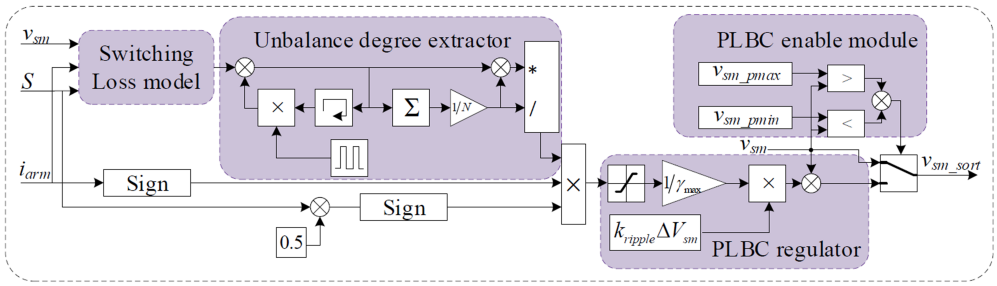

Fig. 4. Submodule level power loss balancing control scheme.

value is able to influence the switching loss. The core idea of the proposed power loss balancing control (PLBC) is to achieve the objective below: SMs with higher switching loss tend to keep the current switching status from further increasing the loss. Instead, SMs with lower switching loss take the duty to track the voltage reference for control purpose. Specifically, the PLBC enhances the probability of changing the gate status of the SM with lower switching loss by adding an adjustment to the real capacitor voltage v_{sm}. The adjustment is decided by the arm current direction, the previous status of the SM, and the switching loss information as illustrated in Table II. Detailed control scheme is shown in Fig. 4.

A. Switching Loss Model

The current-dependent switching energy of the semiconductor can be obtained from the data-sheet of the IGBT module used (e.g., 5SNA 1200G450350 from ABB [17]), and curve-fitted through a second-order polynomial under certain blocking voltage and junction temperature as [8]

$$E_{sw}\left(i_{arm}, T_{ref}, V_{ref}\right) = a_2 i_{arm}^2 + a_1 \left|i_{arm}\right| + a_0, \tag{1}$$

where a_2, a_1 and a_0 are the curve-fitting coefficients, i_{arm} is the arm current, and V_{ref}, T_{ref} are the references of the blocking voltage and the junction temperature in the data-sheet respectively.

The switching energy considering the impact of blocking voltage and junction temperature is [18]

$$\begin{aligned} &E_{sw}\left(i_{arm}, T_j, V_{sm}\right) \\ &= \frac{V_{sm}}{V_{ref}} E_{sw}\left(i_{arm}, T_{ref}, V_{ref}\right)\left[1 + K_T\left(T_j - T_{ref}\right)\right], \end{aligned} \tag{2}$$

where V_{sm} is the average SM voltage, T_j is the junction temperature, and K_T is the temperature coefficient fitted from the data-sheet. Thus, the total switching energy can be calculated by summing up all switching pulse energies.

B. Imbalance Degree Extractor

The proposed PLBC focuses on the power loss imbalance level among SMs instead of the real power loss difference. The imbalance level is defined as the maximum power loss difference over the average power loss among SMs per arm. Thus, an imbalance degree extractor shown in Fig. 4 is designed. The accumulated switching energy ($E_{i_\Sigma sw}$) and the average accumulated switching energy ($E_{\Sigma sw_avg}$) among SMs are calculated first, and the imbalance degree can be extracted through the two values as explained below.

To simplify the analysis, SM [1] is assumed to have a different switching loss with the other $(N-1)$ SMs, where $E_{1_\Sigma sw} > E_{2_\Sigma sw} = E_{3_\Sigma sw} = ... = E_{N_\Sigma sw}$. The average accumulated switching energy and the imbalance degree γ are defined as

$$E_{\Sigma sw_avg} = \frac{E_{1_\Sigma sw} + (N-1)\, E_{2_\Sigma sw}}{N}, \tag{3}$$

$$\begin{aligned} \gamma &= \frac{\max\left(E_{i_\Sigma sw}\right) - \min\left(E_{i_\Sigma sw}\right)}{\min\left(E_{i_\Sigma sw}\right)} \\ &= \frac{E_{1_\Sigma sw} - E_{2_\Sigma sw}}{E_{2_\Sigma sw}}, \end{aligned} \tag{4}$$

where $E_{i_\Sigma sw}$ is the accumulated switching energy for the ith SM, $E_{\Sigma sw_avg}$ is the average accumulated switching energy for N SMs. The output of the imbalance degree extractor for SM [1] can be derived according to (3) and (4) as (5), and further simplified as γ. Since the number of SM per arm is normally larger than 20 in practical MMC applications with NLM [19], γ is in general around 1.

$$y_1 = \frac{\Delta E_{1_\Sigma sw}}{E_{\Sigma sw_avg}} = \frac{E_{1_\Sigma sw} - E_{\Sigma sw_avg}}{E_{\Sigma sw_avg}} = \frac{(N-1)\,\gamma}{\gamma + N} \approx \gamma, \tag{5}$$

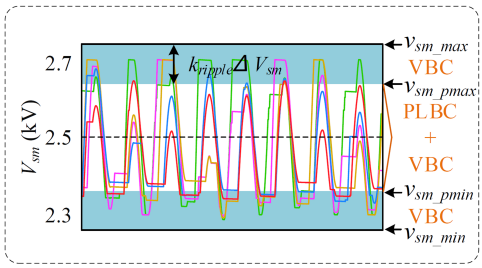

Fig. 5. Operating principle of the PLBC enable module (shown in Fig. 4).

where y_1 and $\Delta E_{1_\Sigma sw}$ are the output of imbalance degree extractor and deviation of accumulated switching energy for SM [1].

It can be seen that γ is the only sensitive parameter for the imbalance degree extractor, which can be used for power loss balancing control. The number of fundamental period N_p for accumulating switching energy per control cycle needs to be chosen since it determines how many switching actions can be used for balancing purpose together with the switching frequency. The average switching frequency for the SMs is 181 Hz in the case study, which means that 7.2 switching actions on average can be used in one fundamental period. Thus, N_p is set as 10 to achieve a relatively high control flexibility utilizing about 72 switching transients in total. Note that N_p is tuned according to the equivalent switching frequency to secure a minimum number of switching actions for the balancing control.

C. PLBC regulator

The function of the PLBC regulator is twofold. One is to adjust its sensitivity to the imbalance degree by altering the threshold of the saturation ($\pm\gamma_{\max}$). The other is to weight the PLBC and the capacitor voltage balancing control (VBC) through changing k_{ripple}, which determines the peak value of the PLBC regulator output. It should be noted that capacitor VBC is always supposed to be given higher priority to secure the normal operation of MMCs. By contrast, PLBC is a secondary objective, which is beneficial to performance optimization of MMC. Therefore, PLBC should not be as aggressive as the capacitor VBC. Otherwise, a larger output of PLBC regulator will result in a higher virtual capacitor voltage for sorting, which might lead to the divergence of the actual capacitor voltage. Moreover, the voltage threshold can be reached much easier regarding to an aggressive PLBC, which will introduce extra switching actions and switching power loss. This is not preferable for practical operation. On the contrary, a small output might weaken the PLBC performance. In this paper, $\gamma_{\max}$ is set as 0.75 and k_{ripple} is set as 0.3.

D. PLBC Enable Module

PLBC enable module is implemented to leave certain control margin for the voltage balancing control (VBC), which means that only VBC is enabled in this range when the actual capacitor voltage exceeds the thresholds, namely $V_{sm_p\max}$ and $V_{sm_p\min}$. They can be set as

$$\begin{cases} V_{sm_\max} = V_{sm_p\max} + k_{ripple}\Delta V_{sm} \\ V_{sm_\min} = V_{sm_p\min} - k_{ripple}\Delta V_{sm}, \end{cases} \tag{6}$$

where $V_{sm_\max}$ and $V_{sm_\min}$ are the capacitor voltage ripple limitations, they are normally under 10% of the rated capacitor voltage, and $V_{sm_p\max}$ and $V_{sm_p\min}$ are the thresholds for disabling the PLBC.

IV. Simulation Verifications

The effectiveness of the proposed power loss balancing control is verified through simulations based on a 30 MVA - 50 kV three-phase MMC with 20 SMs per arm. Two scenarios are simulated, namely the pure active and the pure reactive power transfer. Results are shown in Fig. 6 and Fig. 7 with the accumulated switching energy, the capacitor voltage, the imbalance degree among SMs, and the total power loss.

The spread of switching energy among SMs can be seen from Fig. 6 (a), and the imbalance degree decreases from 50 % to 25 % for control with/without the PLBC observed from Fig. 6 (e). The capacitor voltage ripple remains the same as 10 % of the rated voltage, which is guaranteed by the PLBC enable module. However, it should be noted that the total power loss per arm increases about 1.2 %. It corresponds to the efficiency decrease of the MMC of 0.0048%.

The power loss imbalance is much more severe when pure reactive power is transferred through the MMC as illustrated in Fig. 7. In this case, the maximum imbalance degree is higher than 100 %, which means that certain SM dissipates almost two times the switching loss of other SMs. The loss difference poses a challenge to the reliability of the SM as well as the cooling system design. By contrast, with the help of PLBC, the imbalance degree is reduced to under 20 % as shown in Fig. 7 (e). Moreover, the performance of the capacitor voltage ripple and the total power loss of the MMC are not deteriorated compared with the traditional control without PLBC.

V. Conclusion

This paper proposes a new active thermal control method for the IGBTs in a Modular Multi-level Converter (MMC) based on the switching loss balance control. The switching loss imbalance due to modulation and uneven sub-module capacitance are analyzed. A trade-off between the switching loss balance control and the capacitor voltage control is identified to support the design when enabling the proposed control strategy. In a case study of 30 MW MMC, the IGBT power loss imbalances are reduced from around 50% and 100% to about 25% and 20% under the scenario of unity power factor and pure reactive power transfer, respectively. The results serve as a proof-of-concept of the effectiveness of the proposed control.

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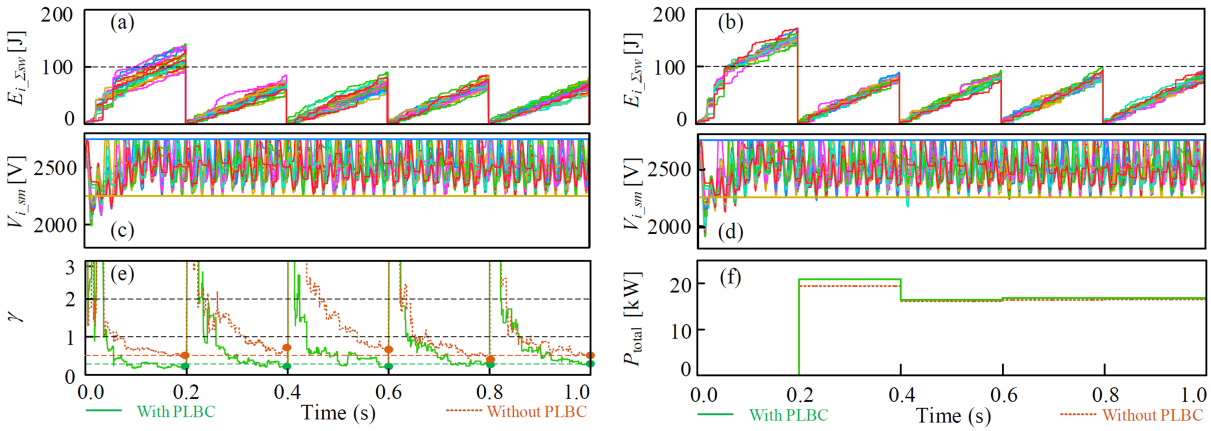

Fig. 6. Simulation results under pure active power transfer: a) and b) Accumulated switching energy without/with the PLBC; c) and d) SM voltage without/with the PLBC; e) Imbalance degree with/without PLBC; f) Total power loss of one arm averaged in 0.2 s with/without PLBC.

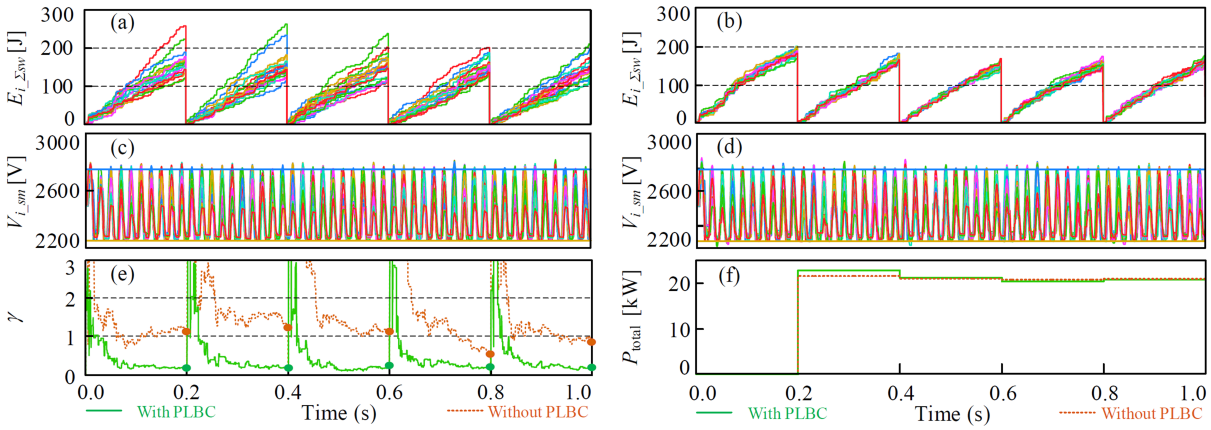

Fig. 7. Simulation results under pure reactive power transfer: a) and b) Accumulated switching energy without/with the PLBC; c) and d) SM voltage without/with the PLBC; e) Imbalance degree with/without PLBC; f) Total power loss of one arm averaged in 0.2 s with/without PLBC.

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