Input current interharmonics in adjustable speed drives caused by fixed-frequency modulation techniques

Soltani, Hamid; Davari, Pooya; Loh, Poh Chiang; Blaabjerg, Frede; Zare, Firuz

Published in:
Proceedings of IEEE Applied Power Electronics Conference and Exposition 2016 (APEC)

DOI (link to publication from Publisher):
10.1109/APEC.2016.7467877

Publication date:
2016

Input current interharmonics in Adjustable Speed Drives caused by fixed-frequency modulation techniques

Hamid Soltani, Pooya Davari, Poh Chiang Loh, and Frede Blaabjerg
Department of Energy Technology
Aalborg University
Aalborg East, Denmark
hso@et.aau.dk, pda@et.aau.dk, pcl@et.aau.dk, fbl@et.aau.dk

Firuz Zare
Danfoss Drives A/S
Global Research & Development Centre
Ulsnaes 1, DK-6300 Graasten, Denmark
fza@danfoss.com

***Abstract*—Adjustable Speed Drives (ASDs) based on double-stage conversion systems may inject interharmonics distortion into the grid, other than the well-known characteristic harmonic components. The problems created by interharmonics make it necessary to find their precise sources, and, to adopt an appropriate strategy for minimizing their effects. This paper investigates the ASD′s input current interharmonic sources caused by applying symmetrical regularly sampled fixed-frequency modulation techniques on the inverter. The interharmonics generation process is precisely formulated and comparative results of different fixed-frequency modulation techniques are presented to evaluate the drive input current interharmonic components. The theoretical analysis and simulation studies are validated with experimental results on a 2.2 kW motor drive system.**

I. Introduction

Adjustable speed drives based on double-stage conversion systems are considered as one of the major sources of interharmonics in the grid, other than the well-known characteristic harmonics [1]. Fig. 1 illustrates the typical block diagram of a double-stage voltage source inverter-fed ASD, where a three-phase front-end diode rectifier is connected back-to-back to a rear-end inverter sharing a common DC link. With connecting two systems running at separate frequencies, the ASD operation can result in interharmonic distortions at both terminals via interactions between the associated harmonics.

Interharmonics are spectral components of voltages or currents, which are not multiple integer of the fundamental supply frequency [2]. Although small in magnitude, interharmonics may cause their own unique problems as well as those in common with the harmonic distortions [3], [4]. The problems mainly have roots in the interharmonic characteristics, where they can spread at a wide range in the frequency spectrum. Light flicker, sideband torques on the motor/generator shaft, interference with control and protection signals, dormant resonance excitations are some of the most significant negative effects caused by interharmonic distortions [5]–[8].

Over the years, many investigations have been dedicated to interharmonics issue, mainly by considering their origins, negative effects on the power supply, accurate detections and identification methods [9]–[19]. Moreover, the accurate

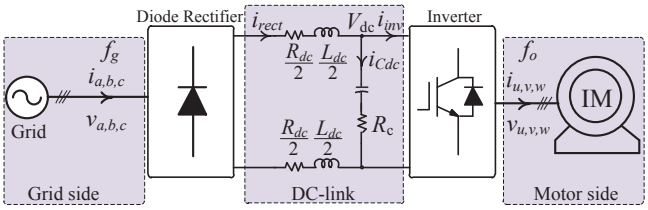

Fig. 1. Equivalent circuit diagram of a typical adjustable-speed drive for system analysis with an Induction Motor (IM).

modeling of the ASD for interaction analysis of interharmonics has initiated several studies [20]–[22]. The ASD interharmonic analyses at the presence of the output currents imbalance, and also, the unbalanced supply side voltages have been investigated in [8], [23]. In addition to the above-mentioned studies, the authors in [24], [25] proposed active compensation methods in order to reduce the drive input current interharmonics at the presence of load currents imbalance.

Interharmonics are usually smaller than the characteristic harmonics and this is why less attention has been devoted to them compared with harmonics issue. But with the rapid growth of power electronic applications, and consequently increasing the interharmonics distortion in the grid, special concerns have been raised to define limitations for interharmonics in respect to their frequencies and amplitudes.

Besides several investigations done so far related to interharmonics, a precise mapping of their origins in ASD applications has always been a challenging issue. This mapping should cover all the operating points of the ASD. Prediction of the drive input current interharmonic frequencies corresponding with a specific operating condition of ASD can prevent undesirable interference with control and protection signals in the power system. With knowing the interharmonics frequencies, the potential dormant resonance excitations can also be avoided.

The authors in [26] have evaluated the interharmonics generation process in ASDs, where a naturally sampled Sinusoidal Pulse Width Modulation (SPWM) technique with

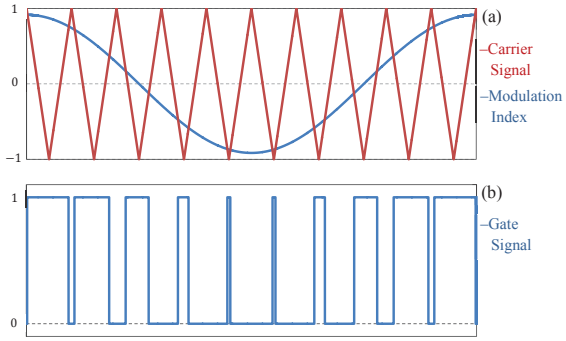

Fig. 2. (a) Symmetrical naturally sampling modulation technique, (b) Switching pulse train for inverter.

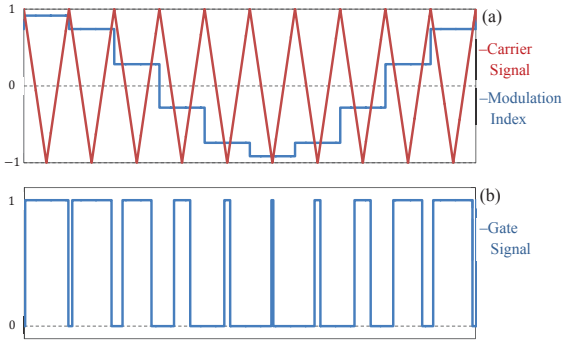

Fig. 3. (a) Symmetrical regular sampling modulation technique, (b) Switching pulse train for inverter.

low switching frequency has been considered for the inverter operation. Introducing proper definitions for the input side, the DC link and the output side harmonics and interharmonics can make it useful for understanding the harmonics interactions and consequently the associated interharmonics.

In this paper, a general analysis is proposed to find the ASD′s input current interharmonic components caused by applying symmetrical regularly sampled fixed-frequency modulation techniques on the inverter. The Space Vector Modulation (SVM) and Discontinuous Pulse Width Modulation-30 degree lagging clamp (DPWM2) are investigated as the most commonly used modulation techniques in motor drive applications. The reference is made to ideal supply conditions in order to only evaluate those interharmonics generated by the interaction between the front-end diode rectifier and the rear-end inverter.

First, the harmonics transfer from the inverter output side to the rectifier input side, which leads to the drive input current interharmonic components is comprehensively formulated in Section II. As a result, the drive input current interharmonic frequencies can precisely be obtained. Thereafter in Section III, a comparative evaluation addresses the results obtained for the symmetrical regularly sampled SVM and DPWM2 techniques. Although the interharmonics amplitude estimation is so complicated due to uncertainties in the system, the obtained results indicate that the DPWM2 may not be suitable choice of modulation from an interharmonics point of view. Finally, the theoretical analysis and simulation studies are validated with experimental results performed on a 2.2 kW ASD.

II. Interharmonics Generation Process

In a double-stage voltage source inverter fed ASD, shown in Fig. 1, the input three-phase AC voltages are rectified first by the diode rectifier to provide a DC voltage for powering the inverter. The DC link is made up of a capacitor and two inductors to make a smoother voltage and current at the DC stage. The inverter then converts the DC voltage to a set of three-phase balanced voltages for driving the motor. The fundamental frequency of the inverter is determined by the demanded motor speed, which typically is not the same as the grid frequency.

A. Harmonic Transfer at Inverter Level

Referring to Fig. 1, in a two-level pulse width modulation strategy, the inverter output pulse trains are generated by comparing two independent periodic signals; a low-frequency reference signal against a high frequency carrier signal. Fig. 2 illustrates the symmetrical naturally sampled PWM technique, where the intersections between the reference sinusoid and the triangle carrier determine the switching pulse edges. The resultant pulsating voltages (which are periodic with respect to the modulated and the modulating signals) harmonic components can be obtained by using the double Fourier integral approach. As a result of this evaluation, the pulsating output voltages v_x $(x = u, v, w)$ are composed of a DC offset, baseband harmonics (simple harmonics of the fundamental output frequency f_o), harmonics of the carrier frequency f_c, and carrier sidebands located around the carrier components [27], and they can generally be represented as

$$\begin{aligned} v_x(t) = \tfrac{A_{00}}{2} + \sum_{n=1}^{\infty} [A_{0n}\cos(n[w_o t - p\tfrac{2\pi}{3}]) \\ + B_{0n}\sin(n[w_o t - p\tfrac{2\pi}{3}])] \\ + \sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} [A_{mn}\cos(mw_c t + n[w_o t - p\tfrac{2\pi}{3}]) \\ + B_{mn}\sin(mw_c t + n[w_o t - p\tfrac{2\pi}{3}])] \end{aligned} \quad (1)$$

where the carrier index and the baseband index variables are notated as m and n, respectively. The fundamental and carrier angular frequencies are also presented as w_o and w_c, respectively. The p values are 0, 1 and -1 with respect to the output phases u, v and w. The harmonic coefficients A_{mn} and B_{mn}, which are defined by a double Fourier integral, can be evaluated in accordance with the selected modulation strategy. The hth harmonic component is also defined in terms of m and n, and it is given as

$$h = m(\frac{w_c}{w_o}) + n \quad (2)$$

In practical applications, it is difficult to implement the naturally sampled PWM in a digital modulation system. Consequently, the regularly sampled modulation technique has

been widely applied instead of the previous method, due to the simplicity of its implementation. In accordance to the regularly sampled PWM strategy, the reference waveform is sampled and kept constant during each carrier interval, and then, it is compared with the triangle carrier waveform, as shown in Fig. 3.

Regarding the Induction Motor (IM) as a highly inductive load, the three-phase AC output currents i_x $(x = u, v, w)$ are assumed to be sinusoidal and they are given as

$$i_u(t) = I_o \cos(w_o t + \theta) \tag{3}$$

$$i_v(t) = I_o \cos(w_o t + \theta - \frac{2\pi}{3}) \tag{4}$$

$$i_w(t) = I_o \cos(w_o t + \theta + \frac{2\pi}{3}) \tag{5}$$

with I_o and θ stated as the amplitude of the output currents and a displacement factor, respectively. Assuming that the inverter does not dissipate or generate power, under balanced load condition, the DC-link inverter-side current can be written as

$$i_{inv}(t) = \frac{1}{V_{dc}}[v_u(t) \cdot i_u(t) + v_v(t) \cdot i_v(t) + v_w(t) \cdot i_w(t)] \tag{6}$$

where V_{dc} represents the DC value of the DC-link voltage. The time-domain expression given in (6) can be applied to obtain the DC-link harmonic components caused by the rear-end inverter operation. It should be noted that the v_x/V_{dc} $(x = u, v, w)$ terms in (6) are usually referred to as inverter switching functions.

Here, in order to identify the interharmonics sources, the effects of baseband and carrier group harmonics have been studied separately. Substituting the baseband harmonic components (first summation in (1)) and (3)-(5) into (6), the corresponding DC-link oscillations i_{inv-b} can be written as (7). It is worth to mention that, in respect to the applied symmetrical regularly sampled modulation techniques, the baseband harmonics coefficients A_{0n} and B_{0n} are potentially existing for all values of n. However, further investigations of (7) show that only the triple multiples of the output frequency w_o will be transferred to the DC link under balanced condition. Thus, the contribution of baseband harmonic components on the DC-link oscillation f^h_{dc-b} can generally be presented as

$$f^h_{dc-b} = 3 \cdot k \cdot f_o\,, \qquad k = 1,\, 2,\, 3,\, ... \tag{8}$$

In respect to (8) it should be mentioned that the *odd* triple multiples of the output frequency (i.e. $3f_o$, $9f_o$, ...) are caused by the corresponding *even* order baseband harmonics of the output frequency (i.e. $\{2^{th},\, 4^{th}\}$, $\{8^{th},\, 10^{th}\}$, ...), and, the *even* triple multiples (i.e. $6f_o$, $12f_o$, ...) are generated by the associated *odd* order baseband harmonics of the output frequency(i.e. $\{5^{th},\, 7^{th}\}$, $\{11^{th},\, 13^{th}\}$, ...).

The effects of the carrier sideband harmonic components of the pulsating output voltage on the DC-link oscillations can be evaluated by the same procedure. With substitution of the carrier sideband harmonics (double summation in (1)) and (3)-(5) into (6), the associated DC-link oscillations i_{inv-s} can be obtained as (9). With a precise inspection of (9), it can be concluded that although the output pulsating voltage contains all sideband carrier harmonics corresponding with the values of m and n, the DC-link inverter-side current only inherits oscillations with the frequencies of the carrier harmonic components, and their differences from the triple multiple of the fundamental frequency w_o. Consequently, the contributions of the carrier sideband harmonics on the DC-link oscillation f^h_{dc-s} can be given as

$$f^h_{dc-s} = \{(m \cdot f_c)\,,\, (m \cdot f_c \pm 3 \cdot k \cdot f_o)\}\,, \qquad k = 1,\, 2,\, 3,\, ... \tag{10}$$

Regarding the DC-link oscillation frequencies in (10), it is worthwhile noting that the first carrier sidebands produce the carrier frequency oscillations at the DC-link. Moreover, the *odd* triplen sidebands of f^h_{dc-s} (i.e. $(m \cdot f_c) - 3f_o$, $(m \cdot f_c) - 9f_o$, ...) are caused by the corresponding *even* order sidebands of the output voltages (with the sets of n as $\{-2, -4\}$, $\{-8, -10\}$, ...), and, the *even* triplen sidebands (i.e. $(m \cdot f_c) - 6f_o$, $(m \cdot$

$$\begin{aligned} i_{inv-b}(t) = \sum_{n=1}^{\infty} [\,&\tfrac{A_{0n} I_o}{2V_{dc}}[\cos((n+1)w_o t + \theta) + \cos((n-1)w_o t - \theta) \\ &+ \cos((n+1)w_o t + \theta - (n+1)\tfrac{2\pi}{3}) + \cos((n-1)w_o t - \theta - (n-1)\tfrac{2\pi}{3}) \\ &+ \cos((n+1)w_o t + \theta + (n+1)\tfrac{2\pi}{3}) + \cos((n-1)w_o t - \theta + (n-1)\tfrac{2\pi}{3})] \\ &+ \tfrac{B_{0n} I_o}{2V_{dc}}[\sin((n+1)w_o t + \theta) + \sin((n-1)w_o t - \theta) \\ &+ \sin((n+1)w_o t + \theta - (n+1)\tfrac{2\pi}{3}) + \sin((n-1)w_o t - \theta - (n-1)\tfrac{2\pi}{3}) \\ &+ \sin((n+1)w_o t + \theta + (n+1)\tfrac{2\pi}{3}) + \sin((n-1)w_o t - \theta + (n-1)\tfrac{2\pi}{3})]] \end{aligned} \tag{7}$$

$$\begin{aligned} i_{inv-s}(t) = \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} &\tfrac{A_{mn} I_o}{2V_{dc}}[\cos(mw_c t + (n+1)w_o t + \theta) + \cos(mw_c t + (n-1)w_o t - \theta) \\ &+ \cos(mw_c t + (n+1)w_o t + \theta - (n+1)\tfrac{2\pi}{3}) + \cos(mw_c t + (n-1)w_o t - \theta - (n-1)\tfrac{2\pi}{3}) \\ &+ \cos(mw_c t + (n+1)w_o t + \theta + (n+1)\tfrac{2\pi}{3}) + \cos(mw_c t + (n-1)w_o t - \theta + (n-1)\tfrac{2\pi}{3})] \\ &+ \tfrac{B_{mn} I_o}{2V_{dc}}[\sin(mw_c t + (n+1)w_o t + \theta) + \sin(mw_c t + (n-1)w_o t - \theta) \\ &+ \sin(mw_c t + (n+1)w_o t + \theta - (n+1)\tfrac{2\pi}{3}) + \sin(mw_c t + (n-1)w_o t - \theta - (n-1)\tfrac{2\pi}{3}) \\ &+ \sin(mw_c t + (n+1)w_o t + \theta + (n+1)\tfrac{2\pi}{3}) + \sin(mw_c t + (n-1)w_o t - \theta + (n-1)\tfrac{2\pi}{3})] \end{aligned} \tag{9}$$

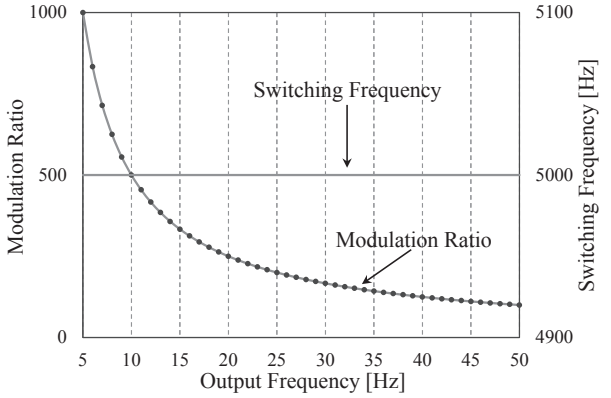

Fig. 4. The inverter switching frequency and the corresponding modulation ratio at different output frequency f_o variation range.

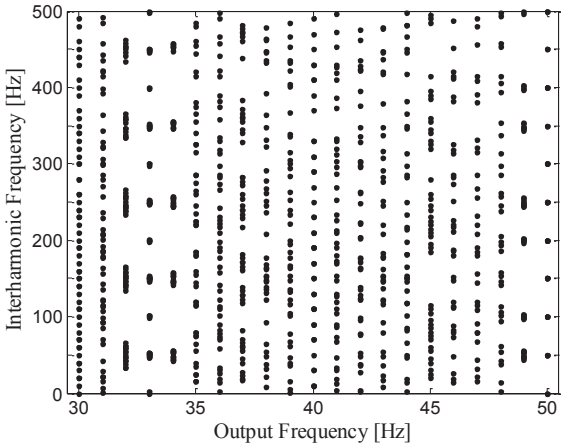

Fig. 5. ASD input current i_a interharmonics frequency location with respect to output frequency f_0 variations, by using (15).

$f_c) - 12f_o$, ...) are produced by the related *odd* order sideband carriers of the output voltages (with the sets of n as $\{-5, -7\}$, $\{-11, -13\}$, ...).

The general expression for the DC-link inverter-side current oscillations, inherited from the switching operation of the inverter can then be obtained with combining (8), and (10) and it can be written as

$$f_{dc}^h = \{f_{dc-b}^h\,,\, f_{dc-s}^h\} \tag{11}$$

B. Harmonic Transfer at Rectifier Level

The DC-link inverter-side current oscillations, after flowing through the DC link stage, will be multiplied by the well-known six-pulse diode rectifier switching functions $\{S_a(t), S_b(t), S_c(t)\}$, defined in (12)-(14),

$$\begin{aligned} S_a(t) = 2\sqrt{3}/\pi[&\cos(w_g t) - 1/5\,\cos(5w_g t) \\ &+1/7\,\cos(7w_g t)\, - 1/11\,\cos(11w_g t) + ...] \end{aligned} \tag{12}$$

$$S_b(t) = S_a(t - T/3) \tag{13}$$

$$S_c(t) = S_a(t + T/3) \tag{14}$$

where the grid voltage fundamental period and the angular frequency are notated as T and w_g.

The modulation between the DC-link harmonics, caused by inverter operation, and the rectifier switching functions results in the input current interharmonic frequencies, and can be expressed as

$$f_{ih} = \left|[6 \cdot (v-1) \pm 1] \cdot f_g \pm f_{dc}^h\right| \qquad v = 1,\ 2,\ 3, ... \tag{15}$$

with f_g stated as the input voltage fundamental frequency.

Fig. 4 illustrates the selected modulation strategy for the inverter, where the switching frequency is considered a constant value of 5 kHz during the output frequency f_o variations from 5 Hz to 50 Hz. The drive input current interharmonic locations, obtained using (15), are plotted in Fig. 5, only for the output frequency f_o range of 30 Hz to 50 Hz. It should be noted that, for plotting Fig. 5, the interactions between the three significant AC side harmonics (with $v = 1,\ 2$ in (15)) and the following DC-link harmonics have been considered:

- the DC-link harmonics below 400 Hz caused by output-side baseband harmonics
- the DC-link harmonics below 300 Hz caused by the first carrier group sidebands
- the DC-link harmonics below 300 Hz caused by the second carrier group sidebands

As it can be observed in Fig. 5, the drive input current interharmonics change their locations with respect to output frequency variations. Most interharmonics overlaps occur at the output frequencies of 33 Hz and 50 Hz, where the interharmonics accommodate at the input side harmonic frequencies and very close to them.

III. Simulation and Laboratory Test Results

The calculation presented in Section II was a general evaluation of the drive input-side current interharmonics with respect to output frequency variations, when a symmetrical regularly sampled modulation strategy is adopted. This strategy is normally implemented in a fixed-frequency modulation technique. To validate the accuracy of the theoretical analysis, a set of simulation and experimental tests were considered based on the adjustable speed drive system shown in Fig. 1 with the parameter values listed in Table I. In this investigation, the most common modulation techniques in ASDs (i.e. SVM and DPWM2) were evaluated in terms of the drive input current interharmonics.

TABLE I
Simulation and Experimental Parameters Values.

Symbol	Parameter	Value
$v_{a,b,c}$	Grid phase voltage	225 V_{rms}
f_g	Grid frequency	50 Hz
L_{dc}, R_{dc}	DC link inductor & resistor	8 mH, 360 mΩ
C_{dc}, R_c	DC Link Capacitor & Resistor	125 μF & 500 mΩ
f_{sw}	Inverter switching frequency	5 kHz
v_{LL}	Induction motor rated voltage	380 V_{rms}
P_{IM}	Induction motor rated power	2.2 kW

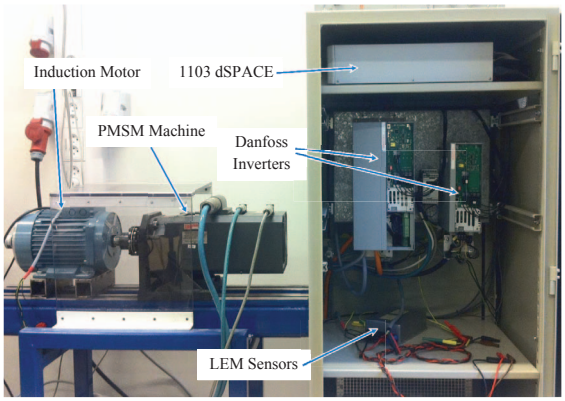

Fig. 6. Laboratory setup for experimental verification.

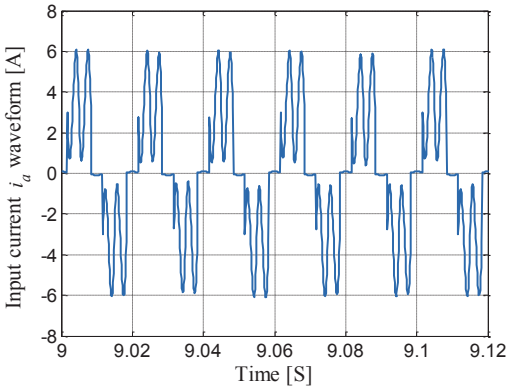

Fig. 8. The simulated ASD input current i_a, when the induction motor is operating at the output frequency f_o= 40 Hz and with a load torque value of 12 Nm using SVM.

Fig. 6 shows the employed experimental setup using two Danfoss inverters rated at 2.2 kW and 10 kW. Moreover, a California MX30 three-phase grid simulator was used to remove the potential grid background distortion. The induction motor is controlled with a constant Voltage-to-Frequency (V/F) strategy using a 2.2 kW inverter, and, the load torque was implemented by controlling a Permanent Magnet Synchronous Machine (PMSM) coupled with the induction motor via a 10 kW inverter. The control algorithm was executed on a dSPACE1103 real-time platform.

A. SVM Modulation Technique

The space vector modulation technique is an advanced, computation-intensive and arguably the best among all PWM strategies for adjustable speed drive applications, where the neutral point of the load is normally isolated. This method considers the interaction of the inverter output phases and optimizes the harmonic content of the three-phase induction motor. In this respect, the ASDs interharmonic components, when a SVM modulation technique is implemented on the inverter, can be subjected to further investigation.

The phase-u reference waveform for applying the space vector modulation is drawn in Fig. 7. By applying a (V/F) control strategy and also considering the drive operating condition, the

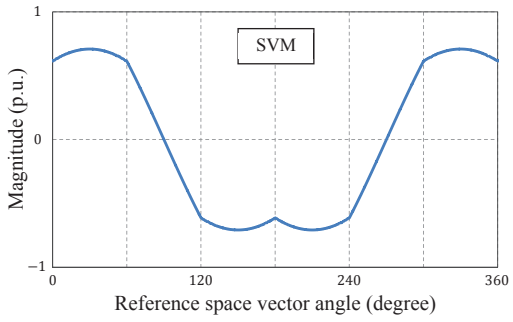

Fig. 7. Phase-u reference waveform for SVM scheme with modulation index M=0.818. The induction motor is controlled with V/F technique at the output frequency f_o= 40 Hz.

modulation index M will be close to 0.818, when the motor is working at the output frequency of 40 Hz. The simulated drive input current i_a waveform is illustrated in Fig. 8, where the SVM modulation technique has been selected as the rear-end inverter switching strategy. The input current i_a interharmonic components obtained using the MATLAB simulation and experimental results are shown in Fig. 9. The interharmonics frequency mapping, as already shown in Fig. 5, has been rescaled in Fig. 9(c) for further clarification. An intersection between the horizontal line at the output frequency f_o of 40 Hz with the plotted black points in Fig. 9(c) results in the corresponding drive input current interharmonic frequencies. As it can be observed, the interharmonics locations obtained using the theoretical analysis in (15) are in good agreement with the MATLAB simulation and experimental results, as illustrated in Figs. 9(a) and (b).

B. DPWM2 Modulation Technique

The discontinuous pulse width modulation-30 degree lagging clamp (DPWM2) scheme, which clamps the inverter pole terminals to the positive and negative terminals of the DC link for a 60° interval each in a fundamental period, is shown in Fig. 10. Since it usually is preferred to avoid the switching when the current through the devices is near its peak value, applying the DPWM2 technique can be found suitable for the applications where the power factor pf is close to 0.866 lagging such as the motor drive application.

Fig. 11 shows the adjustable speed drive input current i_a interharmonics, when the motor is operating at the output frequency f_o of 40 Hz and having a load torque value of 12 Nm, and, a DPWM2 modulation technique is selected for the inverter operation. Like the SVM modulation technique, the reference waveform modulation index M for the inverter operation is close to 0.818 to provide the desired output voltage fundamental frequency based on the selected (V/F) control strategy. As it can be seen in Fig. 11, there is a good agreement between the simulation and experimental results, and the plotted interharmonic frequencies. It is worth to note that the presence of two distinctive interharmonic components

at 70 Hz and 170 Hz is due to higher amplitude of the DC-link third harmonic (of the output frequency) oscillation. As already discussed in Section II, the DC-link third harmonic (of the output frequency) oscillation is basically generated by the second and the fourth order frequency of output voltages.

Generally, addressing the drive input current interharmonics amplitude is a complicated topic, which needs a very precise model of interharmonics interactions, when the ASD is working at different operating conditions. This issue will be more sophisticated knowing that the interharmonics may usually have some overlaps at specific frequencies. In the overlap condition they could easily cancel or intensify each others. But theoretically, the inverter modulation index M, the switching frequency f_{sw} and the passive filter components of the drive

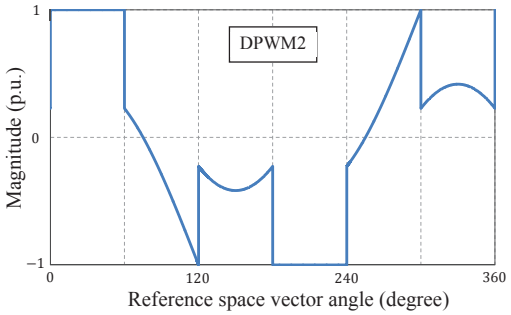

Fig. 10. Phase-u reference waveform for DPWM2 scheme with a modulation index M=0.818. The induction motor is controlled with V/F technique at the output frequency f_o= 40 Hz.

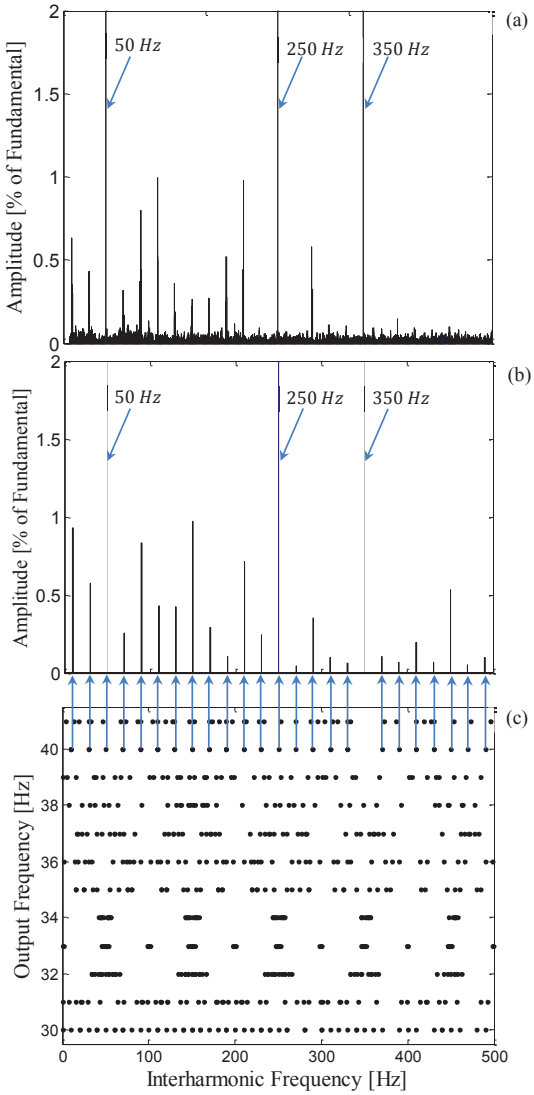

Fig. 9. Drive input current i_a interharmonics at the output frequency f_o= 40 Hz and load torque value of 12 Nm with applying SVM modulation technique: (a) Experimental result, (b) Simulation result, and (c) Output frequency versus estimated interharmonic frequencies using (15).

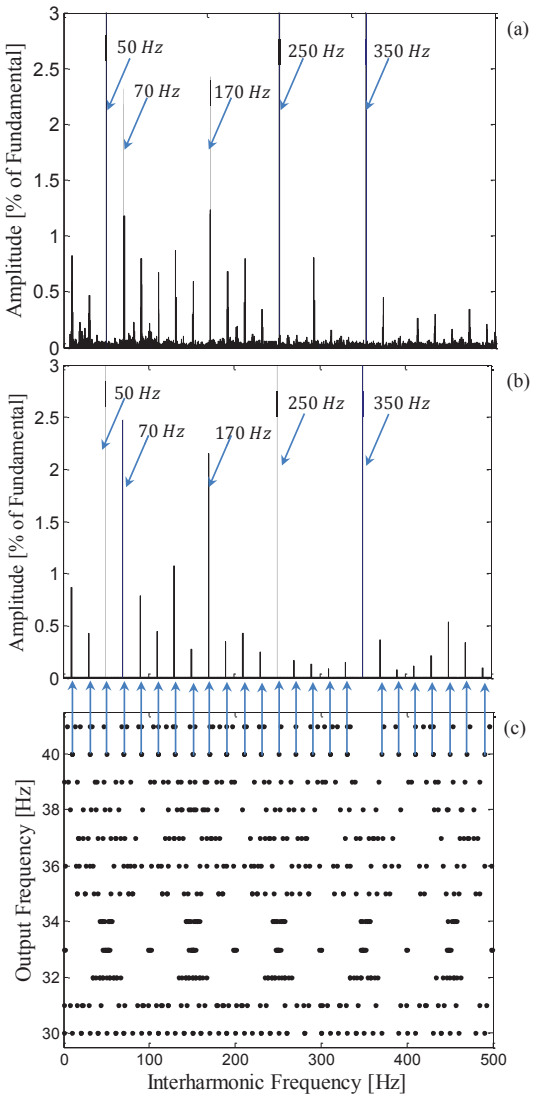

Fig. 11. Drive input current i_a interharmonics at the output frequency f_o= 40 Hz and load torque value of 12 Nm with applying DPWM2 modulation technique: (a) Experimental result, (b) Simulation result, and (c) Output frequency versus estimated interharmonic frequencies using (15).

will determine which modulation strategy may result in lower amplitude input current interharmonics in ASDs.

IV. Conclusion

In this paper, the adjustable speed drive input current interharmonics generated by double-edge symmetrical regularly sampled modulation strategies have comprehensively been analyzed. The investigation has been done at two different fixed-frequency pulse width modulation techniques (i.e. SVM, DPWM2). The harmonics transfer from the output side of the rear-end inverter to the input side of the front-end diode rectifier, which causes the interharmonics distortion, has been analyzed with respect to the baseband harmonics and the carrier sideband harmonics separately. Then, the drive input current interharmonic frequencies have been plotted using the proposed analysis. Finally, the results obtained by MATLAB simulation and experimental tests demonstrate accuracy of the analytical calculations. The investigations provide a precise benchmark for estimating the ASD′s input current interharmonic frequencies, which help to choose the correct frequency resolution for the DFT spectrum analysis.

With respect to the interharmonics amplitudes, it has been shown that applying the DPWM2 modulation technique may give rise to higher interharmonic amplitudes compared with the SVM modulation technique, when the ASD is operating at high switching frequency.

References

[1] P. Davari, Y. Yang, F. Zare, and F. Blaabjerg, "A multi-pulse pattern modulation scheme for harmonic mitigation in three-phase multi-motor drives," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. PP, no. 99, pp. 1–12, Jul. 2015.

[2] A. Testa, M. Akram, R. Burch, G. Carpinelli, G. Chang, V. Dinavahi, C. Hatziadoniu, W. Grady, E. Gunther, M. Halpin *et al.*, "Interharmonics: theory and modeling," *IEEE Trans. Power Del.*, vol. 22, no. 4, pp. 2335–2348, Oct. 2007.

[3] D. Gallo, R. Langella, A. Testa, and A. Emanuel, "On the effects of voltage subharmonics on power transformers: a preliminary study," in *Proc. 11th ICHQP*, Lake Placid, NY, 2004, pp. 501–506.

[4] J. de Abreu and A. Emanuel, "Induction motor thermal aging caused by voltage distortion and imbalance: loss of useful life and its estimated cost," *IEEE Trans. Ind. Appl.*, vol. 38, no. 1, pp. 12–20, Jan. 2002.

[5] D. Gallo, C. Landi, R. Langella, and A. Testa, "IEC flickermeter response to interharmonic pollution," in *Proc. 11th ICHQP*, Lake Placid, NY, 2004, pp. 489–494.

[6] M. Hernes and B. Gustavsen, "Simulation of shaft vibrations due to interaction between turbine-generator train and power electronic converters at the visund oil platform," in *Proc. IEEE Power Convers. Conf. (PCC)*, 2002, pp. 1381–1386.

[7] C. Bowler, "Proposed steady-state limits for turbine-generator torsional response," in *Proc. IEEE Summer Power Meeting*, 2002.

[8] D. Basic, "Input current interharmonics of variable-speed drives due to motor current imbalance," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2797–2806, Oct. 2010.

[9] R. Yacamini, "Power system harmonics. Part 4: Interharmonics," *Power Eng. J.*, vol. 10, no. 4, pp. 185–193, Aug. 1996.

[10] E. W. Gunther, "Interharmonics in power systems," in *Proc. IEEE Power Eng. Soc. Summer Meeting*, 2001, pp. 813–817.

[11] D. Gallo, R. Langella, and A. Testa, "On the processing of harmonics and interharmonics in electrical power systems," in *Proc. IEEE Power Eng. Soc. Winter Meeting*, 2000, pp. 1581–1586.

[12] M. Rifai, T. H. Ortmeyer, and W. J. McQuillan, "Evaluation of current interharmonics from AC drives," *IEEE Trans. Power Del.*, vol. 15, no. 3, pp. 1094–1098, Jul. 2000.

[13] G. Chang, C. Chen, Y. Liu, and M. Wu, "Measuring power system harmonics and interharmonics by an improved fast Fourier transform-based algorithm," *IET Gener. Transm. Distrib.*, vol. 2, no. 2, pp. 193–201, Mar. 2008.

[14] C.-I. Chen and Y.-C. Chen, "Comparative study of harmonic and interharmonic estimation methods for stationary and time-varying signals," *IEEE Trans. Ind. Electron.*, vol. 61, no. 1, pp. 397–404, Jan. 2014.

[15] F. Cupertino, E. Lavopa, P. Zanchetta, M. Sumner, and L. Salvatore, "Running DFT-based PLL algorithm for frequency, phase, and amplitude tracking in aircraft electrical systems," *IEEE Trans. Ind. Electron.*, vol. 58, no. 3, pp. 1027–1035, Mar. 2011.

[16] I. Y.-H. Gu and M. H. Bollen, "Estimating interharmonics by using sliding-window ESPRIT," *IEEE Trans. Power Del.*, vol. 23, no. 1, pp. 13–23, Jan. 2008.

[17] G. W. Chang and C.-I. Chen, "An accurate time-domain procedure for harmonics and interharmonics detection," *IEEE Trans. Power Del.*, vol. 25, no. 3, pp. 1787–1795, Jul. 2010.

[18] D. Gallo, R. Langella, and A. Testa, "A self-tuning harmonic and interharmonic processing technique," *Eur. Trans. Elect. Power*, vol. 12, no. 1, pp. 25–31, Jan./Feb. 2002.

[19] C.-I. Chen and G. W. Chang, "An efficient Prony-based solution procedure for tracking of power system voltage variations," *IEEE Trans. Ind. Electron.*, vol. 60, no. 7, pp. 2681–2688, Jul. 2013.

[20] W. Xu, H. W. Dommel, M. B. Hughes, G. W. Chang, and L. Tan, "Modelling of adjustable speed drives for power system harmonic analysis," *IEEE Trans. Power Del.*, vol. 14, no. 2, pp. 595–601, Apr. 1999.

[21] R. Carbone, F. De Rosa, R. Langella, and A. Testa, "A new approach for the computation of harmonics and interharmonics produced by line-commutated AC/DC/AC converters," *IEEE Trans. Power Del.*, vol. 20, no. 3, pp. 2227–2234, Jul. 2005.

[22] G. W. Chang and S. K. Chen, "An analytical approach for characterizing harmonic and interharmonic currents generated by VSI-fed adjustable speed drives," *IEEE Trans. Power Del.*, vol. 20, no. 4, pp. 2585–2593, 2005.

[23] G. W. Chang, S. K. Chen, H. J. Su, and P. K. Wang, "Accurate assessment of harmonic and interharmonic currents generated by VSI-fed drives under unbalanced supply voltages," *IEEE Trans. Power Del.*, vol. 26, no. 2, pp. 1083–1091, Apr. 2011.

[24] H. Soltani, P. C. Loh, F. Blaabjerg, and F. Zare, "Interharmonic analysis and mitigation in adjustable speed drives," in *Conf. Rec. IECON 40th Annu. Meeting*, 2014, pp. 1556–1561.

[25] H. Soltani, P. Loh, F. Blaabjerg, and F. Zare, "Interharmonic mitigation of adjustable speed drives using an active DC-link capacitor," in *Proc. ICPE-ECCE Asia*, 2015, pp. 2018–2024.

[26] F. De Rosa, R. Langella, A. Sollazzo, and A. Testa, "On the interharmonic components generated by adjustable speed drives," *IEEE Trans. Power Del.*, vol. 20, no. 4, pp. 2535–2543, Oct. 2005.

[27] D. G. Holmes and T. A. Lipo, *Pulse width modulation for power converters: principles and practice*. John Wiley & Sons, 2003, vol. 18.