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Taul, Mads Graungaard; Wang, Xiongfei; Davari, Pooya; Blaabjerg, Frede

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Grid Synchronization of Wind Turbines during Severe Symmetrical Faults with Phase Jumps

Mads Graungaard Taul, Xiongfei Wang, Pooya Davari, Frede Blaabjerg
Dept. of Energy Technology
Aalborg University
Aalborg, Denmark
mkg@et.aau.dk, xwa@et.aau.dk, pda@et.aau.dk, fbl@et.aau.dk

***Abstract*—This paper investigates the performance of a converter synchronization unit during severe symmetrical faults with phase jumps. The loss of synchronization of power converters during low-voltage situations is described and restrictive current limits for stable operation are derived. In order to achieve zero-voltage ride-through capability, the phase-locked loop can be frozen during a fault to ensure stability while complying with grid codes. Since the frozen PLL approach is only applicable in the case of constant frequency and phase angle of the grid voltage, this paper investigates the performance of the frozen PLL during phase jumps and reveals whether a proposed phase compensation technique can be utilized to improve the power transfer of the converter during a severe symmetrical fault. This is done through a comprehensive simulation study where the frozen PLL is analyzed with and without phase compensation for different types of line impedance configurations. It is revealed, that even though the proposed phase compensation method can improve the injected power during a fault situation with phase jumps, a non-compensated frozen PLL can inherently ensure stability and having less complex implementation and acceptable injection of currents when compared to state-of-the-art solutions for loss of synchronization. The ride-through capability of the frozen PLL with and without the proposed compensation method is experimentally verified.**

***Index Terms*—Grid-Connection, Voltage-Source Converter, Grid Fault, Synchronization Stability, Fault Ride-Through**

I. Introduction

With an increasing share of power electronic-based power generation when compared to a conventional synchronous machine-based power system, there is concern about the stability and availability of such systems during abnormal or fault situations. This concern has forced Transmission System Operators (TSOs) and Distribution System Operators (DSOs) to require specific behavior of Distributed Generators (DGs) during irregular events.

For vector-controlled converters to comply with grid-code directives, an accurate estimation of the phase angle of the grid voltage is essential. During weak-grid or low-voltage grid conditions, the instantaneous location of the voltage at the Point of Common Coupling (PCC) can be significantly distorted or possibly even useless due to the Phase-Locked Loop (PLL) being destabilized, which causes instabilities in the current controller [1]. Although analysis of the system performance and stability during nearly zero voltage conditions has not received much attention [1]–[4], a large body of literature describes Low-Voltage Ride-Through (LVRT) capability of Renewable Energy Sources (RES). Several researchers have described Loss Of Synchronization (LOS) of the conventional Synchronous Reference Frame Phase-Locked Loop (SRF-PLL) during extremely low-voltage situations, and a handful of control scheme recommendations to mitigate LOS have previously been published. As LOS arises as a result of high network impedances, low grid voltages, and high active/reactive current injection (dependent on the network impedance), most mitigation methods are developed by modifying the injected currents during a low-voltage situation in order to stabilize the synchronization process of the converter. This includes limiting or nullifying the current injection [5], injecting a reactive/active current ratio equal to the X/R ratio of the network impedance [6], a voltage-dependent active current injection strategy [7], and methods where the active current injection is adaptively regulated based on the estimated frequency error of the PLL [8], [9].

In the case of a zero-voltage situation, none of the grid-following strategies in [5]–[9] can ride-through the fault since the voltage used for synchronization is not present. A simple approach to deal with this issue is proposed in [10], [11] where the PLL is bypassed or frozen at its current state when a low-voltage fault is detected. In this way, the converter can be observed to switch from a grid-following control mode to a grid-forming control mode where its phase angle, obtained for the disabled PLL, happens to be synchronized to the voltage at the PCC. By applying this method, the feedback path within the PLL and the coupling between injected current and estimated voltage phase angle is eliminated which allows for a stable synchronization unit for any low voltage level. This method will only be effective provided that the voltages at the PCC are not exposed to any phase jumps at the fault instant. Nevertheless, if the X/R ratio of the fault impedance is different from that of the equivalent grid impedance, phase jumps will occur and the performance of the frozen PLL structure might be compromised.

This paper aims to analyze how the advantages of using a frozen PLL structure performs during severe symmetrical faults can be extended to include phase jumps. A phase

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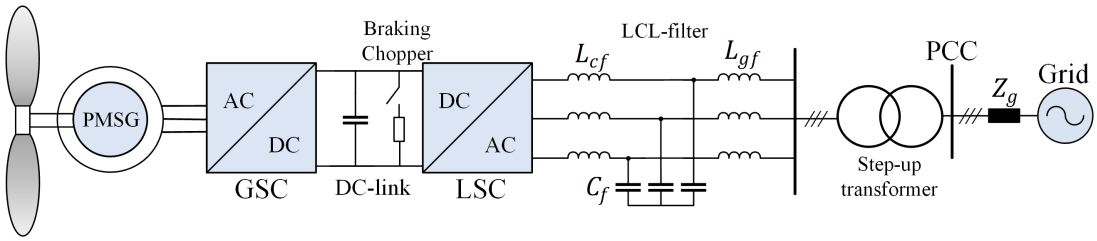


Fig. 1. Type IV wind turbine system with a full-scale power converter connected to the grid through an output LCL filter and step-up transformer. GSC: Generator-side converter, LSC: Line-side converter.

compensation technique is developed to estimate the phase jump and a comprehensive simulation study is conducted to reveal whether improvements in the power injection can be attained by implementing such a phase compensation technique in addition to the frozen PLL structure. The paper is structured as follows: The considered application together with grid requirements are presented in section II. LOS, current injection limits, how the PLL damping influences system stability, and the frozen PLL structure are discussed in section III. Section IV presents the proposed phase compensation technique, investigates how phase jumps influence the PCC voltage and the injected currents during fault events, and reveals how a frozen PLL structure with or without phase compensation has advantages compared to state-of-the-art solutions. The proposed method and findings from the analysis are experimentally verified in section V and conclusions are drawn in section VI.

II. System Overview and Grid Requirements

The system considered in this paper is a distributed generator such as a wind turbine where a full-scale power electronic converter is used to harvest the energy from the wind and deliver it to the grid in the form of sinusoidal currents, see Fig. 1. The physical parameters and control parameters used for the down-scaled system can be seen in Table I. Due to the decoupling between generator-side and line-side for a wind turbine, only the Line-Side Converter (LSC) is considered. The generator-side converter, synchronous machine and mechanical circuits of the wind turbine system are realized as a constant voltage source since the aim for this paper is to investigate the synchronization issues associated with severe grid faults and not interactions between the dc and ac side. During a low-voltage situation where the converter current is strongly limited to around 1 pu, the harvested energy from the wind turbine cannot be delivered fully to the grid. This results in surplus energy being accumulated in the dc-link capacitor resulting in over-voltages during the fault. Usually, the dc-side contains a chopper circuit used to dissipate the surplus energy during a fault which facilitates the assumption of a nearly constant dc-link voltage as depicted in Fig. 2 where the control topology used throughout this paper can also be seen.

TABLE I
MAIN PARAMETERS OF THE SYSTEM IN FIG. 1 AND FIG. 2.

Symbol	Description	Physical Value
S_b	Rated power	7.35 kVA
V_b	Nominal grid voltage	400 V
f_n	Rated frequency	50 Hz
V_n	Peak phase voltage	1 pu
V_{th}	Threshold voltage	0.9 pu
V_{dc}	dc-link voltage	730 V
L_{cf}	Converter-side inductor	0.0707 pu
L_{gf}	Grid-side inductor	0.0433 pu
C_f	Filter capacitor	0.0684 pu
f_{sw}	Switching frequency	10 kHz
f_s	Sampling frequency	10 kHz
Z_L	Line impedance	0.04+0.1j pu
$K_{p,ic}$	Proportional gain of G_{ci}	20
$K_{r,ic}$	Resonant gain of G_{ci}	10000
$K_{p,PLL}$	Proportional gain of PLL	58.28
$K_{i,PLL}$	Integral gain of PLL	267.77

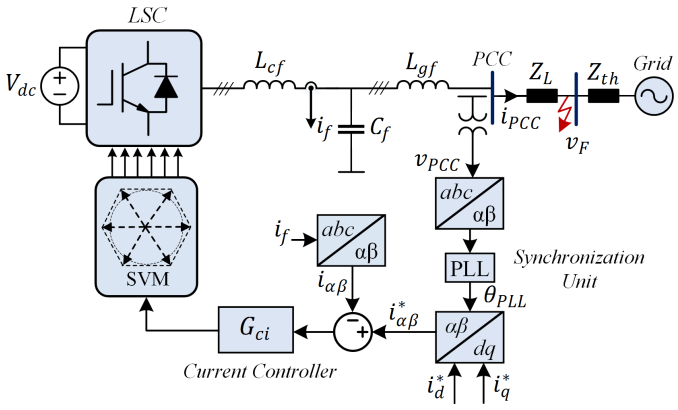
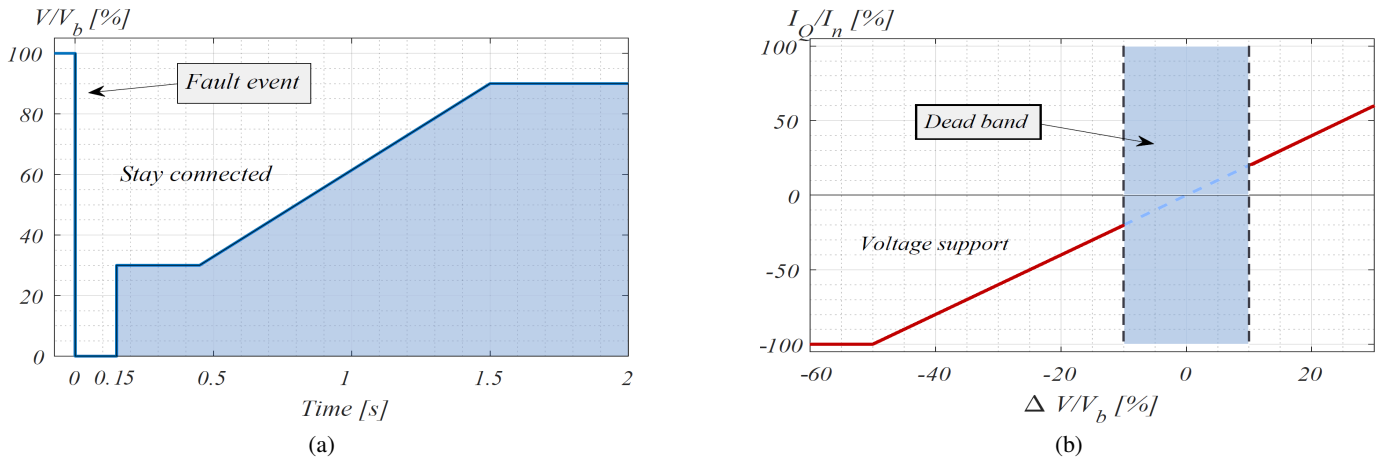


Fig. 2. Structure of grid-side converter control operated in grid-feeding mode. The red arrow indicates the location of a severe symmetrical fault.

With increasing installation of distributed generators, TSOs and DSOs have issued requirements for power converter-based RES. This implies, that such systems should tolerate deep voltage sags and provide voltage support by injecting reactive power into the grid in order to prevent a network to collapse. Such requirements are shown in Fig. 3, where it can be seen that a converter should be able to inject 1 pu of capacitive reactive power during a zero-voltage situation for up to 150 ms.



(a) (b)

Fig. 3. Grid code for wind turbines [12]. (a): Requirement from BDEW for low-voltage ride-through capability during a fault event. V is the line-to-line rms voltage. (b): Voltage support by injection of reactive current. I_n is the nominal line current and I_Q is the required reactive current to be injected.

III. Loss of Synchronization and PLL Freeze

In order to analyze LOS, the steady-state power flow between two buses is considered as presented in [9]. The power flow between two buses connected to a line, considering the effect of line resistance is shown in Fig. 4(a). In order to analyze feasible operating points of the injected current vector, the phasor diagrams shown in Fig. 4(b) and 4(c) are used. The injected current vector is referenced to the sending end voltage (V_{PCC}), which is located on the horizontal axis. The receiving end voltage (V_F) can be represented as a vector with a fixed length and variable phase angle [13]. In Fig. 4(b), one operating point for an injected current is shown. In Fig. 4(c), the current magnitude is increased causing the operating point to be exactly the limit for the summation of $-Z_L I_{PCC}$ and V_{PCC} to be equal to the fault voltage (V_F). If the current magnitude is further increased, an infeasible operating point is attempted, which leads to LOS. Using Fig. 4, the current transfer limits for an arbitrary impedance and fault voltage can be derived under steady-state conditions. In order for the summation of the voltage drop across Z_L and the PCC voltage to stay within the fault voltage magnitude (V_F), the limit situation is where the vertical component of the voltage drop is equal to the fault voltage magnitude as

$$V_F = |Z_L| I_{lim} \sin(\theta_I - \theta_Z) \quad \Longrightarrow \quad I_{lim} = \frac{V_F}{|Z_L| \sin(\theta_I - \theta_Z)}. \tag{1}$$

When injecting full capacitive reactive current ($\theta_I = -90°$), the denominator in (1) is reduced to the line resistance. This means, that the current transfer limit during reactive power injection ($i_q = -I_{lim}$) is solely determined by the voltage level at the fault location and the line resistance.

In Fig. 5(a), the fault voltage is 0.05 pu and as seen in Table I, the resistance of the line is 0.04 pu. According to (1), a stable operating point should exist for $V_F > R_L$. However, this is only true for the case where the input voltage to the PLL is adaptively normalized (see Fig. 6). This indicates that besides a feasible steady-state operating point, the dynamics of the PLL strongly determines whether this equilibrium point can be reached. As pointed out in [14], this happens due to an insufficient damping of the PLL control loop. Here it is identified, that the damping can be increased by increasing $K_{p,PLL}$ or decreasing $K_{i,PLL}$. Using the small-signal model of the PLL which is expressed as

$$\frac{\theta_{PLL}(s)}{\theta_g(s)} = \frac{UK_{p,PLL}s + UK_{i,PLL}}{s^2 + UK_{p,PLL}s + UK_{i,PLL}} \tag{2}$$

where U is the magnitude of the normalized voltage sent to the synchronization unit and comparing this to an approximation of a general second-order system

$$G_{2^{nd}}(s) = \frac{2\zeta\omega_N s + \omega_N^2}{s^2 + 2\zeta\omega_N s + \omega_N^2} \tag{3}$$

where ζ is the damping ratio and ω_N is the natural frequency, it can explicitly be observed that by using the adaptive normalized PLL structure (green structure in Fig. 6), the damping ratio is increased compared to the case of the fixed normalization term (blue structure in Fig. 6).

In Fig. 5(b), the same analysis is performed but with the voltage at the fault location decreased to 0.03 pu which according to (1) should be unstable. As anticipated, this holds true, but it can be seen that the adaptive normalized PLL, in this case, has worse performance. This is due to the fact, that when the input voltage of the PLL is only normalized relative to the nominal voltage, as shown as the blue structure in Fig. 6, then for a decreasing voltage, the dynamics of the PLL is reduced which effectively slows down the PLL and increases its robustness to grid disturbances. From the analysis shown in Fig. 5, it could be beneficial to increase the damping ratio of the PLL by using adaptive normalization of the input. However, for very low voltages, it may have the opposite effect. Therefore, in order to circumvent and remove this problem of using current transfer limits to ensure stability,

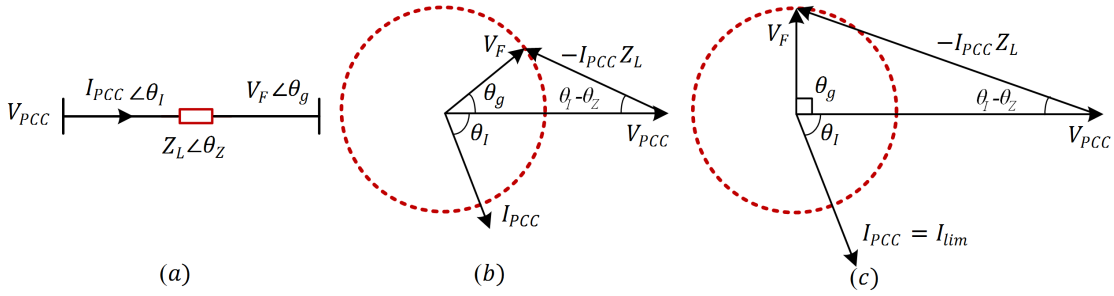
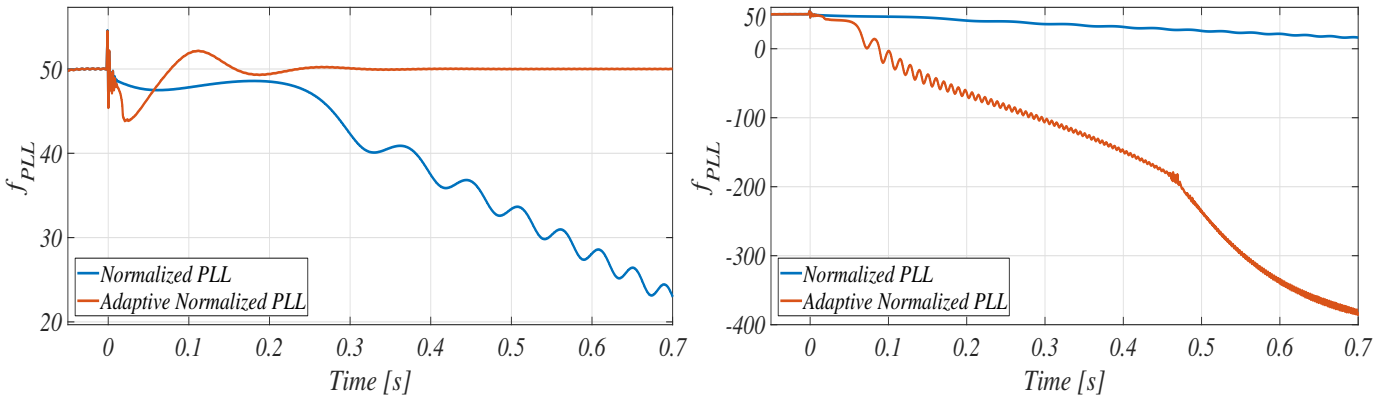


Fig. 4. Power transfer between the wind turbine connection point and fault point represented as a single line diagram and phasor diagram of current injection. The dotted red circle represents a fault voltage with constant magnitude and arbitrary angle and upper case letters denote the magnitude of the complex vector. *(a):* a stable case, *(b):* a limit case where the angle between sending end and receiving end voltage is 90° [9].



(a) Voltage at fault locations drops to 0.05 pu

(b) Voltage at fault location drops to 0.03 pu

Fig. 5. Stability analysis of PLL used to validate current transfer limits presented in (1) during a fault at 0 seconds. PLL saturation limits are not included to show the full effect of LOS.

the PLL can be frozen during the fault such that ride-through can be accomplished during any voltage level.

The process of freezing the PLL means that the action from the PI controller is bypassed (see freeze mode in Fig. 6), which effectively keeps the PLL output at the frequency it had prior to the fault. The activation of the freeze mode (nullifying the error signal in the PLL) is determined by the fault signal (S_F) and the clear signal (S_C) as seen in Fig. 6. The fault signal is set high when the length of the instantaneous v_{PCC} vector drops below a set threshold value (V_{th}) and the clear signal is set high when v_{PCC} rises above V_{th}. The freeze mode is then activated immediately when the fault signal is set high. The calculation of the clear signal is filtered to slow down its response with 20 ms compared to the fault signal. This is done to improve the resynchronization performance by keeping the PLL frozen during the transient when the fault is cleared. Freezing the PLL is a simple and robust solution to deal with LOS if it can be assumed that the voltages at the PCC terminals do not experience any phase jumps during the fault. If the fault impedance has an X/R ratio different from that of the grid impedance, then phase jumps will be present at the fault instant, which may significantly deteriorate the performance of the frozen PLL. Therefore, the subsequent section aims to analyze how the injected currents during a low voltage situation are influenced by potential phase jumps at the fault instant. Furthermore, phase compensation techniques will be proposed to compensate the phase jump when needed.

IV. Analysis of Frozen PLL during Phase Jumps

In order to compensate a potential phase jump, a proposed method which estimates the actual phase jump at the fault location is compared with a method where the instantaneous phase jump at the PCC is compensated. Using the two-bus diagram shown in Fig. 4(a) and by knowing the PCC voltage, the injected current, and the line impedance, the phase difference between the fault location and PCC voltage can be estimated. The voltage at the fault location can be expressed as

$$\boldsymbol{v_F^s} = \boldsymbol{v_{PCC}^s} - \boldsymbol{i_{PCC}^s}(R_L + sL_L) \tag{4}$$

where superscript s denotes that the complex space vector is expressed in the stationary $\alpha\beta$-reference frame and s is the Laplace variable. By applying Park's transformation matrix on both sides ($s \rightarrow s + j\omega_n$), this is transformed to the synchronous dq reference frame as

$$\boldsymbol{v_F} = \boldsymbol{v_{PCC}} - \boldsymbol{i_{PCC}}(R_L + jL_L \underbrace{(\omega + \omega_n)}_{\omega_F}) \tag{5}$$

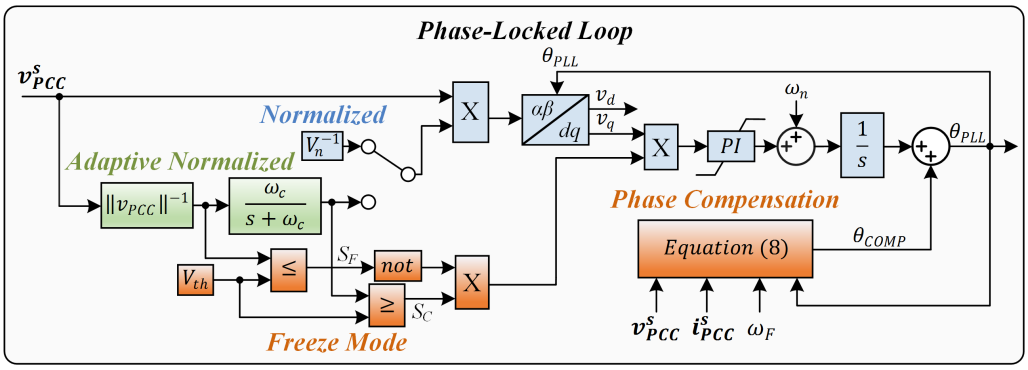


Fig. 6. Structure of proposed PLL with three configurations: normalized, adaptive normalized and freeze mode with phase compensation. ω_F is the frozen PLL angular frequency.

which can be represented by a real and an imaginary part as

$$\mathrm{Re}\{\boldsymbol{v_F}\} = v_{PCC,d} + i_{PCC,q}\omega_F L_L - i_{PCC,d}R_L \quad (6)$$

$$\mathrm{Im}\{\boldsymbol{v_F}\} = v_{PCC,q} - i_{PCC,q}R_L - i_{PCC,d}\omega_F L_L \quad (7)$$

where ω_F is the angular frequency of the frozen PLL and R_L, L_L are the resistance and inductance of the line impedance Z_L, respectively.

The term $\omega + \omega_n$ is replaced with ω_F since the estimated frequency of the frozen PLL will not change during the fault. From this, the angle difference between the voltage at the fault location and the voltage and the PCC can be calculated as

$$\theta_{COMP} = \tan^{-1}\left(\frac{\mathrm{Im}\{\mathbf{v_F}\}}{\mathrm{Re}\{\mathbf{v_F}\}}\right). \quad (8)$$

The proposed phase compensation technique is depicted in Fig. 6. Since this method compensates the phase error in a feed-forward path, a continuous feed-forward will destabilize the system since the terminal voltages and grid currents are directly fed through. To avoid this problem, the phase difference is estimated and corrected once with a single value, 15 ms after the fault, making the converter capable of injecting the desired currents 20 ms after the fault instant. Since the phase angle between the grid voltage and the voltage at the PCC is not zero prior to the fault, only the difference observed in θ_{COMP} is compensated, i.e. the absolute difference is not of interest, only the change.

One might ask why it could be necessary to estimate the phase jump behind the line impedance and not simply inspect the phase change occurring in the voltage at the PCC. In real wind turbine applications, the converter does not have any information about the voltage behind the line impedance and the converter should only react to what is happening at the PCC. However, if the phase jump occurring at the PCC is compensated using the same feed-forward structure as shown in Fig. 6, but instead by estimating the phase jump as

$$\theta_{COMP,pcc} = \tan^{-1}\left(\frac{v_{PCC,q}}{v_{PCC,d}}\right), \quad (9)$$

the injection of capacitive reactive current is noticed to be less, compared to the method presented in (8), in certain scenarios. Therefore, this method is included to analyze how the injected

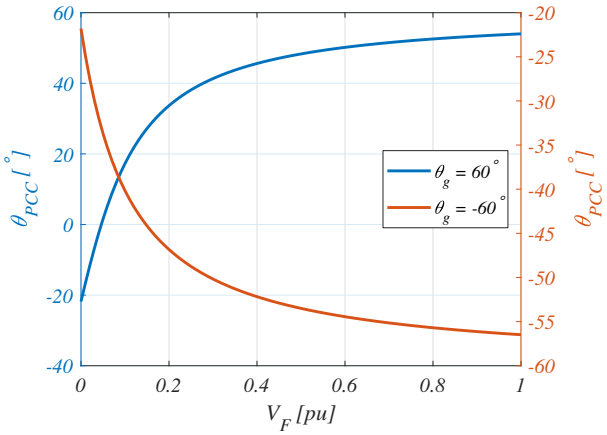


Fig. 7. Phase jump seen on the PCC as a function of the fault voltage magnitude and the sign of the phase jump happening at the fault location. The line impedance considered is $Z_L = R_L + jX_L$ and the converter is considered to inject nominal capacitive reactive current.

current vector is affected by each compensation scheme and to investigate how the PCC voltage is influenced during a fault including a phase jump.

It is noticed, that the phase change occurring at the PCC is not symmetrical with respect to the sign of the phase jump and the phase change seen on the PCC is highly dependent on the fault voltage magnitude V_F, see Fig. 7. The voltage at the PCC is

$$V_{PCC}e^{j\theta_{PCC}} = V_F e^{j\theta_g} + Z_L I_{PCC} e^{j(\theta_I + \theta_Z)} \quad (10)$$

where θ_{PCC} is given relative to θ_{PLL}. Here it can be noticed, that in the extreme situation where $V_F = 0$, the phase angle at the PCC must be $\theta_I + \theta_Z$ which during capacitive reactive current injection is $-90° + 68.2° = -21.9°$, which is seen to exactly match θ_{PCC} for either sign of θ_g in Fig. 7. This means, that when the fault voltage is extremely low, the PCC phase angle is nearly independent on the compensation angle since the converter must supply the resistive losses of the line.

A comprehensive simulation study is conducted to reveal whether the injected current vector can be improved by using phase compensation for both positive and negative phase

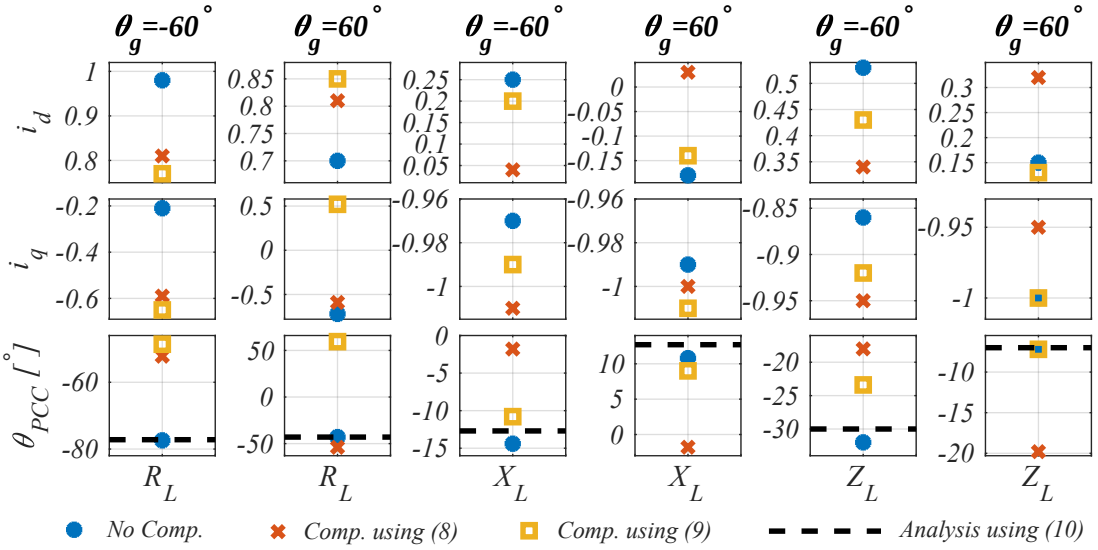


Fig. 8. Simulated case study of resulting active current, reactive current, and PCC voltage angle for different phase jumps and different types of line impedance during a fault where $V_F = 0.03$. θ_{PCC} is given relative to the constantly increasing θ_{PLL}. The ideal desired response is $i_d = 0$, $i_q = -1$, and $\theta_{PCC} = 0°$.

jumps during a fault with a voltage magnitude of 0.03 pu. To that end, the effect is also examined for three different line impedance configurations: purely resistive line, purely inductive line, and a line consisting both of a resistive and a reactive part. This analysis is shown in Fig. 8 where the two compensation methods shown in (8) and (9) are compared to the case without compensation and related to the ideal desired response ($i_d = 0$, $i_q = -1$, and $\theta_{PCC} = 0°$). Regarding the phase change happening on the PCC, it is seen that the case without compensation closely match the predicted phase change calculated from the analysis in (10), which is shown as the black dashed lines and the blue dots in Fig. 8.

For the case with Z_L and $\theta_g = -60°$ and employing the compensation technique in (8) compared to (9), the injected active current can be reduced while the injected capacitive reactive current is increased close to -1 pu. On the other hand, when $\theta_g = 60°$ for the case with Z_L, compensating the phase jump occurring at the fault location results in a decreased power injection accuracy when using (8). Also, it has no effect to compensate the phase jump using (9). Hence, for positive phase jumps in the case of Z_L, it is recommended not to compensate anything and solely use a frozen PLL structure during the fault.

For the inductive line and a positive phase jump, the compensation in (8) shows the best performance in the sense that the ideal response ($i_d = 0$, $i_q = -1$, and $\theta_{PCC} = 0°$) is nearly accomplished. For a negative phase jump, the same tendency is evident. For the resistive line, (9) shows the best performance for negative phase jumps whereas no compensation results in the best performance for positive phase jumps.

Based on the inductive and resistive line some detailed comments must be made. As seen from (1), during capacitive reactive current injection into an inductive line, the current transfer limit approaches infinity. This implies that there is no need to freeze the PLL in the first place, i.e. no need for any compensation. Moreover, one should remember, that the requirements set by the grid code are formed in order for the converter to support the voltage at the PCC. Accordingly, for a resistive grid, this is attained by maximizing the active current injection and not the injection of reactive current. Also, a short circuit fault is mainly resistive [15] which means that for a resistive grid, the phase jump will likely not occur in the first place, i.e. phase compensation is not needed. To that end, by considering that the line and grid impedance in most cases is more inductive than capacitive and knowing that most fault impedances are highly resistive, positive phase jumps are not likely to occur in any practical configuration. Applicable for any line impedance when the fault voltage is extremely low is that it is practically impossible to alter the injected currents to further boost the PCC voltage [7]. Furthermore, the system has negligible sensitivity to voltage phase jumps when V_F is low; therefore even though the current injection can be improved for negative phase jumps for the case of Z_L, one may argue that when looking at the increase in PCC voltage from using no compensation to phase compensation using (8), it is not worth the effort to compensate any phase jump for any line impedance when V_F is low. As an example, the increase in PCC voltage magnitude by using (8) compared to no compensation is only 0.007 pu for the case of Z_L and a negative phase jump. Putting all of this together, the main claims from this analysis are the following:

- A phase jump seen on the PCC is highly dependent on the line impedance and fault voltage magnitude.
- For a resistive line, phase compensation is not needed.
- For an inductive line, the PLL is not required to be frozen, i.e. phase compensation is not needed.
- Since the PCC phase angle and voltage magnitude are nearly independent of injected currents and line impedance, phase compensation can always be avoided when the fault voltage is extremely low.

Comparison of Frozen PLL to Existing Methods: The analysis performed is now related to the methods proposed in [6]–[9] which all increase the active current injection during the fault to ensure stability. In [7], $i_d > 0.4$ pu during the fault and in [8], an additional control loop is introduced to the PLL which increases the active current to 0.3-0.4 pu during a fault where $V_F = 0.02$ pu. In [9], the active current is adaptively changed based on the PLL frequency error which increases the active current to 0.2-0.5 pu dependent on the X/R ratio of the line. Thus, instead of using an additional control loop and having the inconvenience of tuning any additional controller parameters with their own stability issues, freezing the PLL will simply make the PCC voltage shift its phase in order to deliver the needed active power consumed by the line. This is exactly what the methods in [6]–[9] aim to do, but with increased control complexity.

To exemplify this, when $V_F = 0.03$ pu and no phase jump occurs, the frozen PLL structure alone result in $i_d = 0.3$, $i_q = -0.97$ and $\theta_{PCC} = -18°$ which means that by just freezing the PLL during a low voltage fault, the same or perhaps improved power injection capability can be achieved compared to the more complex methods proposed in [6]–[9]. The only disadvantage of this method is the assumption of a constant grid frequency during the fault which could be violated in future low-inertia grids. Anyhow, to avoid this limitation, a simple frequency estimation algorithm (i.e. zero-crossing technique) can be activated during the fault to correct the frozen PLL frequency if needed.

Remark: In case one wishes to compensate a negative phase jump using (8) to improve the injected currents, an estimate for the resistance and reactance of the line can be calculated as proposed in [16], [17].

V. Experimental Validation

The analysis performed in § IV is experimentally verified in the laboratory setup shown in Fig. 9 where the line-side converter is controlled using a dSPACE DS1007 PPC processor board. A severe symmetrical fault with a voltage magnitude of 0.03 pu and a phase jump of $-60°$ is considered for a line impedance consisting of both a resistive and an inductive part. The fault voltage waveform is generated using a grid simulator manufactured by Chroma. The test is performed for a frozen PLL structure with and without the aid of the proposed phase compensation method in (8). The system and control parameters used for the experimental setup are identical to the ones shown in Table. I. The experimental results are shown in Fig. 10 where values for the injected current and PCC voltage during the fault are listed in Table II. These closely match the analytical results and simulation studies shown in Fig. 8. The case with phase compensation shows some deviation from the simulated case which might be due to a low resolution of the voltage measurements when the fault voltage is low and that wires in the laboratory introduce additional resistance in the setup. To avoid the frozen PLL to suddenly be re-enabled, the reconnection is slowly ramped up which as seen in Fig. 10 gives a slow and smooth transition. As it is anticipated, even

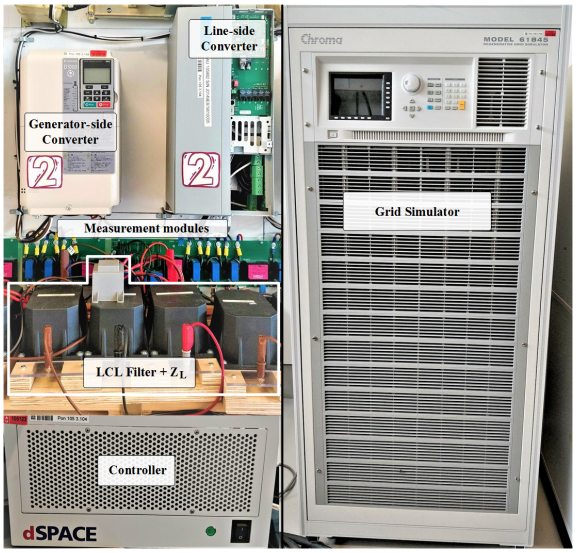


Fig. 9. Laboratory setup used to verify the simulation analysis in Fig. 8. The line-side converter is regulated using a dSPACE control platform to inject currents through a LCL filter into a grid simulator.

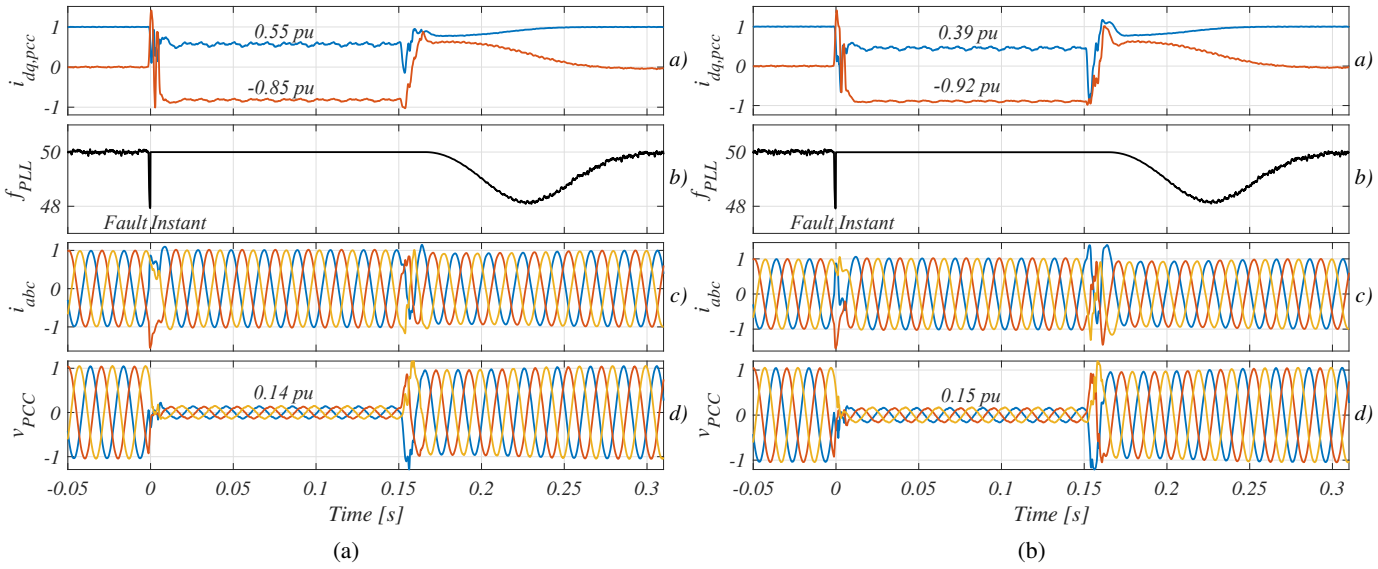
though the phase compensation technique can improve i_d, i_q, and θ_{PCC}, the additional voltage boost at the PCC when using phase compensation is only 0.01 pu. This again supports the recommendation of simply riding through the low-voltage symmetrical fault without using any phase compensation.

VI. Conclusion

With higher penetration of RES into the power system, stable and safe operation during fault events can be a challenge. During severe symmetrical faults, the voltage at the connection point can reach extremely low values which can cause the control system to become unstable when trying to inject the demanded power. To allow for zero-voltage ride-through capability without the need to comply with current injection limits or implementing additional control loops, a frozen PLL structure is employed in this paper. A frozen PLL can ensure stability for any voltage level but how it behaves during phase jumps has not been previously revealed. A comprehensive simulation study is conducted to evaluate how the PCC voltage and current injection capability are influenced during a severe symmetrical fault including voltage phase jumps. Two different phase compensation techniques are compared for the frozen PLL to uncover whether the power transfer can be improved with the aid of phase compensation. This comparison is performed for three types of line impedance

TABLE II
Experimental results during fault of Fig. 10.

Symbol	No Comp.	Comp. using (8)
i_d	0.55 pu	0.39 pu
i_q	-0.85 pu	-0.92 pu
θ_{PCC}	-32.4°	-21.6°
V_{PCC}	0.14 pu	0.15 pu



(a) (b)

Fig. 10. Experimental validation of Fig. 8 for the Z_L for a -60° phase jump during a fault voltage of 0.03 pu. (a): Fault response of PLL freeze without phase compensation. (b): PLL freeze with phase compensation using (8). The per unit values of current and voltage during the fault is given in Tab. II.

configurations to enhance the generality of the study and advice on when to employ the phase compensation. It is shown that phase compensation should only be performed for negative phase jumps occurring for line impedances consisting of both considerable resistance besides reactance. However, even though a proposed phase compensation technique were shown to improve the power transfer during phase jumps, it is revealed that a frozen PLL structure alone can allow for zero-voltage ride-through which is robust to phase jumps when the fault voltage is low. From this, the contribution of this paper is twofold:

i) Revealing how the PCC voltage phase angle together with injected active and reactive currents are influenced by phase jumps during low-voltage situations for three configurations of line impedances.

ii) Based on a comparison between a proposed phase compensation technique and a compensation method based on the instantaneous phase change at the PCC, it is revealed that phase compensation might not be necessary during any low-voltage situations, and that a frozen PLL structure can by itself allow for zero-voltage ride-through, including phase jumps in a stable, simple, and robust manner. The performance of the frozen PLL is compared to state-of-the-art methods to avoid LOS and the power transfer capability of a frozen PLL with and without phase compensation is experimentally verified.

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