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A Currentless Sorting and Selection based Capacitor-Voltage-Balancing Method for Modular Multilevel Converters

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***Abstract*—This letter proposes a currentless sorting and selection (SAS) based capacitor-voltage-balancing method for modular multilevel converters (MMCs). Without the knowledge of arm-current signals, this method has almost the same performance as the conventional SAS method while reducing the sampling signals, compacting the control system and saving the overall cost. In this letter, the derivative of the total capacitor voltage of an arm, instead of the arm current, is employed to determine which sub-modules (SMs) should be inserted or bypassed. Furthermore, the efficacy of the proposed method is verified by experimental results.**

***Index Terms*—Modular Multilevel Converter, currentless sorting and selection, capacitor voltage balancing, experiments**

I. Introduction

THE Modular Multilevel Converter (MMC) has become the most attractive topology for high-power high-voltage applications due to its scalability, modularity and excellent output performance [1] - [10]. Considering the modular structure of an MMC, capacitor voltage balancing is one of the most significant issues for MMCs. Generally, there are mainly two types of capacitor-voltage-balancing schemes, i.e., individual capacitor control [11] and arm control [12] – [15]. The former which requires a closed-loop control for each capacitor is obviously not suitable for MMCs with a large number of capacitors. The latter takes the capacitors in an arm as a whole, sorting capacitor voltages and selecting inserted/bypassed sub-modules (SMs) according to the signal of the arm current, and is named sorting and selection (SAS) method. The SAS method, compared with individual capacitor control, is much more popular due to its simple control structure, especially in high-power high-voltage conditions. However, to the best of our knowledge, arm-current signals are essential in conventional SAS method, which requires the arm-current signals to transmit from the upper-layer controller to the lower-layer one.

To simplify the control and modulation process, this letter proposes a currentless SAS method, which could simplify the control system and eliminates the adverse effects caused by the sensor noise. To present this method clearly, the outline of this letter is given below: the structure and working principles of an MMC are presented briefly in Section II; and then, the currentless SAS approach is comprehensively proposed in Section III; after that, section IV shows some important experimental results, validating the efficacy of the proposed method; finally, conclusions are drawn in Section V.

II. Principles of an MMC

A three-phase MMC, shown in Fig.1, consists of six arms, each of which formed by *N* series-connected SMs and one arm inductor. Generally, the most widely used SM is the half-bridge SM. Each half-bridge SM is composed of two IGBT switches, two anti-parallel diodes, a capacitor, and a bypass switch. Table I shows the relationships between the SM switches and SM states of a half-bridge SM. In Table I, T_{1H},T_{2H} and S_k denote the upper switch, the lower switch and the SM switching function, respectively.

Table I Two states of a half-bridge SM

State	T_{1H}	T_{2H}	S_k
Inserted	on	off	1
Bypassed	off	on	0

To investigate the working principles of an MMC, mathematical relationships of different variables should be studied. Due to the symmetry of an MMC, phase A is taken as an example for simplicity. Applying Kirchhoff's Voltage Law (KVL), Kirchhoff's Current Law (KCL) and neglecting the resistance in Fig.1 yield

$$\begin{cases} u_a = -u_{ua} - L_0 \dfrac{di_{ua}}{dt} + \dfrac{1}{2}U_{dc} \\ u_a = u_{la} + L_0 \dfrac{di_{la}}{dt} - \dfrac{1}{2}U_{dc} \end{cases} \tag{1}$$

$$i_a = i_{la} - i_{ua} \tag{2}$$

where u_a denotes the output voltage of the MMC; u_{ua} and i_{ua} denote the upper-arm voltage and current, respectively; u_{la} and i_{la} denote the lower-arm voltage and current, respectively; U_{dc} denotes the DC voltage; L_0 denotes the arm inductance.

Thus, combining (1) and (2), the output voltage of the MMC u_a can be given by

$$u_a = \frac{1}{2}(u_{la} - u_{ua}) + \frac{L_0}{2}\frac{di_a}{dt} \tag{3}$$

Then, the AC electromotive force (EMF) of the MMC u_{ea} is defined by

$$u_{ea} = \frac{1}{2}(u_{la} - u_{ua}) \tag{4}$$

According to the modulation principle, the SM output is generated by the SM switching function and capacitor voltage [16]. And then, the arm voltages are generated by the sum of SM outputs, expressed as

$$\begin{cases} u_{ua} = \sum_{k=1}^{N} S_k^{ua} u_{ck}^{ua} \\ u_{la} = \sum_{k=1}^{N} S_k^{la} u_{ck}^{la} \end{cases} \tag{5}$$

where S_k^{ua} and S_k^{la} denote the switching functions of the kth SM of the upper and lower arms of phase A, respectively; u_{ck}^{ua} and u_{ck}^{la} denote the capacitor voltages of the kth SM of the upper and lower arms of phase A, respectively.

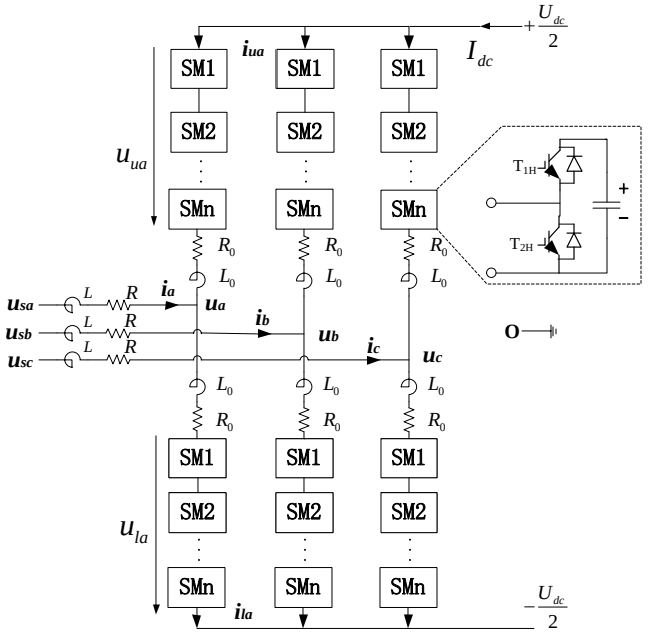

Fig.1 Structure of an MMC

To ensure an MMC works normally, a two-layer control structure is generally widely employed in high-voltage high-power MMCs. As shown in Fig.2, the main controllers (PQ control, DC side control, and circulating current control) are implemented in the central control unit (CCU), while the modulation (nearest level modulation (NLM), and SAS algorithm) is implemented in the arm control unit (ACU) [17]. As the conventional SAS algorithm requires arm-current signals, six arm-current signals have to be transmitted from the CCU to the ACU, adding to the communication burden of the MMC control system. To reduce such burdens, a currentless SAS method is proposed, which can achieve capacitor voltage balancing without arm-current signals. Therefore, the proposed method does not need the arm-current signals (red line in Fig.2).

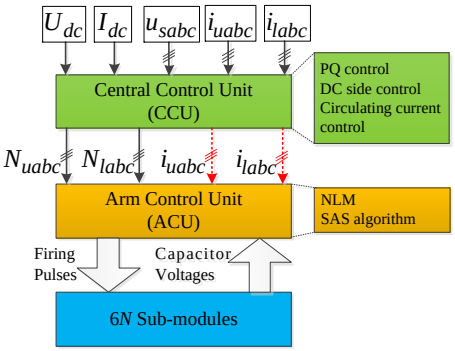

Fig.2 General control structure of an MMC

III. Currentless Sorting and Selection Method

As the mathematical principles of all six arms are identical, the superscripts, denoting the arms and phases, are omitted for the sake of simplicity. Thus, according to the capacitor dynamics, the relationship between the capacitor voltage and the arm current is given by

$$C_k \frac{du_{ck}}{dt} = S_k i_{arm} \tag{6}$$

where C_k, u_{ck} and S_k denote the capacitance, capacitor voltage and switching function of an arbitrary SM; i_{arm} denotes the corresponding arm current of that SM.

Due to manufacturing errors or capacitor degradation, SM capacitances may not be exactly the same in an MMC. Thus, considering the capacitance difference of SMs, (6) becomes

$$C(1+\delta_k)\frac{du_{ck}}{dt} = S_k i_{arm} \tag{7}$$

where δ_k denotes the manufacturing differential ratio (normally ranges from -0.2 to 0.2, thus $1+\delta_k$ is definitely positive). Hence, (7) divided by $C(1+\delta_k)$ becomes

$$\frac{du_{ck}}{dt} = \frac{S_k}{C(1+\delta_k)} i_{arm} \tag{8}$$

For an arm, summing the differential equations of the N SMs yields

$$\left(\sum u_{ck}\right)' = \frac{d}{dt}\sum u_{ck} = \sum \frac{S_k}{C(1+\delta_k)} i_{arm} \tag{9}$$

where $(\,)'$ is used to denote d/dt. According to (9), it is easy to see that the sign of i_{arm} is dependent on the signs of $(\sum u_{ck})'$ and $\sum \frac{S_k}{1+\delta_k}$, given that C is always positive. Thus, the sign of i_{arm} can be derived according to $(\sum u_{ck})'$ and $\sum \frac{S_k}{1+\delta_k}$.

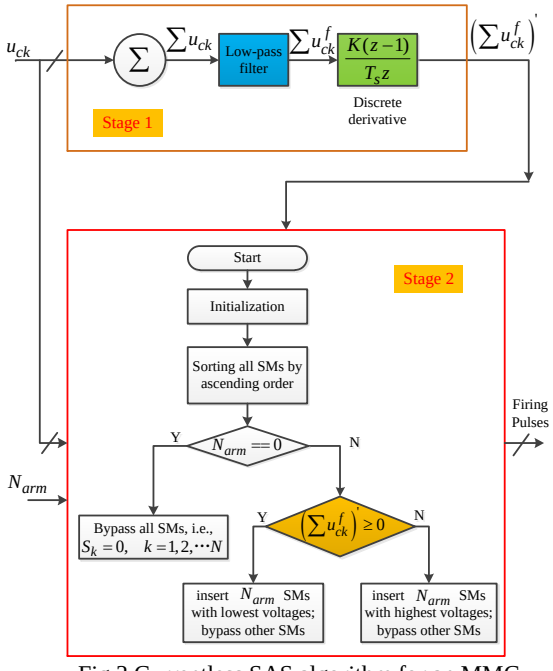

Fig.3 Currentless SAS algorithm for an MMC

As shown in Table I, the two states of a half-bridge SM, inserted or bypassed, have two corresponding S_k, i.e., 1 and 0. Since, C > 0, $1+\delta_k > 0$ and $S_k = 1$ *or* 0, $\frac{S_k}{C(1+\delta_k)}$ is positive

or zero (non-negative), which means that $(\sum u_{ck})'$ has the same sign as that of i_{arm} except $\sum \frac{S_k}{C(1+\delta_k)} = 0$, according to (9). Hence, $(\sum u_{ck})'$ instead of i_{arm} can be taken as the criteria to recognize whether capacitors are in the charging or discharging states. When $(\sum u_{ck})' > 0$, capacitors are in charging states, and the lowest-voltage SMs should be inserted to generate the desired voltage; When $(\sum u_{ck})' < 0$, capacitors are in discharging states, the highest-voltage SMs should be inserted to generate the desired voltage. In addition, as derivation is a little sensitive to sampling noises, a low-pass filter (LPF) is employed to eliminate the high frequency noises of the total capacitor voltage of an arm. Thus, a new algorithm without the knowledge of i_{arm} for half-bridge MMCs is proposed as shown in Fig.3, which contains two stages, i.e. derivative generating (stage 1) and SAS implementation (stage 2).

In stage 1, all capacitor voltages in an arm is firstly added up; and then the sum $(\sum u_{ck})$ is filtered by the LPF, generating $\sum u_{ck}^f$; after that, the discrete derivative of $\sum u_{ck}^f$ is calculated; finally, the derivative of the filtered total capacitor voltage of an arm $(\sum u_{ck})'$, is sent to stage 2. In stage 2, firstly all the inputs including N_{arm}, $(\sum u_{ck})'$ and u_{ck} are initialized; and then, all SMs are sorted by an ascending order of capacitor voltage; after that, one should identify if the desired voltage level equals zero or not: when the desired voltage level N_{arm} is equal to zero, all SMs are bypassed; when N_{arm} is not equal to zero and $(\sum u_{ck})' \geq 0$, N_{arm} lowest-voltage SMs are inserted; otherwise, N_{arm} highest-voltage SMs are inserted. Through the proposed algorithm, the firing pulses of all SMs, which can ensure capacitor voltage balancing, are generated.

IV. Experimental Results

To verify the proposed currentless SAS method, some experiments are carried out in a three-phase down-scaled MMC prototype shown in Fig.4, with the parameters listed in Table II.

Table II Main circuit parameters of the experiments

Items	Symbols	Values
AC Load	R_{Load}	15 ohm
Rated frequency	f	50 Hz
Sampling frequency	f_s	5 kHz
Rated direct voltage	U_{dc}	80 V
Arm inductance	L_0	10 mH
Total number of SMs per arm	N	4
Capacitor voltage	U_c	20 V
SM capacitance	C	4000 uF

Since the main purpose of the simulation is to verify the proposed currentless SAS method, the prototype works as an inverter, supplying a three-phase resistive load. And the nearest level modulation scheme is applied. The experimental results are shown in Fig.5 to Fig.8.

Fig.5 illustrates the original total voltage $\sum u_{ck}$ (blue curve) and the filtered total voltage $\sum u_{ck}^f$ (red curve) of the upper arm of phase A. It can be seen that the time delay T_d between these two waveforms is about 0.002s, which is introduced by the LPF seen in Fig.3.

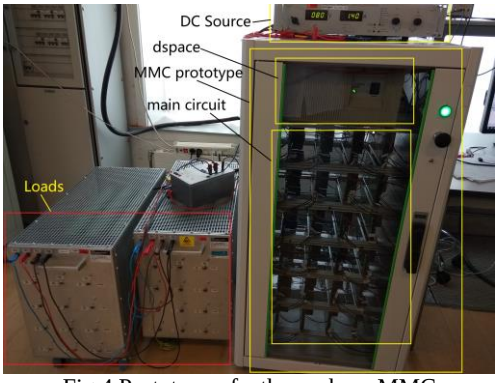

Fig.4 Prototype of a three-phase MMC

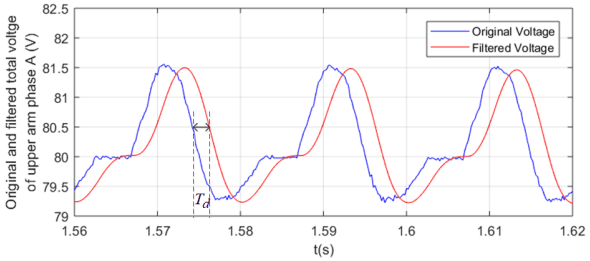

Fig.5 The original and filtered total SM capacitor voltages of the upper arm of phase A

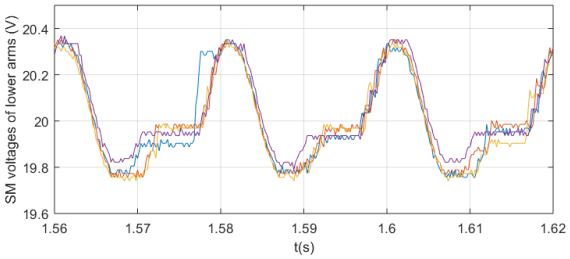

Fig.6 SM voltages of the lower arm of phase A

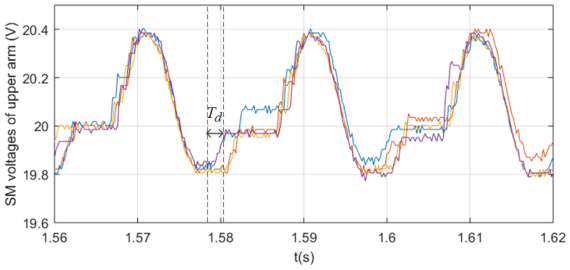

Fig.7 SM voltages of the upper arm of phase A

Fig.6 and Fig.7 show the lower-arm and upper-arm capacitor voltages, respectively. It can be observed that all the capacitor voltages are well balanced with the proposed method.

Fig.8 illustrates the arm currents (the upper figure) and the derivative of total capacitor voltage of the upper arm $\left(\sum u_{ck}^f\right)'$ (the bottom figure). Take a close look around t = 1.58s when the upper-arm current i_{ua} crosses zero from a negative value. It can be seen that the zero-crossing instant of $\left(\sum u_{ck}^f\right)'$ lags T_d, which is caused by the filter. This phenomenon means that $\left(\sum u_{ck}^f\right)'$ and i_{ua} have different signs in the tiny time interval. Furthermore, by checking the very interval of the upper-arm capacitor voltages in Fig.7, there are very small errors, which hardly have any influence on the voltage

balancing performance. Therefore, it can be seen from the experimental results that the proposed method can achieve the capacitor-voltage balancing as expected.

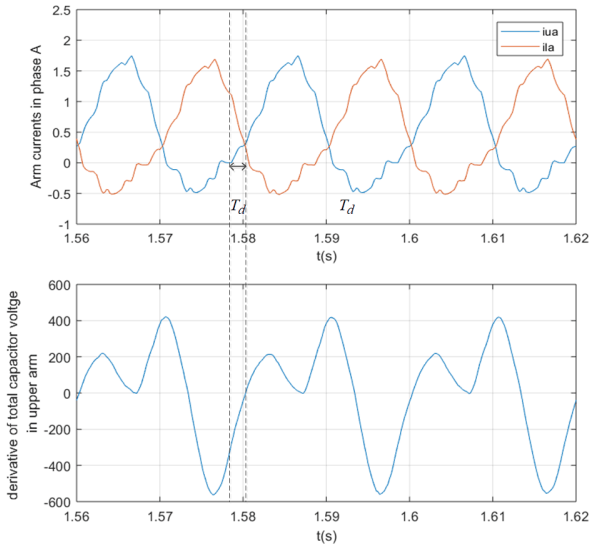

Fig.8 Arm currents of phase A; the derivative of total capacitor voltage of the upper arm of phase A

V. Conclusion

This letter proposes a new currentless SAS based capacitor-voltage-balancing method, which can reduce the transmission of the six arm-current signals in the control system. The ACU only needs the reference voltage level and capacitor voltages, which helps compact the whole system. Followed are the details of the proposed method and the verification of the method by experimental results.

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