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Abstract—Contrary to the phase-locked loop (PLL), which has almost reached a mature stage of development in power and energy applications (particularly in three-phase systems), the frequency-locked loop (FLL) is not a mature technique yet. This is probably because of the implementation of FLLs in the stationary reference frame which makes their modeling, tuning, and performance enhancement more complicated than PLLs. The aim of this paper is conducting a research on three-phase FLLs. Providing a review of recent advances, introducing the concept of inloop filter for designing more advanced FLLs, demonstrating the FLL modeling and tuning in the presence of an inloop filter, analyzing the advantages and disadvantages of using an inloop filter in the FLL structure, and establishing a connection between FLLs and PLLs are the main parts of this research.

Index Terms—Complex coefficient filter, frequency-locked loop (FLL), phase-locked loop (PLL), synchronization, three-phase systems.

I. INTRODUCTION

IN RECENT YEARS, a large number of synchronization techniques have been proposed. Closed-loop synchronization (CLS) techniques (which mainly include phase-locked loops (PLLs) [1], frequency-locked loops (FLLs) [2], [3], and integrated synchronization and control approaches [4]) and open-loop ones [5] are two major categories of synchronization techniques.

FLLs and PLLs are both nonlinear negative-feedback control systems that synchronize their output(s) with their input(s). The main difference between these techniques lies in their working frame. Generally speaking, PLLs are implemented in the synchronous (dq) reference frame, while FLLs are realized in the stationary ($\alpha\beta$) reference frame[1].

Focusing on power applications, PLLs have almost reached a mature stage of development. This is particularly true for the three-phase applications. A very large number of PLLs with distinctive characteristics have been designed by independent research groups in recent years, which can effectively reject the grid voltage disturbances and, at the same time, provide a fast dynamic response and an adequate stability margin. This

makes a further contribution to the field difficult.[2] The PLLs owe this accelerated development to a high extend to their working frame, which is the dq frame. A review of recent advances in three-phase PLLs can be found in [1].

Designing FLLs for power applications dates back to less than twenty years ago. They are, contrary to PLLs, are not a mature technique yet. The slow development of the FLLs compared to PLLs is mainly attributable to their working frame. Roughly speaking, designing a controller/compensator/filter in the $\alpha\beta$ frame is more complicated than designing that in the dq frame. Besides, the implementation of FLLs in the $\alpha\beta$ frame makes their small-signal modeling and, therefore, stability analysis and tuning procedure more complicated. These facts highlight the importance of further contributions to facilitate the modeling procedure of FLLs and enhance their filtering capability.

This paper focuses on three-phase FLLs and makes the following contributions.

1) A review of recent advances on FLLs is provided (see Section II).
2) The concept of inloop filter to enhance the disturbance rejection capability of FLLs is presented (see Section III). As design examples, using the cascaded $\alpha\beta$-frame delayed signal cancelation ($\alpha\beta$DSC) operators [7]–[9] and a first-order complex bandpass filter (CBF) as the FLL inloop filters is proposed, and the FLL modeling, stability analysis, and tuning procedure in the presence of these inloop filters are demonstrated (see Section III-A). A performance comparison between the designed advanced FLLs and a standard FLL is also conducted to highlight their advantages and disadvantages (see Section III-B).
3) The relation between FLLs and PLLs with inloop filters are demonstrated (see Section IV).
4) It is finally shown that a recently designed advanced FLL in [2] is actually an FLL with the inloop CBF. Therefore, it can be modeled and tuned by following the same procedure proposed here (see Section V).

II. REVIEW OF RECENT ADVANCES

Fig. 1(a) illustrates a standard three-phase FLL. k and λ are the control parameters of this FLL, and $\hat{\theta}_1$, $\hat{\omega}_g$, and $\hat{V}_1$ denote the estimated phase, frequency, and amplitude, respectively. The standard FLL is implemented by using a reduced-order generalized integrator (ROGI) [10] in the forward path of a

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A. M. Abusorrah and Y. Al-Turki are with the Department of Electrical and Computer Engineering, Faculty of Engineering, and Center of Research Excellence in Renewable Energy and Power Systems, King Abdulaziz University, Jeddah 21589, Saudi Arabia (e-mail: aabusorrah@kau.edu.sa; yaturki@yahoo.com).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

[1]Very recently, some attempts for implementing synchronous-reference frame FLLs have been made [6].

[2]Only potential research opportunities in the field seem to be those focused on the modeling and stability analysis of PLLs, particularly by considering their dynamic interaction with power converters.
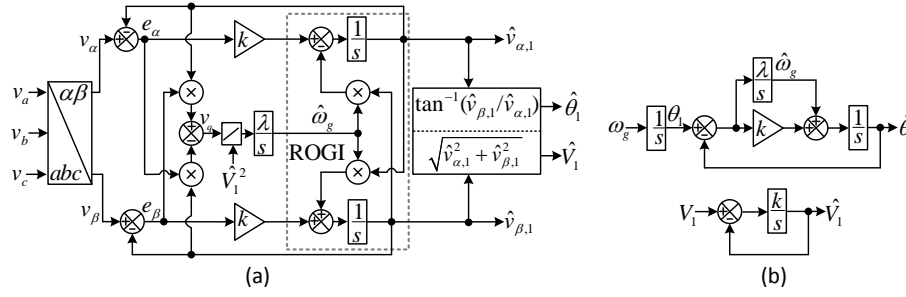
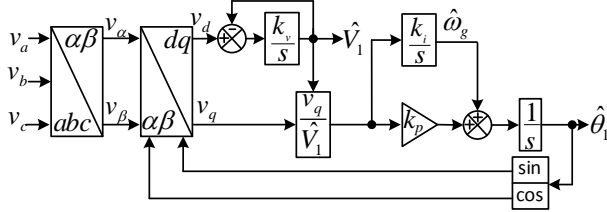Fig. 1. (a) Standard three-phase FLL and (b) its small-signal model.

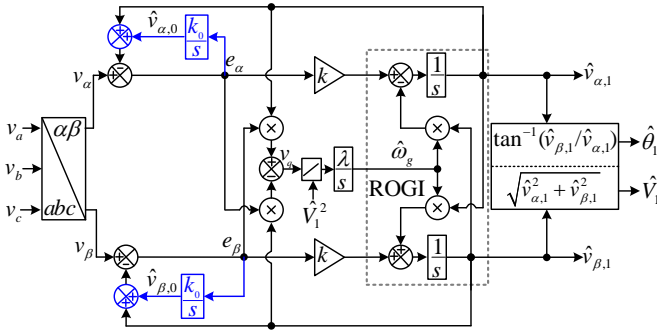Fig. 2. Block diagram of an SRF-PLL.

Fig. 3. An FLL with enhanced DC offset rejection capability.

unity feedback control loop for extracting the grid voltage fundamental component and a frequency estimator for adjusting its center frequency. The historical development of this structure has been explained in [2].

In [1], a small-signal model for the standard FLL is derived as shown in Fig. 1(b). As this model is the same as that of the synchronous-reference frame PLL (SRF-PLL)[3] illustrated in Fig. 2, it is conducted that the standard FLL and this SRF-PLL are equivalent systems. The assumptions behind this equivalence are $k_p = k_v = k$ and $k_i = \lambda$, where k_p and k_i are the proportional and integral gains of the SRF-PLL, respectively, and k_v is the low-pass filter (LPF) cutoff frequency in the SRF-PLL amplitude estimation loop. This equivalence implies that the standard FLL, like a simple SRF-PLL, has a very limited filtering capability. To tackle this problem, some attempts have been made recently. In what follows, these efforts are briefly explained.

To enhance the FLL DC-offset rejection capability, two integrators (as highlighted in Fig. 3) may be included in the

standard FLL structure [12]–[14]. These integrators provide an estimation of the grid voltage DC component and, therefore, completely reject its disturbing effect on the FLL performance. They, however, may slightly degrade the FLL harmonic filtering capability and high-frequency noise immunity. Notice that using these integrators mathematically equivalent to including two high-pass filters inside the FLL control loop.

To enhance the FLL imbalance and harmonic filtering capability, a parallel configuration of two or more first-order CBFs[4] with a cross-feedback network may be used [13]–[17]. Fig. 4 illustrates the simplest possible case, which includes two units for detecting and separating the fundamental-frequency positive-sequence (FFPS) and fundamental-frequency negative-sequence (FFNS) components. Notice that the frequency detector is connected to the main unit, i.e., the unit that extracts the FFPS component. The main advantage of this approach is that a parallel unit, in addition to making the main unit immune to the disturbing effect of the grid voltage imbalance or a harmonic component, extracts that disturbance component. Therefore, it may be used as a signal decomposition technique. The main limitation is that removing/extracting an additional disturbance component requires an extra unit, which increases the computational burden. It is worth mentioning here that a direct discrete-time implementation of this idea has been proposed in [18].

In [19], including an additional degree of freedom (which is a complex gain from the signal processing point of view) to the standard FLL structure is suggested. Fig. 5 illustrates a possible implementation of this idea. According to [19], using this extra degree of freedom, placing the closed-loop poles can be performed more optimally, which results in a dynamic performance enhancement without significantly affecting the filtering capability.

In [2], a resemblance between a first-order CBF[5], which is the basic building block of the standard FLL, and a first-order LPF is established. It is discussed that a first-order CBF is realized by replacing the pure integrator of a first-order LPF by a ROGI. Therefore, a second-order CBF, which is called the second-order sequence filter (SOSF) in [2], may be constructed by replacing two pure integrators of a second-order LPF by two ROGIs. Fig. 6 illustrates a SOSF-based FLL (SOSF-FLL), which is realized by adding the phase/frequency/amplitude detection parts of the standard FLL to the SOSF.

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[3]This SRF-PLL has a small difference compared to the standard SRF-PLL [11]. In this version, the output of the integrator of the proportional-integral (PI) controller is considered as the estimated frequency.

[4]Using a ROGI in a unify feedback structure results in a first-order CBF.

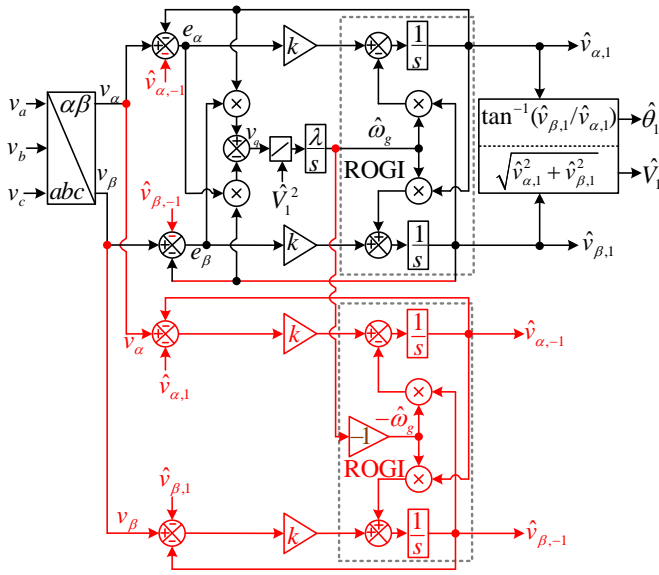[5]It is called the sinusoidal first-order system in [2].

Fig. 4. An FLL with an enhanced grid voltage imbalance rejection ability.
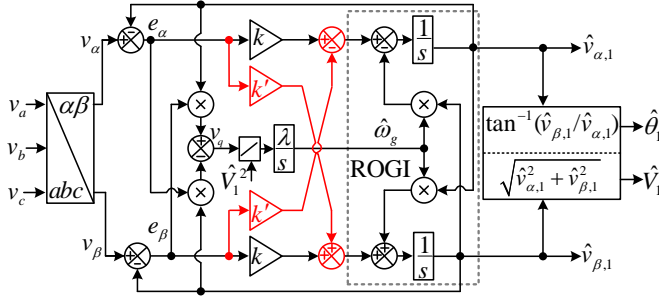

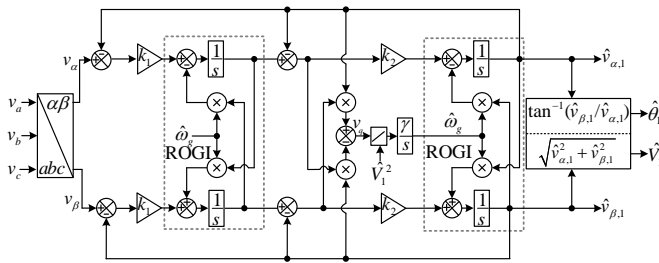Fig. 5. Standard FLL with an extra degree of freedom.

Fig. 6. Block diagram of the SOSF-FLL.

III. CONCEPT OF INLOOP FILTER IN FLLS

If it is assumed that the estimated frequency $\hat{\omega}_g$ is a constant, the output signals of the ROGI in Fig. 1(a) can be expressed in the space vector notation as

$$\underbrace{\hat{v}_{\alpha,1}(s) + j\hat{v}_{\beta,1}(s)}_{\vec{v}_{\alpha\beta,1}(s)} = \underbrace{\frac{k}{s - j\hat{\omega}_g + k}}_{G_{\alpha\beta}(s)} \underbrace{(v_\alpha(s) + jv_\beta(s))}_{\vec{v}_{\alpha\beta}(s)}. \quad (1)$$

The transfer function $G_{\alpha\beta}(s)$ describes a first-order CBF with the center frequency at $\hat{\omega}_g$. This filter passes the FFPS component and attenuates other frequency components. The attenuation level highly depends on the CBF bandwidth. The FLL filtering capability can be enhanced by narrowing the
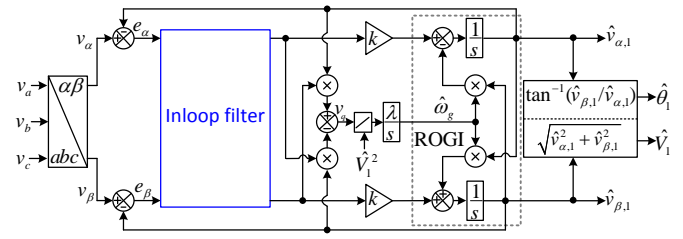
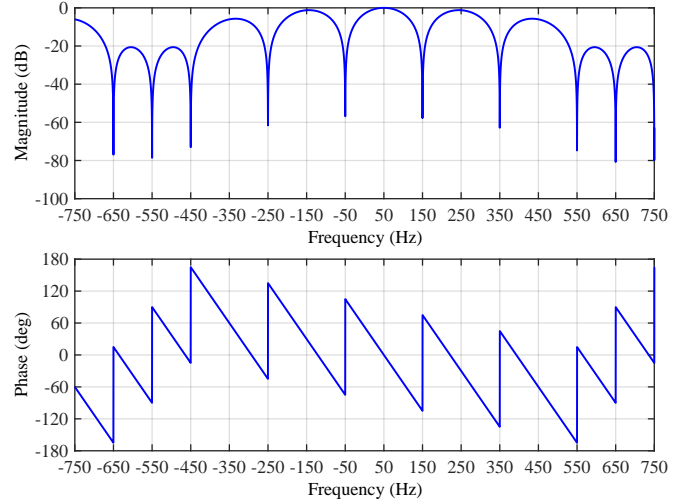

Fig. 7. Standard FLL with an inloop filter.

Fig. 8. Frequency response of two cascaded $\alpha\beta$DSC operators with the delay factors 4 and 24.

CBF bandwidth, but at the cost of degrading its dynamic behavior.

Inspired by the concept of inloop filter in PLLs, a filtering stage may be included in the FLL control loop to enhance its filtering capability. The general structure of the standard FLL with an inloop filter can be observed in Fig. 7. Notice that the FLL acts on the fundamental component of the error signals (e_α and e_β) in the estimation of the grid voltage fundamental parameters and, therefore, the inloop filter should pass this component as fast as possible, preferably without any change. Besides, the error signals contain all disturbances of the grid voltage (probably with a slight change in the magnitude and initial phase) and, consequently, the inloop filter should attenuate/reject them. Considering these facts, it can be concluded that the FLL inloop filter should be a band-pass-like filter that passes the FFPS component and blocks anticipated disturbances of the grid voltage. There are a large number of filters that may satisfy these conditions. Indeed, most filters that have been proposed as the PLL prefiltering stage may be employed as the FLL inloop filter. A review of all these filters can be found in [1]. The filtering techniques presented in [20] may also be interesting options. In what follows, as design examples, employing the $\alpha\beta$DSC operators [7], [8] and a first-order CBF as the FLL inloop filter is considered.
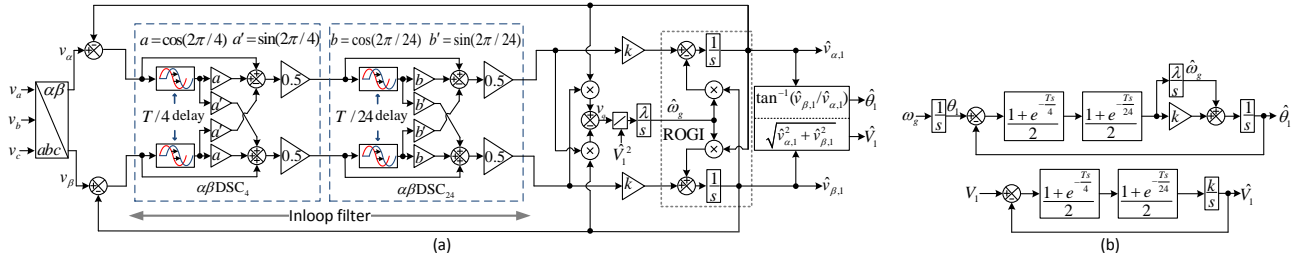
A. Design Examples

Fig. 9. (a) FLL with inloop $\alpha\beta$DSC operators (briefly called the DSC-FLL), and (b) its small-signal model.

1) FLL With Inloop $\alpha\beta$DSC Operators: The $\alpha\beta$DSC operator is a non-recursive filter which may be used for different signal processing tasks. When extracting the FFPS component and rejecting disturbances such as harmonics, grid voltage imbalance, etc. are intended, this operator is expressed as [7], [8]

$$\alpha\beta DSC_n(s) = \frac{1 + e^{\frac{j2\pi}{n}} e^{-\frac{Ts}{n}}}{2} \qquad (2)$$

where T and n denote the fundamental period and the operator delay factor, respectively. Notice that the operator filtering capability depends on its delay factor. Also notice that a single operator may not be able to block all concerned disturbances, and often two or more operators with different delay factors are cascaded to reject them. Selecting the number and delay factor of cascaded operators depends on the expected disturbances in the FLL input. Here, a typical case (the presence of harmonics of order $h = -5, +7, -11, +13, \cdots$ and the FFNS component) is considered. Removing these disturbances requires two cascaded $\alpha\beta$DSC operators with delay factors of 4 and 24. Fig. 8 illustrates the frequency response of these operators. It can be seen that they pass the FFPS component and reject the concerned disturbances. In addition to the concerned dominant disturbances, some other disturbance components are also rejected.

Fig. 9(a) illustrates the standard FLL with these two operators as its inloop filter. This structure is briefly referred to as the DSC-FLL. The small-signal model of this FLL can be obtained as shown in Fig. 9(b). Developing this model can be carried out following a similar procedure as that described in Appendix A. In this appendix, the modeling of a standard FLL with a single inloop $\alpha\beta$DSC operator is presented.

Using Fig. 9(b), the phase open-loop transfer function of the DSC-FLL can be obtained as

$$G_{ol}^\theta(s) = \frac{\hat{\theta}_1(s)}{\theta_1(s) - \hat{\theta}_1(s)} = \frac{1 + e^{-\frac{Ts}{4}}}{2} \frac{1 + e^{-\frac{Ts}{24}}}{2} \frac{ks + \lambda}{s^2}. \quad (3)$$

Replacing the delay terms in (3) by their first-order Padé approximations (i.e., $e^{-\frac{Ts}{4}} \approx \frac{1-Ts/8}{1+Ts/8}$ and $e^{-\frac{Ts}{24}} \approx \frac{1-Ts/48}{1+Ts/48}$) results in

$$G_{ol}^\theta(s) \approx \frac{1}{\frac{T}{8}s+1} \frac{1}{\frac{T}{48}s+1} \frac{ks+\lambda}{s^2} \approx \frac{1}{\underbrace{\left(\frac{T}{8}+\frac{T}{48}\right)}_{T_d}s+1} \frac{ks+\lambda}{s^2}.$$

$$(4)$$

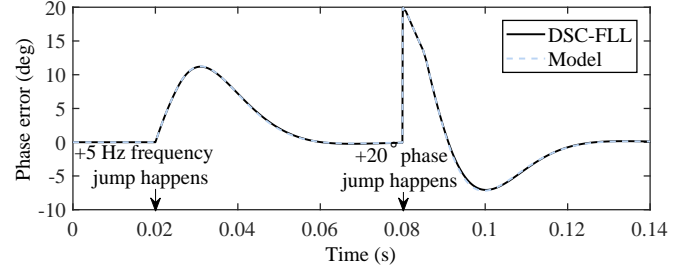Now, according to the symmetrical optimum method [21],

Fig. 10. Accuracy evaluation of the DSC-FLL model. The frequency jump, for the sake of clarity, is exaggeratedly large. Happening such a large frequency change is very unlikely in practice.

[22], k and λ can be selected as

$$\begin{aligned} k &= \frac{1}{gT_d} \\ \lambda &= \frac{1}{g^3 T_d^2} \end{aligned} \qquad (5)$$

where $g = \tan(PM) + 1/\cos(PM)$ is the phase margin (PM) determining factor. A PM equal to $45°$ (which corresponds to the optimum damping factor $1/\sqrt{2}$ for the closed-loop poles) is recommended in [22]. By following this recommendation, the control parameters can be calculated as $k = 142$ and $\lambda = 8354$.

The accuracy evaluation of the DSC-FLL model seems necessary here because tuning the control parameters was based on this model. Fig. 10 compares the phase error response of the DSC-FLL under frequency/phase jumps with that predicted by its model. These results confirm that the DSC-FLL model is very accurate. The model can also accurately predict the DSC-FLL dynamic behavior in response to an amplitude change. The results of this test, however, are not shown to save the space.

2) FLL With Inloop CBF: A first-order CBF with the center frequency at the fundamental frequency ω_g may also be a good option for the FLL inloop filter. Equation (6) describes such a CBF in the Laplace domain, in which ω_p is the CBF cutoff frequency, and Fig. 11(a) illustrates the standard FLL with this CBF as its inloop filter.

$$CBF(s) = \frac{\omega_p}{s - j\omega_g + \omega_p} \qquad (6)$$

Notice that the cutoff frequency ω_p determines the CBF filtering capability. This fact is clear from Fig. 12, which shows the CBF frequency response for different values of ω_p. Therefore, to enhance the FLL disturbance rejection capability, the cutoff frequency ω_p should be as low as possible.
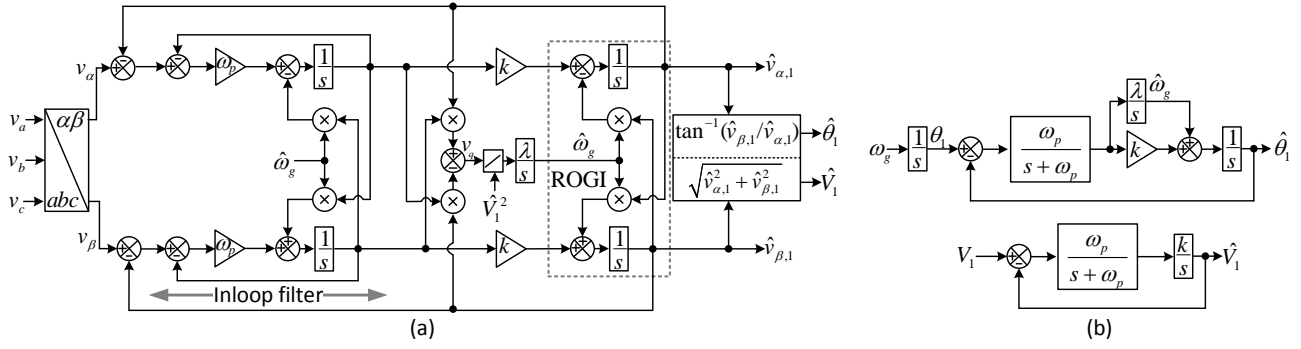
Fig. 11. (a) FLL with an inloop CBF (briefly called the CBF-FLL), and (b) its small-signal model.
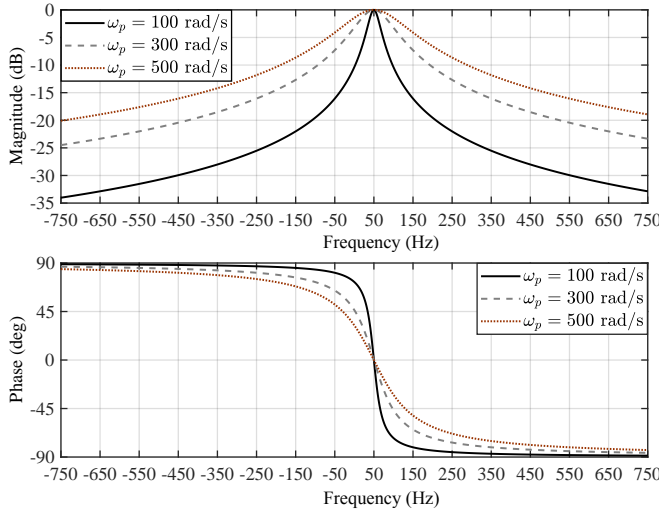

Fig. 12. Frequency response of (6) for different values of ω_p.

Fig. 13. Accuracy evaluation of the CBF-FLL model.

TABLE I
CONTROL PARAMETERS

FLL	Parameters
Standard FLL	$k = 160$, $\lambda = 12791$
DSC-FLL	$k = 142$, $\lambda = 8354$
CBF-FLL	$k = 142$, $\lambda = 8354$, $\omega_p = 343$ rad/s

Fig. 11(b) shows the small-signal model of the CBF-FLL. Deriving this model is based on the general approach presented at the end of Appendix A. Based on this model, the phase open-loop transfer function of the CBF-FLL can be obtained as

$$G_{ol}^{\theta}(s) = \frac{\hat{\theta}_1(s)}{\theta_1(s) - \hat{\theta}_1(s)} = \frac{\omega_p}{s + \omega_p} \frac{ks + \lambda}{s^2}. \quad (7)$$

Notice that this transfer function is similar to (4), i.e., the phase open-loop transfer function of the DSC-FLL. Therefore, to have a fair condition of comparison, the same control parameters as those of the DSC-FLL are selected for the CBF-FLL. These parameters are summarized below

$$\omega_p = \frac{1}{T_d} = \frac{48}{7T} = 343$$
$$k = 142 \quad (8)$$
$$\lambda = 8354.$$

The accuracy assessment of the CBF-FLL model is carried out under the same tests as those used for the accuracy evaluation of the DSC-FLL model (Fig. 10). Fig. 13 shows the results of this assessment. The model is obviously very accurate.
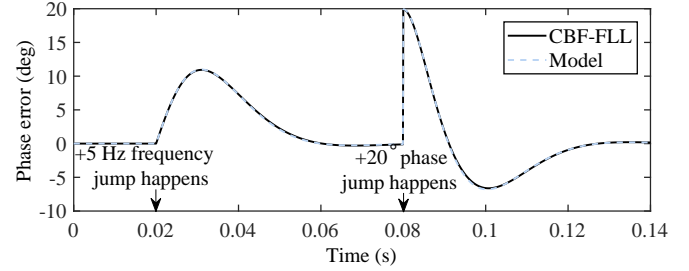
B. Performance Comparison

1) Theoretical Comparison: Table I summarizes the control parameters selected for the standard FLL, DSC-FLL, and CBF-FLL, and Table II shows the characteristic transfer functions of these FLLs. These transfer functions can be obtained using the small-signal models of these FLLs. Using this information, the frequency response of these characteristic transfer functions can be obtained as shown in Fig. 14. Based on these Bode plots, the following observations are made:

- The DSC-FLL and CBF-FLL have a lower stability margin than the standard FLL. To be more exact, the PM of the DSC-FLL and CBF-FLL (according to their phase open-loop Bode plots) are $43.7°$ and $45°$, respectively, while the PM of the standard FLL is $65.5°$. This result was expected because, as shown in Fig. 9(b) and Fig. 11(b), the inloop filter causes a phase delay in the DSC-FLL and CBF-FLL models. Considering that the PM of a control system is correlated with its overshoot in response to a step input, it can be concluded that the DSC-FLL and CBF-FLL experience a larger overshoot than the standard FLL in response to phase jumps.
- The DSC-FLL and CBF-FLL have a very close frequency response in the low-frequency range (i.e., the frequencies

TABLE II
CHARACTERISTIC TRANSFER FUNCTIONS OF FLLS. OLTF=OPEN-LOOP TRANSFER FUNCTION, CLTF=CLOSED-LOOP TRANSFER FUNCTION.

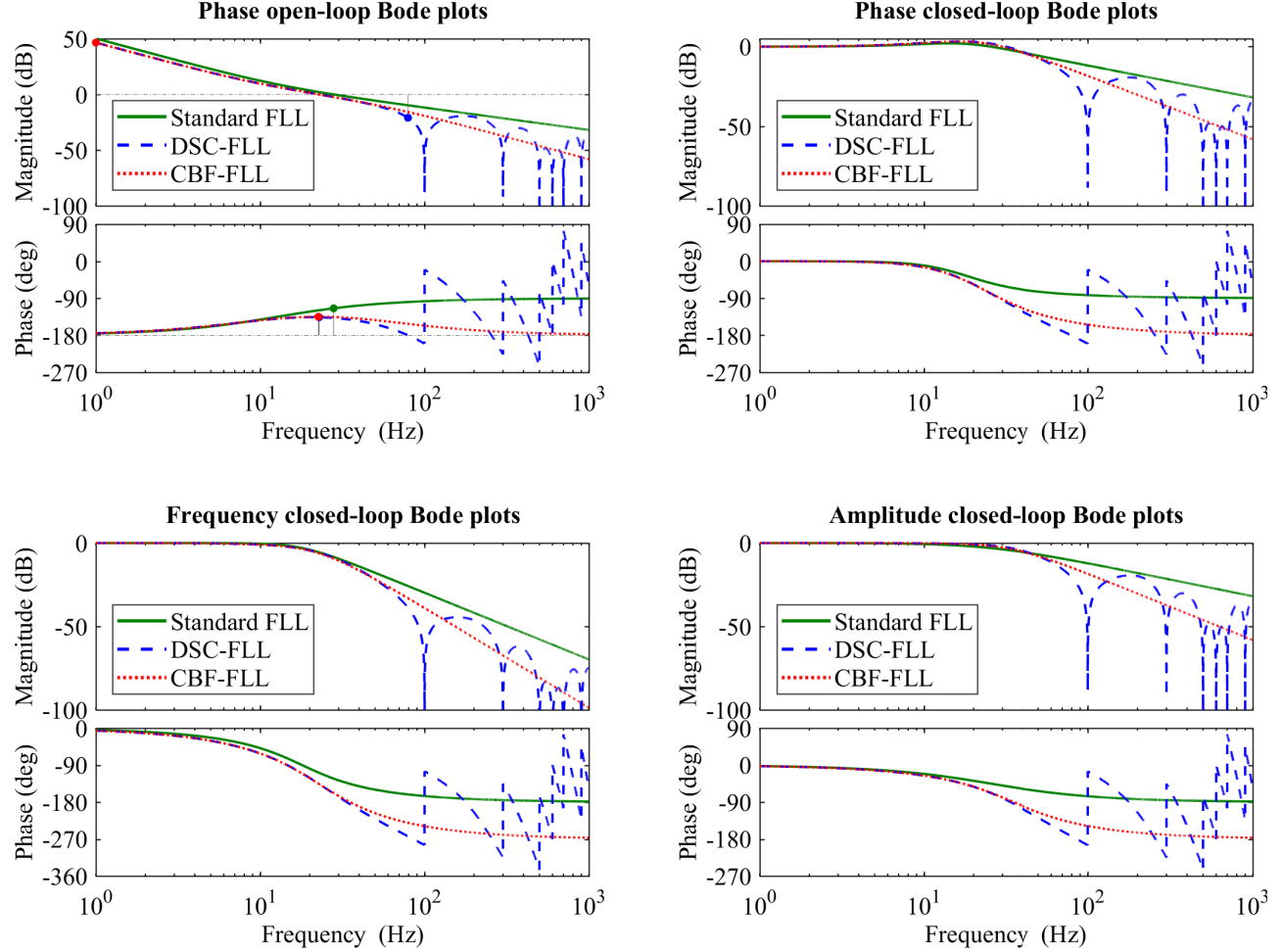| FLL	Phase OLTF	Phase CLTF	Frequency CLTF	Amplitude CLTF
Standard FLL	$\frac{ks+\lambda}{s^2}$	$\frac{ks+\lambda}{s^2+ks+\lambda}$	$\frac{\lambda}{s^2+ks+\lambda}$	$\frac{k}{s+k}$
DSC-FLL	$\underbrace{0.5\left(1+e^{-Ts/4}\right)0.5\left(1+e^{-Ts/24}\right)}_{F(s)}\frac{ks+\lambda}{s^2}$	$\frac{ksF(s)+\lambda F(s)}{s^2+ksF(s)+\lambda F(s)}$	$\frac{\lambda F(s)}{s^2+ksF(s)+\lambda F(s)}$	$\frac{kF(s)}{s+kF(s)}$
CBF-FLL	$\frac{\omega_p}{s+\omega_p}\frac{ks+\lambda}{s^2}$	$\frac{\omega_p(ks+\lambda)}{s^3+\omega_p s^2+\omega_p ks+\omega_p\lambda}$	$\frac{\lambda\omega_p}{s^3+\omega_p s^2+\omega_p ks+\omega_p\lambda}$	$\frac{k\omega_p}{s^2+\omega_p s+k\omega_p}$

Fig. 14. Frequency response of the characteristic transfer functions of the standard FLL, DSC-FLL, and CBF-FLL.

lower than the fundamental frequency). Consequently, a close dynamic behavior for these two FLLs is expected.

- The settling time of the standard FLL is predicted to be close to that of the CBF-FLL and DSC-FLL because the closed-loop frequency responses of all of them have almost the same bandwidth.
- The DSC-FLL, thanks to its $\alpha\beta$DSC operators, offers the best disturbance rejection capability. The CBF-FLL has the second best performance, and the standard FLL has the worst performance.

2) Experimental Comparison: In this section, an experimental performance comparison between the standard FLL [Fig. 1(a)], the DSC-FLL [Fig. 9(a)] and the CBF-FLL [Fig. 11(a)] is conducted. To perform the experimental tests, the dSPACE 1006 platform is employed. The sampling frequency in this study is 12 kHz. Table I summarizes the values of the control parameters. The FLL input signals are generated using the dSPACE.

The following tests are designed for the performance comparison between FLLs.

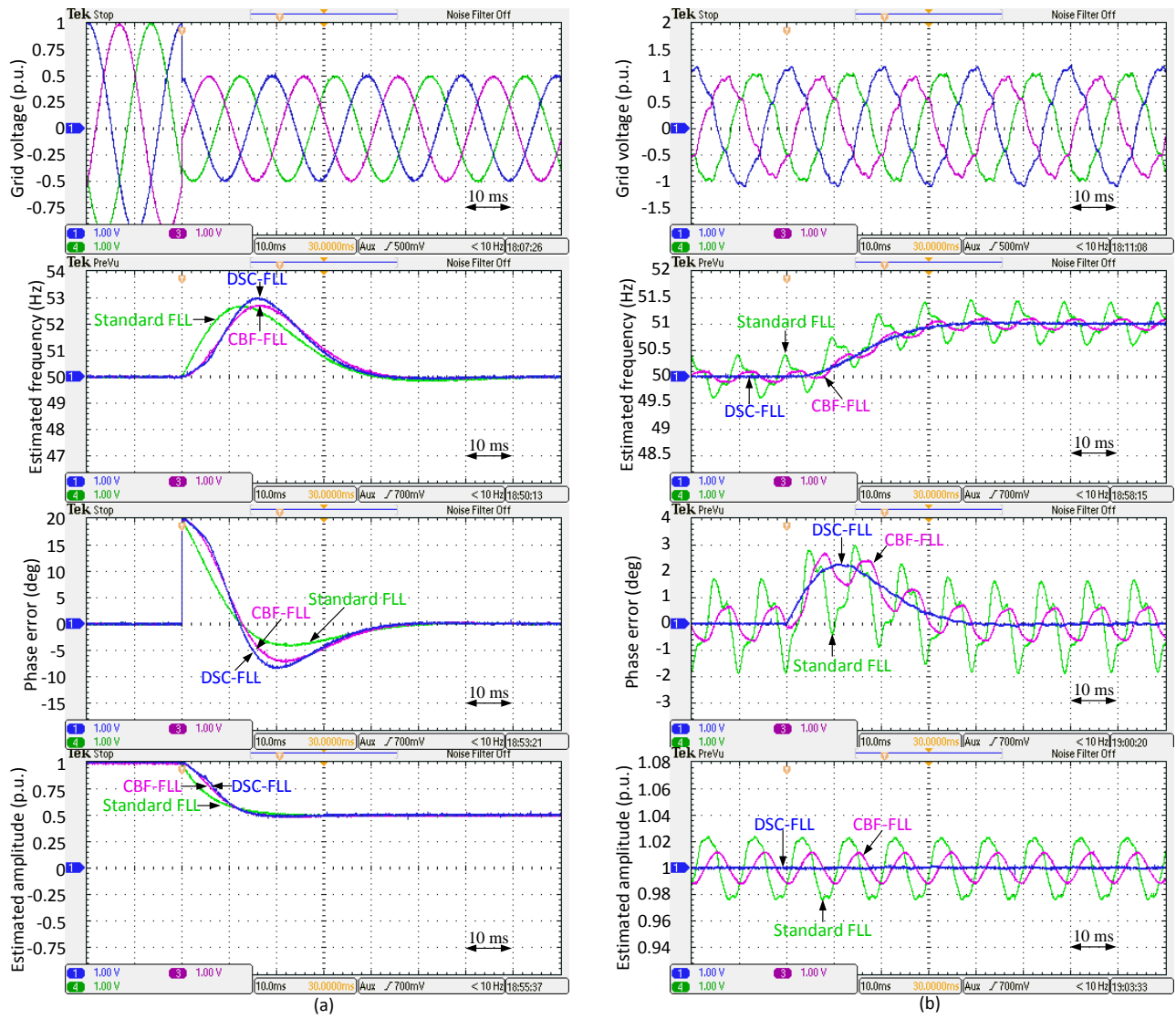- Test 1: A $+20°$ phase jump with a 0.5-p.u. symmetrical

Fig. 15. Results of (a) Test 1 and (b) Test 2.

voltage sag occurs.

- Test 2: The grid voltage is distorted and unbalanced and, at the same time, a +1 Hz frequency jump happens. The magnitude of the FFPS and FFNS components in this test are 1 p.u. and 0.1 p.u., respectively. The total harmonic distortion of the phase A, B, and C are around 7%, 8.3%, and 7.7%, respectively.

Results of Test 1 are shown in Fig. 15(a). As predicted before, the DSC-FLL and CBF-FLL demonstrate a close dynamic behavior, and all FLLs have a close settling time (around two cycles). The DSC-FLL and CBF-FLL, however, experience a larger phase overshoot. As explained before, this is because of their lower PM.

Fig. 15(b) demonstrates the results of Test 2. All FLLs have a close speed of response. The difference is that the DSC-FLL effectively rejects disturbances, however, the standard FLL suffers from rather large oscillatory ripples. The performance of the CBF-FLL in this test is something between that of the DSC-FLL and standard-FLL.

IV. RELATION BETWEEN FLLs AND PLLs

It is shown in [1] that the standard FLL [Fig. 1(a)] is equivalent to the synchronous reference frame PLL (SRF-FLL) [Fig. 2] if $k_p = k_v = k$ and $k_i = \lambda$. Therefore, there should be a relation between the standard FLL and the SRF-PLL when they employ inloop filters. Finding this relation is the objective of this section.

As a case study, consider the DSC-FLL [Fig. 9(a)], which is the standard FLL with two cascaded $\alpha\beta$DSC operators as its inloop filter. The small-signal model of this FLL is shown in Fig. 9(b). An SRF-PLL that employs two cascaded dq-frame DSC (dqDSC) operators[6] as its inloop filter also has the same model. The block diagram of such a PLL, briefly called the DSC-PLL, is shown in Fig. 16(a). As the DSC-FLL and the DSC-PLL both have the same small-signal model, it seems safe to say that they are equivalent systems from the small-signal point of view. The same conclusion can be

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[6]A dqDSC operator is the dq-frame equivalent of the $\alpha\beta$DSC operator described in (2).
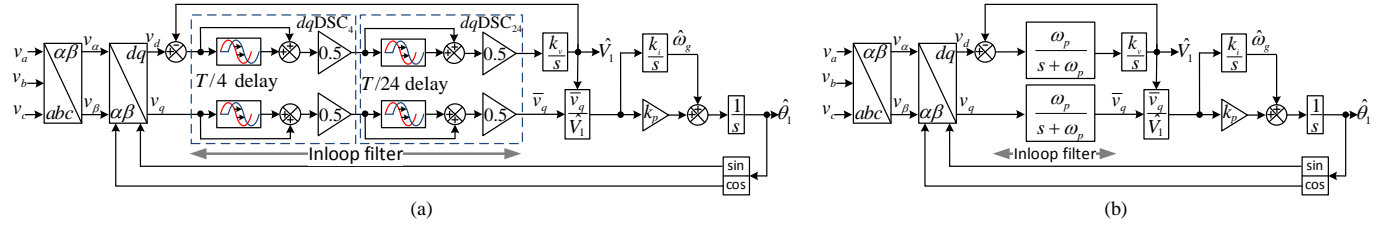
Fig. 16. (a) SRF-PLL with inloop dqDSC operators, briefly called the DSC-PLL. (b) SRF-PLL with inloop LPFs, briefly called the LPF-PLL.

Fig. 17. (a) Performance comparison of the DSC-FLL and DSC-PLL in response to (a) 20° phase jump, (b) 0.5-p.u. symmetrical voltage sag, (c) +5−Hz frequency jump, (d) 20° phase jump and, at the same time, 0.5-p.u. symmetrical voltage sag, and (e) harmonically distorted and imbalanced grid condition under an off-nominal frequency (55 Hz). To highlight the differences, exaggeratedly large frequency drifts and highly distorted and imbalanced grid conditions are considered in some tests. These situations rarely happen in practice.
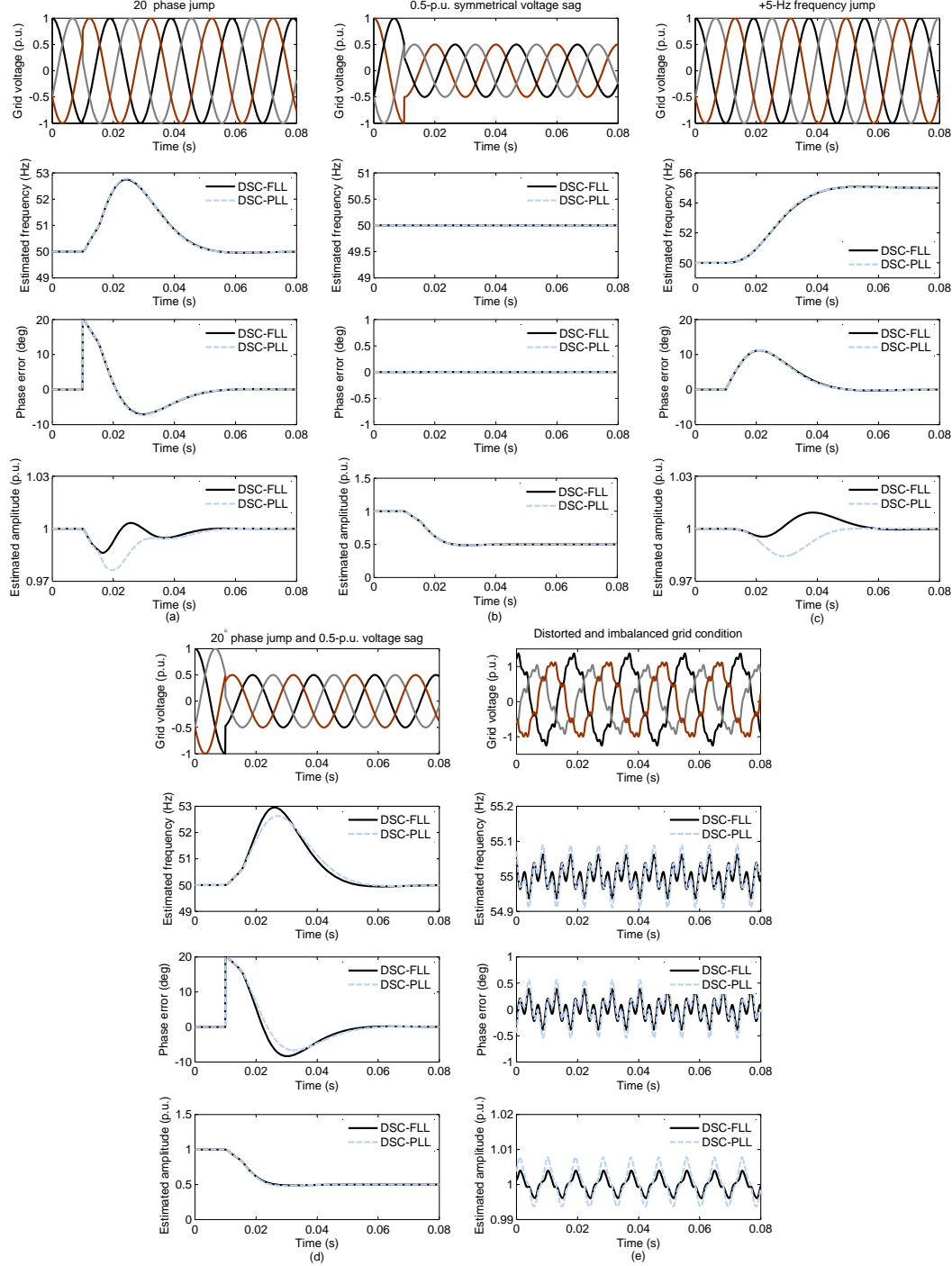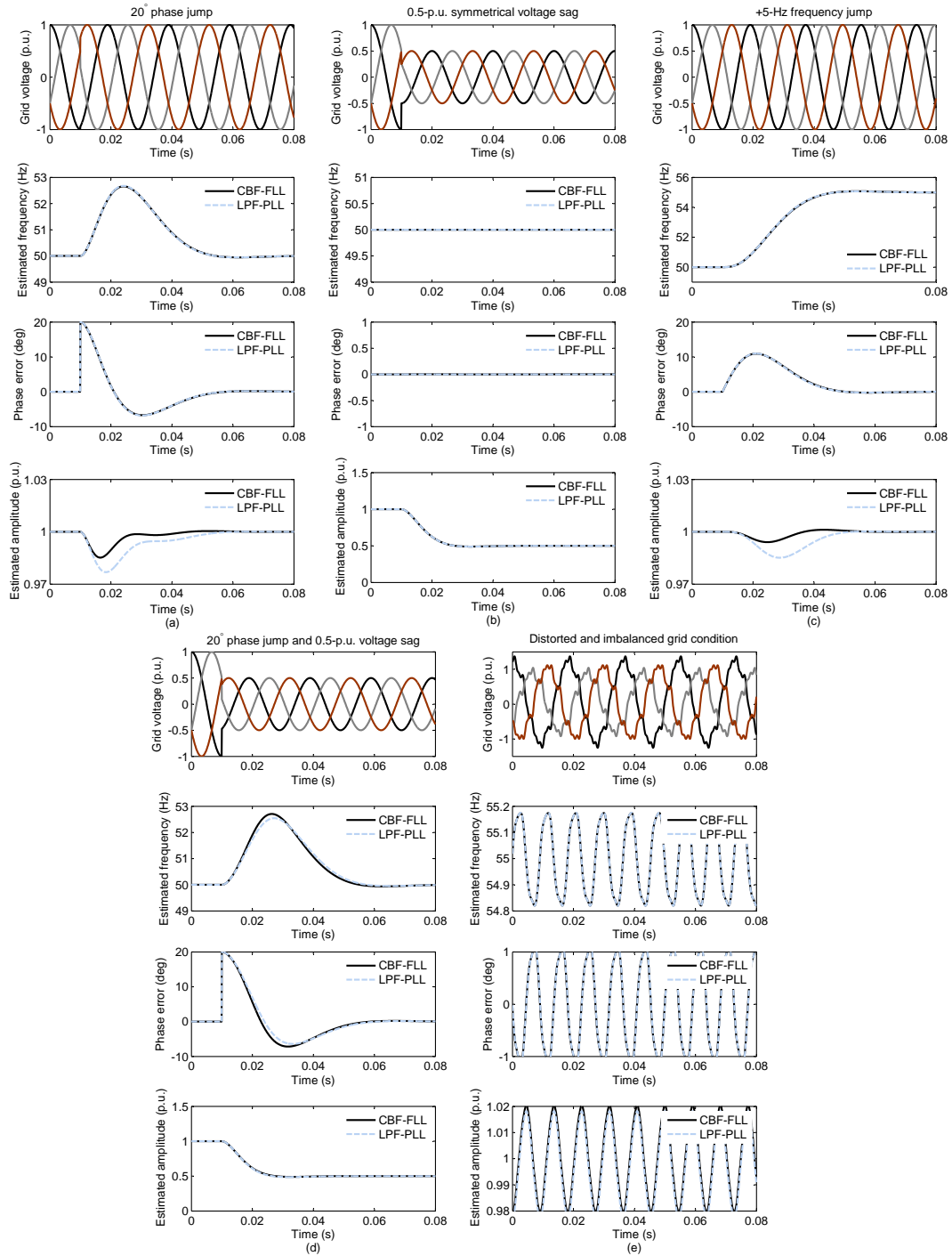
Fig. 18. (a) Performance comparison of the CBF-FLL and LPF-PLL in response to (a) $20°$ phase jump, (b) 0.5-p.u. symmetrical voltage sag, (c) $+5-$Hz frequency jump, (d) $20°$ phase jump and, at the same time, 0.5-p.u. symmetrical voltage sag, and (e) harmonically distorted and imbalanced grid condition under an off-nominal frequency (55 Hz).

made about the CBF-FLL [Fig. 11(a)] and the LPF-PLL [Fig. 16(b)]. There are, however, some aspects that their models cannot predict. This issue may result in a slight performance difference between an FLL and its corresponding PLL. Some numerical results are presented in what follows to highlight these differences.

Figs. 17(a), (b), (c), and (d) compares the transient behavior of the DSC-FLL and DSC-PLL in response to different tests.

These plots, particularly those shown in Fig. 17(d), demonstrate a small dynamic performance difference between the DSC-FLL and DSC-PLL. A reason is that, in both the DSC-FLL and DSC-PLL, there is a coupling between the amplitude and phase/frequency estimation dynamics, but this coupling is not the same in them. This fact is immediately clear from the amplitude normalization stages in the DSC-FLL and DSC-PLL. Fig. 17(e) compares the steady-state performance of

the DSC-FLL and DSC-PLL under a highly distorted and imbalanced grid condition. The grid frequency is fixed at 55 Hz. No very large performance difference is observed between them. The same conclusion can be made by comparing the CBF-FLL and LPF-PLL. Fig. 18 demonstrates the results of this comparison.

In summary, it can be concluded that the DSC-FLL and DSC-PLL (CBF-FLL and LPF-PLL) are equivalent systems from a small-signal perspective, and may demonstrate some small differences in response to large disturbances.

V. COMPARISON OF CBF-FLL AND SOSF-FLL

Fig. 6, as mentioned before, illustrates the block diagram of the SOSF-FLL. The complex signal flow graph description of this structure is shown in Fig. 19(a). After some simple manipulations, it can be represented as Fig. 19(b) and then as Fig. 19(c). The scaler implementation of Fig. 19(c) is shown in Fig. 19(d). This structure is exactly the same as the CBF-FLL [Fig. 11(a)] if the following condition between the parameters of these two FLLs holds.

$$\begin{aligned} k_1 &= k \\ k_2 &= \omega_p \\ \gamma &= \frac{\omega_p \lambda}{k}. \end{aligned} \qquad (9)$$

In summary, the SOSF-FLL and CBF-FLL are equivalent systems if (9) holds. This equivalence can also be verified numerically. To save the space, the numerical results are not shown.

VI. CONCLUSION

In this paper, a research on three-phase FLLs was conducted. First, a review of recent advances in the field was performed. Then, the concept of inloop filter for designing advanced FLLs was proposed. As design examples, the application of the $\alpha\beta$DSC operators and a first-order CBF as the FLL inloop filters was considered and the FLL modeling and tuning in the presence of these filters were performed. It was then demonstrated theoretically and verified experimentally that using an inloop filter enhances the disturbance rejection capability of a standard FLL, but at the cost of reducing its PM and, therefore, causing a larger phase overshoot during phase jumps and faults. Some further evidence on the equivalence of FLLs and PLLs was also given. Finally, it was proved that the CBF-FLL and SOSF-FLL are equivalent systems.

APPENDIX A
MODELING OF A STANDARD FLL WITH A SINGLE INLOOP $\alpha\beta$DSC OPERATOR

To simplify the modeling of the DSC-PLL [Fig. 9(a)], its basic version [see Fig. 20] that uses only one $\alpha\beta$DSC operator as the inloop filter, is modeled here. In the small-signal modeling procedure, it is assumed that the $\alpha\beta$-axis input and output signals are

$$\begin{aligned} v_\alpha(t) &= V_1 \cos(\theta_1) \\ v_\beta(t) &= V_1 \sin(\theta_1) \end{aligned} \qquad (10)$$

$$\begin{aligned} \hat{v}_{\alpha,1}(t) &= \hat{V}_1 \cos(\hat{\theta}_1) \\ \hat{v}_{\beta,1}(t) &= \hat{V}_1 \sin(\hat{\theta}_1) \end{aligned} \qquad (11)$$
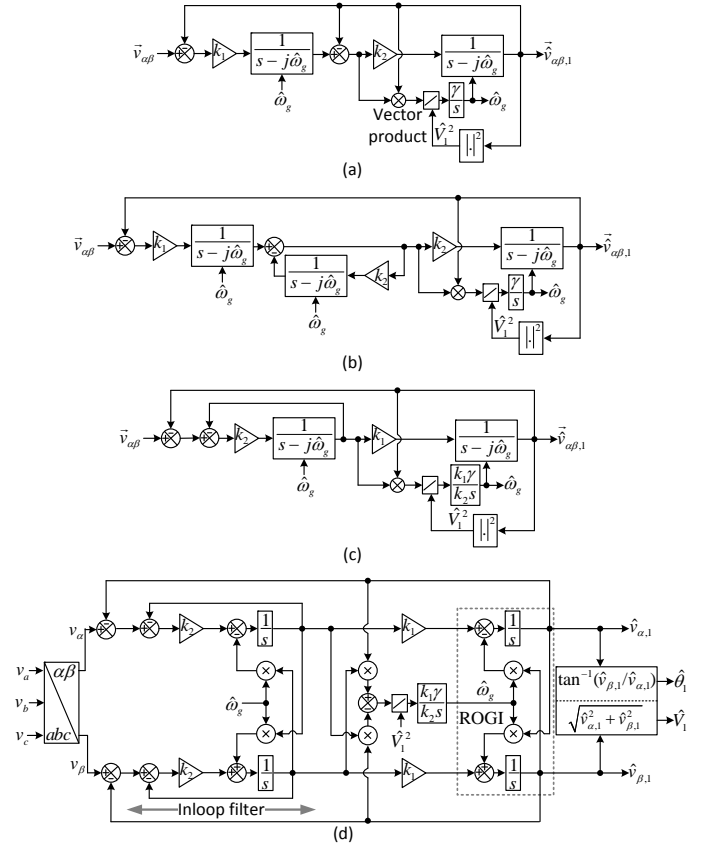

Fig. 19. (a) SOSF-FLL described with the complex signal flow graph, and (b) and (c) its alternative representations. (d) scaler realization of Fig. 19(c).

where V_1 ($\hat{V}_1$) and θ_1 ($\hat{\theta}_1$) denote the actual (estimated) amplitude and phase, respectively, are all functions of time. It is also assumed that the actual and estimated quantities are very close.

A. Modeling of Amplitude Estimation Dynamics

According to Fig. 20, the estimated amplitude can be expressed as

$$\hat{V}_1(t) = \sqrt{\hat{v}_{\alpha,1}^2(t) + \hat{v}_{\beta,1}^2(t)}. \qquad (12)$$

Differentiating (12) with respect to time gives

$$\dot{\hat{V}}_1(t) = \frac{\hat{v}_{\alpha,1}(t)\dot{\hat{v}}_{\alpha,1}(t) + \hat{v}_{\beta,1}(t)\dot{\hat{v}}_{\beta,1}(t)}{\hat{V}_1(t)}. \qquad (13)$$

where, according to Fig. 20,

$$\dot{\hat{v}}_{\alpha,1}(t) = -\hat{\omega}_g(t)\hat{v}_{\beta,1}(t) + kv'_\alpha(t) \qquad (14)$$

$$\dot{\hat{v}}_{\beta,1}(t) = \hat{\omega}_g(t)\hat{v}_{\alpha,1}(t) + kv'_\beta(t). \qquad (15)$$

Substituting (14) and (15) into (13) yields

$$\dot{\hat{V}}_1(t) = k\frac{\hat{v}_{\alpha,1}(t)v'_\alpha(t) + \hat{v}_{\beta,1}(t)v'_\beta(t)}{\hat{V}_1(t)} \qquad (16)$$

in which

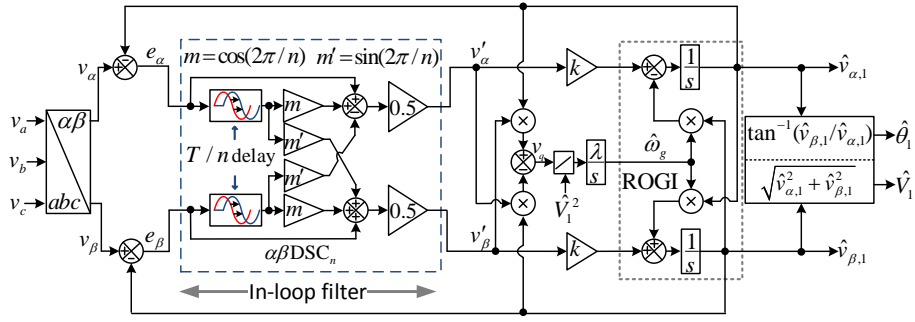$$v'_\alpha(t) = 0.5\left[e_\alpha(t) + me_\alpha(t - T/n) - m'e_\beta(t - T/n)\right] \qquad (17)$$

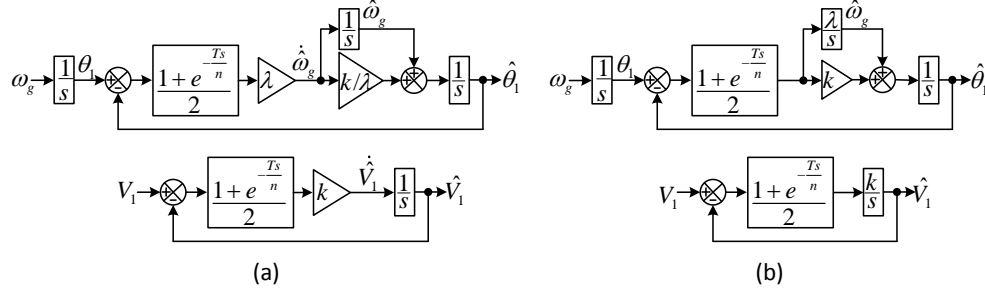Fig. 20. Standard FLL with a single inloop $\alpha\beta$DSC operator.

Fig. 21. (a) Linearized model of Fig. 20, and (b) its alternative representation.

$$v'_\beta(t) = 0.5\left[e_\beta(t) + me_\beta(t - T/n) + m'e_\alpha(t - T/n)\right]. \tag{18}$$

Notice that $e_\alpha(t) = v_\alpha(t) - \hat{v}_{\alpha,1}(t)$ and $e_\beta(t) = v_\beta(t) - \hat{v}_{\beta,1}(t)$. Using equations (10), (11), (17), and (18), (16) can be rewritten as

$$
\begin{aligned}
\dot{\hat{V}}_1(t) = \frac{k}{2}\Big[& V_1(t)\cos\left(\theta_1(t) - \hat{\theta}_1(t)\right) - \hat{V}_1(t) \\
& + V_1^d(t)\cos\left(\theta_1^d(t) - \hat{\theta}_1(t) + 2\pi/n\right) \\
& - \hat{V}_1^d(t)\cos\left(\hat{\theta}_1^d(t) - \hat{\theta}_1(t) + 2\pi/n\right)\Big]
\end{aligned} \tag{19}
$$

where $V_1^d(t) = V_1(t - T/n)$, $\hat{V}_1^d(t) = \hat{V}_1(t - T/n)$, $\theta_1^d(t) = \theta_1(t - T/n)$, and $\hat{\theta}_1^d(t) = \hat{\theta}_1(t - T/n)$.

Assuming that $\theta_1(t) \approx \hat{\theta}_1(t)$, (19) can be approximated by

$$\dot{\hat{V}}_1(t) \approx \frac{k}{2}\left[\left\{V_1(t) - \hat{V}_1(t)\right\} + \left\{V_1^d(t) - \hat{V}_1^d(t)\right\}\right]. \tag{20}$$

Based on (20), the linearized model predicting the amplitude estimation dynamics can be derived as shown in Fig. 21.

B. Modeling of Phase/Frequency Estimation Dynamics

In this section, a small-signal model for predicting the phase and frequency estimation dynamics is developed. During this procedure, the amplitude dynamics are neglected.

Using Fig. 20, the equations representing its frequency estimation dynamics can be expressed as

$$\dot{\hat{\omega}}_g(t) = \frac{\lambda}{\left[\hat{V}_1(t)\right]^2}\left[v'_\beta(t)\hat{v}_{\alpha,1}(t) - v'_\alpha(t)\hat{v}_{\beta,1}(t)\right]. \tag{21}$$

Using equations (10), (11), (17), and (18), (21) can be rewrit-

ten as

$$
\begin{aligned}
\dot{\hat{\omega}}_g(t) \approx \frac{\lambda}{2}\Big[& \sin\left(\theta_1(t) - \hat{\theta}_1(t)\right) + \sin\left(\theta_1^d(t) - \hat{\theta}_1(t) + 2\pi/n\right) \\
& - \sin\left(\hat{\theta}_1^d(t) - \hat{\theta}_1(t) + 2\pi/n\right)\Big].
\end{aligned} \tag{22}
$$

Assuming that $\theta_1 \approx \hat{\theta}_1$, (22) can be approximated by

$$\dot{\hat{\omega}}_g(t) \approx \frac{\lambda}{2}\left[\left\{\theta_1(t) - \hat{\theta}_1(t)\right\} + \left\{\theta_1^d(t) - \hat{\theta}_1^d(t)\right\}\right]. \tag{23}$$

Differentiating from the estimated phase angle, which is expressed as $\hat{\theta}_1(t) = \tan^{-1}\left(\hat{v}_{\beta,1}(t)/\hat{v}_{\alpha,1}(t)\right)$, gives

$$
\begin{aligned}
\dot{\hat{\theta}}_1(t) &= \frac{\dot{\hat{v}}_{\beta,1}(t)\hat{v}_{\alpha,1}(t) - \dot{\hat{v}}_{\alpha,1}(t)\hat{v}_{\beta,1}(t)}{\underbrace{\hat{v}_{\alpha,1}^2(t) + \hat{v}_{\beta,1}^2(t)}_{\left[\hat{V}_1(t)\right]^2}} \\
&= \frac{\hat{\omega}_g(t)\left[\hat{v}_{\alpha,1}^2(t) + \hat{v}_{\beta,1}^2(t)\right] + k\overbrace{\left[v'_\beta(t)\hat{v}_{\alpha,1}(t) - v'_\alpha(t)\hat{v}_{\beta,1}(t)\right]}^{\left[\hat{V}_1(t)\right]^2\dot{\hat{\omega}}_g(t)/\lambda}}{\left[\hat{V}_1(t)\right]^2} \\
&= \hat{\omega}_g(t) + \frac{k}{\lambda}\dot{\hat{\omega}}_g(t).
\end{aligned} \tag{24}
$$

Using (23) and (24), the linearized model predicting the phase/frequency estimation dynamics can be derived as shown in Fig. 21.

A second look at Fig. 20 and its small-signal model, i.e., Fig. 21(b), suggests a general yet simple approach for modeling FLLs with inloop filter. The FLL illustrated in Fig. 20, as mentioned before, is a standard FLL with an $\alpha\beta$DSC operator as its inloop filter. And the small-signal model of this FLL is the same as that of the standard one with the dq-frame

equivalent of its inloop filter. Therefore, as a general modeling approach, the small-signal model of the standard FLL with an inloop filter can be obtained by including the *dq*-frame equivalent of the inloop filter transfer function into the small-signal model of the standard FLL. A hidden assumption here is that the *dq*-frame equivalent of the inloop filter transfer function is a real (as opposed to complex) coefficient filter.

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