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An Eight-Switch Five-Level Current Source Inverter

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***Abstract* — This paper proposes an eight-switch three-phase five-level current source inverter (CSI), which employs only one traditional H6 inverter and two shunt branches at the DC side to realize the five-level switching. The corresponding space vector modulation (SVM) strategy for the proposed CSI topology is also presented, which uses the two shunt-connected power switches to add certain special modulation-state segments to ensure the switching instants completed under lower current stresses and lower power dissipation. Compared with the state-of-the-art CSI solutions, the proposed topology has a comparable hardware cost as the three-level H6 CSI, while outputs five-level currents. The low output THD may help to reduce the sizes of the passive components in the system, and the modulation scheme reduces the switching and conduction losses of the semiconductor switching devices in H6 CSI module, which can make it possible to increase the output current rating of the system in a certain degree. Simulation and experimental results verified the performance of the proposed CSI.**

***Index Terms* — current source inverter; multi-level converter; modulation.**

I. Introduction

In general, inverter topologies can be categorized into two types—voltage source inverter (VSI) and current source inverter (CSI). In the past and until now, VSI has been the dominant inverter topology. At the same time, attempts toward advancing the CSI have never been stopped, and the penetration of CSI topologies continuously challenges the VSI market, mainly due to the uniqueness of CSI topologies (e.g., the inherent short-circuit protection ability, high voltage boost capability, and superior dv/dt performance). On the contrary, these unique aspects are the critical issues for the VSI applications [1], [2]. In this respect, the CSI topologies are promising, especially in certain applications, e.g. high power electric drives [3] and photovoltaic (PV) systems [4], requiring a high voltage boosting capability.

Additionally, to reduce the dependence of bulky output filters for less harmonic emissions and also to lower the voltage stress on power devices, multilevel technologies have firstly been introduced to VSI systems. As such, low-rating power devices can be used (contributing to cost reduction), and also potentially, a high efficiency can be achieved. Thus, many multilevel VSI systems have been commercialized in the past few years, among which the neutral point clamped (NPC) multilevel inverters, flying capacitor (FC) multilevel inverters, cascaded H-bridge (CHB) multilevel inverters, and modular multilevel converters (MMC) are the favorites [5]-[7]. In a similar way, the multilevel switching characteristics can be a great added value to CSI topologies [8]. In recent years, many attempts have been made to improve the multilevel CSI (MCSI) technologies. For instance, the single-rating inductor MCSI was proposed by employing multiple H6 CSI modules connected in parallel on the AC side [9], [10]. However, current circulating and imbalance issues are associated with this kind of MCSI topology. Furthermore, to remove the passive elements of the modules, the multi-rating inductor MCSI was introduced in [11] to alleviate the current circulating and imbalance problem and a paralleled-MCSI with independent DC-links was introduced in [12]. The paralleled-MCSI topology effectively addresses the issues of circulating currents and unbalances, whose corresponding modulation schemes were proposed in [13] and [14]. Moreover, an improved paralleled MCSI topology using a shared DC-link was presented in [15]. In addition, certain variants like the buck-boost derived MCSI [16] have been developed to extend the operating range. To enable the high-power operation, a current source modular multilevel converter (CS-MMC) was proposed in [17], which utilizes multiple current source cells connected in parallel with a significant increased number of power devices and inductors.

With the above considerations, this paper first reviews the general configuration characteristics of various MCSI topology solutions. Then, this paper proposes an eight-switch three-phase five-level CSI topology with the corresponding space vector modulation (SVM) strategy, which enables the eight-switch CSI topology output the five-level switching current but using fewer power switches, thereby lowers hardware cost. It should be pointed that the SVM scheme is much simpler than the conventional methods, being another advantage of the proposed inverter. The rest of this paper is organized as follows. In Section II, the conventional MCSI topological attempts are briefly introduced. In Section III, the circuit configurations for the proposed eight-switch three-phase five-level CSI topology are proposed, and then the compatible modulation strategies using the SVM are presented

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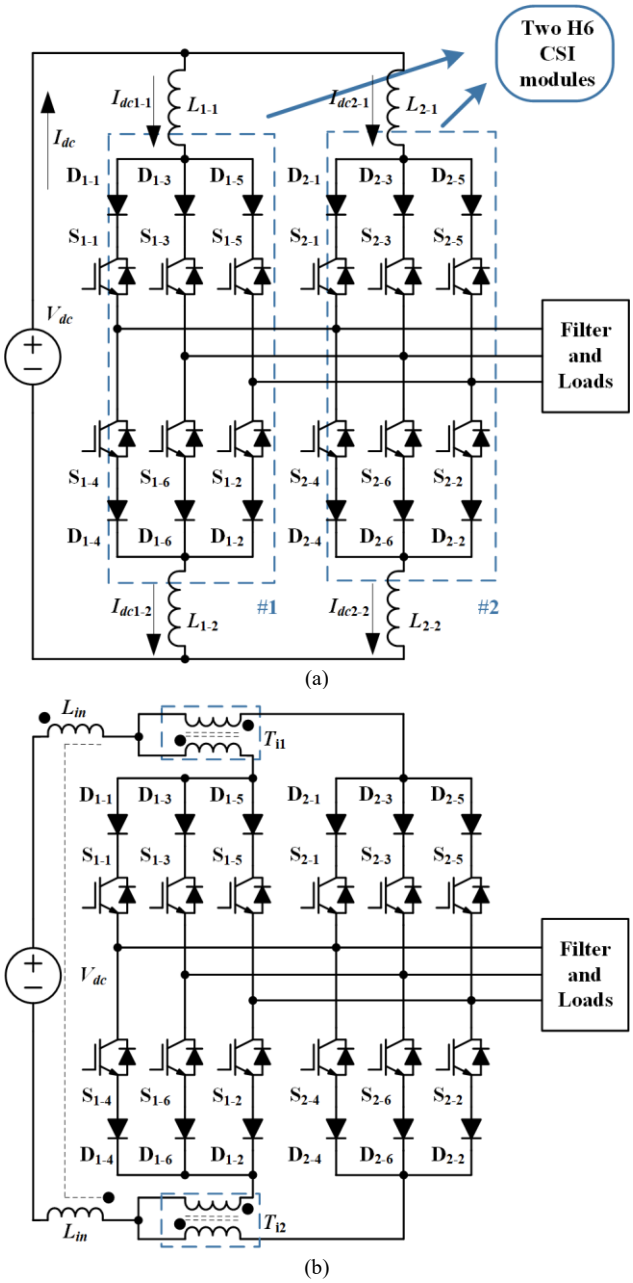

Fig. 1. Three-phase single-rating inductor MCSI topologies: (a) with four inductors of the same rating and (b) with two interleaved inductors (coupled inductors).

in detail. The modulation sequences as well as the characteristics of operation are also analyzed. Finally, Matlab simulation and the experimental tests are presented to verify the performance of the proposed topology.

II. Topologies and Modulation of Three-Phase Multilevel CSIs

A conventional CSI consisting of six power switches is the simplest and most fundamental CSI. The DC current flows through two power switches, and commutates between lateral arms, which has six active states and three null states. To reduce the current stress on each power switch, multi-level technologies were introduced to CSI. There are several types of three-phase MCSI topologies, i.e., the single-rating inductor MCSI, the multi-rating inductor MCSI, the paralleled H-bridge MCSI, the buck-boost MCSI, and the CS-MMC systems, which will be briefly introduced below.

Fig. 1(a) shows the conventional five-level single-rating

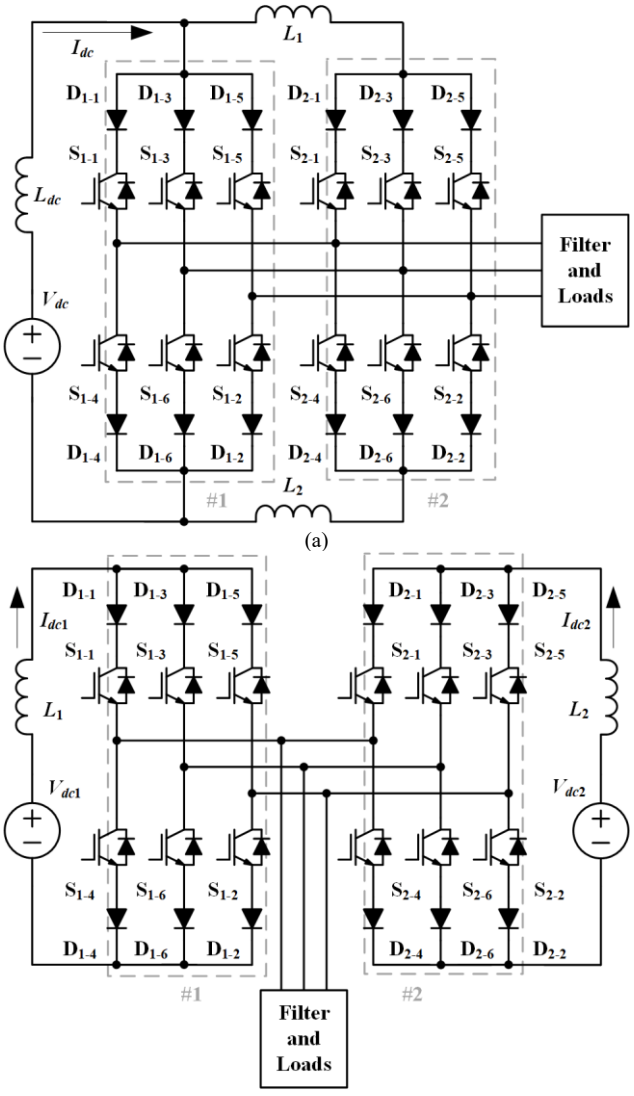

Fig. 2. Three-phase five-level CSI topologies derived from the single-rating MCSI shown in Fig. 1(a): (a) with two multi-rating inductors and (b) using two-parallel H-bridge inverters.

inductor MCSI [9], [10], which consists of two H6 converter modules connected in parallel on the AC side. In this way, five-level output currents can be obtained. On the DC side, two H6 modules are connected to the DC rail four inductors (two for each) as illustrated in Fig. 1(a). The inductors are of the same current rating, contributing to the reduction of the current ripples. However, due to the parasitic parameters in the system, the output current may be unbalanced, or the DC current may circulate between two modules. This becomes the major drawback of single-rating inductor MCSI, which hinders its applications. Notably, the single-rating inductors ($L_{1\text{-}1}$, $L_{1\text{-}2}$, $L_{2\text{-}1}$, and $L_{2\text{-}2}$) can be replaced with interphase inductors (coupled inductors) as shown in Fig. 1(b). Doing so further contributes to the reduction of current ripples and overall system volume. More specifically, when the SVM is adopted to control the MCSI, the inductance of the single-rating inductors can theoretically be reduced to L' as [15]:

$$L' = (1 - \frac{1}{\sqrt{3} m_a}) L_o \tag{1}$$

where m_a is the modulation index and L_o is the original inductor value.

The multi-rating inductor five-level CSI and the paralleled

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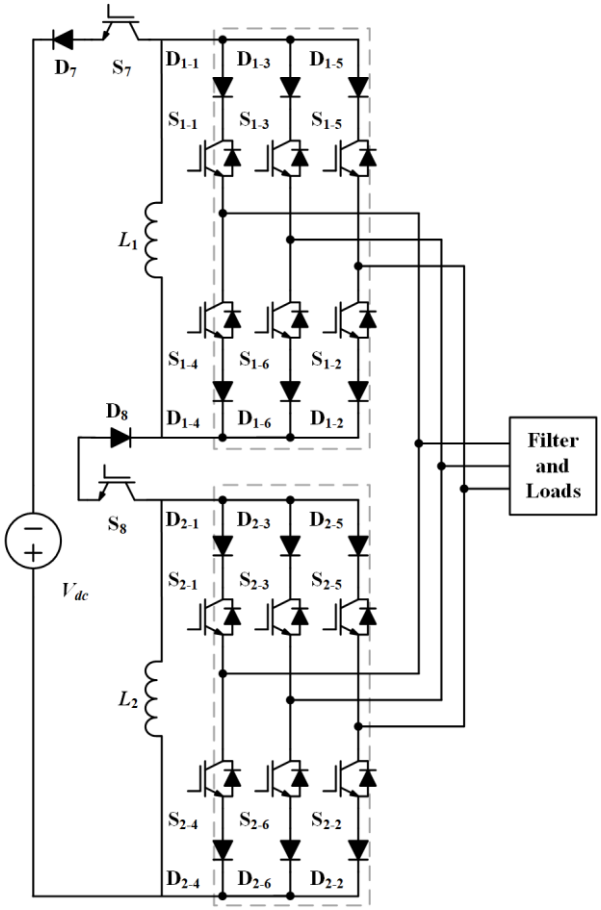

Fig. 3. Circuit schematic of the buck-boost five-level CSI.

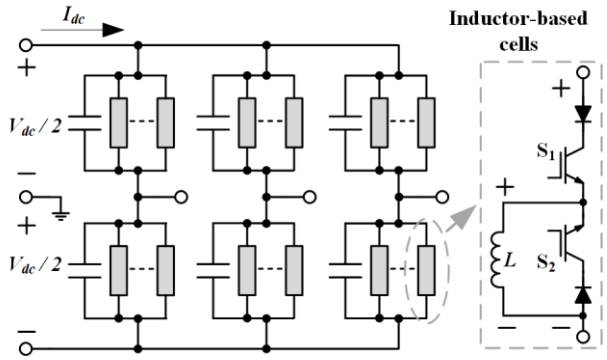

Fig. 4. Three-phase current source MMC topology with its inductor-based cells.

H-bridge five-level CSI are shown in Fig. 2(a) and (b), respectively. Both topologies can be derived from the classic single-rating inductor MCSI shown in Fig. 1(a). Clearly, each of the two five-level CSI topologies consists of two H6 CSI modules. The multi-rating inductor five-level CSI can be taken as a dual FC voltage-fed multilevel converter. Two different inductors are employed to split the input current [18], and there are no passive components in the sub-H6 modules, as shown in Fig. 2(a). However, the problem of circulating and unbalance currents still exists. To solve this, the paralleled H-bridge MCSI with two independent current sources can be adopted [19]. It resembles the single-rating inductor MCSI by using two DC current sources in such a way to address the unbalance and current-circulating issues. However, the parallel H-bridge inverter shown in Fig. 2(b) has two major disadvantages, i.e., requiring two sources, which limits practical applications, and unequal input currents, which challenges the implementation.

Furthermore, the buck-boost five-level CSI was presented to extend the operating range [16]. The configuration of this topology is shown in Fig. 3. As it can be observed, different from the conventional boost operation, the aim of this topology is to realize the low voltage output. However, the current unbalance issue remains, and the configuration of power switches in series with the voltage source is not recommended for high power applications, limiting the development of this MCSI topology. Another MCSI topology is the CS-MMC topology [17], which can be considered as the dual topology of the voltage-source MMC. Here, the CS-MMC employs inductor-based cells, as shown in Fig. 4, which are connected in parallel. Apparently, the CS-MMC possesses the high-power capability with integrated multiple cells, but it utilizes much more power devices and inductors, which may lead to high costs as well as high volume.

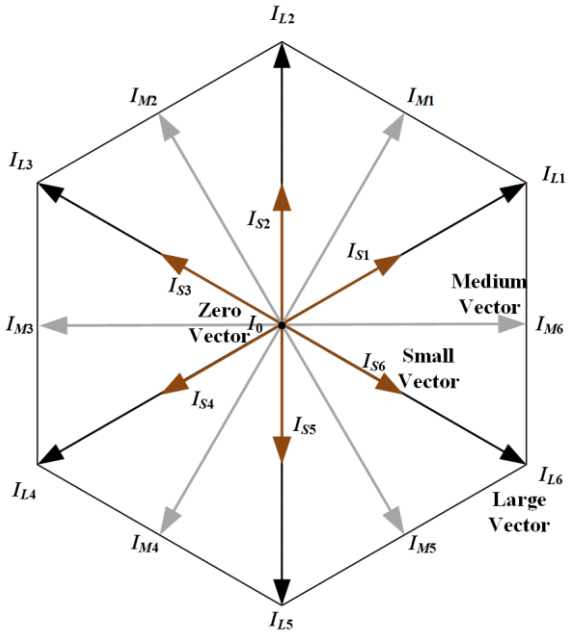

Fig. 5. Space vector diagram of the conventional five-level CSI topologies.

Except for the CS-MMC solution, all the above prior-art three-phase five-level CSIs consist of two H6 CSI modules. In addition, the current-available technology of the five-level SVM schemes for these MCSI topologies is mainly to control the switching combinations of two H6 converters. Normally, the space vectors can be classified into four types, i.e., zero, small, medium, and large vectors [14], as shown in Fig. 5. Then, the modulation scheme has 81 combinations for five-level CSI systems [15], which makes it very complicated and difficult to control and implement. A list of the switching combinations for the conventional five-level CSI SVM is given in Table I. The switching combinations are represented here with {xx;yy}, where the numbers of 'xx' and 'yy' refer to the corresponding ON-switch in the first and the second H6 inverter module, respectively. For instance, the vector {16; 23} means that the power devices of #1 and #6 of the first H6 inverter and the power devices of #2 and #3 of the second H6 inverter are switched on.

In fact, the conventional H6 CSI utilizes the least number of power devices, but the resultant current stress is the highest. Furthermore, the efficiency and power quality issue have been plagued for many years in the applications of CSI topologies. On the other hand, the majority of three-phase MCSI topologies use multiple H6 CSI modules to solve the above problem. However, in this case, the hardware costs as well as

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TABLE I
SWITCHING COMBINATIONS FOR THE CONVENTIONAL FIVE-LEVEL CSI

Space vectors		ON-switching combinations	Output currents		
			Phase-A	Phase-B	Phase-C
Large vectors	I_{L1}	{12;12}	I_{dc}	0	$-I_{dc}$
	I_{L2}	{23;23}	0	I_{dc}	$-I_{dc}$
	I_{L3}	{34;34}	$-I_{dc}$	I_{dc}	0
	I_{L4}	{45;45}	$-I_{dc}$	0	I_{dc}
	I_{L5}	{56;56}	0	$-I_{dc}$	I_{dc}
	I_{L6}	{16;16}	I_{dc}	$-I_{dc}$	0
Medium vectors	I_{M1}	{23;12} {12;23}	$0.5I_{dc}$	$0.5I_{dc}$	$-I_{dc}$
	I_{M2}	{34;23} {23;34}	$-0.5I_{dc}$	I_{dc}	$-0.5I_{dc}$
	I_{M3}	{45;34} {34;45}	$-I_{dc}$	$0.5I_{dc}$	$0.5I_{dc}$
	I_{M4}	{56;45} {45;56}	$-0.5I_{dc}$	$-0.5I_{dc}$	I_{dc}
	I_{M5}	{16;56} {56;16}	$0.5I_{dc}$	$-I_{dc}$	$0.5I_{dc}$
	I_{M6}	{12;16} {16;12}	I_{dc}	$-0.5I_{dc}$	$-0.5I_{dc}$
Small vectors	I_{S1}	{16;23} {23;16} {12;14} {14;12} {12;36} {36;12} {12;25} {25;12}	$0.5I_{dc}$	0	$-0.5I_{dc}$
	I_{S2}	{12;34} {34;12} {23;14} {14;23} {23;36} {36;23} {23;25} {25;23}	0	$0.5I_{dc}$	$-0.5I_{dc}$
	I_{S3}	{23;45} {45;23} {34;14} {14;34} {34;36} {36;34} {34;25} {25;34}	$-0.5I_{dc}$	$0.5I_{dc}$	0
	I_{S4}	{34;56} {56;34} {45;14} {14;45} {45;36} {36;45} {45;25} {25;45}	$-0.5I_{dc}$	0	$0.5I_{dc}$
	I_{S5}	{45;16} {16;45} {56;14} {14;56} {56;36} {36;56} {56;25} {25;56}	0	$-0.5I_{dc}$	$0.5I_{dc}$
	I_{S6}	{56;12} {12;56} {16;14} {14;16} {16;36} {36;16} {16;25} {25;16}	$0.5I_{dc}$	$-0.5I_{dc}$	0
Zero vector	I_0	{14;14} {14;36} {14;25} {36;14} {36;36} {36;25} {25;14} {25;36} {25;25} {12;45} {45;12} {23;56} {56;23} {34;16} {16;34}	0	0	0

the space occupation will be increased significantly, leading to lower power density, and also the associated issues like the current unbalance and the current-circulating are even challenging and difficult to tackle in those topologies. It is thus necessary to develop cost-effective CSI solutions.

III. THE PROPOSED EIGHT-SWITCH FIVE LEVEL CSI

A. Eight-switch five-level CSI topology

In light of the above considerations, an eight-switch three-phase five-level CSI is proposed in this paper, whose circuit diagram is shown in Fig. 6. It can be observed that two shunt branches are connected in parallel between the current source and a conventional H6 converter. In specific, two power switches, S_7 and S_8, are self-commutating devices. Diodes D_7 and D_8 are connected in series with S_7 and S_8 to ensure reliable reverse voltage-blocking. These two shunt-connected switches are used to bypass the input current of the rear-end H6 circuitry. Besides, diodes D_9 and D_{10} are employed to prevent the circulating current. The DC-link inductors L_1 and L_2 are employed for suppressing the DC current ripples. Furthermore, in order to balance the shunt-branch currents, L_1 and L_2 are configured with the same rating, and the interphase inductors (coupled inductors) can also be adopted to further reduce the volume. Fig. 6(a) illustrates the proposed eight-switch five-level CSI topology with normal inductor configurations. And as seen in Fig. 6(b), an inductor L_d with the interphase inductors L_{t1} and L_{t2} is included. According to (1), if using the configuration of Fig. 6(b) to generate the same current ripple, then the total DC-side inductance value (L_d + L_{t1}) can be reduced to $1-\frac{1}{\sqrt{3}m_a}$ times of the original L_1 [15], [20]. Regardless of the dc inductors' configuration, this paper assumes the topology in Fig. 6(a) to elaborate the operational principle and performance of the proposed CSI.

In the proposed CSI, the input current of the rear-end inverter has three states, i.e., 0, $0.5I_{dc}$, and I_{dc}. Depending on the output current modes, the space vectors can be classified as zero, small, and large vectors. Accordingly, there will be 37 switching combinations in theory for the whole converter,

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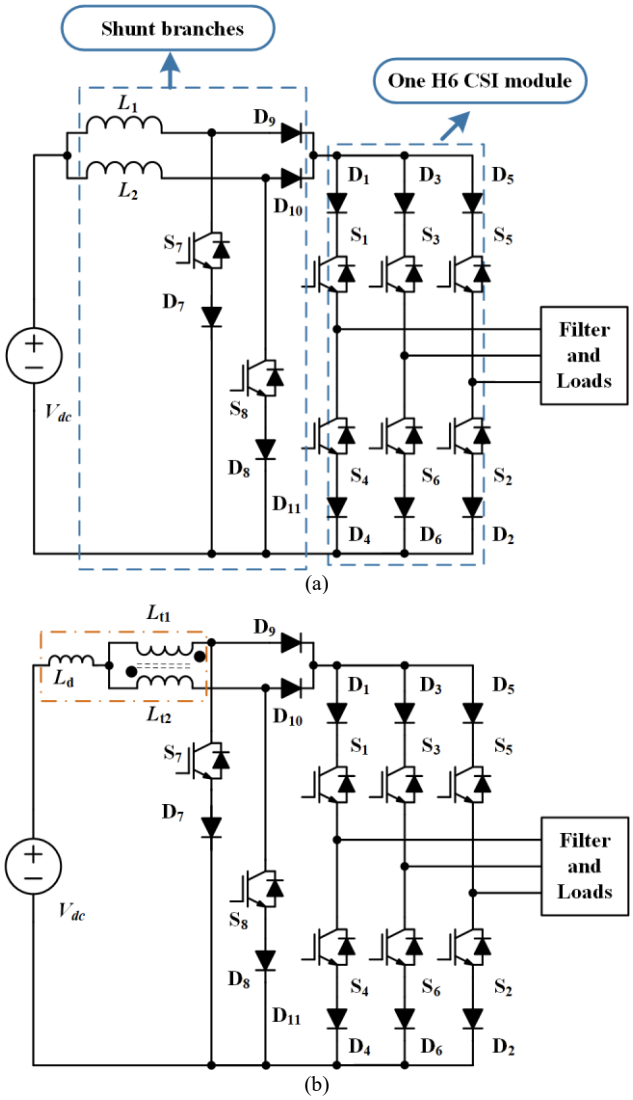

Fig. 6. Proposed eight-switch five-level CSI topology with (a) two same rating inductors and (b) interleaved inductors.

including 6 large-vector switching combinations, 12 small-vector switching combinations and 19 zero-vector switching combinations. All the possible switching combinations with the corresponding output currents are categorized in Table II, where the numbers refer to the corresponding ON-switch in the proposed CSI. However, it can be found that most of the zero-vector switching combinations are redundant, for example, {1478} gives two paths for shunt-DC currents. In order to obtain lower conduction currents as well as the dissipation, the zero vector can select with the switching combination of {78}. Therefore, when excluding the redundant switching combinations and considering the discharging period of the two inductors, the modulation states of the proposed eight-switch five-level CSI can be defined into 13 vectors, which can then be obtained with 19 possible switching combinations.

Fig. 7 further shows the exampled equivalent circuits for each kind of vectors. In detail, the zero vector can be obtained, when both S_7 and S_8 are turned ON, and then all the output currents are bypassed as shown in Fig. 7(a). When only S_7 or S_8 is turned ON, a small vector can be generated as shown in Fig. (b), and in this case, the output current will be $0.5I_{dc}$. When S_7 and S_8 are both turned OFF as shown in Fig. 7(c), the large vectors can be generated being the same as those for the conventional H6 CSI, where only one upper-arm switch (S_1, S_3, S_5) and one-lower arm switch (S_4, S_6, S_2) of the rear-end H6 inverter are turned ON, leading to the output current being I_{dc}. Therefore, the proposed CSI can generate a five-level output current.

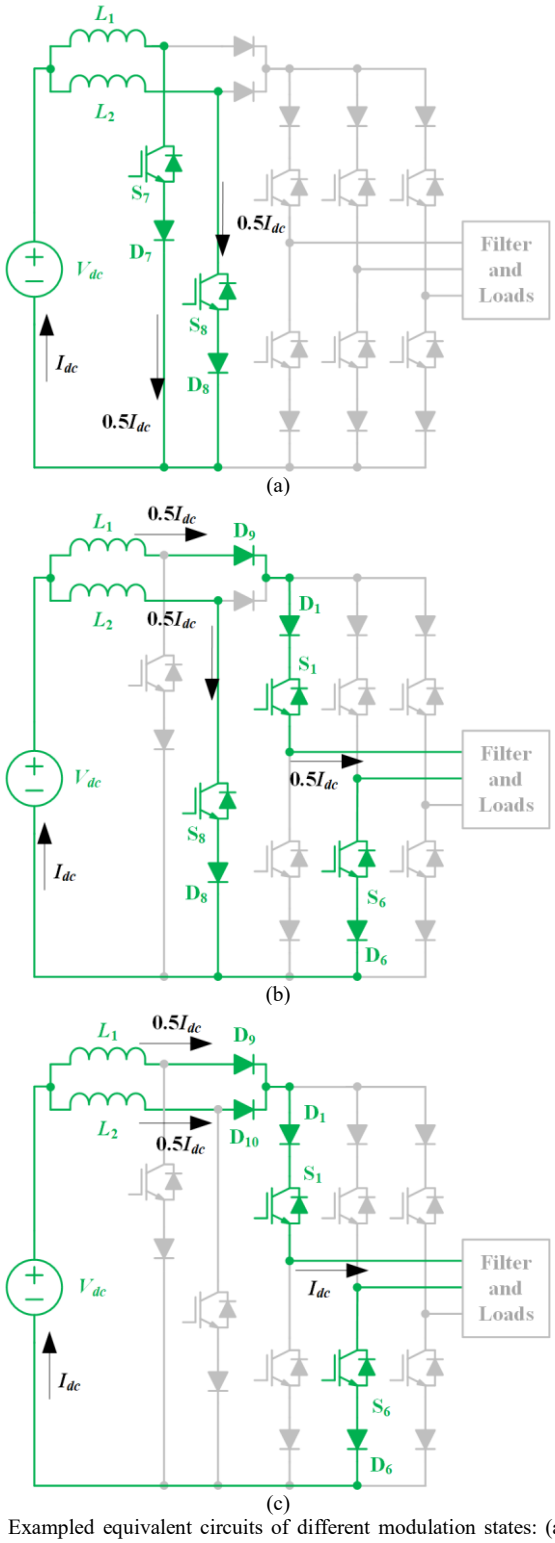

Fig. 7. Exampled equivalent circuits of different modulation states: (a) zero vector, (b) small vector, and (c) large vector.

Compared to the prior-art three-phase five-level CSIs, one feature of the proposed CSI topology is that it utilizes fewer power switching devices. That is, the eight-switch CSI topology does not require two H6 converters (i.e., in total, a minimum of 12 power switches and 12 power diodes), but eight power switches and 10 power diodes to generate a five-level output. In addition, the SVM method for the

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TABLE II
SWITCHING COMBINATIONS FOR THE PROPOSED FIVE-LEVEL CSI

Space vectors		ON-switching combinations	Output currents		
			Phase-A	Phase-B	Phase-C
Large vectors	I_{L1}	{12}	I_{dc}	0	$-I_{dc}$
	I_{L2}	{23}	0	I_{dc}	$-I_{dc}$
	I_{L3}	{34}	$-I_{dc}$	I_{dc}	0
	I_{L4}	{45}	$-I_{dc}$	0	I_{dc}
	I_{L5}	{56}	0	$-I_{dc}$	I_{dc}
	I_{L6}	{16}	I_{dc}	$-I_{dc}$	0
Small vectors	I_{S1}	{127} {128}	$0.5I_{dc}$	0	$-0.5I_{dc}$
	I_{S2}	{237} {238}	0	$0.5I_{dc}$	$-0.5I_{dc}$
	I_{S3}	{347} {348}	$-0.5I_{dc}$	$0.5I_{dc}$	0
	I_{S4}	{457} {458}	$-0.5I_{dc}$	0	$0.5I_{dc}$
	I_{S5}	{567} {568}	0	$-0.5I_{dc}$	$0.5I_{dc}$
	I_{S6}	{167} {168}	$0.5I_{dc}$	$-0.5I_{dc}$	0
Zero vector	I_0	{14} {36} {25} {78} {147} {367} {257} {148} {368} {258} {1478} {3678} {2578} {1278} {2378} {3478} {4578} {5678} {1678}	0	0	0

proposed CSI can be much simpler, which avoids the complicated combinations of the dual converters.

B. Space Vector Implementation

As mentioned above and listed in Table II, there are 13 potentially available space vectors that can be obtained by 19 switching combinations, and subsequently, five-level output currents can be generated. In order to generate a proper switching sequence, the modulation should follow these principles:

a) Always use the nearest current vectors to generate the reference vector to reduce output harmonics.
b) Keep the switching operation of S_7 and S_8 equally distributed in one switching period in order to reduce the dc inductors' current ripple.
c) Use S_7 and S_8 to add certain special modulation-state segments to ensure the switching instants completed under lower current stresses and lower power dissipation.

To select and use the nearest vectors to synthesize the reference vector, the general method is to use three vectors to define the triangular region, in which the target reference vector locates. Fig. 8 illustrates this synthesizing principle. If let any three vectors ($\vec{i}_a$, $\vec{i}_b$ and $\vec{i}_c$) to define a triangular region in the $\alpha\beta$ plane, and the reference vector $\vec{i}_{ref}$ locates within this region, then $\vec{i}_{ref}$ can be synthesized from

$$\vec{i}_{ref} = \vec{k}_a + \vec{k}_b + \vec{i}_c = \frac{\left|\vec{k}_a\right|}{n_a}\vec{i}_a + \frac{\left|\vec{k}_b\right|}{n_b}\vec{i}_b + (1 - \frac{\left|\vec{k}_a\right|}{n_a} - \frac{\left|\vec{k}_b\right|}{n_b})\vec{i}_c \quad (2)$$

where n_a and n_b are the distances between the adjacent vectors.

As exemplified in Fig. 9(a) for Sector I, each sextant has 2 large vectors, 2 small vectors and 1 zero vector. Based on the above principles, the modulation scheme is proposed to partition each sector into five regions. That is, in this paper, the overall space vector diagram of the eight-switch five-level CSI can be divided into 30 regions, as shown in Fig. 9(b).

The modulation strategy can be classified into two operational modes: Mode 1 (three-level switched currents) and Mode 2 (five-level switched currents), which will be illustrated below in detail by taking Fig. 9(a) as an example.

In Mode 1, the reference vector locates in Region 1 (ΔABE), which is defined within $\{I_{S6}, I_{S1}, I_0\}$, as shown in Fig. 9(a). That is, the converter modulates with the same zero and small vectors as the conventional five-level CSI solutions. And the AC output will be 3-level switching currents. The detailed operational sequences for Sector I in one modulation period are illustrated in Fig. 10, where t_{act1} and t_{act2} are the switching transitions for the rear-end H6-inverter switches (S_1-S_6), while t_{n1}-t_{n6} are the switching transitions for the shunt branch switches of S_7 and S_8. In addition, the switching interval between t_{n2} and t_{n3} and the switching interval between t_{n4} and t_{n5} are generated to ensure the zero current switching (ZCS) for S_2 and S_6, respectively, where S_7 and S_8 are turned ON simultaneously, leading to the expected zero vector. This ZCS configuration makes the equivalent commutation behave the same as that for the H7 CSI in [21]. It has been discussed and demonstrated in [21] that, the shunt connected switch can take over all the switching losses, and effectively promote the efficiency of CSI.

In mode 2, when the modulation index m_a is above 0.5, the reference in Sector I can rotate among Region 2, Region 3, Region 4, and Region 5, with 5-level switched currents at the AC output. It is defined that Region 2 and Region 5, Region 3 and Region 4 are symmetric about the angle bisector of Sector I. When the reference vector locates in Region 2, the nearest three composition space vectors are $\{I_{L6}, I_{S1}, I_{S6}\}$. Similarly, the vector compositions for Region 5 are $\{I_{S6}, I_{L1}, I_{S1}\}$, as shown in

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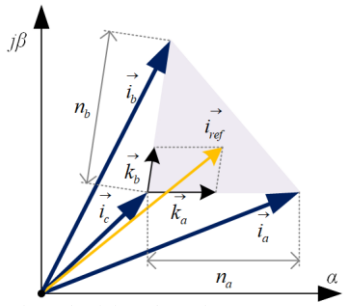
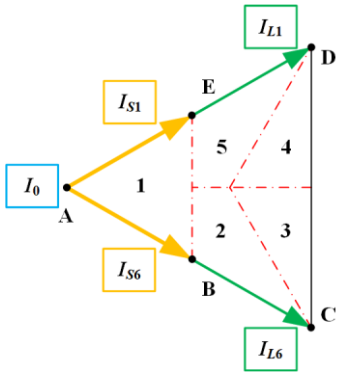
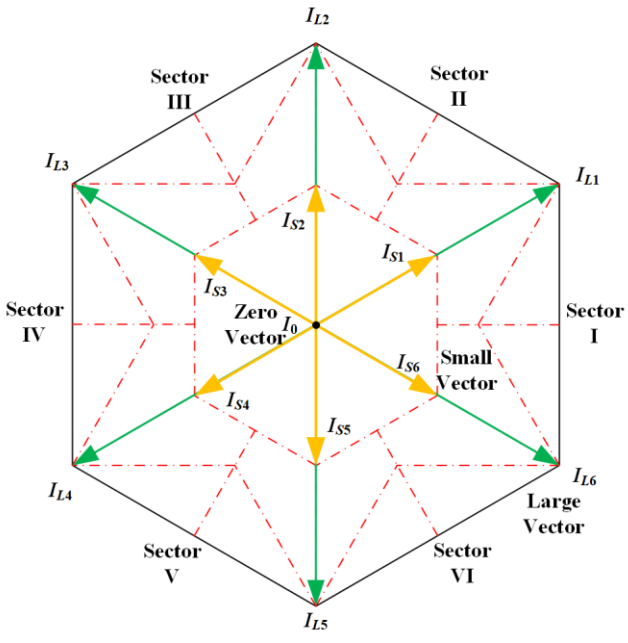


Fig. 8. Illustration of synthesizing the reference current with three arbitrary vectors.



(a)



(b)

Fig. 9. Vector diagrams of the proposed SVM for the eight-switch five-level CSI topology: (a) region divisions in Sector I and (b) overall space vectors.

Fig. 9(a). The corresponding switching intervals for Region 2 and Region 5 are demonstrated in Fig. 11(a) and Fig. 11(d), respectively. In those switching intervals, S_7 or S_8 is employed to keep an extended turning-ON interval within T_{ins}, so that the switching for S_2 and S_6 can operate with only $0.5I_{dc}$. As for Region 3 in Fig. 9(a), the nearest space vector composition will be $\{I_{L6}, I_{L1}, I_{S6}\}$. However, in order to switch S_2 and S_6 with small vector ($0.5I_{dc}$), another small space vector I_{S1} should be inserted. That is, the vector compositions become $\{I_{S6}, I_{L6}, I_{S1}, I_{L1}\}$, and the switching sequences are demonstrated in Fig. 11(b). Accordingly, the vector compositions of Region 4 are the same, i.e., $\{I_{L6}, I_{S1}, I_{L1}, I_{S6},\}$ but with different dwell time and switching sequence, and the switching sequences are demonstrated in Fig. 11(c). It is noted that region 3 and region

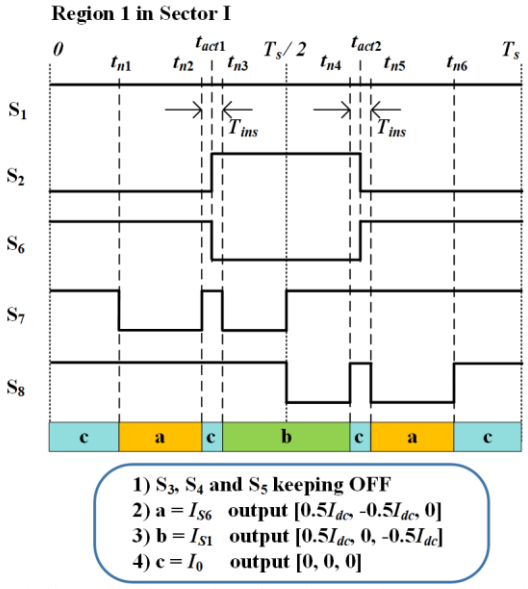


Fig. 10. Switching interval operation of Mode 1 (Region 1, in one period).

4 should have the additional intervals (T_{ins}) for S_7 or S_8 to ensure the switching of S_2 and S_6 being under a lower current stress, i.e., $0.5I_{dc}$.

It should be noted that there is no medium vector (e.g., {12;16} of the conventional five-level SVM in Table I) in the proposed five-level CSI modulation because the current can only flow through two phase legs in one converter-bridge. In addition, for balancing the inductor currents and keeping low current ripples, the power switches S_7 and S_8 should be operated with an equal duration in one switching period. Therefore, in the proposed modulation scheme, the switching sequences of S_7 are theoretically in symmetry with that of S_8 in a half-period.

According to the above modulation scheme, the dwell time of the SVM states should be carefully calculated. Taking Region 2 of Sector I as an example, the current reference should be synthesized with I_{L6}, I_{S1} and I_{S6} referring to Fig. 9(a), which are expressed as

$$\begin{cases} I_{L6} = \dfrac{2\sqrt{3}}{3} I_{dc} e^{-j\frac{\pi}{6}} \\ I_{S1} = \dfrac{\sqrt{3}}{3} I_{dc} e^{j\frac{\pi}{6}} \\ I_{S6} = \dfrac{\sqrt{3}}{3} I_{dc} e^{-j\frac{\pi}{6}} \end{cases} \tag{3}$$

Subsequently, the reference vector I_{ref} can be synthesized using

$$\begin{cases} I_{ref} = m_a I_{dc} e^{j\theta} \\ T_S I_{ref} = T_a I_{L6} + T_b I_{S1} + T_c I_{S6} \\ T_a + T_b + T_c = T_S \end{cases} \tag{4}$$

where m_a is the modulation index, T_S is the switching period, and T_a, T_b, and T_c refer to the corresponding dwell time within one period for vectors I_{L6}, I_{S1} and I_{S6}.

As for Region 3 of Sector I, the current reference is synthesized with four vectors $\{I_{S6}, I_{L6}, I_{S1}, I_{L1}\}$ as shown in Fig. 9(a), among of which, current vectors I_{S6}, I_{L6}, and I_{S1} are the same as (3), and the vector I_{L1} can be expressed as

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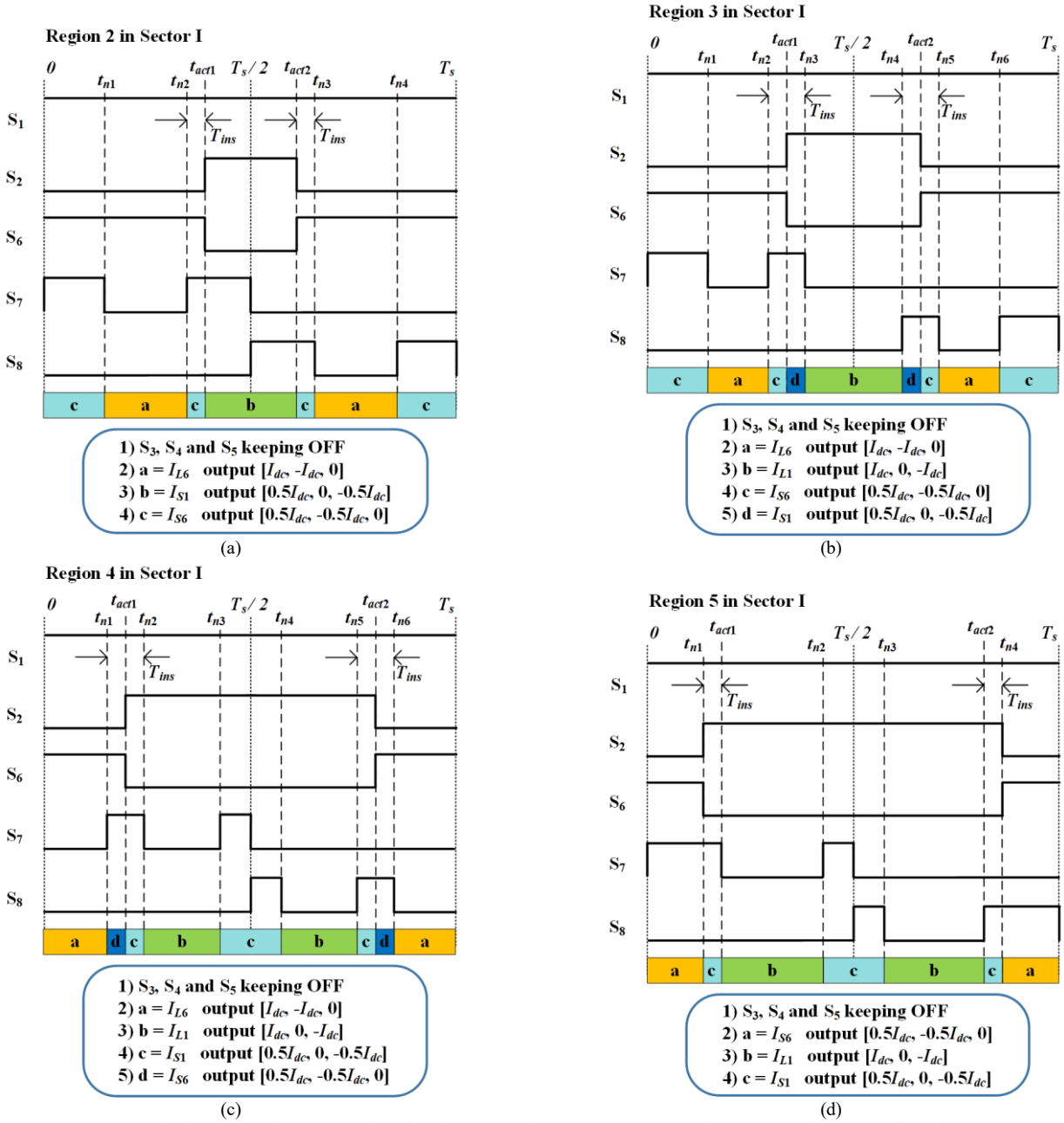

(a) (b) (c) (d)

Fig. 11. Switching interval operation of Mode 2 in one period: (a) Region 2, (b) Region 3, (c) Region 4, and (d) Region 5.

$$I_{L1} = \frac{2\sqrt{3}}{3} I_{dc} e^{j\frac{\pi}{6}} \tag{5}$$

The state I_{S1} is the pre-set interval to guarantee the switching completion of S_2 and S_6. If the dwell time of I_{S1} is denoted as T_d, the current reference vector can be synthesized with

$$\begin{cases} I_{ref} = m_a I_{dc} e^{j\theta} \\ T_S I_{ref} = T_a I_{L6} + T_b I_{L1} + T_c I_{S6} + T_d I_{S1} \\ T_a + T_b + T_c + T_d = T_S \end{cases} \tag{6}$$

Specifically, T_d can be regulated by T_{ins}, following

$$T_{[n2,act1]} = T_{[act1,n3]} = T_{[n4,act2]} = T_{[act2,n5]} = \frac{1}{2} T_{ins} = \frac{1}{2} T_d \tag{7}$$

where T_a, T_b, T_c, and T_d refer to the corresponding dwell time within one period for vectors I_{L6}, I_{L1}, I_{S6} and I_{S1}, and $T_{[n2,act1]}$, $T_{[act1,n3]}$, $T_{[n4,act2]}$, and $T_{[act2,n5]}$ are the corresponding time interval between each switching transitions. In a similar way, all dwell time can be calculated, and the resultant dwell time in Sector I has been summarized in Table III.

C. Current Balancing Scheme

The current unbalance is a typical problem for multi-level CSIs. In fact, the unbalanced current input will degrade the output power quality, and may result in instability or even system damage [22]-[26]. Thus, a few current balancing methods for the single-rating inductor MCSI have been presented in the literature. Some of these current balancing solutions modified the modulation strategies, e.g., the phase-shifted PWM [24], but with a basic open-loop control, which cannot guarantee the accuracy. For a closed-loop scheme, the common method for current balancing is to sample the DC input currents (such as $I_{dc1\text{-}1}$ and $I_{dc2\text{-}1}$ in Fig. 1(a)), and uses the sampled currents to re-distribute the vector states (zero vectors [20], active vectors [25], and medium vectors [26]) in the modulation schemes. In this way, the unbalancing

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TABLE III
DWELL TIME AND VECTORS IN SECTOR I

Region	Vector	Overall Dwell Time
1	I_{S6}	$T_a = 2m_aT_s\sin(\frac{\pi}{6}-\theta)$
	I_{S1}	$T_b = 2m_aT_s\sin(\frac{\pi}{6}+\theta)$
	I_0	$T_c = T_s - T_a - T_b$
2	I_{L6}	$T_a = T_s(2m_a\cos\theta - 1)$
	I_{S1}	$T_b = 2m_aT_s\sin(\frac{\pi}{6}+\theta)$
	I_{S6}	$T_c = T_s - T_a - T_b$
3	I_{L6}	$T_a = T_s[\sqrt{3}m_a\sin(\frac{\pi}{3}-\theta)-1]+\frac{1}{2}T_{ins}$
	I_{L1}	$T_b = m_aT_s\sin(\frac{\pi}{6}+\theta)-\frac{1}{2}T_{ins}$
	I_{S6}	$T_c = T_s - T_a - T_b - T_d$
	I_{S1}	$T_d = T_{ins}$
4	I_{L6}	$T_a = m_aT_s\sin(\frac{\pi}{6}-\theta)-\frac{1}{2}T_{ins}$
	I_{L1}	$T_b = T_s[\sqrt{3}m_a\sin(\frac{\pi}{3}+\theta)-1]+\frac{1}{2}T_{ins}$
	I_{S1}	$T_c = T_s - T_a - T_b - T_d$
	I_{S6}	$T_d = T_{ins}$
5	I_{S6}	$T_a = 2m_aT_s\sin(\frac{\pi}{6}-\theta)$
	I_{L1}	$T_b = T_s(2m_a\cos\theta - 1)$
	I_{S1}	$T_c = T_s - T_a - T_b$

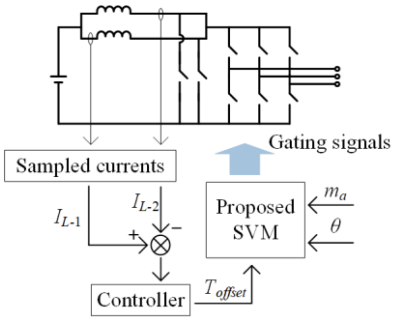

Fig. 12. Control diagram for current balancing scheme.

issue can be addressed to a large extent. However, these solutions incur heavy computation, since for the basic modulation there are already 81 switching combinations.

Obviously, the proposed modulation scheme ensures the power switches S_7 and S_8 with symmetrical equal operation to balance the inductor currents $I_{L\text{-}1}$ and $I_{L\text{-}2}$. In addition, the inductors L_1 and L_2 are configured with the same current rating. However, in practical applications, the currents of $I_{L\text{-}1}$ and $I_{L\text{-}2}$ may not be exactly the same, because of the electrical parasitic parameters of the two shunt branch components. Therefore, the current balancing issue should also be considered in the proposed topology.

Nevertheless, the DC side configuration of the proposed CSI topology has some unique features. That is, $I_{L\text{-}1}$ and $I_{L\text{-}2}$ are mainly controlled by S_7 and S_8 and their turn-on operation will charge L_1 and L_2, respectively. Fortunately, S_7 and S_8 theoretically have an equivalent role for the rear-end inverter, so that the switching of S_7 or S_8 can be controlled independently as long as the sum of their dwell time in one modulation period is a certain fixed value. Therefore, considering the above features, the basic operation for the proposed CSI topology is to adjust the switching transitions of S_7 and S_8 in a way to balance the inductor currents, while keeping the same overall dwell time of each state.

When the switch S_7 (or S_8) is turned ON, the inductor L_1 (or L_2) will be directly charged by the DC source V_{dc}. Therefore, the peak and trough values of the two inductor current ripples are interleaved by a half switching period. Setting the inductor currents to be sampled every half switching cycle can obtain the initial current I_{z1}, I_{z2} and the half cycle current I_{h1}, I_{h2}. And let $I_{L\text{-}1}$ and $I_{L\text{-}2}$ be the actual sampled average currents of the two inductors and $I_{L\text{-}1}{}^*$ and $I_{L\text{-}2}{}^*$ be the demanded ideal current values, the corresponding currents can be expressed as (8) when assuming $I_{L\text{-}1}$ is larger than $I_{L\text{-}2}$.

$$\begin{cases} I_{L\text{-}1} = \dfrac{1}{2}(I_{z1}+I_{h1}) \\ I_{L\text{-}2} = \dfrac{1}{2}(I_{z2}+I_{h2}) \\ \Delta I_{L\text{-}1} = I_{L\text{-}1} - I_{L\text{-}1}{}^* = \dfrac{V_{dc}}{L_1}\dfrac{1}{2}T_{offset} \\ \Delta I_{L\text{-}2} = I_{L\text{-}2}{}^* - I_{L\text{-}2} = \dfrac{V_{dc}}{L_2}\dfrac{1}{2}T_{offset} \\ I_{L\text{-}1}{}^* = I_{L\text{-}2}{}^* = \dfrac{1}{2}I_{dc} \end{cases} \tag{8}$$

where T_{offset} is the switching transition offset. Depending on the above equations, T_{offset} can be expressed as

$$T_{offset} = \frac{2(I_{L\text{-}1}-I_{L\text{-}2})}{V_{dc}}\frac{L_1L_2}{L_1+L_2} \tag{9}$$

Therefore, the operation of S_7 and S_8 can be adjusted by T_{offset} in order to obtain the relatively equal inductor currents. Taking Region 2 of Sector I as an example (shown in Fig. 11(a)), the switching transitions t_{n1} and t_{n4} can be modified as

$$\begin{cases} t_{n1}' = t_{n1} - T_{offset} \\ t_{n4}' = T_s - t_{n1}' - 2T_{offset} \end{cases} \tag{10}$$

where t_{n1} and t_{n4} are the original switching transitions, and t_{n1}' and t_{n4}' refer to the regulated new transitions. Notably, other operational intervals remain unchanged in this case.

In a similar way, this switching regulation scheme can be applied to all the modulation regions, and the resultant inductor currents will then be balanced. Fig. 12 shows the control diagram of the proposed current balancing scheme. The inductor currents are sampled by half switching cycle to obtain the average values $I_{L\text{-}1}$ and $I_{L\text{-}2}$. And then, they are subtracted and the result is given into the controller to produce the switching transition offset T_{offset} using (8)-(9). With the information of modulation index m_a and delay angle θ, the proposed modulation strategy is able to calculate out the actual modified switching transitions, which can effectively resolve the current balancing issue.

D. Operational feature benchmarking

Table IV compares the switching and conducting characteristics in Sector I for one carrier period (with the symmetric 5-segment modulation) among the four selected MCSI solutions, i.e., the conventional H6 CSI, conventional 5-level CSI, and the proposed eight-switch 5-level CSI.

The power-device count of the proposed eight-switch five-level CSI is obviously less than the conventional

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TABLE IV
COMPARISON OF SWITCHING AND CONDUCTING CHARACTERISTICS
IN SECTOR I FOR ONE CARRIER PERIOD (WITH SYMMETRIC 5-SEGMENT MODULATION)

Topology	Conventional H6 CSI	Single-rating inductor 5-level CSI	Proposed eight-switch 5-level CSI			
Output waveform	3-level	5-level	5-level			
Power Switches	6	12	8			
Power diodes	6	12	10			
Switching current stress	S_1-S_6	S_1-S_{12}	Mode 1		Mode 2	
			S_1-S_6	S_7, S_8	S_1-S_6	S_7, S_8
	I_{dc}	$0.5I_{dc}$	ZCS	$0.5I_{dc}$	$0.5I_{dc}$	$0.5I_{dc}$
Switching counts	8	16	4	12	4	8
Conducting current	I_{dc}	$0.5I_{dc}$	Zero	Small	Large	
			$0.5I_{dc}$	$0.5I_{dc}$	I_{dc}	
Conducting switches	2	4	2	3	2	
Conducting diodes	2	4	2	4	2 ($0.5I_{dc}$)+2 (I_{dc})	

single-rating five-level CSI. More specifically, the switch count has reduced by one third. The proposed CSI has two operational modes. In Mode 1, switches S_1-S_6 can operate with zero current switching, while S_7 and S_8 switch with $0.5I_{dc}$ resulting in 12 switching counts per switching cycle. In Mode 2, all the power switches can operate with $0.5I_{dc}$, and the total switching counts is 12 either. It means that the switching losses of the proposed CSI can be three-quarters of the conventional single-rating five-level CSI.

For the current stress, the current rating through the additional switch S_7 or S_8 is half of that in the rear-end switches (S_1-S_6) for the proposed topology as summarized in Table IV, which means the switches S_1-S_6 (together with D_1-D_6) can be relatively high power but cheap devices, while S_7 and S_8 (may together with D_7-D_{10}) can be employed by high performance devices with low current rating. This feature enables a cost-effective customization according to the CSI applications. Furthermore, it gives the possibility to improve the efficiency by only using SiC switches for S_7 and S_8.

TABLE V
PARAMETERS OF THE PROPOSED EIGHT-SWITCH
FIVE-LEVEL CURRENT SOURCE INVERTER

Parameters	Value
Power rating	3.18 kW
DC current I_{dc}	12 A
DC inductance, L_1, L_2	5 mH
AC filter capacitance	10 μF
Switching frequency (S_1-S_6)	5 kHz
Switching frequency (S_7, S_8)	10 kHz
Output AC frequency	50 Hz
Load resistance	16 Ω

IV. PERFORMANCE EVALUATION

A. Simulation Results

Referring to Fig. 6(a), a simulation model has been built up in MATLAB/SIMULINK to evaluate the performance of the proposed eight-switch five-level CSI topology. The system parameters are listed in Table V. The DC current is maintained at 12 A in the simulations. Resistor of 16 Ω is adopted as the load with AC output capacitor filter. The performance of the proposed MCSI is compared with the conventional H6 inverter.

Fig. 13 first compares the phase-A output currents of the conventional H6 CSI and the proposed eight-switch five-level CSI, where the modulation index m_a is 0.8. In this case, the H6 CSI is employed with a 5-mH DC inductor to obtain a relatively comparable DC inductor current ripple, while other configuration parameters are the same as the proposed converter. It can be seen in Fig. 13 that the proposed eight-switch CSI topology achieves a five-level output current (blue lines) as expected, while the H6 CSI only produces three-level switching current. When the AC capacitor filters are added, the corresponding filtered currents of phase-A are shown as the red lines. Furthermore, the three-phase output voltages and currents of the proposed CSI are shown in Fig. 14. The performance of the proposed MCSI is further validated

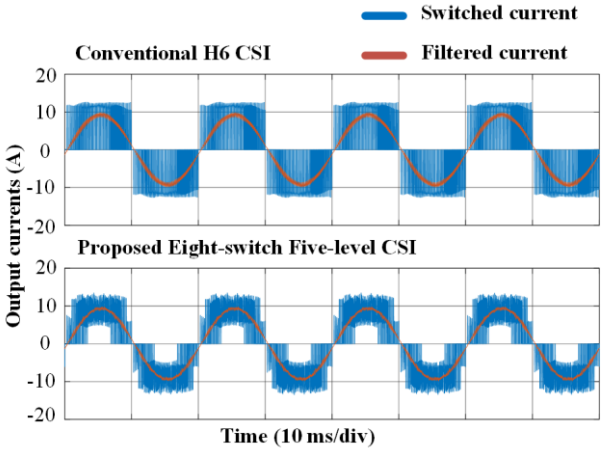

Fig. 13. Simulation results of the proposed converter (output currents of phase-A).

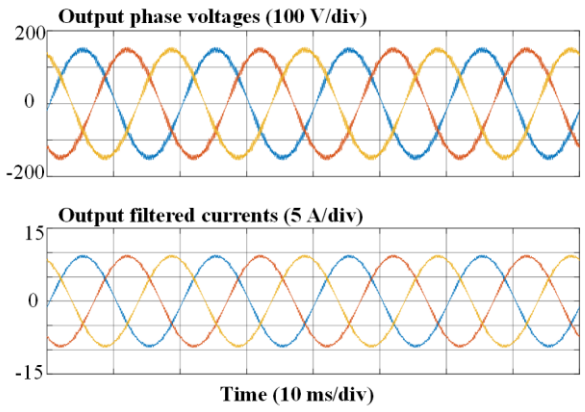

Fig. 14. Output three-phase voltages and filtered currents of the proposed five-level CSI.

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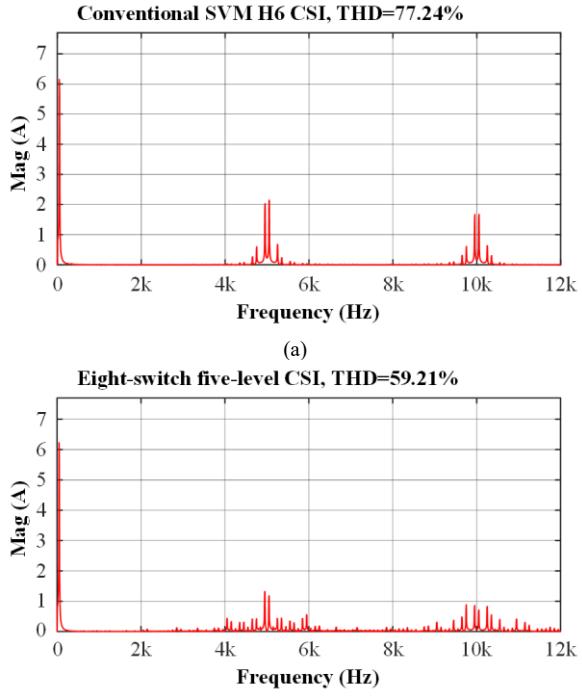

Fig. 15. Harmonic components of the output switched current (Fig. 13) of (a) the conventional H6 CSI and (b) the proposed eight-switch five-level CSI.

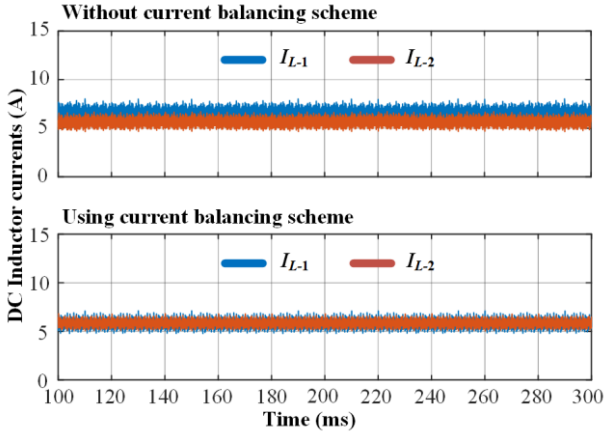

Fig. 16. Comparisons (simulations) of the inductor currents of the eight-switch five-level CSI topology without and with the current balancing control scheme (L_1: 4.5 mH, L_2: 5.5 mH).

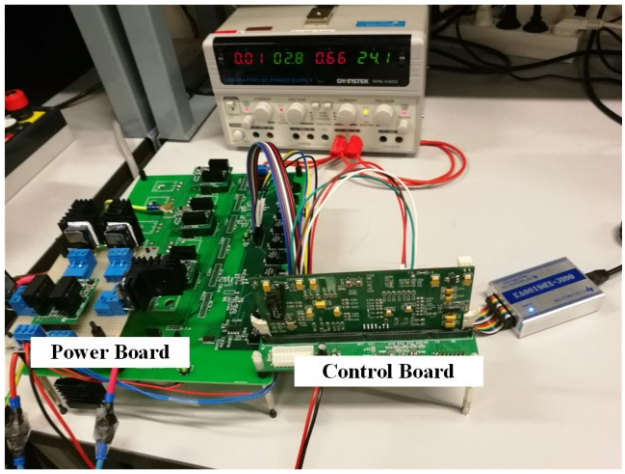

Fig. 17. Experimental setup of the proposed eight-switch five-level CSI.

through the fast Fourier transform (FFT) analysis of the output switching currents (see Fig. 13), as shown in Fig. 15, where the

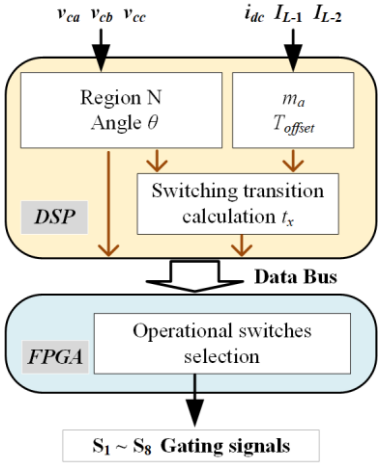

Fig. 18. Implemented control system for the proposed eight-switch five-level CSI shown in Fig. 17.

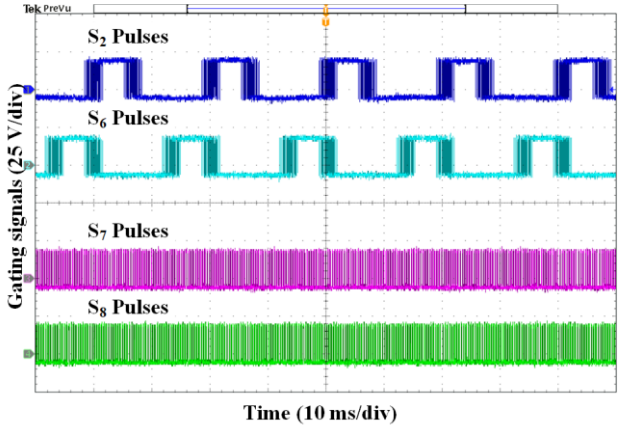

Fig. 19. Gating sequences (experiments) for the power devices S_2, S_6, S_7 and S_8 of the proposed eight-switch five-level CSI topology.

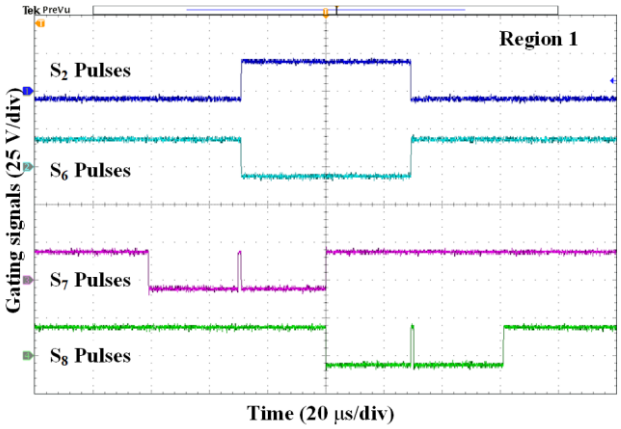

Fig. 20. Detailed switching intervals (experiments) for the power devices S_2, S_6, S_7 and S_8 of Region 1 (m_a: 0.3).

switching frequency harmonic components in the proposed CSI are much lower than the conventional H6 CSI. As a result, the total harmonic distortion (THD) value of the switching current in eight-switch five-level CSI is 59.21 %, while it is 77.24% for the conventional H6 CSI topology. Therefore, it has been validated that the proposed eight-switch five-level CSI has better output performances over the conventional H6 CSI.

Additionally, the proposed current balancing scheme is also tested. The inductance of the eight-switch five-level CSI in the simulation model is changed, where L_1 is 4.5 mH and L_2 is 5.5 mH. Fig. 16 shows the inductor currents of the proposed

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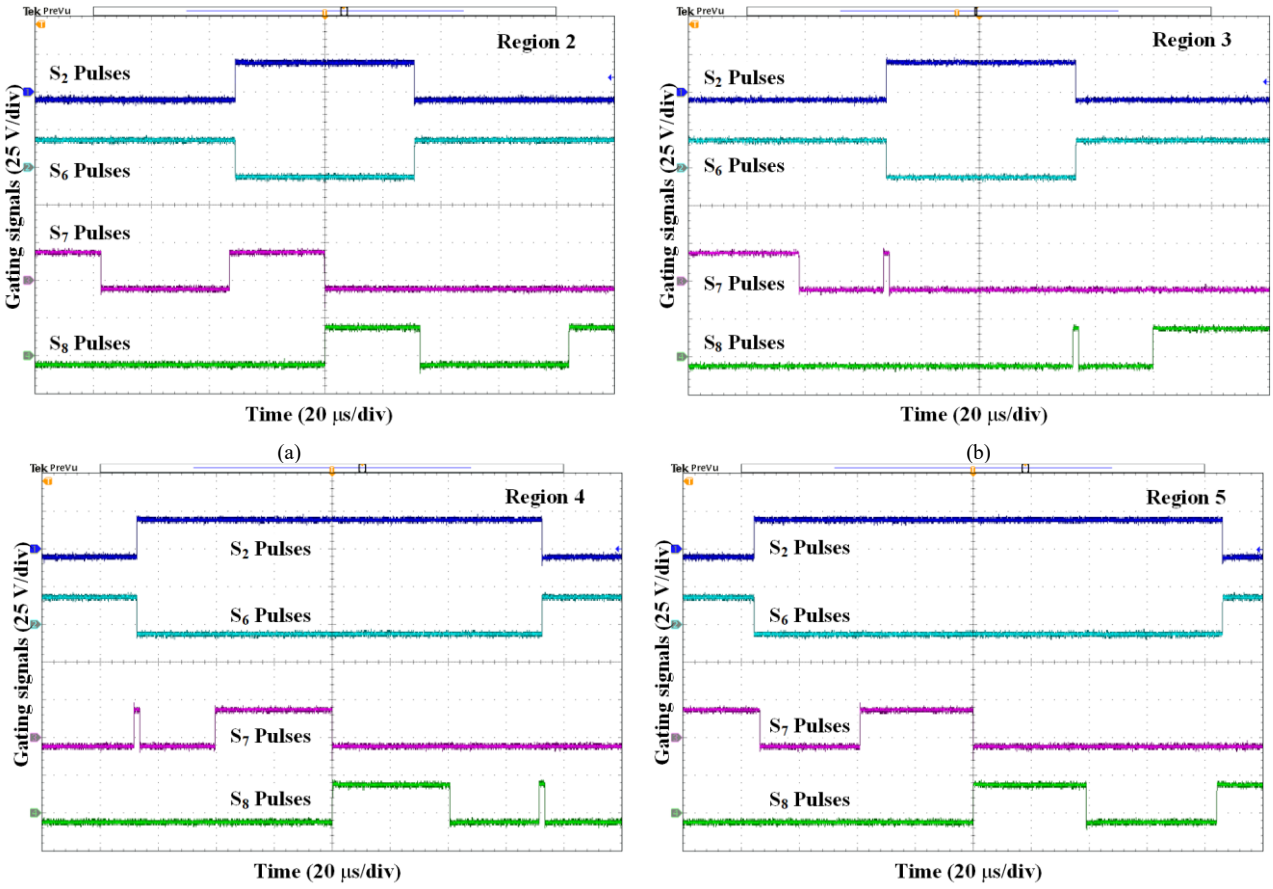

Fig. 21. Detailed switching intervals (experiments) for the power devices S_2, S_6, S_7 and S_8 of (a) Region 2, (b) Region 3, (c) Region 4, and (d) Region 5 (m_a: 0.8).

inverter without and with the current balancing control. As observed in Fig. 16, when the converter is operating without any current balancing control but only with the basic modulation scheme, the currents through L_1 and L_2 are not balanced, where L_1 carries more input current than L_2 and withstands a relatively higher current ripple. By contrast, when employing the proposed current balancing scheme discussed in Section III(C), the currents $I_{L\text{-}1}$ and $I_{L\text{-}2}$ of the proposed CSI topology are well balanced. The effectiveness of the current balancing strategy is thus verified.

B. Experimental Verifications

To further validate the performance of the proposed eight-switch five-level CSI topology, a downscale experimental prototype has been built up in the laboratory. Fig. 17 shows the experimental setup, and Fig. 18 illustrates the implementation diagram of the control system, respectively. As shown in Fig. 18, on the control board, the AC voltages and the sampled DC inductor currents are input to the micro controller unit, which is a Digital Signal Processor (DSP, TMS320F28335). The region judgement and the switching time calculation (together with the current balancing algorithm) are implemented in the DSP controller. Then, the calculated results are directly transferred to another processor unit, i.e., an FPGA xc3s500e from XILINX Spartan3E, to implement the switching selection and the driving pulses generation functions. On the power board, the other power switches S_1-S_6 are silicon IGBT devices from Infineon (part no.: IKW20N60T), while all the power diodes are from CREE (part no.: C2D20120D). To obtain a cost-effective performance, power switches S_7 and S_8 (part no.: C2M0160120D) are SiC devices from CREE. The other parameters are the same as those listed in Table V.

With the proposed SVM scheme presented in Section III, the experimental gating sequences for S_2, S_6, S_7, and S_8 are shown in Fig. 19. Clearly, the extra power devices S_7 and S_8 are switched more frequently than the other power switches in the proposed modulation. However, the use of SiC power devices for S_7 and S_8 will not compromise the entire system efficiency. In addition, the driving pulses for switches S_2, S_6, S_7, and S_8 of Region 1 are presented in Fig. 20 with the modulation index m_a = 0.3. When m_a becomes 0.8, the corresponding zoomed view of the switching intervals for the power devices S_2, S_6, S_7 and S_8 in Region 2-5 are shown in Fig. 21. The time interval of T_{ins} is set to 3μs. Seen from Fig. 20 and 21, the switching transitions of different switches and the actual switching process in Sector I can be clearly identified, which fully complies with the proposed modulation scheme.

Furthermore, the experimental results of phase-A voltage, output switched current, and inductor currents $I_{L\text{-}1}$ and $I_{L\text{-}2}$ are shown in Fig. 22, while the FFT analysis of output filtered current in phase-A is shown in Fig. 23. As expected, the proposed converter outputs five-level switching currents. Moreover, the output filtered current and voltage are almost purely 50Hz sinusoidal waveforms with very low harmonics. This indicates that the proposed system can achieve a high-quality output with a lower power devices count compared to the prior-art MCSI topologies. Additionally, two inductor currents $I_{L\text{-}1}$ and $I_{L\text{-}2}$ are maintained at around 6A with almost the same current ripple, which validates that the proposed current balancing strategy also perform well.

In order to compare the efficiency performance, three additional prototypes including: a) conventional 3-level H6

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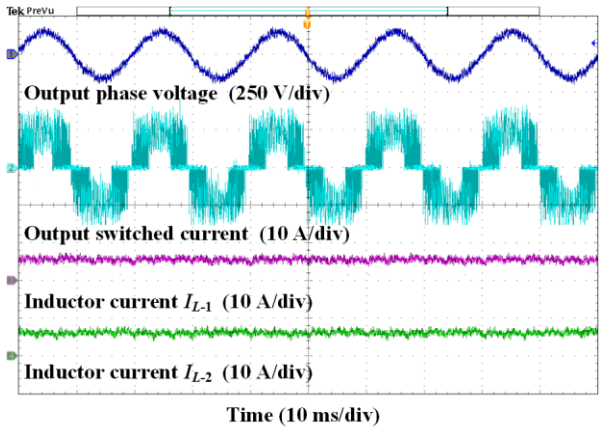

Fig. 22. Performance (experiments) of the proposed CSI topology (m_a: 0.8).

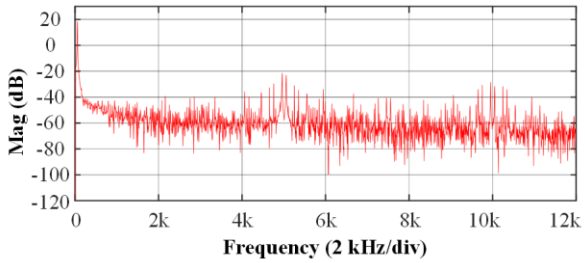

Fig. 23. FFT performance (experiments) of the proposed CSI topology (output filtered current).

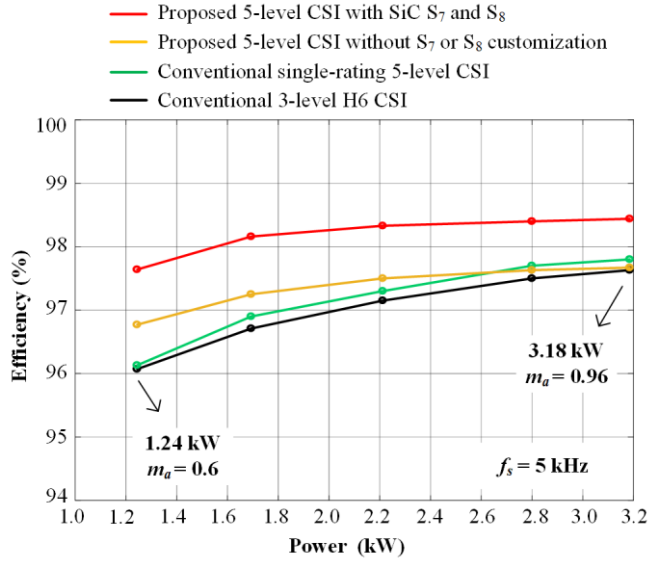

Fig. 24. Efficiency comparison of the selected converters: conventional 3-level H6 CSI, conventional single-rating inductor 5-level CSI, the proposed 5-level CSI with SiC S_7 and S_8, and the proposed 5-level CSI without customization.

CSI, b) conventional single-rating inductor 5-level CSI, and c) the proposed CSI without S_7 or S_8 customization (i.e., silicon devices), have been built up with the same experimental parameters. More specifically, except for the SiC devices of S_7 and S_8 in the proposed cost-effective CSI solution, all the power switches and the power diodes are employed with the same devices (IKW20N60T and C2D20120D). Beyond that, to make a proper comparison, these converters should be evaluated under the same conditions (operating with the same output value and the same modulation index). Subsequently, a series of efficiency data of the selected converters can be recorded and compared as shown in Fig. 24. The tested power rating is from 1.24 kW to 3.18 kW, and the modulation index m_a ranges from 0.6 to 0.96.

It can be concluded from Fig. 24 that the proposed eight-switch five-level CSI, which employs SiC MOSFETs for S_7 and S_8, achieves the highest efficiency compared to the rest. At the power of 3.18 kW and the basic switching frequency (S_1-S_6) of 5 kHz, the efficiency of the proposed CSI reaches 98.46% and is almost 1% higher than that of the conventional H6 CSI. On the other hand, when the converter is configured with silicon devices for S_7 or S_8, the efficiency drops as expected. In some cases, when the power rating is higher than 2.5 kW (m_a=0.85), the efficiency is even lower than the conventional single-rating inductor 5-level CSI, as shown in Fig. 24. Despite the absence of SiC power switches, this efficiency-cross phenomenon is affected by the corresponding modulation index m_a. With the proposed modulation scheme, the switching losses of the proposed CSI may be lower than that of the conventional 5-level CSI. However, the dwell time of large vectors (conducting with I_{dc}) will become longer with the increase of m_a, and thus leading to the increase of the conduction losses. As also shown in Fig. 24, the efficiencies of the conventional 3-level H6 CSI, conventional single-rating inductor 5-level CSI, and the proposed CSI without customized power devices for S_7 or S_8 are quite close. However, as demonstrated, only with SiC power devices of S_7 and S_8, the proposed CSI can achieve a significant efficiency improvement. In all, the above simulations and experimental tests have validated the effectiveness of the proposed eight-switch five-level CSI topology in terms of low device count and high power quality. It thus can be a promising solution for CSI applications.

V. Conclusion

This paper proposes an eight-switch three-phase five-level CSI topology. Moreover, the SVM strategy as well as its operational principle was presented in detail. In addition, the operational features and superior advantages of the proposed CSI have been discussed and benchmarked. Focusing on the unique advantages of the newly proposed topology, it performs five-level output currents, while employs with a comparable hardware cost as the three-level H6 CSI. The low output THD may help to reduce the sizes of the passive components in the system, especially the output filters. And the “small vector” can reduce the switching and conduction losses of the semiconductor switching devices in H6 CSI module, which make it possible to increase the output current rating of the system in a certain degree. The corresponding performance has been validated through simulation and experimental results.

References

[1] A. R. Beig and V. T. Ranganathan, “A novel CSI-fed induction motor drive,” *IEEE Trans. Power Electron.*, vol. 21, no. 4, pp. 1073–1082, Jul. 2006.

[2] B. Wu, J. Pontt, J. Rodriguez, S. Bernet, and S. Kouro, “Current-source converter and cycloconverter topologies for industrial medium-voltage drives,” *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2786–2797, Jul. 2008.

[3] D. Banerjee, and V. T. Ranganathan, " Load-Commutated SCR Current-Source-Inverter-Fed Induction Motor Drive With Sinusoidal Motor Voltage and Current," *IEEE Trans. Power Electron*., vol. 24, no. 4, pp. 1048-1061, Feb. 2009.

[4] B. Sahan, A. N. Vergara, N. Henze, A. Engler, and P. Zacharias, “A Single-Stage PV Module Integrated Converter Based on a Low-Power Current-Source Inverter,” *IEEE Trans. Ind. Appl.*, vol. 55, no. 7, pp. 2602-2609, Jul. 2008.

[5] M. Marchesoni and P. Tenca, "Diode-clamped multilevel converters: a practicable way to balance DC-link voltages," *IEEE Trans. Ind. Electron.*, vol.49, no.4, pp 752-765, Aug. 2002.
[6] J. Rodriguez, S. Bernet, W. Bin, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.
[7] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
[8] B. Wu, High-Power Converters and AC Drives. *New York/Piscataway*, NJ, USA: Wiley/IEEE Press, 2006.
[9] S. Daher, R. Silva, and F. Antunes, "Multilevel current source Inverter-the switching control strategy for high power application," in *Proc. IEEE 22nd Conf. IEEE Ind. Electron. Soc.*, vol. 3, pp. 1752–1757, Aug. 1996.
[10] Z. Bai and Z. Zhang, "Conformation of multilevel current source converter topologies using the duality principle," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2260–2267, Sep. 2008.
[11] H. A. C. Braga and I. Barbi, "A new technique for parallel connection of commutation cells: Analysis, design, and experimentation," *IEEE Trans. Power Electron.*, vol. 12, no. 2, pp. 387–395, Mar. 1997.
[12] K. Sangshin and H. A. Toliyat, "Multilevel current source inverter topology based on dual structure associations," in *Proc. IEEE 39th Ind. Appl. Conf.*, vol. 2, pp. 1090–1095, Oct. 2004.
[13] D. Xu and B. Wu, "Multilevel current source inverters with phase shifted trapezoidal PWM," in *Proc. IEEE 36th Power Electron. Spec. Conf.*, pp. 2540–2546, Jun. 2005.
[14] D. Xu and B. Wu, "Space Vector Modulation for High Power Five Level Current Source Inverters," in *Proc. IEEE 37th Power Electron. Spec. Conf.,* pp. 1–6, Jun. 2006.
[15] B. S. Dupczak, A. J. Perin, and M. L. Heldwein, "Space Vector Modulation Strategy Applied to Interphase Transformers-Based Five-Level Current Source Inverters," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2740–2751, Jun. 2012.
[16] F. Gao, P. C. Loh, F. Blaabjerg, and D. M. Vilathgamuwa, "Five-Level Current-Source Inverters With Buck–Boost and Inductive-Current Balancing Capabilities," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2613-2622, Aug. 2010.
[17] A. Nami, L. Jiaqi, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC Applications: Review on converter cells and functionalities," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18-36, Jan. 2015.
[18] B. P. McGrath and D. G. Holmes, "Natural current balancing of multi cell current source converters," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1239–1246, May 2008.
[19] J. Wang, J. Dai, B. Wu, D. Xu, and N. R. Zargari, "Megawatt wind energy conversion system with diode rectifier and multilevel current source inverter," in *Proc. IEEE Energy Convers. Congr. Expo.*, pp. 871–876, Sep. 2011.
[20] Z. Bai, H. Ma, D. Xu, and B. Wu, "Control Strategy With a Generalized DC Current Balancing Method for Multimodule Current-Source Converter," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 366–373, Jan. 2014.
[21] W. Wang, F. Gao, Y. Yang, and F. Blaabjerg, "Operation and modulation of H7 current source inverter with hybrid SiC and Si semiconductor switches," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 1, pp. 387–399, Mar. 2018.
[22] V. Vekhande, N. Kothari, and B. G. Fernandes, "Switching State Vector Selection Strategies for Paralleled Multilevel Current-Fed Inverter Under Unequal DC-Link Currents Condition", *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1998-2009, 2015.
[23] X. Zhang, T. Wang, X. Wang, G. Wang, Z. Chen, and Dianguo Xu, "A Coordinate Control Strategy for Circulating Current Suppression in Multiparalleled Three-Phase Inverters", *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 838-847, 2017.
[24] L. Jun, K. W. E. Cheng, D. Sutanto, and D. H. Xu, "A multimodule hybrid converter for high-temperature superconducting magnetic energy storage systems (HT-SMES)," *IEEE Trans. Power Del.*, vol. 20, no. 1, pp. 475–480, Jan. 2005.
[25] Z. Wang, K. T. Chau, B. Yuwen, Z. Zhang, and F. Li, "Power compensation and power quality improvement based on multiple-channel current source converter fed HT SMES," *IEEE Trans. Appl. Supercond.*, vol. 22, no. 3, pp. 5701204-1–5701204-4, Jun. 2012.
[26] N. Binesh and B. Wu, "5-level parallel current source inverter for high power application with DC current balance control," in *Proc. IEEE Int. Electric Mach. Drives Conf. (IEMDC)*, pp. 504–509, 2011.

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