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Full Discrete Modeling, Controller Design and Sensitivity Analysis for High Performance Grid-Forming Converters in Islanded Microgrids

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Abstract **– Recent works have shown that state-feedback decoupling of capacitor voltage allows for drastic bandwidth enlarging of current controllers for grid-former converters in islanded microgrids. Furthermore, Smith predictor and lead compensation have been also proved as very effective implementations for compensating the controller delays. These features are key to fulfil demanding requirements in terms of voltage regulation in islanded applications. This work deepens in the discrete-time domain modelling and implementation issues of the abovementioned techniques. A full discrete-time and sensitivity analyses reveal phenomena not properly modelled in previous works, which limits the performance: the presence of high-frequency oscillations due to discrete poles with negative real part. Subsequently, proper design countermeasures (i.e., limit bandwidth) are proposed. Discrete implementation of the voltage controller is also addressed, and design guidelines are provided. Experimental tests in accordance with the high demanding standards for UPS systems verify the theoretical analysis.**

Keywords **– Control system analysis, current control, microgrids, power quality, voltage control.**

I. INTRODUCTION

The design of voltage and current regulators for Voltage Source Inverters (VSI) should aim to achieve good performance during steady-state and transient conditions, which, in practice, means to work with both wide bandwidth and stability margins. Poor dynamics of these regulators are responsible for degraded performance of the overall control system. Thus, effective control of voltage and current is mandatory to succeed in implementing the desired feature of each application. According to [1], it is desirable from any current or voltage regulator the following: i) to achieve zero steady-state error; ii) accurately track the commanded reference during transients and reject any disturbance; iii) have a bandwidth as wider as possible; iv) compensate for low order harmonics.

One of the most widely structure used in the output of VSI is the LC filter. To improve the dynamic properties of the system (increased bandwidth and damping factor) multiloop or cascaded loops are used to control the system [2]. The idea is to use an inner current regulator with fast dynamics to compensate for input and harmonic load disturbances. Its reference input comes from the outer voltage loop which is responsible for controlling the output voltage, and has lower dynamics as compared to the inner loop. The inductor current (i_L) [3] or capacitor current (i_C) [4] are the feedback variables used for the inner current loop. By using i_C improves the disturbance rejection properties of the system. The main reason is that the load current (i_o) has a direct influence on this variable. However, by using i_C inherently does not provide overcurrent information. If i_L is used overcurrent protection is easily implemented. Therefore, there is a trade-off between both strategies. Another way to improve disturbance rejection is to use disturbance input decoupling also referred as load current feedforward strategy [5].

Independently of the controller structure, the effect of delays and voltage coupling of the capacitor voltage and inductor current (output LC filters) should be carefully considered in the design stage [6], [7], [8]. Furthermore, no matter the variable used as feedback the control structure disturbance rejection properties will be directed affected by the controller bandwidth.

Even though substantial research has been done in systems with a strong electromotive force, e.g. grid connected and drives applications [9], the isolated microgrid structure had not been discussed in depth, until some recent publications [7], [8], [10]. Overall, those works show that a state decoupling between the capacitor voltage and inductor current in VSI with LC output filter drastically improves the dynamics of the inner regulators, and hence, also permit an enlarging of outer loops. However, those analyses were done on the continuous time domain, which do not accurately describe the dynamics when the inner current bandwidth is well beyond one tenth of the sampling frequency. The reason is the fact that the approximation used for the delay becomes inaccurate in the high frequency range and this has substantial impact on the analysis of the control loops.

The aim of this paper is to extend previous works to fully describe the physical modelling and controller development in the z-domain. The goal is to provide new insights of the real behavior of very high bandwidth inner controllers and provide new design guidelines to address phenomena only identified in the discrete domain. Two structures based on a lead compensator structure and Smith predictor are considered as they are proved to be effective to enlarge the bandwidth of the inner current control. Subsequently, a sensitivity analysis is also performed to reveal the advantages and disadvantages of each technique. Considering a very high bandwidth inner current controller, a PR structure is considered for the voltage loop. A Nyquist

based design is provided and considers the previous current controller design. Discretization and implementation issues of the voltage loop anti-wind up scheme are detailed. The anti-wind up structure based on a feedback path is considered [6]. This technique allows the states to be driven by bounded signals in any condition, i.e. also during demanding transients, which represents a major advantage compared to conventional anti-wind up implementations, e.g. the frozen or back-calculation schemes, as shown in [6, 11, 12]. However, a strictly proper implementation in the discrete domain of the PR controller should be derived. Otherwise, the feedback path introduces an algebraic loop and the structure would not be feasible [13]. The derivation of the PR with feedback based anti-wind up is provided. Finally, the solutions proposed are verified experimentally according to the requirements imposed by IEC 62040 standard to Uninterruptible Power Supply (UPS) systems.

Even though the techniques presented in this paper to enlarge the bandwidth of the inner current loop are applied to isolated microgrids, the same concepts can be applied to grid-connected microgrids [14], [15]. In these applications, it is important that the current controller loop has enough bandwidth to provide the required current harmonic to the loads without attempting the voltage quality.

II. SYSTEM DESCRIPTION AND MOTIVATION

In isolated microgrids the VSI is implemented with an LC filter at its output. In general, it operates in voltage control mode with the capacitor voltage and inductor currents being the controlled states. Inner current regulation is also a desired feature to provide dynamic peak limitation, especially in UPS applications [16]. In Fig. 1 the block diagram including a three-phase inverter with its regulators is presented. The aim of the inner current loop is to track the commands from the outer voltage loop and to ensure fast dynamic disturbance rejection within its bandwidth [17].

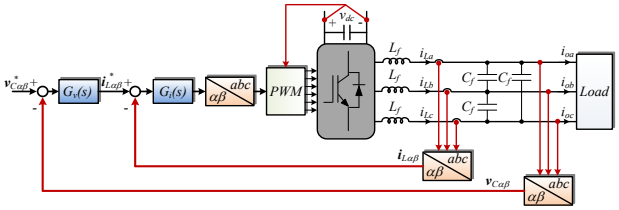


Fig. 1 Block diagram of a three phase VSI with voltage and current loop

The simplified block diagram of the closed-loop system is shown in Fig. 2, where $V^*_{c\alpha\beta}$ and $I^*_{L\alpha\beta}$ are the reference voltage and current vectors and $I_{o\alpha\beta}$ is the output current vector, which acts, in general, as a disturbance to the system. In case the load could be modelled by a generic impedance, $I_{o\alpha\beta}$ would be directly related to the capacitor voltage [17]. L_f and C_f are the filter inductor and capacitor, respectively. R_f is the equivalent series resistance of the inductor. $G_i(z)$ and $G_v(z)$ represent the current and voltage regulators transfer functions (TF) in the discrete-time domain. There is one sample computation delay due to the implemented regular sampled symmetrical PWM strategy [18]. $G_{dec}(z)$ is the TF related to the decoupling of the cross-coupling states, designed to compensate for the system delay within the current controller bandwidth, as proposed in [7]. The discrete time model of the plant was developed in [8]. By using this model, the block diagram in the discrete time domain is shown in Fig. 3. The transfer functions of the plant model in discrete time domain are given by (1) and (2), with T_s being the controller sampling rate.

$$G_{iv}(z) = \frac{C_f \frac{\omega_n^2}{\omega_d} e^{-\xi\omega_n T_s} sin(\omega_d T_s) z^{-1}}{1 + \frac{\omega_n}{\omega_d} e^{-\xi\omega_n T} \sin(\omega_d T_s - \phi)\, z^{-1}} \quad (1)$$

$$\omega_n^2 = \frac{1}{L_f C_f}; \quad \xi = \frac{1}{2\omega_n}\frac{R_f}{L_f} = \frac{R_f}{2}\sqrt{\frac{C_f}{L_f}}$$

$$G_c(z) = \frac{V_{C\alpha\beta}(z)}{I_{C\alpha\beta}(z)} = \frac{a_1 + a_2 z^{-1}}{b_1(1 - z^{-1})} \quad (2)$$

$$a_1 = 1 - \frac{\xi\omega_n}{\omega_d} e^{-\xi\omega_n T} sin(\omega_d T_s) - e^{-\xi\omega_n T} cos(\omega_d T_s)$$

$$a_2 = \frac{\xi\omega_n}{\omega_d} e^{-\xi\omega_n T_s} sin(\omega_d T_s) - e^{-\xi\omega_n T_s} cos(\omega_d T_s) + e^{-2\xi\omega_n T_s}$$

$$b_1 = C_f \frac{\omega_n^2}{\omega_d} e^{-\xi\omega_n T_s} sin(\omega_d T_s)$$

Even though this plant derivation has been detailed in [8], and a partial study was performed in [10], the controller analysis in the discrete-time domain is not fully described. This work reveals that a full discrete design and analysis show that a dominant oscillating pole could be identified in the following conditions:

- The proportional gain is very large.
- There is a mismatch between the estimated plant parameters and the real ones. This mismatch is more important in the case of Smith predictor.

Furthermore, the system can become unstable for very high gains or mismatches among the real and estimated plant parameters. These results cannot be identified in the continuous-time domain analysis. Specifically, if the predicted delay used in the Smith predictor is bigger than twice the real one, the system becomes unstable.

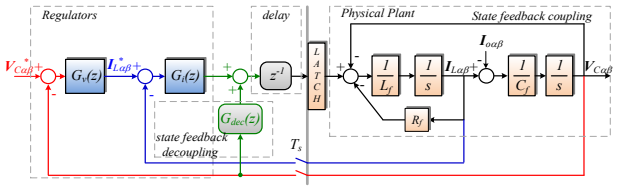


Fig. 2. Simplified block diagram of the closed-loop system

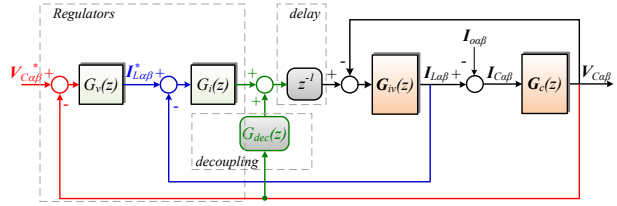


Fig. 3. Block diagram of the closed-loop system shown in discrete time domain

III. CURRENT REGULATOR DESIGN

The main design objective for the current regulator is to achieve a large bandwidth (f_{bw}), in order to avoid interaction among cascaded loops, resulting in a reliable overall controller [19]. One fundamental difference between the design in continuous time domain and in the discrete time domain is that in the former, in general, it is necessary to make an approximation of the delay introduced by the computation and PWM. A first order Padé approximation is normally used. Depending on this approximation the resulted analysis can lead to wrong conclusions, since rational approximations of the delay are only accurate up to 0.2 times the sampling frequency i.e., the approximation is valid only in a limited frequency range. On the other hand, in discrete time domain the computation and PWM transfer functions are accurate up to the Nyquist frequency.

The system and current control parameters used both in the simulation and in laboratory tests are presented in Table I. A simple P controller is considered as regulator for the current loop, i.e. $G_i(z) = k_{pI}$. The main idea behind this decision is to simplify the implementation and achieve a high-bandwidth tuning of the inner loop. This design strategy is reasonable, since the main application objectives are expressed in terms of the outer loop variable: the capacitor voltage should be controlled in closed-loop with steady-state zero error for the fundamental and low order harmonics (see Section IV). With reference to Fig. 3, the transfer function (TF) of the inner current loop is (3). If the controlled states are not decoupled, i.e. $G_{dec}(z) = 0$, (3) becomes (4). The dynamic performance of the system is made by neglecting $I_{o\alpha\beta}(z)$ in (4), i.e., by the analysis of the inner loop tracking performance.

TABLE I
System Parameters

Parameter	Value
Switching frequency	$\boldsymbol{f_s = 10\ kHz\ (T_s = 100\ \mu s)}$
Filter inductance	$L_f = 1.8\ mH$
Filter capacitor	$C_f = 27\ \mu F$
Inductor ESR	$R = 0.1\ \Omega$
Linear load	$R_l = 68\ \Omega$
Non linear load	$C_{NL} = 235\ \mu F$ $R_{NL} = 184\ \Omega$ $L_{NL} = 0.084\ mH$

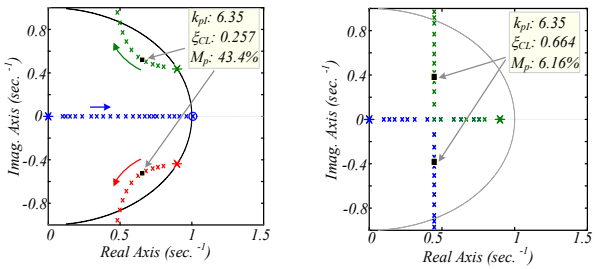
By looking just at the command tracking features, the root locus for the inner current loop without voltage decoupling is shown in FIG. 4(a). The system has low damping and hence high overshoot. This is true whatever gain is selected. The highest damping that can be achieved is $\xi_{CL} = 0.257$ for $k_{pI} = 6.35$. And the system become unstable for $k_{pI} > 14.7$.

$$I_{L\alpha\beta}(z) = \frac{G_{iv}(z)G_i(z)z^{-1}}{1 + G_{iv}(z)G_i(z)z^{-1} - G_{iv}(z)[G_{dec}(z)z^{-1} - 1]G_c(z)} I^*_{L\alpha\beta}(z) - \frac{G_{iv}(z)[G_{dec}(z)z^{-1} - 1]G_c(z)}{1 + G_{iv}(z)G_i(z)z^{-1} - G_{iv}(z)[G_{dec}(z)z^{-1} - 1]G_c(z)} I_{o\alpha\beta}(z) \quad (3)$$

$$I_{L\alpha\beta}(z) = \frac{G_{iv}(z)G_i(z)z^{-1}}{1 + G_{iv}(z)G_i(z)z^{-1} + G_{iv}(z)G_c(z)} I^*_{L\alpha\beta}(z) + \frac{G_{iv}(z)G_c(z)}{1 + G_{iv}(z)G_i(z)z^{-1} + G_{iv}(z)G_c(z)} I_{o\alpha\beta}(z) \quad (4)$$

To analyze the effect of decoupling the controlled states, voltage decoupling is considered. This corresponds to design $G_{dec}(z)$ in Fig. 3 as a Lead-Lag filter to compensate for one sample delay ($100\ \mu s$) at the fundamental frequency (50 Hz) [7]. The resulting TF is shown in (5). This TF is valid if the output voltage has almost no low order harmonics within its bandwidth. This is true only if the voltage regulator design is capable to eliminate the harmonics at this voltage. As will be shown later, with enough voltage regulator bandwidth this assumption is reasonable. Therefore, it is possible to conclude that the output voltage does not affect anymore the inner current loop. This result in an easier design of the controller, with better dynamics, and with a dynamic behavior that is not load sensitive. As shown in the root locus of FIG. 4(b), for the same bandwidth as in FIG. 4(a) the system achieves higher damping (less overshoot).

Even though the inner control loop achieves higher damping when the decoupling is done the maximum achievable bandwidth is limited due to the delay introduced by the discrete time implementation. For example, for a bandwidth of $\boldsymbol{2570\ Hz\ (k_{pI} = 14)}$ the damping achieved is $\boldsymbol{\xi_{CL} = 0.1}$.



(a) (b)

Fig. 4. Root locus for the inner current loop with P regulator: (a) without voltage decoupling and including the system delay - $k_{pI} = 6.35$; (b) with ideal voltage decoupling and including the system delay - $k_{pI} = 6.35$: * – open loop poles; ■ closed-loop poles; o – zeros

$$\frac{I_{L\alpha\beta}(s)}{I^*_{L\alpha\beta}(s)} = \frac{G_i(z)G_{iv}(z)z^{-1}}{1 + G_i(z)G_{iv}(z)z^{-1}} \quad (5)$$

It is possible to widen the system bandwidth and still achieve a reasonable damped closed-loop system by compensating the system delays. This can be achieved by means of 1) lead compensator and 2) Smith Predictor. In principle, these strategies can be extended to other controllers.

a. *Lead Compensator*

By considering perfect decoupling (the state feedback decoupling path in Fig. 2 exactly cancels out the physical state feedback coupling) the structure of lead compensator, also referred to as 'Delay prediction and Feedback' [2], is shown in Fig. 5. With this structure it is possible to widen the inner loop bandwidth without decreasing the damping factor. The tuning solution obtained in the discrete-time

domain provide the natural frequency ($\boldsymbol{\omega_n}$) and damping factor ($\boldsymbol{\xi}$) The cut-off/bandwidth frequency ($\boldsymbol{\omega_{b\omega}}$) and phase-margin (PM) can be obtained as follow [20]:

$$\omega_{b\omega} = \omega_n\sqrt{-2\xi^2 + \sqrt{1+4\xi^4}}. \tag{6}$$

$$PM = \text{atan}\frac{2\xi}{\sqrt{-2\xi^2 + \sqrt{1+4\xi^4}}}. \tag{7}$$

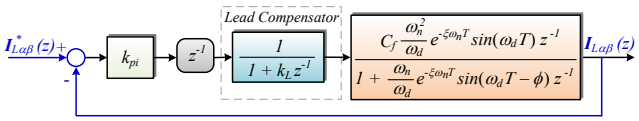


Fig. 5. Current loop model including the lag introduced by PWM update, and the model of the lead compensator $\boldsymbol{G_L(z) = 1/(1+k_L z^{-1})}$

The closed-loop TF becomes

$$\frac{I_{L\alpha\beta}(z)}{I^*_{L\alpha\beta}(z)} = \frac{k_{pI}b}{(z+k_L)(z-a)+k_{pI}b}. \tag{8}$$

Where $b = C_f\frac{\omega_n^2}{\omega_d}e^{-\xi\omega_n T}\,sin(\omega_d T)$;$a = \frac{\omega_n}{\omega_d}e^{-\xi\omega_n T}sin(\omega_d T - \phi)$.

The poles of this TF must satisfy the following relationship

$$z^2 - (p_1+p_2)z + p_1p_2 = z^2 + (k_L - a)z - k_L a + k_{pI}b \tag{9}$$

where p_1, p_2 are the desired pole locations, defined as:

$$p_{1,2} = e^{-\xi\omega_n T_s}[\cos(\omega_d T_s) \pm jsin(\omega_d T_s)],\ \omega_d = \omega_n\sqrt{1-\xi^2}$$

Solving the system leads to:

$$\begin{cases} k_L = a - (p_1+p_2) \\ k_{pI} = (p_1p_2 + k_L a)/b. \end{cases} \tag{10}$$

For the case $\omega_n = 2\pi 2400$ rad/s and $\xi_{CL} = 0.707$, the poles are located at $p_{1,2} = 0.166 \pm j0.26$ and bandwidth of the system is $f_{b\omega} = 3.1$ kHz. The resulting root locus with the lead compensator gains $k_L = 0.5609$ and $k_{pI} = 11.58$ are shown in Fig. 6a. The poles are more on the left compared to the previous case, which means the system is faster.

The system is even faster when the controller is designed for a wider bandwidth, e.g., $\boldsymbol{\omega_n = 2\pi 3000\ rad/s}$ and $\boldsymbol{\xi_{CL} = 0.707}$. The resulting root locus with the lead compensator, and the closed loop poles for $\boldsymbol{k_L = 0.5609}$ and $\boldsymbol{k_{pI} = 14.15}$ are shown in Fig. 6b. It can be noticed that the theoretical one-to-tenth rule can be overcome in this specific application [11].

The proposed technique provides a wider bandwidth for the same damping factor. For a bandwidth of 3 kHz the system with the lead compensator is much more damped ($\boldsymbol{\xi_{CL} = 0.707}$) than the one without the lead compensator ($\boldsymbol{\xi_{CL} = 0.12}$). Note that with the lead compensator the system becomes 2nd order and the maximum achievable bandwidth occurs when the two closed-loop poles are located at the origin. Thus, the fastest system response is limited in two sampling times.

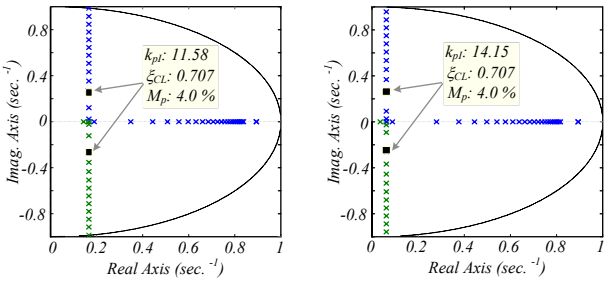


Fig. 6. Root locus of an RL load including the lag introduced by PWM update, with the lead compensator: (a) $\boldsymbol{k_L = 0.5609;\ k_{pI} = 11.58}$; (b) $\boldsymbol{k_L = 0.7694;\ k_{pI} = 14.15}$

The sensitivity to changes in the physical plant parameters, i.e. the filter inductor L_f and its equivalent series resistance R, is investigated (see Table I for the nominal values). The system is less sensitive to variations in R (see Fig. 7a) than to changes in L_f. The eigenvalue migration as the inductance value changes is shown in Fig. 7b. It can be noticed that for inductance values less than 0.9 mH (50% of the rated value - $L_{f,rated}$) the system becomes unstable.

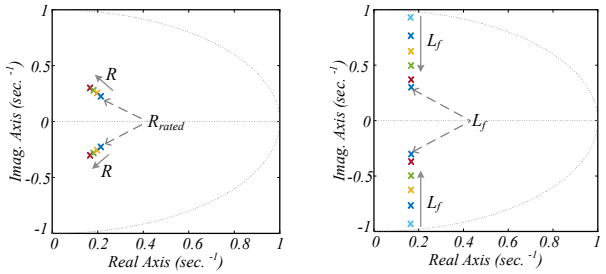


Fig. 7. Eigenvalue migration as a function of variation in: (a) $R = R_{rated} = 0.1\,\Omega \rightarrow R = 2\,\Omega$; (b) $L_f = 0.9\,mH \rightarrow L_{f,rated} = 1.8\,mH$

b. Smith Predictor

The structure of a Smith Predictor is shown in Fig. 8. The basic idea is to build a parallel model which cancels the system delay (modelled by the z^{-1} term in series with the plant). In this way, the design of the controller can be performed using the un-delayed model of the plant.

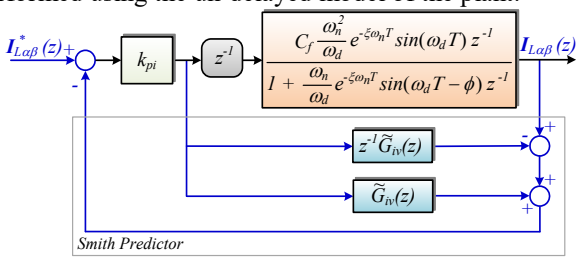


Fig. 8. Block diagram for design the inner current loop, including the lag introduced by computational delay, and the model of the Smith Predictor.

The closed-loop FT of the block diagram of Fig. 8 is shown in (11),

$$\frac{\tilde{I}_{L\alpha\beta}(z)}{I^*_{L\alpha\beta}(z)} = \frac{k_{pI}G_{iv}(z)z^{-1} + k_{pI}\tilde{G}_{iv}(z) - k_{pI}\tilde{G}_{iv}(z)z^{-1}}{1 + k_{pI}G_{iv}(z)z^{-1} + k_{pI}\tilde{G}_{iv}(z) - k_{pI}\tilde{G}_{iv}(z)z^{-1}} \tag{11}$$

If $\tilde{G}_{iv}(z) = G_{iv}(z)$, (11) simplifies to

$$\frac{I_{L\alpha\beta}(z)}{I^{*}_{L\alpha\beta}(z)} = \frac{k_{pI}G_{iv}(z)}{1 + k_{pI}G_{iv}(z)}. \qquad (12)$$

Thus, the resulting TF of the system is first-order. The respective root locus is shown in Fig. 9. For a system with $\omega_n = 2\pi 2400\ rad/s$ the corresponding bandwidth of closed-loop system is $f_{b\omega} = 3.1kHz$, the same obtained with the lead compensator. It is also observed that the gain of the controller $k_{pI} = 14$.

Unlike the lead compensator method, the resulting system model with Smith Predictor becomes 1st order when the estimated delay and system parameters are equal to the real ones (see root locus in Fig. 9). Therefore, the fastest response is limited to only one sampling time (deadbeat) and is thus faster than with the lead compensator.

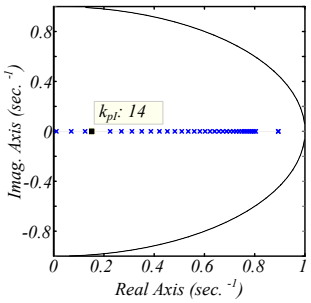
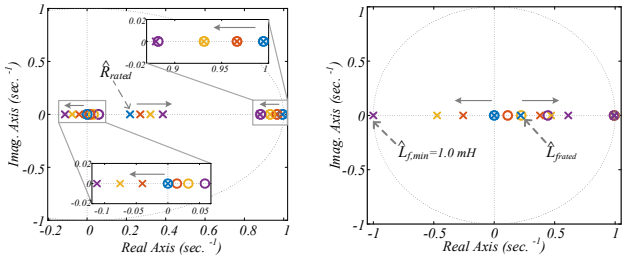


Fig. 9. Root locus of the system in Fig 11 including the lag introduced by PWM update, with the Smith Predictor – correct estimate of the delay and parameters.

However, robustness issues must be considered with this method. If there is any model error, especially in the delay itself, the Smith predictor can degrade the system performance. These aspects are verified through sensitivity to changes in the values of the equivalent series resistance (R_{SP}), and in the inductance (L_{SP}) used in the Smith predictor. These analyses are presented in Fig. 10. For both cases, two poles, one at the origin and the other at the right half-plane of the z plane, are canceled by zeros, and the resulting system is a the first-order with a dominant pole in the real axis. This happens when the Smith Predictor's estimated parameters are the same as the plant model ($R_{SP} = R$, and $L_{SP} = L_f$). However, when there is an error in the estimated parameters the system becomes of third order.

For both R_{SP} and L_{SP} variations with respect to the rated values, the pole and zero in the unit circle move slightly to the left and because they remain very close to each other they do not influence the dynamics of the system. For variations of R_{SP}, the displacement of the pole and zero at the origin is also very small. Thus, the dominant pole, which moves to the right, continues to determine the dynamics of the system, slowing it down as R_{SP} increases. It can be stated that the system is robust against variations in R. In contrast, the pole and zero at the origin undergo large displacement for small variations of L_f, as can be seen in Fig. 10b. For inductance values below 1 mH the system becomes unstable, however even for small decreases of L_{SP} with respect to L_f the pole at the origin moves to the left half plane. So, oscillation with half of switching frequency is expected. On the contrary, if $L_{SP} > L_f$ the pole at the origin moves to the right and the system slows down in comparison to the case where the parameters used in the Smith predictor are equal to the real ones.



(a) (b)

Fig. 10. Eigenvalue migration as a function of variation in: (a) $R = R_{rated} = 0.1\ \Omega \rightarrow R = 2\ \Omega$; (b) $L_f = L_{frated} = 1{,}8mH \rightarrow L_f = 1{,}0\ mH$ - Smith Predictor for a designed bandwidth of $f_{b\omega} = 3.1\ kHz$.

Fig. 11 shows the step response for two different inductance values and for the same designed bandwidth. Note that the lower the estimated inductance value, L_{SP}, with respect to the inductance of the plant model, L_f, the greater will be the oscillation. As predicted, the oscilation frequency is half of the switching frequency. Therefore, the system is more sensitive to variations in the inductance L_f than to variations in R.

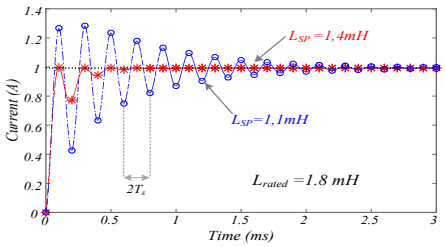


Fig. 11. Step response for two values of inductance - Smith Predictor for a designed bandwidth of $f_{b\omega} = 3.1\ kHz$.

Fig. 12 shows the closed loop zeros and poles migration for different values of the delay used in the Smith predictor ($T_{d,SP}$). When $T_{d,SP} = T_s$, the resulted system is first order (red x in the real axis). It is observed that as $T_{d,SP}$ is different from the system delay, the system order increases, and the closed-loop poles become complex, resulting in an oscillatory response during transients. For $T_{d,SP} = 0.5T_s$ there are 4 poles: one at the origin, one at the unit circle, and 2 complex conjugate pair. The poles at the origin and at the unit circle cancel out with 2 zeros. The resulting complex conjugate pair dominates the response. For $T_{d,SP} > T_s$ the system becomes 5th order: one pole at the origin, one at the unit circle, 2 complex conjugate pair, and one in the real axis. The complex conjugate poles are in the left half z plane. Therefore, oscillation with half of the switching frequency is expected. The poles at the origin and at the unit circle cancel out with 2 zeros. The remaining dominant pole is more to the right, resulting in a slower response. Even though it is not shown in Fig. 12, when $T_{d,SP} > 2T_s$ the system becomes unstable.

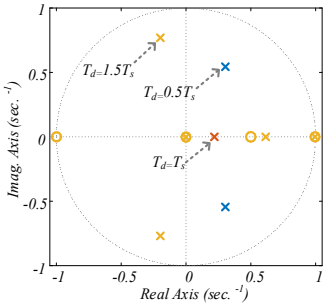


Fig. 12. Eigenvalue migration for the predicted computation delay $T_{d,SP} = 0.5T_S$, T_s, and $1.5T_s$.

IV. VOLTAGE CONTROLLER DESIGN

The voltage controller aims to provide zero steady-state error for the load voltage reference with an acceptable transient response (e.g., reference and load changes). A PR voltage controller with lead compensation is proposed

$$G_v(s) = k_{pV} + \sum_{h=1,5,7} k_{iV,h} \frac{s\cos(\varphi_h) - h\omega_1 \sin(\varphi_h)}{s^2 + (h\omega_1)^2}. \quad (13)$$

which after discretization becomes (using zero-order-hold)

$$G_v(z) = k_{pV} + \sum_{h=1,5,7} k_{iV,h} \frac{[\sin(\varphi_h + h\omega_1 T_s) - \sin(\varphi_h)]z^{-1} + [\sin(\varphi_h - h\omega_1 T_s) - \sin(\varphi_h)]z^{-2}}{h\omega_1[1 - 2z^{-1}\cos(h\omega_1 T_s) + z^{-2}]}$$

The proportional gain k_{pV} determines the bandwidth of the voltage regulator, and is designed for a bandwidth around 300 Hz. It is possible to achieve such a wide bandwidth because the inner current loop bandwidth can be increased by means of the lead compensator structure. Although there is no practical interaction between the loops due to wide separation in bandwidth, the tuning of the voltage loop did not consider the inner current loop as an ideal one.

Subsequently, the fundamental resonant gain is selected having into account the design rule (in S-domain)

$$k_{iV,1} \geq 2k_{pV}\omega_1 \quad (14)$$

The idea is to move the main zeros of the PR controller as far as possible from the right half plane by identifying the critically damped solution for them.

Significantly lower gain is provided to the harmonic gains. Then, the phase-leading angles at each harmonic frequency φ_h are set such that the trajectories of the open loop system on the Nyquist diagram, with the PR regulators tuned at the fundamental frequency, 5th and 7th harmonics, guarantee a sensitivity peak η higher than a threshold value [21]. In this work the threshold has been set to $\eta = 0.6$ at no-load conditions. After calculating the phase-leading angles, the resonant gain at the fundamental frequency $k_{iV,1}$ can be slightly readjusted to have a fast response to changes in the fundamental component.

In Fig. 13 the Nyquist diagram of the system in Fig. 2 with the parameters of Table II is shown. The sensitivity peak is almost equal to 0.8 at no-load condition with all the harmonic resonators activated. Considering the closest to the -1 point unit circle intersection, a cut-off frequency of 300 Hz with phase-margin 47 deg. also provides a reasonable estimation of the system relative stability. The natural frequency provides a good estimation of the system bandwidth [21]. There is not relevant difference between the Nyquist trajectories obtained in S-domain and Z-domain.

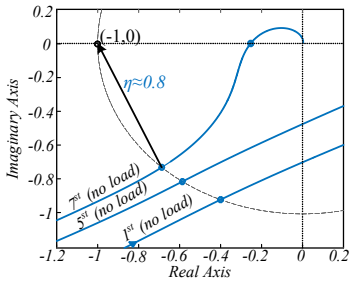


Fig. 13. Nyquist diagram of the system at no-load condition (command tracking of the reference voltage)

The harmonic resonant gains are selected to fulfill the requirements set by the IEC 62040 standard for UPS systems, without compromising stability.

TABLE II
VOLTAGE REGULATOR PARAMETERS

Parameter	Value
Proportional gain	$k_{pV,1} = 0.085$
Integral gain @50Hz	$k_{iV} = 53.5$
Integral gain @250Hz	$k_{iVh5} = 15$
Integral gain @350Hz	$k_{iVh7} = 15$

V. ANTI-WIND UP IMPLEMENTATION

As the voltage regulator bandwidth is relatively high in the proposed design, this implies that it is probably going to work in saturation. Therefore, an anti-wind up scheme for the main resonant controller (i.e., the one at fundamental component) has been implemented. It should be noted that no anti-wind up scheme is needed for the current loop since there is no state that potentially winds up. Several different implementations of anti-windup exist in literature. The classical one for a PI controller is shown in Fig. 14a [11, 12]. Similar approach was implemented in [22] for PR controllers, with a modified version implemented in [23] as shown in Fig. 14b.

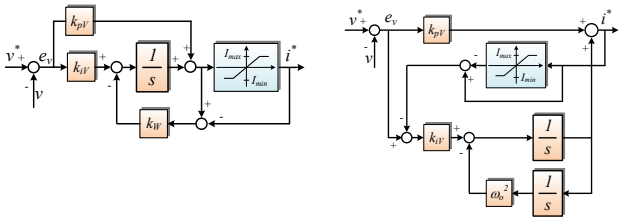


Fig. 14. Classical anti-windup technique: (a) for PI controllers; (b) for PR controllers

Though these strategies prevent windup, their implementations are highly dependent on the choice of the gain k_w. The bigger this gain is, the bigger its influence will be on the anti-windup strategy. However, if k_w is set too high the controllers can become unstable once its output saturates. Therefore, its tuning methodology is, in general, implemented by "rules of thumb".

A more feasible approach to implement anti-wind up strategy is shown in Fig. 15 [21], with similar concepts presented in [24]. The basis of this strategy is that the states of the controller (feedback block in Fig. 15) are driven by the actual (i.e. constrained) plant input rather than the

unconstrained controller error. As a result, the tuning of this anti-wind up strategy is much easier, and is simply the definition of the saturation limits. In this application, this limit is just the maximum allowed current by the inverter.

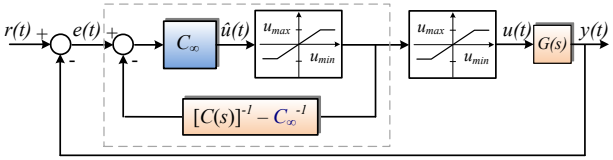


Fig. 15. Plant inversion based anti-wind up scheme [21].

According to [21], the controller $C(s)$ should be: i) biproper, i.e. zero relative degree between the TF numerator and denominator; and ii) minimum phase. If this is the case, the controller can be split into a direct feedthrough term (C_∞) and a strictly proper transfer function $\bar{C}(s)$.

$$C(s) = C_\infty + \bar{C}(s). \tag{15}$$

For the case of an ideal PR controller

$$C_\infty = k_{pV}; \qquad \bar{C}(s) = k_{iV}\frac{\cos(\varphi_1)\, s - \omega_1 \sin(\varphi_1)}{s^2 + \omega_o^2} \tag{16}$$

In normal operation ($u_{min} < \hat{u}(t) < u_{max}$), the closed-loop TF (within the dotted line in Fig. 15) is equal to $C(s)$. During saturation, the input to the controller states is bounded. Assuming the controller in Fig. 15 is implemented in continuous time domain, $\bar{C}(s)$ is strictly proper and the feedback implementation $\{[C(s)]^{-1} - C_\infty^{-1}\}$ is realizable. However, as the anti-wind up scheme is implemented in the discrete-time domain, interesting issues arise. In general, the discrete-time implementation of the feedback path in normal operation (without the saturation block) takes the form in Fig. 16. If $b_0 \neq 0$, $\bar{C}(z)$ is biproper and implementation of the feedback path in Fig. 16 is not realizable (a physical algebraic loop arises). This can be directly related to the discretization method used for $\bar{C}(s)$.

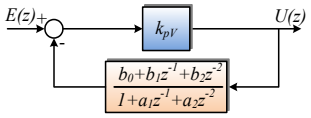


Fig. 16. Anti-wind up implementation in the discrete-time domain during normal operation

A possibility to avoid the algebraic loop can be to use as discretization methods Zero-Order Hold (ZOH), Forward Euler (FE) or Zero-Pole Matching (ZPM), which guarantee $b_0 = 0$. However, the performance of the voltage controller is degraded if FE is used as discretization method [25] (zero steady-state error is not achieved). This can be seen in Fig. 17, where the frequency response of $\bar{C}(z)$ is shown for these three discretization methods. The gain at the resonant frequency is no more infinite if FE is used as discretization method. Therefore, Zero-Order Hold was used for practical implementation because it produces a strictly proper $\bar{C}(z)$ without degrade its performance.

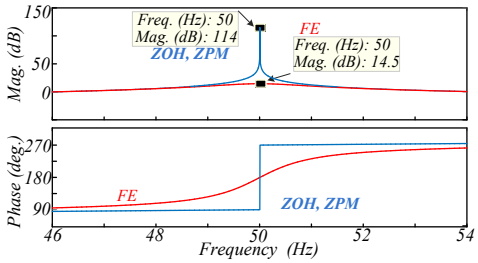


Fig. 17. Frequency response of the resonant controller using ZOH, ZPM and FE

By using ZOH, the gains of the voltage controller are calculated by (17). By observing that most of the output voltage is related to the fundamental frequency it is not necessary to use anti-windup for the harmonic controllers.

$$\begin{aligned}
b_1 &= -\frac{k_{i,1}\left[\sin(\varphi_h + h\omega_1 T_s) - \sin(\varphi_h)\right]}{k_p^2 h\omega_1} \\
b_2 &= -\frac{k_{i,1}\left[\sin(\varphi_h - h\omega_1 T_s) - \sin(\varphi_h)\right]}{k_p^2 h\omega_1} \\
a_1 &= -2\cos(\omega_1 T_s) + \frac{k_{i,1}\left[\sin(\varphi_h + h\omega_1 T_s) - \sin(\varphi_h)\right]}{k_p h\omega_1} \\
a_2 &= 1 + \frac{k_{i,1}\left[\sin(\varphi_h - h\omega_1 T_s) - \sin(\varphi_h)\right]}{k_p h\omega_1}
\end{aligned} \tag{17}$$

VI.EXPERIMENTAL RESULTS

The power system of Fig. 1 was tested to check the theoretical analysis presented. For this purpose, a low scale test-bed has been built using a Danfoss 2.2 kW converter, driven by a dSpace DS1006 platform. The LC filter parameters and operational information are presented in Table I. In all the tests voltage decoupling is performed as shown in Fig. 2.

A. Current regulator tests

To compare the proportional controller with/without lead compensator schemes in terms of dynamic response, a step change of the inductor current is performed. To achieve approximately zero steady-state error with different control structures, the reference is multiplied by a constant ($I_{refgain}$), which is equivalent to multiply by a gain the closed-loop TF of the inductor current. It should be noted that the dynamics of the system with the current loop only, i.e. voltage loop disabled, and current reference generated manually, is not affected by this gain, which is also significantly lower as the bandwidth is widened. For the system with the proportional gain only (see Fig. 5 without the lead compensator), the step response is degraded as k_{pI} is increased (see Fig. 18). This result also shows that due to additional losses the system setup has more damping than expected. In Fig. 19 the step response is even less damped and more oscillatory for $k_{pI} = 16.82$. From these results it is clear that the effect of system delays limits the achievable bandwidth.

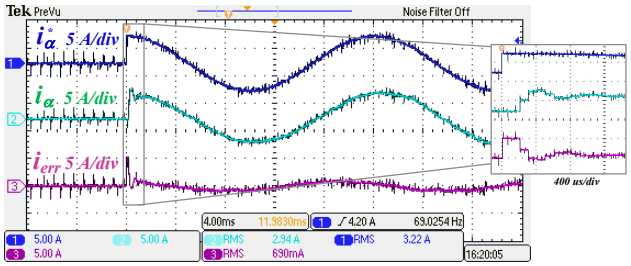


Fig. 18. Step response – P controller: $\boldsymbol{k_{pI} = 11.56}$, reference (5 A/div), real (5 A/div) and inductor current error (5 A/div) (α-axis), time scale (4 ms/div)

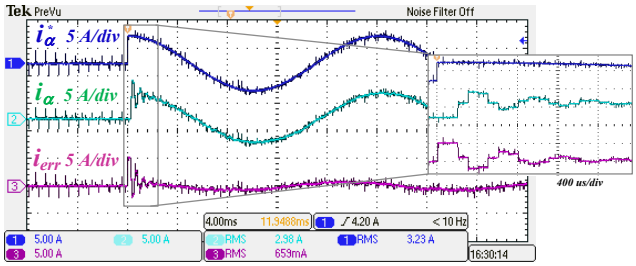


Fig. 19. Step response – P controller: $\boldsymbol{k_{pI} = 16.82}$, reference (5 A/div), real (5 A/div) and inductor current error (5 A/div) (α-axis), time scale (4 ms/div)

If the control structure with a lead compensator is used (see FIG. 5), the bandwidth can be widened in comparison to the case with just the proportional controller for the same k_{pI} value, without degrading the dynamic performance. The step response for $\omega_n = 2\pi 2000$ rad/s, i.e. $k_{pI} = 11.56$, is less oscillatory, as shown in Fig. 20. As the proportional gain is designed to achieve $\omega_n = 2\pi 3000\pi$ rad/s, i.e. $k_{pI} = 16.82$ (see Fig. 21), the step response is more damped than the one in Fig. 19. The result showed in Fig. 21 represents the maximum achievable bandwidth for the case with the lead compensator which corresponds to deadbeat case (2 sample periods for a 2nd order system). It must be noted that the switching ripple due to the PWM strategy does not degrade the current loop response even with the high current controller gain. The reason is that synchronous sampling was used in the measurements [8].

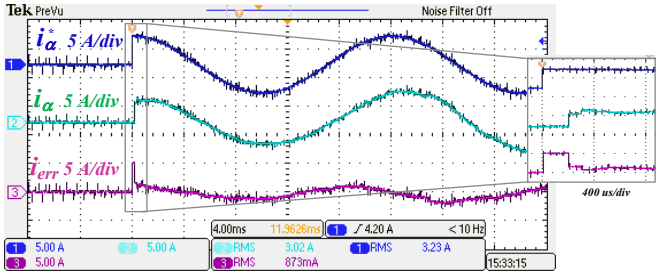


Fig. 20. Step response – P controller with lead compensator: $\boldsymbol{k_{pI} = 11.56}$, $\boldsymbol{k_L = 0.475}$, reference (5 A/div), real (5 A/div) and inductor current error (5 A/div) (α-axis), time scale (4 ms/div)

If the Smith Predictor is used the system can be even faster than the case with the lead compensator. As predicted in the simulation analysis whenever the system parameters and predicted delay are equal to the model parameters, the best performance that can be achieved with the Smith predictor is deadbeat (one sample) as compared to 2 samples in the case with the lead compensator. This result can be seen in Fig. 22.

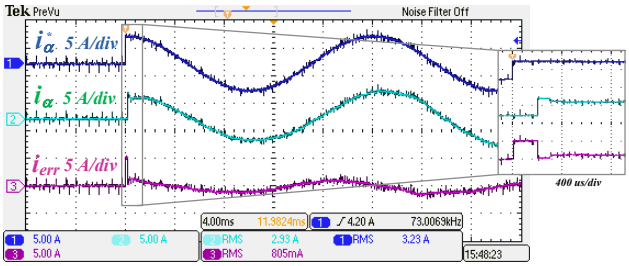


Fig. 21. Step response – P controller with lead compensator: $\boldsymbol{k_{pI} = 16.82}$, $\boldsymbol{k_L = 0.868}$, reference (5 A/div), real (5 A/div) and inductor current error (5 A/div) (α-axis), time scale (4 ms/div)

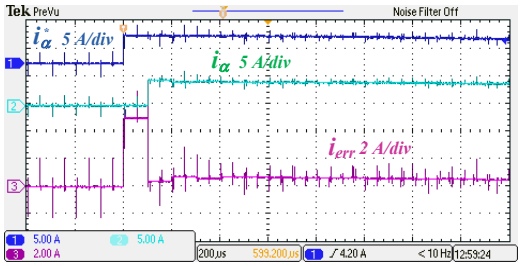
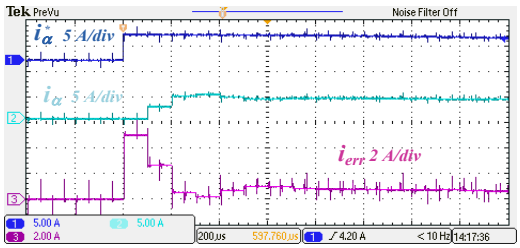
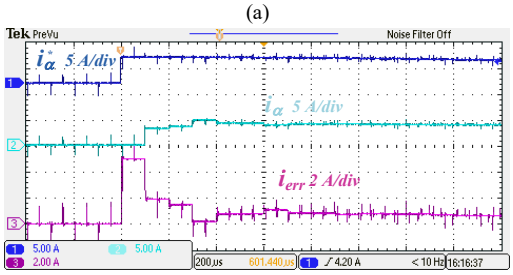


Fig. 22. Step response, reference (5 A/div), real (5 A/div) and inductor current error (2 A/div) (α-axis), time scale (200 μs/div): P controller + Smith Predictor, $k_{pI} = 12.6$.

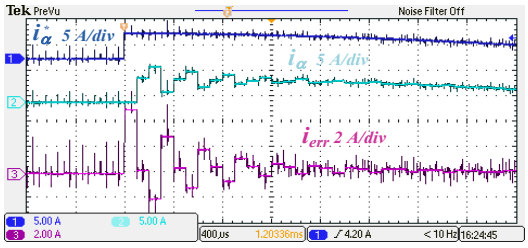
The Smith Predictor is almost insensitive to changes in resistance. Therefore, just the sensitivity to changes in the predicted values of the inductance (L_{SP}) and computation delay ($T_{d,SP}$) was verified. For this purpose, the predicted inductor value L_{SP} was set 1.5 times the rated value [see Fig. 23(a)]. Even with huge variations in this parameter, the step response has an acceptable behavior. As expected, the effect of increase L_{SP} with respect to the real inductance slow down the system response. The predicted computation delay $T_{d,SP}$ was changed to $0.5T_s$ and $1.5T_s$, as can be seen in Fig. 23(b) and Fig. 23(c). The system becomes more oscillatory during transients, in particular if $T_{d,SP}$ is higher than the real computation delay. For delay $T_{d,SP} = 1.5T_s$ it can be seen the oscillation at half of the switching frequency as was concluded in the simulation analysis.



(a)



(b)



(c)

Fig. 23. Sensitivity analysis on predicted plant values for the Smith predictor - reference (5 A/div), real (5 A/div) and inductor current error (2 A/div) (α-axis), time scale (200 µs/div): (a) $L_{SP} = 1.5L_{SP,rated}$; (b) $T_{d,SP} = 0.5T_{d,SP,rated}$; (c) $T_{d,SP} = 2T_{d,SP,rated}$.

B. *Voltage regulator tests*

The following results (Fig. 24 toFig. 28) regarding the voltage loop are obtained with voltage decoupling, P controller as current regulator, Smith predictor, and the anti-wind up scheme proposed in the previous section. The parameters of the system are presented in Table I. A diode bridge rectifier with an LC output filter supplying a resistive load is used as nonlinear load. Its parameters are presented in Table I. A 100% nonlinear step load change is performed with the harmonic compensators (HC) tuned at 5th and 7th harmonics (see Fig. 24). The results obtained are compared to the envelope of the voltage deviation v_{dev} as reported in the IEC 62040-3 standard for UPS systems [see Fig. 25]. It can be seen that the system reaches steady-state in less than half a cycle after the load step change. The dynamic response is within the limits imposed by the standard. For linear step load changes the results are better, even with just the fundamental voltage controller (HC are not necessary for linear loads).

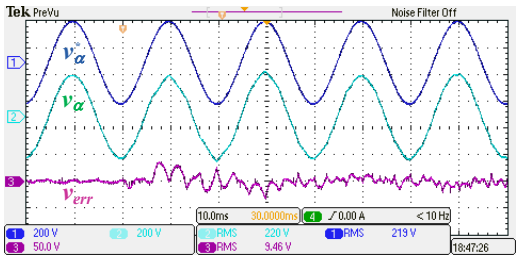


Fig. 24. Nonlinear step load changing (0 – 100%): reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis), time scale (10 ms/div)

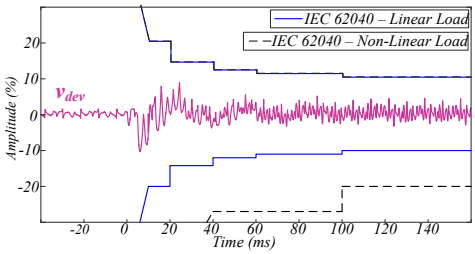
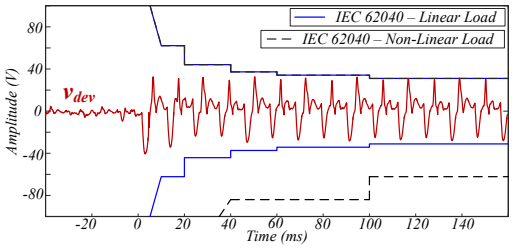
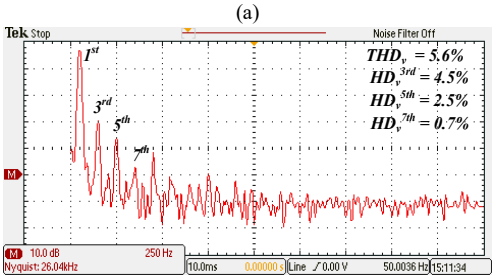


Fig. 25. Nonlinear step load changing (0 – 100%): Dynamic characteristics according to IEC 62040-3 standard for linear loads: overvoltage ($v_{dev} > 0$) and undervoltage ($v_{dev} < 0$)

To confirm the effectiveness of the proposed design, a 100% nonlinear unbalance (one phase open at the input of the diode bridge rectifier) step load change is performed, using just the fundamental harmonic compensator at the voltage controller. The response is again in the boundaries imposed to linear loads [see Fig. 26(a)]. The FFT results in Fig. 26(b) shows the harmonic content at steady state. It is shown the mitigation of the 3rd harmonic component by a large extent, even with just the resonator tuned at the fundamental frequency. These results show the benefits of widening the bandwidth for the voltage loop, which can be achieved with the design of the inner current loop based on Smith predictor.



(a)



(b)

Fig. 26. Unbalance nonlinear step load changing (0 – 100%): (a) Dynamic characteristics according to IEC 62040 standard for linear and nonlinear loads: overvoltage ($v_{dev} > 0$) and undervoltage ($v_{dev} < 0$) without HC; (b) FFT of the capacitor voltage.

The effects of the anti-wind up scheme are shown in Fig. 27 and Fig. 28. As the anti-wind up scheme is implemented, a step change of the reference voltage results in a less oscillatory response.

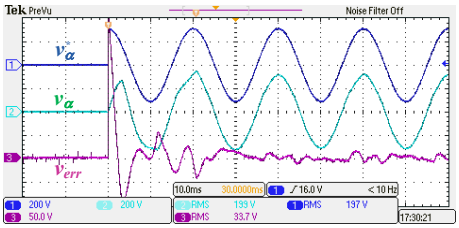


Fig. 27. Step response of the reference voltage: without anti-windup scheme, reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis), time scale (10 ms/div)

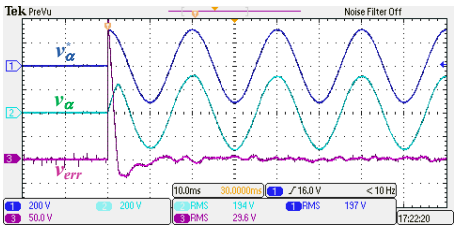


Fig. 28. Step response of the reference voltage: with anti-wind up scheme, reference (200 V/div), real (200 V/div) and capacitor voltage error (50 V/div) (α-axis), time scale (10 ms/div)

VII. CONCLUSIONS

The proposed work deepens on the discrete implementation of high performance controllers for islanded microgrids and UPS applications.

It is shown how both the lead compensator and Smith predictor are very suitable to enhance bandwidth and increase damping: in nominal conditions, it is possible to achieve deadbeat response with two sample periods for the case of the lead compensator and one sample period for the case of the Smith predictor. However, the Smith predictor is more sensitive to the parameters of the system, especially the computation delay. The sensitivity analysis in the discrete-time domain reveals that oscillation with half of the switching frequency or even instability is prone to occur if there are mismatch among the real and the estimated parameters used in the implementation. The best trade-off solution has been found to be the implementation with the Smith predictor, since the computation delay in microcontrollers is accurately estimated. Subsequently, a PR controller for the voltage loop is obtained. As the bandwidth of the voltage loop is widened, an anti-wind up scheme is considered to improve the robustness in the response to load transients. The proposed design in the discrete-time domain avoids algebraic loops, which could arise depending on the discretization method. The theoretical approaches have been verified by experimental results. Specific requirements set by the IEC 62040-3 standard for UPS systems have been validated by laboratory tests, which prove the suitability of the proposed solutions.

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