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A Second Look

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Steady-State Linear Kalman Filter-Based PLLs for Power Applications: A Second Look

Saeed Golestan, *Senior Member, IEEE*, Josep M. Guerrero, *Fellow, IEEE*, and Juan. C. Vasquez, *Senior Member, IEEE*

***Abstract*—In three-phase power and energy applications, the synchronous reference frame phase-locked loop (SRF-PLL) is a popular tool for the synchronization purposes. The SRF-PLL can be easily and effectively customized for different scenarios by changing its loop filter. Recently, some supposedly different PLLs using the steady-state linear Kalman filter (SSLKF) have been developed. The main aim of this letter is to analyze these PLLs. It is demonstrated that they are actually equivalent to some well-known SRF-PLL structures and, therefore, provide no advantage compared to them.**

***Index Terms*—Fixed gain filter, Kalman filter, phase-locked loop (PLL), synchronization, synchronous reference frame PLL (SRF-PLL), three-phase systems.**

I. Introduction

THE phase-locked loop (PLL) is regarded as one of the most popular tools for the grid synchronization of power electronics converters and extracting the grid voltage parameters in energy and power applications [1]–[3]. Recently, there have been intensive research efforts towards developing efficient PLLs. In three-phase systems, which this letter focuses on, the majority of these efforts are based on a standard structure, known as the synchronous reference frame PLL (SRF-PLL) [1]. The conventional SRF-PLL structure can be observed in Fig. 1(a). In this PLL, the phase error information is generated by transferring the three-phase grid voltage signals into the synchronous reference frame. The loop filter [a proportional-integral (PI) regulator] is responsible for regulating the phase error signal v_q to zero, and its output signal is considered as an estimation of the grid voltage frequency.

The conventional SRF-PLL has some drawbacks. The first problem is that the frequency estimated by the SRF-PLL undergoes an abrupt change when a phase jump happens [4]. This phenomenon is because of the coupling between frequency and phase variables. Notice that these parameters are estimated by a single loop in the conventional SRF-PLL [4]. Inspired by the enhanced PLL (EPLL) structure [3], [4], which has been developed based on an optimization procedure, this problem may be alleviated by tapping the frequency from the PI integrator output. Fig. 1(b), which is referred to as the enhanced SRF-PLL (ESRF-PLL), illustrates this idea.

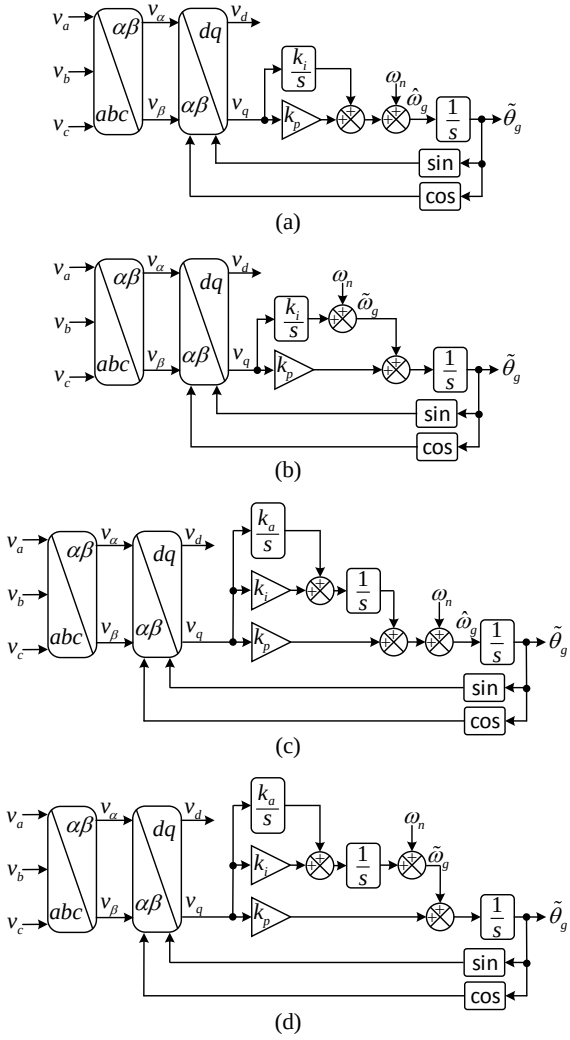

Fig. 1. Block diagram of (a) conventional SRF-PLL, (b) enhanced SRF-PLL (ESRF-PLL), (c) type-3 SRF-PLL, and (d) enhanced type-3 SRF-PLL (ET3-SRF-PLL). v_a, v_b, and v_c denote the three-phase input signals of the PLLs, v_α and v_β are the grid voltage signals in the stationary ($\alpha\beta$) frame, and v_d and v_q are the grid voltage signals in the synchronous (*dq*) frame. k_p, k_i, and k_a are the loop filter parameters. ω_n is the nominal value of the grid frequency. $\tilde{\theta}_g$ is the estimated phase angle. $\hat{\omega}_g$ and $\tilde{\omega}_g$ both denote the estimated frequency.

Another drawback of the conventional SRF-PLL is that it cannot follow frequency ramps with a zero phase error because

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it is a type-2 control system [5]. To deal with this problem, a type-3 SRF-PLL like that shown in Fig. 1(c) may be employed [6], [7]. The loop filter transfer function in this PLL is as $k_p + k_i/s + k_a/s^2$, where k_p, k_i, and k_a are its control parameters.

The type-3 SRF-PLL, similar to the conventional SRF-PLL, suffers from a large transient in the estimated frequency when a phase angle jump happens. Therefore, it can be alleviated in a similar manner as the ESRF-PLL [see Fig. 1(d)]. This structure is referred to as the enhanced type-3 SRF-PLL (ET3-SRF-PLL).

Recently, some synchronization techniques for employing in power and energy applications have been designed which apparently have different structures compared to the conventional SRF-PLL and its variants. The general structure of these techniques, which are often referred to as the steady-state linear Kalman filter-based PLLs (SSLKF-PLLs)[1] [8]–[10] and sometimes the fixed gain filter [11], can be observed in Fig. 2. As shown, the prediction and correction stages are two main parts of these techniques.

The main aim of this letter is analysing these so-called new synchronization methods [8]–[11]. It is demonstrated here that they are equivalent with some well-known SRF-PLLs. This equivalence means that these synchronization techniques offer no advantage compared to the well-known SRF-PLLs.

II. Analysis of SSLKF-PLLs

A. SSLKF-PLL Based on a Two-State Prediction Model

Fig. 2, as mentioned before, illustrates the general structure of an SSLKF-PLL. In developing a two-state version of this PLL, it is assumed in [8] that the frequency of the PLL input signal does not experience large variations. Based on this assumption, the following two-state prediction model is considered [8]

$$\begin{aligned} &\boldsymbol{x}(n) = \boldsymbol{A}\boldsymbol{x}(n-1) \\ &y(n) = \boldsymbol{C}\boldsymbol{x}(n) \\ &\boldsymbol{x}^T = \begin{bmatrix} \theta_g & \omega_g \end{bmatrix}; \boldsymbol{A} = \begin{bmatrix} 1 & T_s \\ 0 & 1 \end{bmatrix}; C = \begin{bmatrix} 1 & 0 \end{bmatrix} \end{aligned} \quad (1)$$

in which n denotes the current sample, θ_g and ω_g are the grid voltage angle and angular frequency, respectively, and T_s is the sampling time. Throughout this letter, $T_s = 0.0001$ s (which corresponds to a sampling frequency equal to 10 kHz) is considered.

Based on the model described in (1), the following steps are conducted by the prediction/correction filter to accurately estimate the state variables [8]:

1) Predicting the states at the next sampling time

$$\tilde{\boldsymbol{x}}(n) = \boldsymbol{A}\hat{\boldsymbol{x}}(n-1). \quad (2)$$

2) Correcting the predicted states using the phase error information

$$\hat{\boldsymbol{x}}(n) = \tilde{\boldsymbol{x}}(n) + \boldsymbol{\kappa}\theta_e(n) \quad (3)$$

[1]Strictly speaking, the SSLKF-PLL may not be regarded as a Kalman filter because, as shown in Fig. 2, its correction vector is fixed. Notice that implementing a Kalman filter involves adjusting its gains according to the Kalman filter theory in each sampling period.

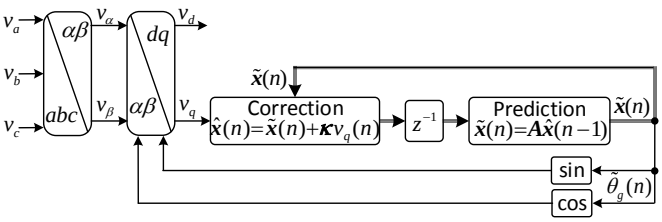

Fig. 2. General structure of the SSLKF-PLL (also known as the fixed gain filter).

where $\boldsymbol{\kappa}^T = \begin{bmatrix} \kappa_1 & \kappa_2 \end{bmatrix}$ is referred to as the correction vector, and $\theta_e(n) = \theta_g(n) - \boldsymbol{C}\tilde{\boldsymbol{x}}(n) = \theta_g(n) - \tilde{\theta}_g(n)$.

Based on (1)-(3), the PLL discrete-time implementation can be derived as shown in Fig. 3(a). This PLL is briefly called the SSLKF-PLL2 as it is based on a two-state prediction model. Notice that the signal $v_q(n) = \sin(\theta_g(n) - \tilde{\theta}_g(n)) \approx \theta_g(n) - \tilde{\theta}_g(n) = \theta_e(n)$ contains the phase error information and is used for the correction stage. A hidden assumption here is considering the grid voltage amplitude equal to 1 p.u.

By applying the block diagram algebra to the correction and prediction stages of Fig. 3(a), an alternative representation of the SSLKF-PLL2 can be achieved as shown in Fig. 3(b). Notice that, in this structure, $\frac{T_s z}{z-1}$ and $\frac{T_s}{z-1}$ describe two integrators discretized using backward and forward Euler methods, respectively. Considering this fact, the s-domain equivalent of the SSLKF-PLL2 can be obtained as illustrated in Fig. 3(c). This structure is the same as the ESRF-PLL [see Fig. 1(b)] if $\kappa_1' = \kappa_1/T_s = k_p$ and $\kappa_2' = \kappa_2/T_s = k_i$. Therefore, it can be concluded that the SSLKF-PLL2 and the ESRF-PLL are equivalent systems.

B. SSLKF-PLL Based on a Three-State Prediction Model

In designing this PLL, it is assumed that large frequency ramping changes during normal operating conditions are likely. Based on this assumption, the following three-state prediction model is considered [9], [10]

$$\begin{aligned} &\boldsymbol{x}(n) = \boldsymbol{A}\boldsymbol{x}(n-1) \\ &y(n) = \boldsymbol{C}\boldsymbol{x}(n) \\ &\boldsymbol{x}^T = \begin{bmatrix} \theta_g & \omega_g & a_g \end{bmatrix}; \boldsymbol{A} = \begin{bmatrix} 1 & T_s & T_s^2/2 \\ 0 & 1 & T_s \\ 0 & 0 & 1 \end{bmatrix} \\ &\boldsymbol{C} = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix} \end{aligned} \quad (4)$$

where $a_g = d\omega_g/dt$. Using this model, the state prediction/correction procedure can be carried out as follows

$$\tilde{\boldsymbol{x}}(n) = \boldsymbol{A}\hat{\boldsymbol{x}}(n-1). \quad (5)$$

$$\hat{\boldsymbol{x}}(n) = \tilde{\boldsymbol{x}}(n) + \boldsymbol{\kappa}\theta_e(n) \quad (6)$$

where $\boldsymbol{\kappa}^T = \begin{bmatrix} \kappa_1 & \kappa_2 & \kappa_3 \end{bmatrix}$.

Based on (4)-(6), the PLL structure shown in Fig. 4(a) can be derived. This PLL is named the SSLKF-PLL3 as it is based on a three-state prediction model.

Using the block diagram algebra, the SSLKF-PLL3 can be rearranged as shown in Fig. 4(b). Considering that $\frac{T_s z}{z-1}$

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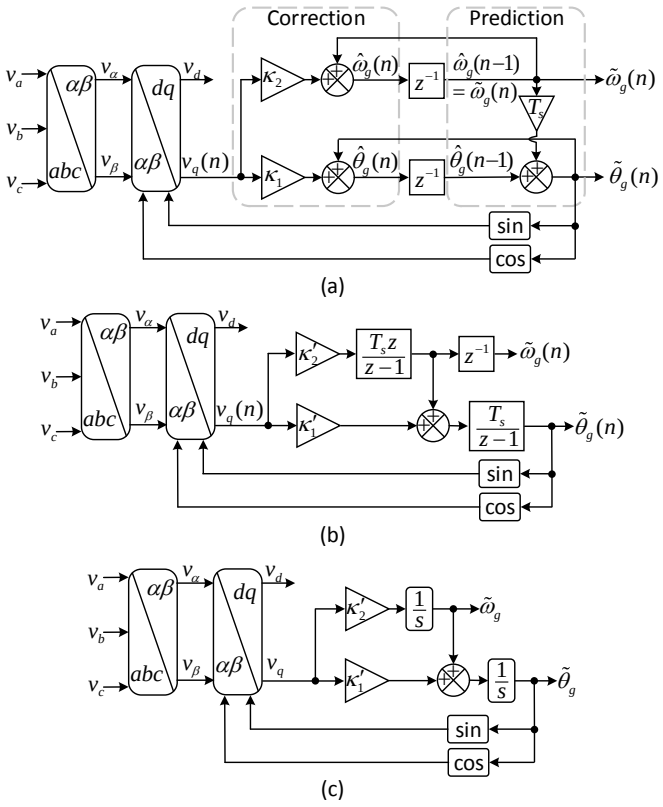

Fig. 3. (a) SSLKF-PLL based on a two-state prediction model. This PLL is briefly referred to as the SSLKF-PLL2. (b) An alternative representation of the SSLKF-PLL2, which may be obtained by applying the block diagram algebra to Fig. 3(a). (c) The s-domain equivalent of the SSLKF-PLL2. $\kappa_1' = \kappa_1/T_s$ and $\kappa_2' = \kappa_2/T_s$.

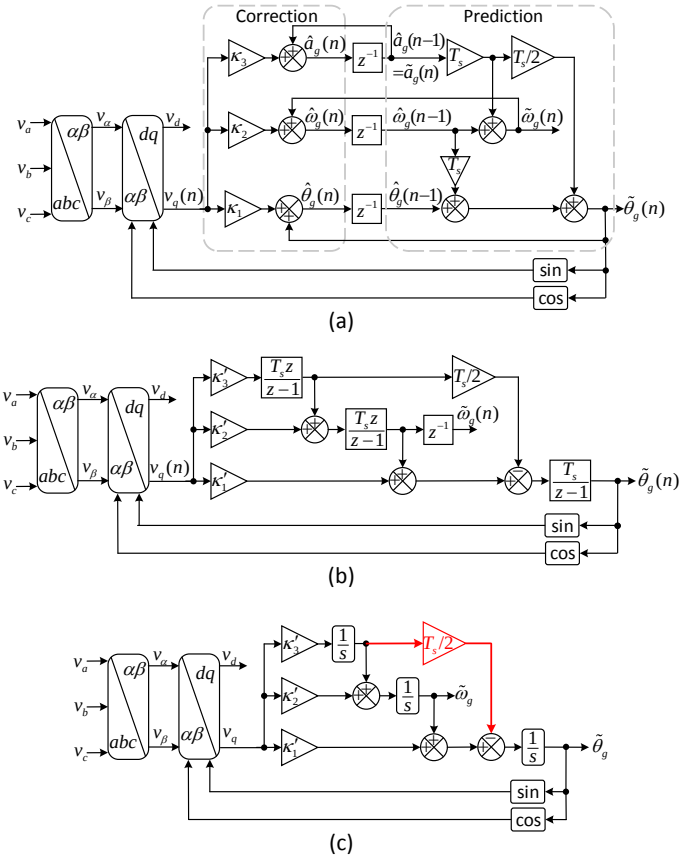

Fig. 4. a) SSLKF-PLL based on a three-state prediction model. This structure is briefly called the SSLKF-PLL3. (b) An alternative representation of the SSLKF-PLL3, which is achieved by applying the block diagram algebra to Fig. 4(a). (c) The s-domain equivalent of the SSLKF-PLL3. $\kappa_1' = \kappa_1/T_s$, $\kappa_2' = \kappa_2/T_s$, and $\kappa_3' = \kappa_3/T_s$.

and $\frac{T_s}{z-1}$ are both discrete integrators, the s-domain equivalent of Fig. 4(b) can be obtained as depicted in Fig. 4(c). The highlighted (red-color) path in Fig. 4(c) has a very negligible influence on the SSLKF-PLL3 performance as it has a very small gain (i.e., half the sampling period). By neglecting it, we can observe that the SSLKF-PLL3 and the ET3-SRF-PLL [see Fig. 1(d)] are equivalent systems if $\kappa_1' = \kappa_1/T_s = k_p$, $\kappa_2' = \kappa_2/T_s = k_i$, and $\kappa_3' = \kappa_3/T_s = k_a$.

It is worth mentioning here that researchers who are working in the communication field are well aware of the strong similarity of PLLs and Kalman filters. They have reported these similarities in some research and tutorial articles [12]–[14].

III. Tuning

A. SSLKF-PLL2

Using Fig. 3(c), the s-domain small-signal model of the SSLKF-PLL2 can be derived as shown in Fig. 5(a). Notice that, as mentioned before, the grid voltage amplitude is assumed to be 1 p.u. Based on this model, the closed-loop transfer function relating ω_g to $\tilde{\omega}_g$ can be derived as

$$\tilde{\omega}_g(s) = \frac{\kappa_2'}{s^2 + \kappa_1' s + \kappa_2'} \omega_g(s). \tag{7}$$

By defining $\kappa_1' = \kappa_1/T_s = 2\zeta\omega_n'$ and $\kappa_2' = \kappa_2/T_s = (\omega_n')^2$ and selecting the natural frequency ω_n' and the damping factor ζ according to the preferred (required) dynamic behavior, the SSLKF-PLL2 control parameters are chosen. Notice that the natural frequency is the most influential factor in determining the PLL bandwidth and, hence, its noise immunity and transient response speed, while ζ is the major factor in determining the damping of the dynamic response and, consequently, the PLL phase margin (PM). Here, $\zeta = 1/\sqrt{2}$ (which in the literature is regarded as an optimum damping factor for second-order systems) and $\omega_n' = 125$ rad/s are selected. These values correspond to $\kappa_1 = 0.01768$ and $\kappa_2 = 1.5625$.

B. SSLKF-PLL3

Using Fig. 4(c), the s-domain small-signal model of the SSLKF-PLL3 can be derived as shown in Fig. 5(b). For the sake of simplicity in the tuning procedure, we have neglected the highlighted (red color) path in Fig. 4(c). As mentioned before, it has a very negligible influence on the SSLKF-PLL3 performance.

Using Fig. 5(b), the following open-loop transfer function can be obtained

$$G_{ol}(s) = \frac{\tilde{\omega}_g(s)}{\omega_g(s) - \tilde{\omega}_g(s)} = \frac{\kappa_2' s + \kappa_3'}{s^2(s + \kappa_1')}. \tag{8}$$

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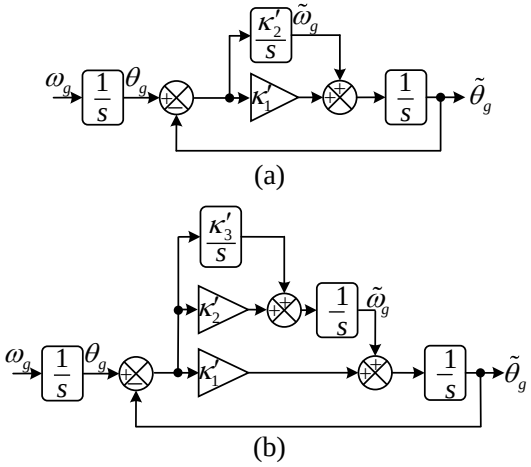


Fig. 5. s-domain small-signal model of (a) the SSLKF-PLL2 and (b) the SSLKF-PLL3.

TABLE I
CONTROL PARAMETERS

	Parameters
SSLKF-PLL2	$\kappa_1 = 0.01768$, $\kappa_2 = 1.5625$,
ESRF-PLL	k_p=176.8, $k_i = 15625$
SSLKF-PLL3	$\kappa_1 = 0.03018$, $\kappa_2 = 3.7722$, $\kappa_3 = 195.3125$
ET3-SRF-PLL	k_p=301.8, $k_i = 37722$, $k_a = 1953125$

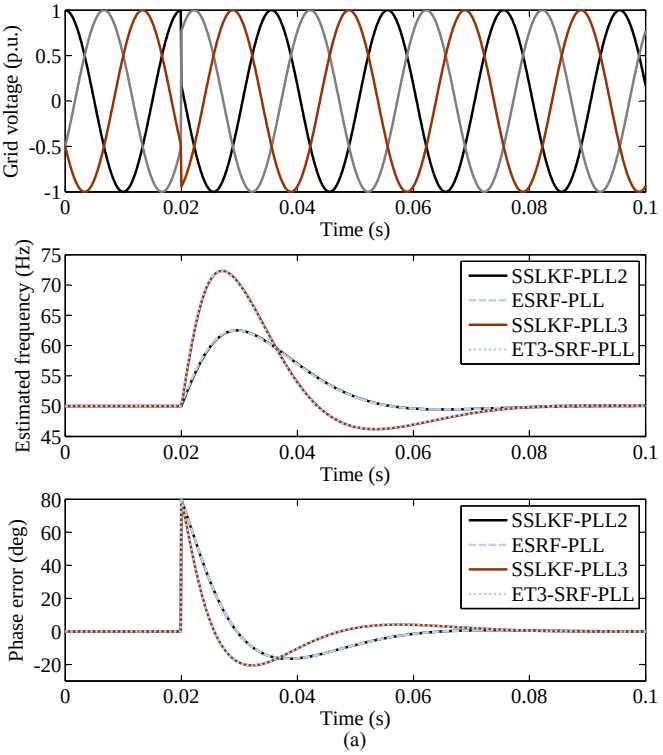
Because this open-loop transfer function has two poles at the origin and a pole-zero pair with non-zero values, the symmetrical optimum method sounds to be the best option for selecting its control parameters [15], [16]. Applying this approach, which sets the gain crossover frequency at the geometric mean of the pole-zero pair to maximize the PM, yields

$$\begin{aligned} \kappa_1' &= \kappa_1/T_s = b\omega_c \\ \kappa_2' &= \kappa_2/T_s = b\omega_c^2 \\ \kappa_3' &= \kappa_3/T_s = \omega_c^3. \end{aligned} \tag{9}$$

In (9), ω_c denotes the gain crossover frequency and determines the speed of dynamic response and the level of noise immunity, and b is a factor that specifies the PM as $PM = \tan^{-1}[(b^2-1)/(2b)]$. Here, $b = \sqrt{2}+1$ (which corresponds to $PM = 45°$) and $\omega_c = 125$ rad/s are chosen. These values correspond to $\kappa_1 = 0.03018$, $\kappa_2 = 3.7722$, and $\kappa_3 = 195.3125$.

IV. PERFORMANCE COMPARISON

To support the theoretical findings of this letter (i.e., the equivalence of the SSLKF-PLL2 [Fig. 3(a)] and ESRF-PLL [Fig. 1(b)], and the equivalence of the SSLKF-PLL3 [Fig. 4(a)] and ET3-SRF-PLL [Fig. 1(d)]), some numerical and experimental results are presented. The numerical results are obtained using Matlab/Simulink and the experimental ones are provided using a dSPACE platform. In obtaining the experimental results, the three-phase input signals of the PLLs are generated by the dSPACE platform. The control parameters of all PLLs can be found in Table I. It is worth mentioning here that the backward and forward Euler methods are used for the discretization of the loop filter and voltage-controlled oscillator of the SRF-PLLs, respectively.



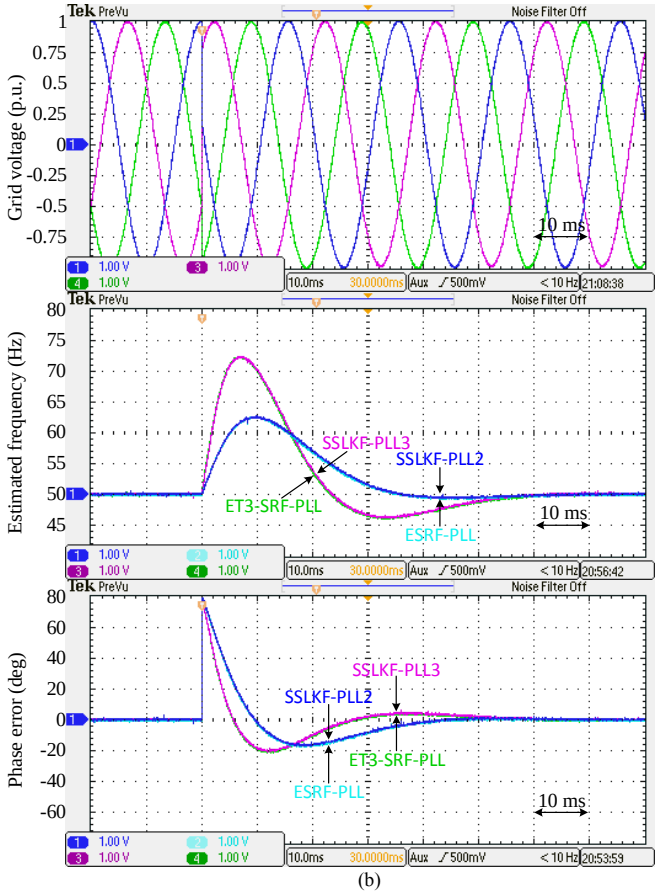


Fig. 6. (a) Simulation results and (b) experimental results of Test 1.

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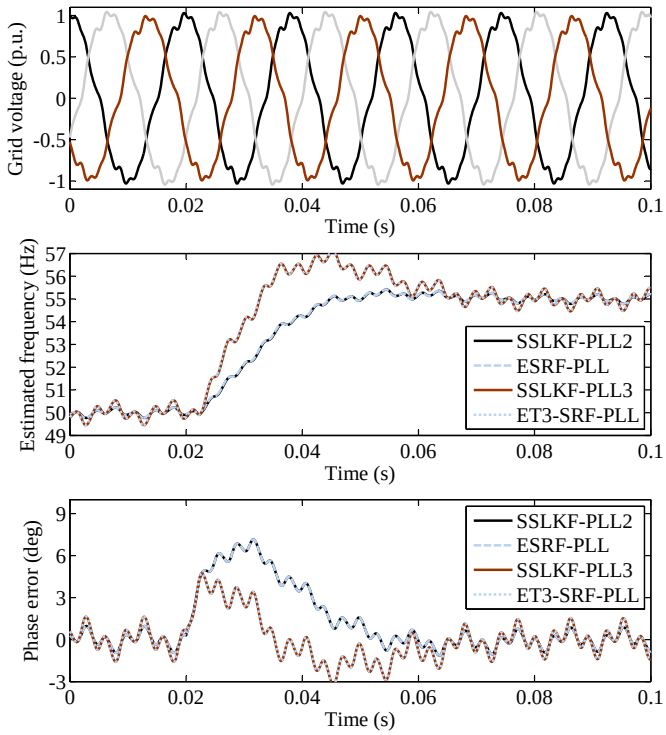

Fig. 7. Simulation results of Test 2.

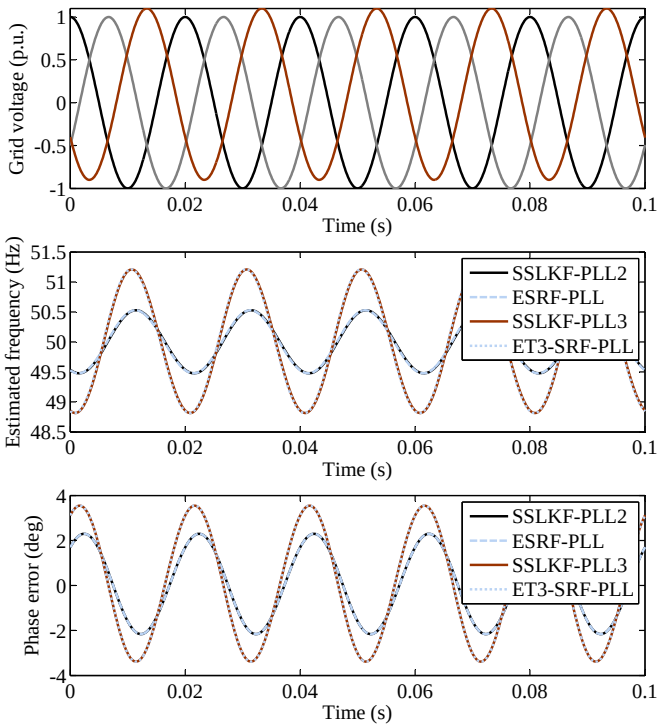

Fig. 8. Simulation results of Test 3.

Four tests are performed. The description of these tests is as follows.

Test 1: A 80° phase angle jump.

Test 2: A $+5$ Hz frequency jump under a harmonically distorted and imbalanced grid condition.

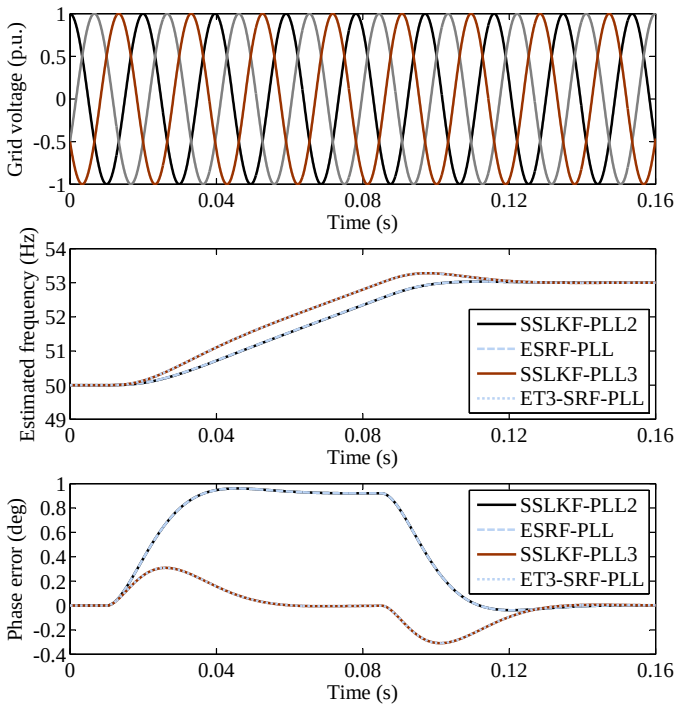

Fig. 9. Simulation results of Test 4.

Test 3: Presence of 0.1 p.u. dc component in one phase of the grid voltage three-phase signal.

Test 4: A $+40$ Hz/s ramping change in the grid voltage frequency for a duration of 0.075 s.

Fig. 6 shows the simulation and experimental results of Test 1. Table II summarizes the details of the obtained results. As expected, the SSLKF-PLLs and their corresponding SRF-PLLs demonstrate well-matched results. To save the space, the experimental results are not shown for the rest of the tests.

Figs. 7, 8, and 9 demonstrate the simulation results of Tests 2, 3, and 4, respectively. The details can be found in Table II. In all these tests, again, it is observed that the SSLKF-PLLs and their corresponding SRF-PLLs demonstrate well-matched results.

V. Conclusion

In this letter, an analysis of two SSLKF-PLLs, which have been recently designed and proposed for the synchronization in power and energy applications, was conducted. It was shown that these SSLKF-PLLs are mathematically equivalent to two well-known SRF-PLLs, which have a rather long history of use in power and energy applications. To support this theoretical finding, some numerical and experimental tests were conducted. The obtained results were confirmed that the SSLKF-PLLs and their corresponding SRF-PLLs are equivalent systems. It means that the SSLKF-PLLs have no advantage/disadvantage compared to their corresponding SRF-PLLs.

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TABLE II
SUMMARY OF RESULTS. B/A DENOTES BEFORE/AFTER THE FREQUENCY JUMP.

	SSLKF-PLL2/ESRF-PLL	**SSLKF-PLL3/ET3-SRF-PLL**
Test 1		
2% settling time	40 ms (2 cycles)	52 ms (2.6 cycles)
Phase overshoot	16.6° (20.7%)	20.5° (25.6%)
Peak frequency deviation	12.5 Hz	22.3 Hz
Test 2		
Peak-to-peak phase error (B/A)	1.92°/1.75°	3.2°/2.93°
Peak-to-peak frequency error (B/A)	0.46 Hz/0.42 Hz	1.09 Hz/1 Hz
Test 3		
Peak-to-peak phase error	4.46°	6.93°
Peak-to-peak frequency error	1.05 Hz	2.39 Hz
Test 4		
Steady-phase phase error during frequency ramp	0.92°	0°

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