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# Development of Simulink Based Modeling Platform for 3.3kV/400A SiC MOSFET Power Module


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***Abstract*— The main objective of this paper is to develop a Simulink based modeling platform for a commercial 3.3 kV/400 A SiC MOSEFT power module. The implemented equivalent circuit of 3.3 kV SiC MOSFET in Simulink platform is based on the original well–established single–chip Mc Nutt/Hefner model. The developed model has been validated with the experimental data both for static and dynamic tests at several temperatures. The dynamic simulations have further been verified with various gate resistances that accurately describes the transient operation during turn-on and turn off of the pulse sequence. The influence of various parasitic elements (i.e., stray inductances) have been studied. Finally, the operation of a Buck converter, whose switch consists of two modules in series, has been verified, studying the converter efficiency under various circuit parameters.**



***Keywords*— *SiC MOSFETs, Device Simulation, SiC device modeling, Wide bandgap devices, SiC power modules***


## I. Introduction

Recently, Silicon Carbide (SiC) material has shown promising results and is now well–believed to be the material of choice due to its superior physical properties (i.e. high critical electric field strength, wide bandgap, saturation velocity, thermal conductivity etc.,) for a diverse range of power applications. Because of these physical properties, SiC based semiconductor devices [1 – 10] offer faster switching capabilities, higher breakdown voltage and lower on–resistance using thin, low–doped drift layer compared to conventional Si counterpart that fairly help to reduce the on–state losses besides efficient and relaxed cooling requirement. This further leads to more system compactness, higher system efficiency and well suited to high–temperature electronic applications where the scope of using Si power devices is limited. While low voltage SiC devices (i.e., diodes, BJTs, MOSFETs, JFETs) in the voltage range from 1.2 – 1.7 kV are commercially available for a diverse range of PV, automotive and industrial applications, high voltage SiC devices (> 3.3 kV) [11 – 16] still wait for their market entry.

While fair SiC device technological progress is witnessed recently, SiC device modeling activity still lags behind the device development. Simple analytical device models [7 – 10] with few set of parameters are required to facilitate the power converter design, optimize the gate drivability, study the impact of various circuit parasitics with an overall impact to lower the development cost and effort of potential power circuit. Several numerical, table based, physical [6] and empirical models have been published in the literature for Si and SiC based power devices with various degree of accuracy, complexity, scalability and validity range under different operating condition. Note that simple and more compact device models [1, 5 – 10] are required for accurate description of the physics of device operation on one side and accurate behavior of circuit predictability on the other side. So far, research activity related to the development of compact device models for high voltage SiC devices (> 3.3 kV) is still very limited and not visible mostly in the scientific literature.

The main objective of this work is therefore to develop and implement simple physical model in Simulink platform using 3.3 kV/400 A SiC MOSFET power module. The model chosen in the present work is based on the original comprehensive physics–based SiC MOSFET modeling work presented by McNutt/Hefner for single chip SiC MOSFET devices. A parameter extraction routine has been developed to facilitate quick extraction of device parameters from initial guesses supported by the measurement data. Results have finally been validated with static and dynamic experimental results. The developed model has further been validated under various test conditions such as gate resistance, temperature and stray inductances. The predicted energy losses show fair match with the experimental data in all cases.

## II. Model Description

The model implemented in this work is based on the original work by McNutt/Hefner [1] that takes into account both the current component coming from the main part of the MOSFET channel and the conduction current, which originated from the channel's corners. Note that the conduction process at the corners is induced at lower gate voltages than the main part. The total current $I_{mos}$ is then described by the (1), representing these two regions with $I_{mosh}$ for the main channel and $I_{mosl}$ for the corner. This division is accomplished by inserting in the model two threshold voltages, one for each part of the device operation. Moreover, the SiC MOSFET operation is separated in two more regions namely linear and saturation region. The voltage across the device primarily defines which part of the current component dominates in the conduction process.

$$I_{mos} = I_{mosh} + I_{mosl} \tag{1}$$

During the device conduction, the total drain–source voltage $V_{dds}$ consists of the voltage across the MOSFET channel $V_{ds}$, the voltage–drop along the drift part of the layer with resistance $R_b$ and the voltage–drop across the series drain resistance $R_s$ as well described by (2)

$$V_{dds} = V_{ds} + (R_b + R_s)I_{mos} \tag{2}$$

The resistor $R_s$ (representing the substrate part of the device) is constant, while the epitaxial resistor $R_b$ is varying both with the depletion region width and the operating temperature, and its value is given by (3).

$$R_b = \frac{W_b - W_{dsj}}{qAN_b\mu_n} \quad (3)$$

The internal capacitances as illustrated in Fig. 1, define the dynamic response of the model and finally shape the transient characteristics. The gate–source capacitance $C_{gs}$ mostly remains constant during the device operation, whereas the gate–drain $C_{gd}$ capacitance (4) and drain–source capacitance $C_{ds}$ (5) are voltage–dependent. Moreover, $C_{gi}$ capacitor is inserted in the model when the gate voltage reaches large negative voltages but is excluded here due to its insignificant impact in the device operation. Furthermore, the temperature dependency of the device physical behavior was included in the model through a set of modeling parameters such as threshold voltage $V_{th}$, saturation $K_p$ and linear $K_{fl}$ region transconductance, transverse electric field parameter θ, bulk electron mobility $\mu_n$, the intrinsic carrier concentration $n_i$ and the built–in junction potential $V_{bi}$. The values of the above parameters are changing according to the temperature, affecting the model current–voltage behavior [1].

$$C_{gd} = \begin{cases} C_{oxd}, & for\ V_{ds} \le V_{gs} - V_{Td} \\ \frac{C_{oxd}C_{gdj}}{C_{oxd}+C_{gdj}}, & for\ V_{ds} \le V_{gs} - V_{Td} \end{cases} \quad (4)$$

$$C_{ds} = \frac{A_{ds}\epsilon_{semi}}{W_{dsj}} \quad (5)$$

The methodology for the parameter extraction is presented in [1, 3]. The theoretical values that form the initial guess were directly extracted first from the static and dynamic characteristics similar to [1, 3]. This extraction procedure is composed of two parts. The first part refers to the static validation and the second part refers to the parameters which govern the dynamic behavior of the model. The extraction procedure for each part was iterated for different parameters during static and dynamic validation until the final set of parameters are obtained that validate the experimental results with the lowest defined error margin. The static validation was obtained with two set of experimental data namely with constant gate–source voltage ($V_{gs}$) and sweeping drain–source voltage $V_{ds}$ at fixed temperature and the other one with fixed drain–source voltage and varying gate–source voltage $V_{gs}$ to get the transfer characteristics of SiC MOSFET module.

The dynamic validation is made through a double pulse test, investigating the turn–on and off characteristics of the transistor. The electrical circuit is shown in Fig. 2, describing the experimental setup. The inductive load is supplied by 2.0 kV DC bus voltage. The stray elements ($L_{stray}$, $L_g$ and $L_s$) of the topology are included in the schematic reflecting the overall bus bar and other stray elements (i.e., power module, gate–emitter drivability etc.,) existing in the test setup. The final extracted parameter values in the Simulink model, are presented in Table 1. A complete experimental detail along with static and dynamic behavior under different test condition of 3.3 kV, 400 A SiC power module is given elsewhere [4].

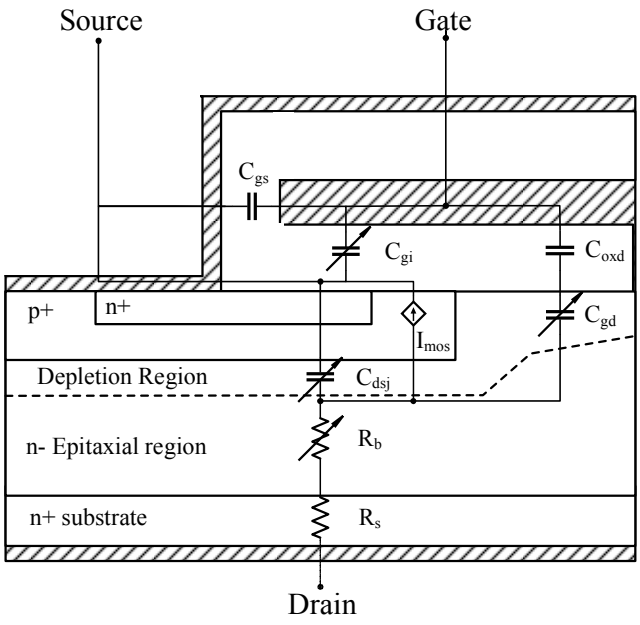



Fig.1. A schematic cross–section of SiC MOSFET power module.

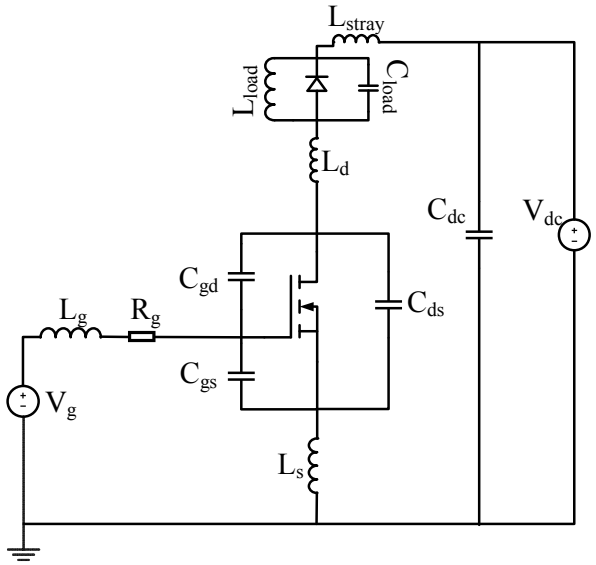



Fig.2. Double pulse test electrical circuit used in the Simulink platform.

## III. Model Validation

### A. Static validation

A thorough validation of the model is performed with experimental data under different bias conditions and for different temperatures. Fig. 3 illustrates the experimental and simulated I–V characteristics for different gate voltages at room temperature. It can be observed that the model shows a fair agreement at different gate drive voltages. A fair agreement is further obtained at higher temperatures (i.e., 25°C and 150°C) as shown in Fig. 4 at a gate bias of 20 V. Moreover, the validity of the model from transfer characteristics at different temperatures can also be observed in Fig. 5 at constant drain–source bias of 10.0 V where the trend of decreasing threshold voltage with the increase of temperature is clearly observed. The extracted on–resistance ($R_{on}$) comparison between the experimental and simulation results at a gate bias of 20 V is presented in Fig. 6, indicating again a fair agreement between experimental and model values. For example, experimental (model) on–resistance $R_{on}$

of 6.0 mΩ (6.0 mΩ) at 300 K and 20.0 mΩ (19.5 mΩ) at 425 K is obtained. Note that the increase in the on–resistance (i.e., estimated by the slope of the linear portion of $I_{ds} - V_{ds}$ curves for a given gate bias) with the temperature is primarily a result of reduction in the overall bulk mobility of electrons in the JFET region and drift layer at high temperatures consistent to the previous observations [3, 4, 7]. A threshold voltage (i.e., predicted from the linear portion of the transfer characteristics for a given drain–source bias) decrease with increasing temperature is clearly seen in Fig. 6 as well.

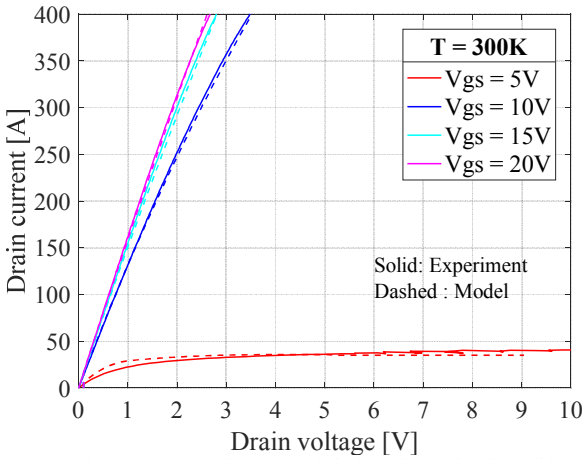



Fig.3. Drain current as a function of drain voltage for four different gate voltages (5, 10, 15, 20 V) at 300 K.

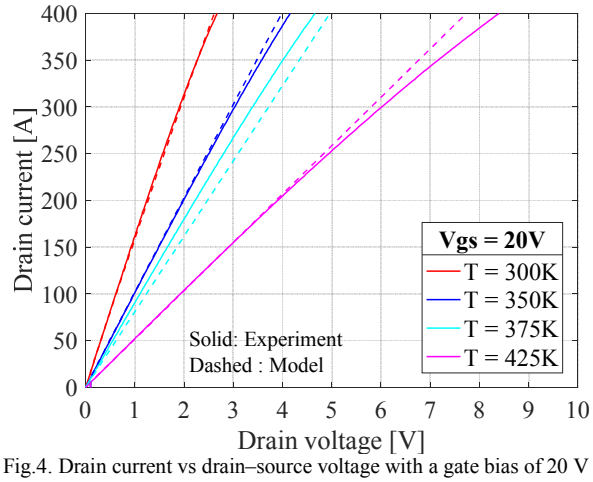



Fig.4. Drain current vs drain–source voltage with a gate bias of 20 V at 300, 350, 375 and 425 K.

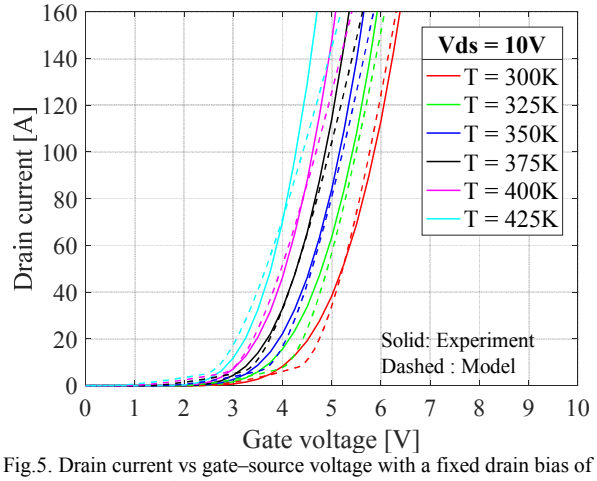



Fig.5. Drain current vs gate–source voltage with a fixed drain bias of 10 V at 300, 350, 375 and 425 K.

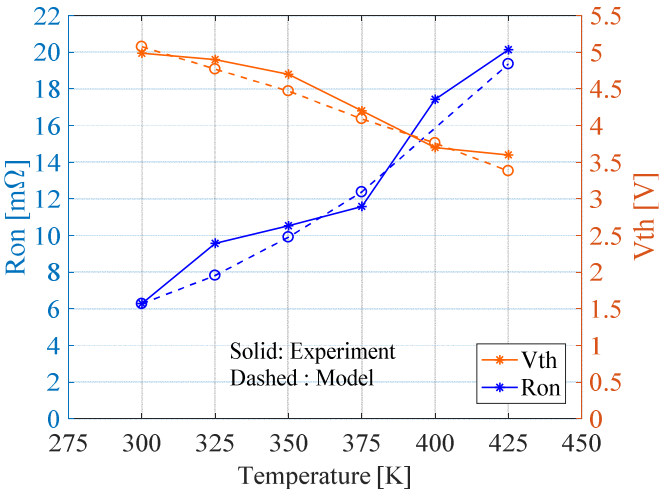



Fig.6. On–resistance $R_{on}$ (left–axis) at gate voltage of 20 V and threshold voltage (right–axis) as a function of temperature for 3.3 kV SiC module.

TABLE I EXTRACTED PARAMETERS FOR A 3.3 KV/400 A SIC MOSFET

| Parameter | | Value |
|---|---|---|
| $K_{p0}$ | Satur. region transconductance (A/V$^2$) | 120 |
| $\theta_0$ | Transverse electric field parameter (1/V) | 0.319 |
| $V_{t0}$ | Threshold voltage (V) | 4.2 |
| $K_{fl}$ | Linear region transconductance | 0.001 |
| $dVT_l$ | Low current threshold voltage diff. (V) | 1.5 |
| $P_{vf}$ | Pitch–off voltage factor | 0.75 |
| $R_s$ | Series drain resistance (mΩ) | 0.862 |
| $N_b$ | Base dopant density (x10$^{16}$cm$^{-3}$) | 2.25 |
| $W_b$ | Metallurgical drift region (cm) | 0.0031 |
| $A$ | Device active area (cm$^2$) | 0.588 |
| $K_{f0}$ | Linear region transconductance factor | 1.05 |
| $C_{gs}$ | Gate–drain capacitance (nF) | 40 |
| $C_{ox}$ | Gate oxide capacitance (nF) | 10 |
| $\alpha_{gd}$ | Gate–drain overlap area (cm$^2$) | 0.0038 |
| $V_{Td0}$ | Gate–drain overlap depletion thres. (V) | –10 |
| $V_{bi}$ | Built–in junction potential (V) | 3.1 |
| $\theta_1$ | Temperature coefficient | 0.8 |
| $K_{p1}$ | $K_p$ Temperature coefficient | 0.95 |
| $K_{f1}$ | $K_f$ Temperature coefficient | 2.8 |
| $V_{T1}$ | Threshold voltage temp. coefficient | –0.015 |

## B. *Dynamic validation*

The transient characteristics of the model are presented in Fig. 7 at a supply voltage of 2.0 kV. A double pulse test with inductive load for 3.3 kV, 400 A SiC MOSFET module has been performed for different temperatures, supply voltage and load currents using in–house gate drive unit and for different temperatures [4]. With fixed gate pulse sequence, a load inductance was varied to get the required load current during double pulse tests. As it is shown in the Fig. 7, the model accurately predicts the dynamic waveforms during turn on and off transients, estimating the correct di/dt and dv/dt slopes. For example, experimental (simulated) turn on and turn off energy loss was 65.0 (68.0) and 133 (106) mJ respectively, at 2.0 kV and 350 A. A relatively smaller simulated turn off energy loss is observed due to less turnoff voltage overshoot. However, the drain voltage overshoot at turn–off and the trend of the gate voltage swing is qualitatively correctly predicted by the

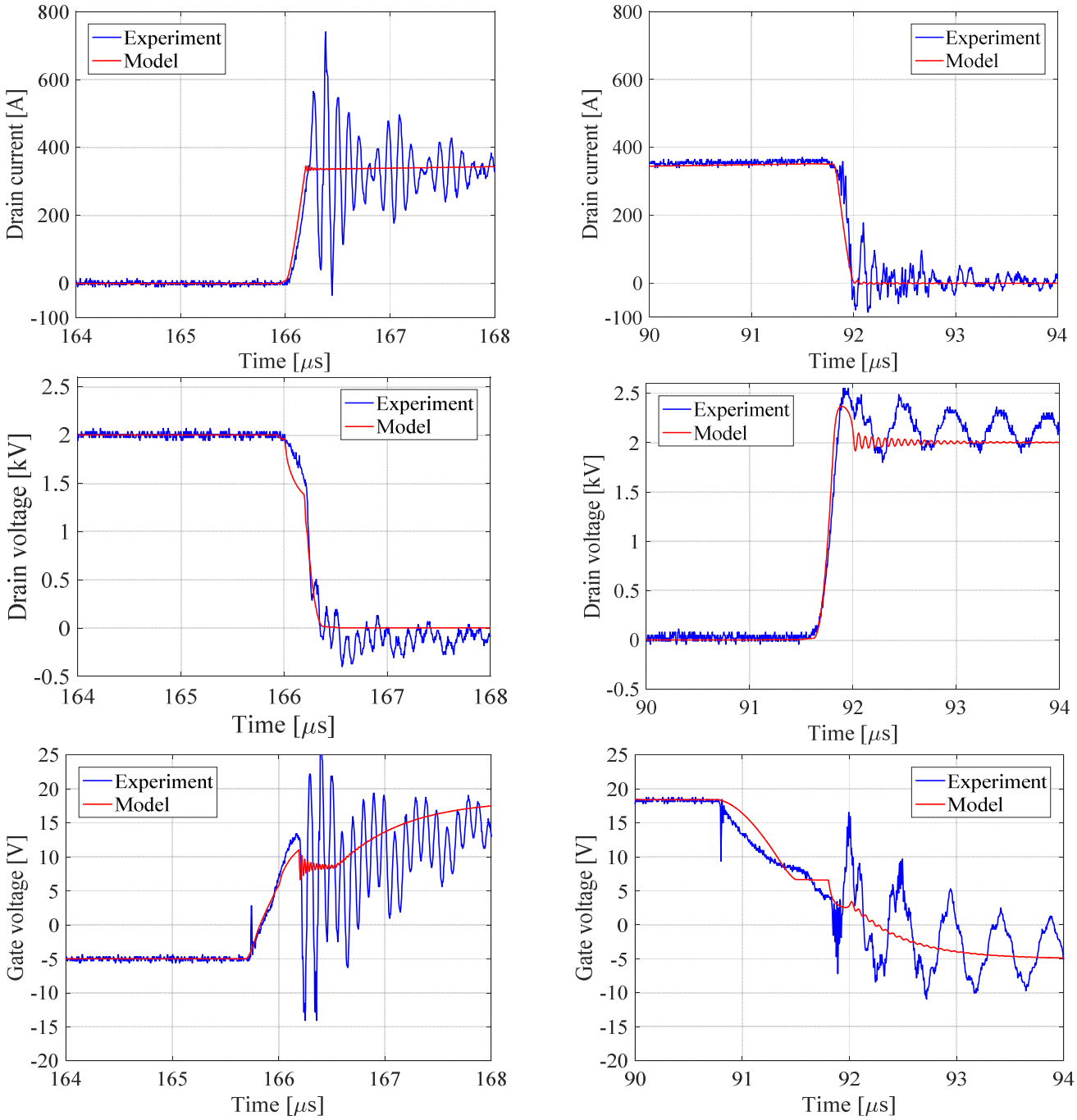



Fig.7. Experimental and simulated turn on (left) and turn off (right) waveforms for a 3.3kV SiC MOSFET at $V_{ds}$= 2.0 kV, $I_d$=350 A and $V_{gs}$=–5 to 20 V

simulation. The observed oscillations in the experimental data probably come from the stray elements of the experimental setup associated to close proximity of gate–voltage probe, Rogowski current sensing coil and high voltage probe in the test setup.

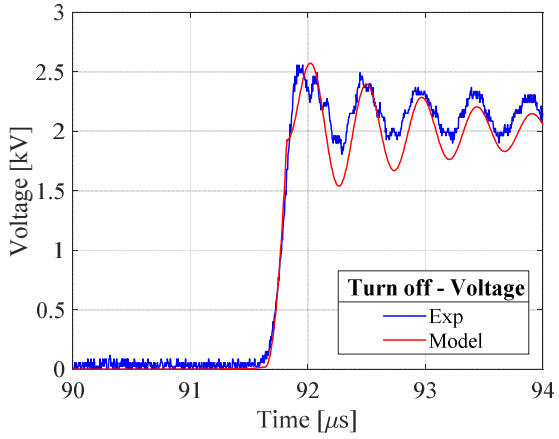
By inserting a small stray capacitor in parallel with the stray inductance ($L_{stray}$) in Fig. 2, the voltage turn–off oscillations are reproduced by the model and presented in Fig. 8. The stray inductance is 180 nH, whereas the capacitance is 30.5 nF. The frequency of the oscillations from the experiment is 2.17 MHz, and the model results in a resonant frequency of 2.15 MHz, using equation (6). With this adjustment, the model turn–off losses increase to 111 mJ, reducing fairly the difference with the experiment data. Similarly, gate oscillations are introduced by inserting extra small stray inductances ($L_{s1}$ = 3 nH, $L_{s2}$ = 1.5 nH, and $L_{s3}$ = 40 nH) in parallel with the stray capacitance (30 nF) in the gate–emitter loop, thus verifying the appearance of gate oscillations in the experimental data as illustrated in Fig. 8b. The modified schematic is shown in Fig. 8c.

$$f = \frac{1}{2\pi\sqrt{L_{stray}C_{stay}}} \tag{6}$$

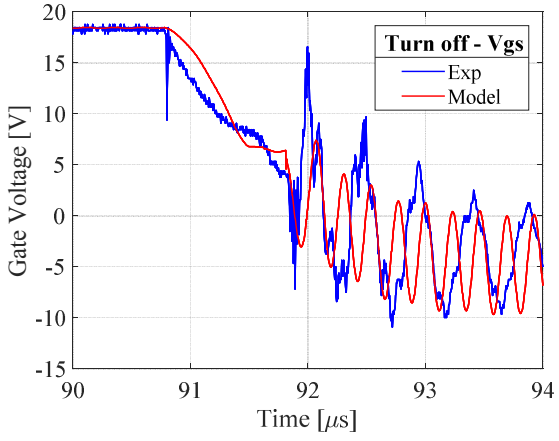
The impact of different gate resistors and temperature in the dynamic behavior of the model was tested separately. The influence of gate resistance is illustrated in Fig. 9. Resistor values of 6.0 Ω, 10.0 Ω, 15.0 Ω, 20.0 Ω and 27.0 Ω were investigated both in experiments and simulations. The turn on and off energy losses show a quasi–linear increasing trend as $R_g$ becomes larger, because of the drain current and voltage

require more time for switching and the area for the switching losses increases. The model predicts accurately this analytical trend, with a relatively small error margin. It is important to note, that the total energy loss with $R_g$ = 27.0 Ω is 3 times higher than the total energy loss with $R_g$ = 6.0 Ω. The switching waveforms are presented in Fig. 10, showing the impact of the gate resistor on the transient behavior of the module. As the value of the gate resistor is low, the switching is fast and the dv/dt and di/dt get large values. For higher values of gate resistors, the voltage and current rates decrease, and the oscillations are reduced resulting to lower overshoots.

The switching energy loss for different temperatures is presented in Fig. 11. The operating temperature increases from 300 K to 425 K with a constant step of 25 K. Due to the higher temperature, the threshold voltage decreases, producing a time shifting for the waveforms, where the turn–on happens earlier and the turn–off later for higher temperatures [4]. Overall, analytical trend is quite consistent with the experimental data indicating a slight increase in the switching energy loss with variation of temperature. However, the slopes of the drain current and voltage during turn on/off are not significantly affected by the temperature.



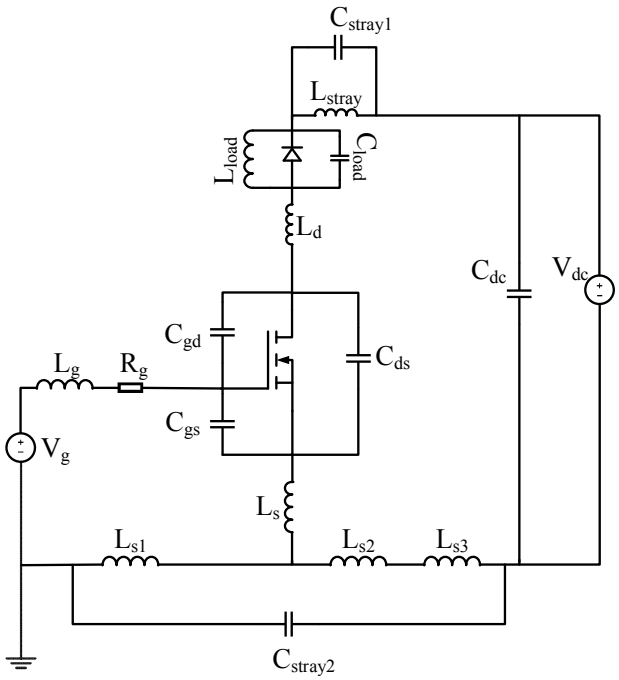

(a)




(b)

## IV. Stray Inductances

One important circuit parameter is the stray inductance that induces unwanted stress on the operational behavior of switches as a result of fast transient in the loop. For example, an overvoltage during fast transient with a given gate drivability (e.g., $R_g$) between the source-drain terminals may lead the device outside of its safe operating area. The model predictability is investigated here with varying overall loop inductance in the circuit. Figure 12 illustrates the energy dependency of the system with the overall stray inductance in the system. The turn on losses decrease around 51.8 % as the stray inductance increases, while the turn off losses increase 53 %. Moreover, the total switching losses of the circuit seem to remain almost constant, with a slight increase of 4 mJ. The turn on losses reduce, because of the faster drop of the drain voltage, whereas the turn off losses rises due to the larger turn off voltage overshoot.




(c)

Fig.8. (a)Turn–off volatage with introduction of oscillations in model by inserting a small stray capacitor in parallel with the stray inductance, (b) Turn–off gate bias with oscillations, by inserting stray inductances and capacitor in source terminal, and (c) schematic with all the parasitic elements.

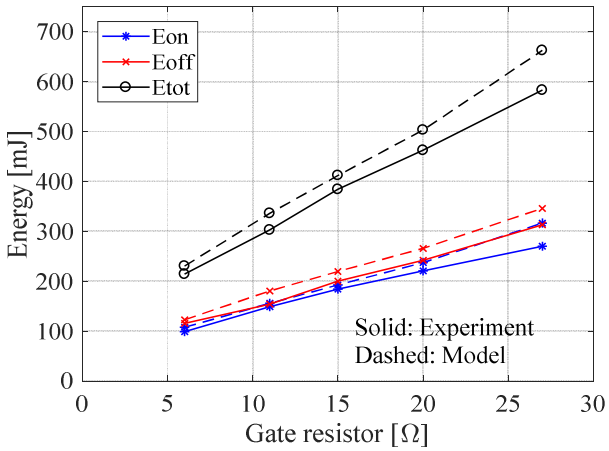



Fig.9. Energy losses for different gate resistors at 2.0 kV and 350 A.

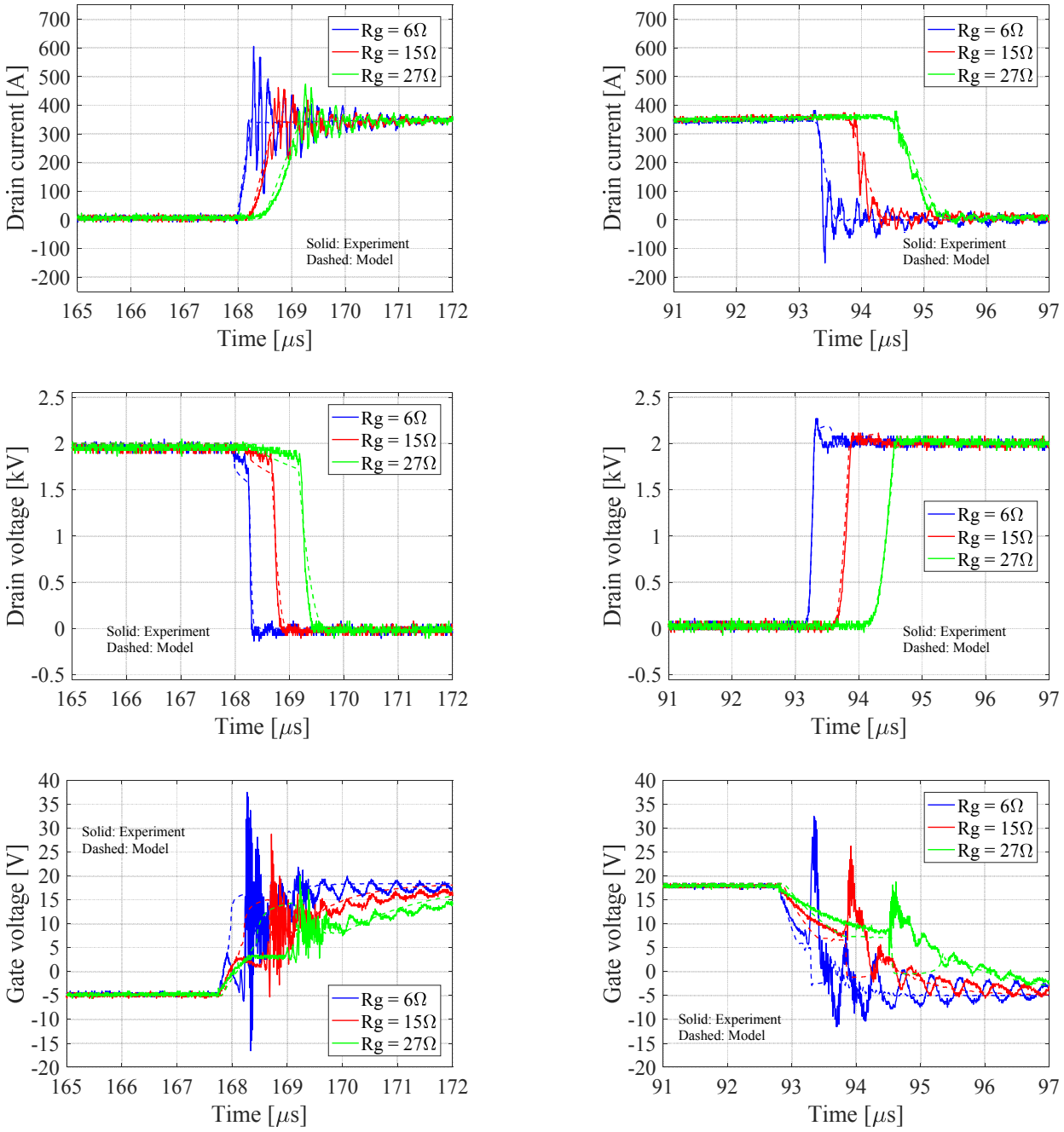



Fig.10. Experimental and simulated turn on (left) and turn off (right) waveforms for a 3.3kV SiC MOSFET at gate resistors 6, 16, and 27 Ω.

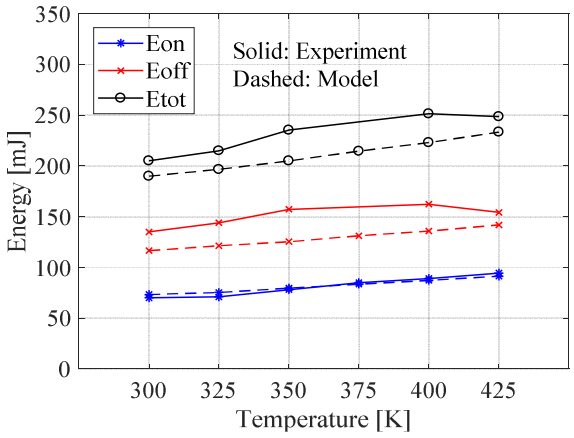



Fig.11. Energy losses for different temperatures at 2.0 kV and 350 A.

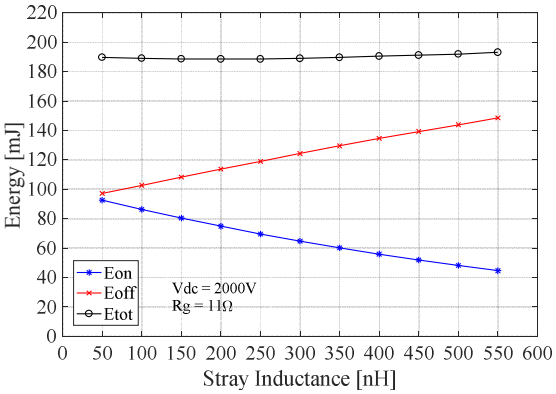



Fig.12. Energy losses as a function of stray inductances at a supply voltage of 2000 V

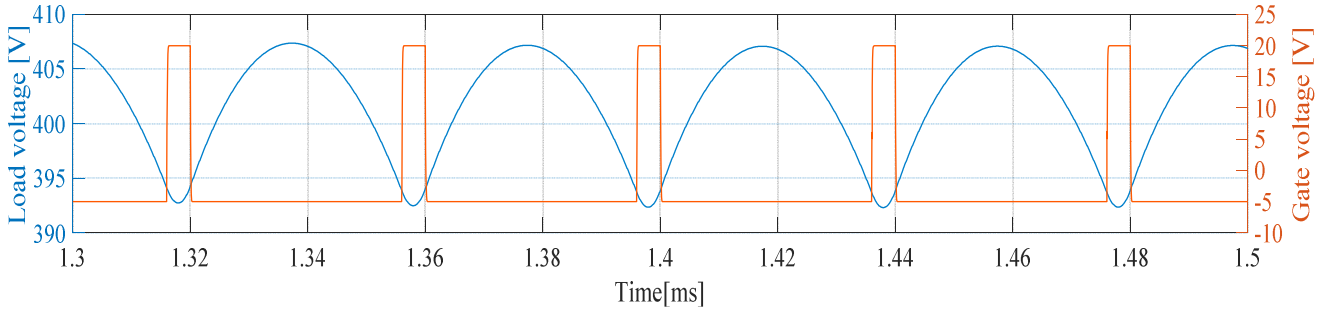



Fig.13. Buck converter output voltage and gate voltage with an input voltage of 4.0 kV.

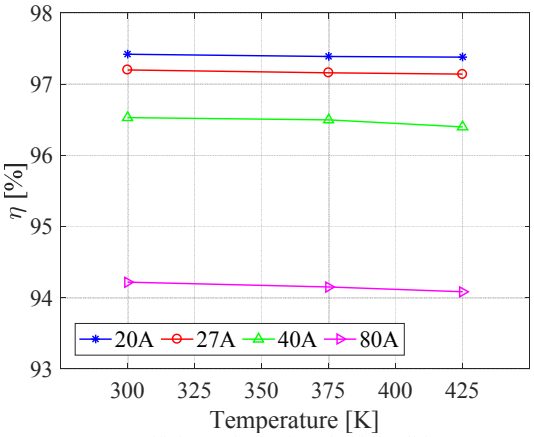



Fig.14. Converter efficiency for various load conditions (20, 27, 40, 80 A).

## V. Buck Converter

The model was finally evaluated through a buck converter topology. Two SiC MOSFET modules are connected in series to increase the complexity of the system. The input voltage is $V_{in}$ = 4 kV, the duty cycle is $D$ = 10 %, the switching frequency is 25 kHz, and the load resistor is 20 Ω. The output voltage ($V_o$) for this converter is 400 V, given by (7).

$$V_o = DV_{in} \tag{7}$$

Fig. 13 illustrates the continuous conduction mode (CCM) operation of the designed converter, showing the well modulation performance of the model. It should be mentioned that it is not the scope of the work to develop an ideal buck converter here, but it merely reflects the validity of the model to support such converter design. For this reason, the output voltage presents ripples, according to the values of the system's inductor (L = 1 mH) and capacitor (C = 5 µF), resulting in a 4% current and voltage ripple. The average voltage output is 401.8 V, as it was initially designed. The efficiency of the converter is mainly defined by the high diode losses, whereas both the conduction and the switching losses of the model are low, as expected. The efficiency of the converter with various loads and several junction temperatures, is plotted in Fig. 14. The temperature affects the two SiC MOSFET in series, as the diode model was not temperature adjustable. The result is according to the analysis in the dynamic behavior. Both the on–resistance and switching losses (Fig. 11) are slightly increased in elevated temperatures, showing a small degradation in the system's efficiency.

## VI. Conclusions

In this work, a simple and accurate Simulink based modeling platform for 3.3 kV, 400 A SiC MOSFET module is developed for the first time. The model has been verified with extensive static and dynamic characteristics where a fair agreement has been obtained under various test conditions (i.e., temperatures, gate resistances, stray inductances, supply voltages, load current etc.,). With the present model, a complete buck converter design with two devices in series was built and evaluated. The developed model presented here will provide a useful input support tool not only to design various power converters but also to predict the analytical energy loss trend for various topologies in high power applications.

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