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# **A Lumped-Charge Approach Based Physical SPICE-Model for High Power Soft-Punch Through IGBT**

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**Abstract**—This paper presents a new lumped-charge approach based physical model for high power soft-punch through (SPT) IGBT. IGBT physical models should consider the fabrication technologies used to optimize the device behaviour for specific applications. The proposed model focuses on the chip structure designed by ABB for high power IGBT and can apply to other IGBTs with homogeneous structures. Based on the SPT+ concept combined with an enhanced planar cell design for the optimization of lower power losses, different particular mathematical approaches are used to describe their functions in the proposed model. The temperature dependence of the model is also included because the chip temperature of IGBT in practical applications is higher than the room temperature and changed with service conditions. The physics-based IGBT model has been implemented in PSpice and validated with experiments, which considers both the block voltage non-punch through (NPT) condition and punch through (PT) condition during turn-off transient. The simulation results show a good agreement with the experiment results.

**Index Terms**—Insulated gate bipolar transistor (IGBT), soft punch through (SPT), enhanced planar, lumped-charge model, physical model.

NOMENCLATURE

$A$	Device active area [cm <sup>2</sup> ]	$q_{pi}$	The lumped charge at node $i$ [C/cm <sup>2</sup> ]
$A_{gd}$	Gate–drain overlap area [cm <sup>2</sup> ]	$p_i$	The hole concentration at node $i$ [C/cm <sup>3</sup> ]
$C_{bj}$	Junction capacitance of the collector PN junction [F]	$Q_{p,SPT}$	The hole charge in the SPT layer [C]
$C_{bd}$	diffusion capacitance of the collector PN junction [F]	$Q_{p,N-}$	The hole charge in the N- region [C]
$C_{oxd}$	Gate–drain overlap capacitance [F]	$T$	Temperature [K]
$C_{ds}$	Drain–source capacitance [F]	$T_{nom}$	Nominal temperature [K]
$d$	The width of the undepleted region of N- region [cm]	$V_{j1}$	The voltage drop across the PN junction [V]
$d_{SPT}$	The width of the undepleted region of SPT layer [cm]	$V_{ji}$	The voltage drop between node $j$ and $i$ [V]
$I_C$	Collector current [A]	$V_T$	Thermal voltage [V]
$i_{CONT,i}$	recombination current at node $i$ [A]	$V_{th}$	The MOSFET threshold voltage [V]
$i_{p,ij}$	Hole current from node $i$ to node $j$ [A]	$V_{lim}$	The critical voltage [V]
$i_{n,ij}$	Electron current from node $i$ to node $j$ [A]	$V_{ds}$	The MOSFET drain-source voltage [V]
$i_{p,5o}$	The hole current following out of the P+ emitter [A]	$V_{dg}$	The MOSFET drain-gate voltage [V]
$J_{sne}$	Reverse saturation electron current density [A/ cm <sup>2</sup> ]	$V_{dep}$	The voltage generator of the model [V]
$J_{snh}$	Reverse saturation hole current density [A/ cm <sup>2</sup> ]	$w_B$	The width of the base region [cm]
$K_P$	Transconductance parameter [A/ V <sup>2</sup> ]	$w_{SPT}$	The width of the SPT layer [cm]
$n_i$	Intrinsic carrier concentration [cm <sup>-3</sup> ]	$\tau_{SPT}$	Excess carrier lifetime in SPT layer [s]
$N_{SPT}$	The doping concentration of the SPT layer [cm <sup>-3</sup> ]	$\tau_B$	Excess carrier lifetime in base region [s]

$N_B$	The doping concentration of the N-region [cm <sup>-3</sup> ]	$\mu_n$	Mobility of holes [cm <sup>2</sup> /(Vs)]
$q$	Electronic charge [C]	$\mu_p$	Mobility of Electrons [cm <sup>2</sup> /(Vs)]

## I. INTRODUCTION

Insulated Gate Bipolar Transistor (IGBT) power modules are the most widely used as well as the most critical switching power semiconductor devices in power electronic systems in the high-power range [1]. For the design and analysis of power electronic converters, a good IGBT circuit model could help device manufacturers and circuit designers to study, simulate, and predict the behavior of the devices and converters. However, the simulation accuracy significantly depends on the IGBT models. Generally, the IGBT models could be classified as the behavior model and the physical model [2]. When the simulation is devoted to analyzing the device transient behaviour and power losses in the circuit or doing the design of reliability, the ideal switches and behavior models are not sufficient and must be substituted by suitable physical models [3, 4]. The physical model based on semiconductor physics could not only provide a better simulation accuracy but also give an insight of the internal behavior of IGBT.

Physical modeling of a specific IGBT, firstly, should consider the fabrication technologies used to optimize the device behavior for particular applications. For the SPT-IGBT and other IGBTs with similar structures, the soft-punch through (SPT) or “field-stop” layer shown in Fig. 1 is used to reduce the thickness and conduction losses of the chip [5].

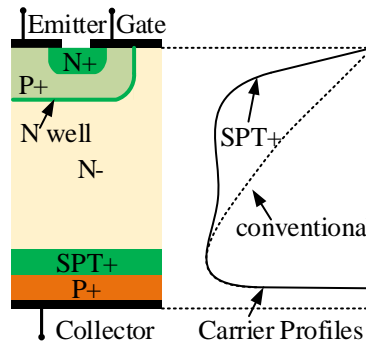


Fig. 1. SPT+ planar IGBT enhanced carrier profile compared to the conventional IGBT.

In recent years, many physics-based IGBT models with or without SPT layer have been presented in [6-17]. In [6-8], Patrick R. Palmer *et al.* proposed a Fourier based solution for the ambipolar diffusion equation and established a series of IGBT models. However, these models can only be used in high-level injection condition, and because of the Fourier transform, parameters in the base region are no longer with practical physical significance. The lumped-charge model could

be used both in high-level and low-level injection, and all the parameters in the model have physical significance. In [9-14], the classical Hefner modeling method is used to establish different kinds of IGBT model. But most of them only make the description of the carrier distribution during the steady-state. In the transient state, a shape function related to carrier distribution in the base region is given to describe the distribution of carriers in different transients, such as turn-on, turn-off and short circuit. However, it's hard to use one shape function to describe different carrier distribution transient.

For this reason, in [15], M. Cotorogea proposes a new Hefner model to improve the model accuracy. In the new model, the base region of IGBT is divided into three parts, and three different shape functions are presented to describe the carrier distribution in each area. Although the accuracy of the model is improved, it becomes too complicated to implanted in circuit simulation. However, the lumped-charge model doesn't need to solve the ambipolar diffusion equation and can be used to characterize the distribution of carriers under different conditions.

For the high power IGBT, there will be an apparent difference between the NPT transient and the PT transient on the turn-off behavior. Fig. 2 illustrates the difference in the experiment results of an ABB 3.3kV/1500A SPT-IGBT. At the PT turn-off transient, the tail current shows a snap-off behavior which may cause circuit oscillation. Moreover, the transient characteristics are essential for IGBT applications, so research on it is vital. However, there is no discussion about this question in the above literature.

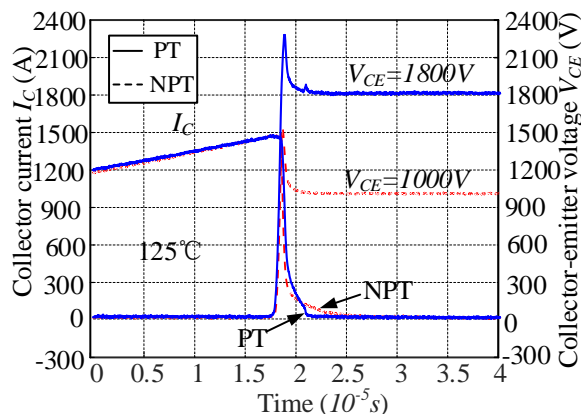


Fig. 2. IGBT block voltage non-punch through (NPT) condition compared to punch through (PT) condition at turn-off transient.

On the other hand, the SPT-IGBT of ABB uses the planar gate technology with an N-well (the enhancement layer) to improve the carrier profile compared to the conventional planar IGBT (see Fig. 1). Thus, the charge of the carrier in the base region increased significantly. Due to the conductivity modulation effect, the IGBT can obtain lower forward drop and guarantee the block voltage without using the trench gate technology. This kind of carrier distribution also known as the carrier concentration enhanced effect. For the physical modeling of IGBT, it's always a challenge to model them in the

transient process. In [15, 16], the enhanced effect is discussed, but it is only modeled in the on-state model. And for the transient analysis, a four-order polynomial shape function is used to describe the carrier distribution. Because the model is established to analyze the relationship between  $di_C/dt$  during turn off and other parameters, this kind of shape function can satisfy the requirements. For the quantitative characterization of electrical characteristics under different conditions, this model has the same problems with other shape function models as discussed above.

This paper presents a new lumped-charge physical model for high power SPT-IGBT considering the SPT concept combined with an enhanced planar cell both in the on-state and transient model. The IGBT model is divided into a bipolar part model and a unipolar part model. The temperature dependence of the model is also included. Finally, the model has been implemented in the PSpice circuit simulator and been validated with experiments by an ABB 3.3kV/1500A SPT-IGBT under both the block voltage non-punch through (NPT) condition and punch through (PT) condition at the turn-off transient with different collector current.

## II. THE LUMPED-CHARGE IGBT MODEL

The history of IGBT physical modeling is as long as forty years, and a lot of physics-based models have been proposed [2]. Most of the physical models are based on the high-level injection hypothesis to solve the ambipolar diffusion equation (ADE) proposed by Hefner. These models can only give a specific distribution (linear or polynomial) to the carriers. However, the carriers have different distributions in different operation mode [15]. Especially, when it comes to the SPT or Field-stop layer, the high-level injection hypothesis is not suitable all the time [14]. Besides, since the low-level injection in the N-base region is not modeled, these models cannot get a good simulation result to the conductivity modulation process during the switching transient.

Compared with other IGBT physical models, the lumped-charge approach doesn't need to solve the ADE in the drift region [18]. In this model, the current transport equation and the carrier continuity equation are expressed respectively in the lumped-charge form. This feature allows us to separately consider the roles of hole's and electron's currents in the base region of IGBT, and avoid the high-level injection approximations. Besides, the lumped-charge model represents a good tradeoff between accuracy and simplicity, and more suitable for being implemented into circuit simulation platforms [18]. Therefore, in this paper, we use the lumped-charge modelling method to establish the model of high power SPT-IGBT.

### A. The structure of the SPT-IGBT

Physical modeling of IGBTs should base on specific chip structure, and different chip structures result in different behaviors. From the view of the current path, IGBT can be seen as a PNP-BJT paralleled with a MOSFET, and the BJT base

current controlled by the gate of the MOSFET part. Fig. 1 shows the chip structure of SPT-IGBT and the detailed introduction of it are reported in [5]. As discussed above, the SPT layer is used to reduce the thickness of the chip and conduction losses. The planar gate technology with an N-well (the enhancement layer) under the P-well is used to improve the carrier profile.

### B. The bipolar part of the model

The bipolar part model of the IGBT describes the behavior of the excess carriers injected into the drift region including the PN junction. In this section, we are going to establish the model of SPT layer, N-base region, and the N-well. First of all, we need to clarify the assumptions of the model and build the coordinate system required by the model.

#### 1) The assumptions of the model

Fig. 3 (the solid line) schematically shows the bipolar part doping concentration of the IGBT. During the modeling process, we use the dashed line to simulate the actual doping concentration. So, the doping is uniform in each region. Based on the assumption, all the semiconductor junctions are abrupt junctions. The bipolar part model in this paper consists of a PN junction model supplying the electron current at the collector of the IGBT ( $x=0$ ), the models describing the carrier behavior in SPT layer and the N-base region. According to the principle of the lumped-charge approach [18], two nodes (node 2 and 3h) are put in the SPT layer, and three nodes (node 3l, 4 and 5) are placed in the N-base region.

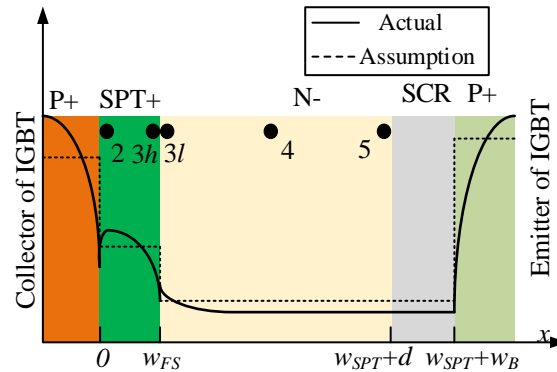


Fig. 3. Coordinate system used to develop the bipolar part model.

#### 2) The model of the SPT layer

The PN junction model at the collector of the IGBT describes the recombination current  $i_{CONT,2}$  in the P+ collector. According to the PN junction model,

$$i_{CONT,2} = A \cdot J_{sne} \left[ \exp\left(\frac{V_{j1}}{V_T}\right) - 1 \right] + (C_{bd} + C_{bj}) \frac{dV_{j1}}{dt}, \quad (1)$$

where  $A$  is the active device area of IGBT,  $J_{sne}$  is the reverse saturation electron current density,  $V_{ji}$  is the voltage drop across the PN junction and  $V_T$  is the thermal voltage,  $C_{bd}$  and  $C_{bj}$  are the diffusion capacitance and junction capacitance separately.

The inject current contributes to the injection of holes at the edge of the junction ( $x=0$ ) in the SPT layer. Thus,

$$q_{p2} = \begin{cases} (qAn_i \sqrt{\frac{i_{CONT,2}}{A \cdot J_{sne}}} + qA \frac{n_i^2}{N_{SPT}}), & (i_{CONT,2} \geq 0) \\ qA \frac{n_i^2}{N_{SPT}} & , \quad (i_{CONT,2} < 0) \end{cases} \quad (2)$$

where  $q_{p2}=qAp_2$ ,  $p_2$  is the hole concentration at node 2,  $N_{SPT}$  is the doping concentration of the SPT layer.

Due to the width of SPT layer is very small, and the distribution of the carrier in this region could be seen as linear [16].

Based on this assumption, the hole current  $i_{p,23}$  and the electron current  $i_{n,23}$  following from node 2 to node 3h are given as

$$\begin{cases} i_{p,23} = \frac{q_{p2} - q_{p3}}{T_{p23}} + \frac{q_{p3h} V_{23}}{T_{p23} V_T} \\ i_{n,23} = \frac{q_{p2} - q_{p3}}{T_{n23}} + \frac{q_{p3h} + q_{SPT}}{T_{n23}} \frac{V_{23}}{V_T} \end{cases} \quad (3)$$

where  $q_{SPT}=qAN_{SPT}$ ,  $N_{SPT}$  is the doping concentration of SPT layer.  $V_{23}$  is the voltage drop between node 2 and 3h,  $T_{p23}$  is the hole transit time and  $T_{n23}$  is the electron transit time between nodes.

The recombination current  $i_{CONT,3}$  is result from the charge of excess carrier  $Q_{p,SPT}$  in the SPT layer. According to the linear assumption of the carrier distribution,

$$Q_{p,SPT} = \frac{1}{2}(q_{p2} + q_{p3h} - 2q_{p,SPT}) \cdot d_{SPT} \quad , \quad (4)$$

where  $d_{SPT}$  is the width of the undepleted region in the SPT layer,  $q_{p,SPT}=qAn_i^2/N_{SPT}$ . Then, base on the charge control equation,  $i_{CONT,3}$  could be given as

$$i_{CONT,3} = \frac{dQ_{p,SPT}}{dt} + \frac{Q_{p,SPT}}{\tau_{SPT}} \quad , \quad (5)$$

where  $\tau_{SPT}$  is the average excess carrier lifetime in the SPT layer.

### 3) The model of the N-base region

The hole current following out of the SPT layer equals the hole current following into the N- base region. Thus,

$$i_{CONT,3} = i_{p,23} - i_{p,34} \quad , \quad (6)$$



where,  $i_{p,34}$  is the hole current flowing from node 3l to node 4.

Using the quasi-equilibrium simplification at the boundary of SPT layer and the N- base region,

$$q_{p3h}(q_{p3h} + q_{SPT}) = q_{p3l}(q_{p3h} + q_{N-}), \quad (7)$$

where  $q_{N-} = qA N_{N-}$ ,  $N_{N-}$ , is the doping concentration of the N- base region.

The hole current  $i_{p,34}$  and the electron current  $i_{n,34}$  following from node 3l to node 4 are given as

$$\begin{cases} i_{p,34} = \frac{q_{p3l} - q_{p4}}{T_{p34}} + \frac{q_{p4}}{T_{p34}} \frac{V_{34}}{V_T} \\ i_{n,34} = \frac{q_{p3l} - q_{p4}}{T_{n34}} + \frac{q_{p4} + q_{N-}}{T_{n34}} \frac{V_{34}}{V_T} \end{cases}. \quad (8)$$

The recombination current  $i_{CONT,4}$  is result from the charge of excess carrier  $Q_{p4,N-}$  in the N- region. Due to the linear assumption of the carrier distribution,

$$Q_{p4,N-} = \frac{1}{2}(q_{p3l} + q_{p4} - 2q_{p,N-}) \cdot \frac{d}{2}, \quad (9)$$

$$i_{CONT,4} = \frac{dQ_{p4,N-}}{dt} + \frac{Q_{p4,N-}}{\tau_B}. \quad (10)$$

where  $d$  is the width of the undepleted region in the N- region,  $q_{p,N-} = qA n_i^2 / N_B$ ,  $N_B$  is the doping concentration of base region is the average excess carrier lifetime in the base region.

Similarly, the hole current  $i_{p,45}$  and the electron current  $i_{n,45}$  following from node 4 to node 5 are obtained by

$$\begin{cases} i_{p,45} = \frac{q_{p4} - q_{p5}}{T_{p45}} + \frac{q_{p4}}{T_{p45}} \frac{V_{45}}{V_T} \\ i_{n,45} = \frac{q_{p4} - q_{p5}}{T_{n45}} + \frac{q_{p4} + q_{N-}}{T_{n45}} \frac{V_{45}}{V_T} \end{cases}. \quad (11)$$

The recombination current  $i_{CONT,5}$  is result from the charge of excess carrier  $Q_{p5,N-}$  in the N- region. For the linear assumption of the carrier distribution from node 4 to 5,

$$Q_{p5,N-} = \frac{1}{2}(q_{p4} + q_{p5} - 2q_{p,N-}) \cdot \frac{d}{2}, \quad (12)$$

$$i_{CONT,5} = \frac{dQ_{p5,N-}}{dt} + \frac{Q_{p5,N-}}{\tau_B}. \quad (13)$$

In the conventional planar IGBT (see Fig. 1), the excess carrier concentration of node 5 could be assumed to be zero. So,  $q_{p5} = 0$ . However, in the SPT-IGBT, the structure of N-well improves the carrier profile of the base region and  $q_{p5}$  doesn't

equal zero anymore. We need to consider the influence of the N-well and give a mathematical description to the function of it.

#### 4) The model of the N-well

On static without the space charge region (SCR) in the N- region, the distribution of the carriers in it (see Fig. 1) looks like a PiN diode. Continue the previous analysis, the hole current following out of the P+ emitter is given by

$$i_{p,5o} = i_{p,45} - i_{CONT,5}. \quad (14)$$

According to the physical model of PiN diode [6],

$$i_{p,5o} = (A - A_{gd}) \cdot J_{snh} \left( \frac{q_{p5}}{q_{N-}} \right). \quad (15)$$

where  $A_{gd}$  is the active gate–drain overlap area,  $J_{snh}$  is the reverse saturation hole current density of the junction at the IGBT emitter. According to the expression of (15), this junction could be modeled as a controlled current source in the circuit simulator. The voltage drop across it is decided by the drain-source voltage ( $V_{ds}$ ) of the MOSFET which is paralleled to the current source.

However, during the switching transient, when the space charge region punches through the N-well, the hole concentration of node 5 will be swept to zero again due to the electric field in the SCR. Here, we establish the relationship between  $q_{p5}$  and  $V_{ds}$  as follow

$$q_{p5} = \begin{cases} \frac{i_{p,5o} \cdot q_{N-}}{(A - A_{gd}) \cdot J_{snh}} \cdot \frac{V_{lim} - V_{ds}}{V_{lim}}, & V_{ds} \leq V_{lim} \\ 0 & , V_{ds} > V_{lim} \end{cases}, \quad (16)$$

where  $V_{lim}$  is the critical voltage when the space charge region punches through the N-well. By this method, the carrier enhanced effect of the N-well is not only modeled in the on-state model but also the transient model for continuous circuit simulation.

#### 5) The transient model of the PT condition

When the block voltage punches through the N- region during the transient, there will be no excess carriers left in the base region. So, we need to reconsider how to deal with these lumped charges (node 3l, 4, 5 in the base region) in it and make sure the model is continuous.

According to the charge control equation (5), (9), and (12), when the block voltage non-punch through the base region,

$$i_{p,23} - i_{p,5o} = \frac{dQ_{p,SPT}}{dt} + \frac{dQ_{p,N-}}{dt} + \frac{Q_{p,SPT}}{\tau_{SPT}} + \frac{Q_{p,N-}}{\tau_B}, \quad (17)$$

where,

$$Q_{p,N-} = Q_{p4,N-} + Q_{p5,N-}. \quad (18)$$

In the case of PT condition, equation (17) cannot be used anymore. Because there is no  $Q_{N-}$  at this time. Besides,  $Q_{N-}$  cannot equal zero in order to avoid the converge problem of the model, else the nodes ( 3l, 4 and 5 ) need to be removed.

In this paper, we proposed that limit the width of the undepleted region in the N- region as a fixed value and small enough in the case of PT condition.

For the  $d$  is fixed, no carriers are swept out by the electric field in the SCR. Then,

$$\frac{dQ_{p,SPT}}{dt} \gg \frac{dQ_{p,N-}}{dt}. \quad (19)$$

And for the  $d$  is small enough and  $T_B \gg \tau_{SPT}$ ,

$$\frac{Q_{p,SPT}}{\tau_{SPT}} \gg \frac{Q_{p,N-}}{\tau_B}. \quad (20)$$

So, the approximation as bellow can obtained in the case of PT condition.

$$i_{p,23} - i_{p,5o} \approx \frac{dQ_{p,SPT}}{dt} + \frac{Q_{p,SPT}}{\tau_{SPT}}. \quad (21)$$

Then, equation (17) can be used to model the PT condition without remove the nodes 3l, 4 and 5.

### C. The MOSFET part of the model

The MOSFET part of the IGBT model supplies the electron current to the bipolar part and can control the turn-on and turn-off of the device by the gate voltage. In this paper, an advanced level-3 MOSFET model in PSpice has been used to describe the unipolar structure of SPT-IGBT. The static characteristic is given as follow

$$I_{MOS} = \begin{cases} 0 & (V_{gs} < V_{th}) \\ K_p [(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2] & (V_{gs} - V_{th} \geq V_{ds}) \\ \frac{K_p}{2}(V_{gs} - V_{th})^2 & (V_{gs} - V_{th} < V_{ds}) \end{cases}. \quad (22)$$

For the dynamic behavior of the MOSFET, a series voltage-controlled generator on the capacitance  $C_{oxd}$  is build to present the nonlinear behavior of the capacitance in depletion conditions, and the source capacitance  $C_{gs}$  is considered as constant. The drain-source capacitance  $C_{ds}$  is set as zero due to the displacement current in it is much smaller compared to the rated current of the high power IGBT.

Here, we can get the lumped-charge model of the SPT-IGBT as illustrated in Fig. 4. The voltage generator  $V_{dep}$  (Fig. 4) is

determined by a controlled voltage source defined as

$$V_{dep} = \begin{cases} V_{dg} + V_n \left(1 - \sqrt{1 + \frac{2V_{dg}}{V_n}}\right), \\ 0 \end{cases} \quad (23)$$

Where,  $V_{dg}$  is intrinsic gate-drain voltage, and  $V_n$  is a normalization factor mainly dependent on the gate–drain overlap area and doping concentration of base region.

#### D. The temperature dependence of the model

Due to the characteristics of IGBT are influenced by temperature. Physical modeling of IGBT should also describe the temperature properties. The primary temperature dependent models of IGBT used in this paper are listed as follow.

1) The Electron and Hole mobility: the mobility of carriers related to temperature and doping concentration, the model of them defined as

$$\mu_p = 54.3 \cdot (T/300)^{-0.57} + \frac{407 \cdot (T/300)^{-2.33}}{\left(1 + \frac{N_B}{2.35 \times 10^{17} \cdot (T/300)^{2.4}}\right)^\alpha}, \quad (24)$$

$$\mu_n = 88 \cdot (T/300)^{-0.57} + \frac{1252 \cdot (T/300)^{-2.33}}{\left(1 + \frac{N_B}{1.26 \times 10^{17} \cdot (T/300)^{2.4}}\right)^\alpha}, \quad (25)$$

where,  $\alpha = 0.88(T/300)^{-0.146}$ .

2) Carrier lifetime: The hole lifetime  $\tau_{SPT}$  and  $\tau_B$  is given as

$$\tau_{SPT}(T) = \tau_{SPT}(T_{nom})(T / T_{nom})^{1.5}, \quad (26)$$

$$\tau_B(T) = \tau_B(T_{nom})(T / T_{nom})^{1.7}. \quad (27)$$

3) Transconductance parameter: the forward voltage drop in n- channel of the MOS is decided by  $K_p$ , and

$$K_p(T) = K_p(T_{nom})(T / T_{nom})^{-0.8}. \quad (28)$$

4) Channel threshold voltage of the gate

$$V_{th}(T) = V_{th}(T_{nom}) - 1.27 \times 10^{-2}(T - T_{nom}). \quad (29)$$

### III. MODEL IMPLEMENTATION AND VALIDATION

#### A. Model implementation

For circuit simulation of power semiconductor devices, PSpice is one of the mostly used simulators nowadays. The lumped-charge SPT-IGBT model discussed in the previous sections has been transferred into the form of an equivalent circuit (see Fig. 4) and implemented in PSpice circuit simulator. Then, the model has been validated with experiments with both static and transient characteristics.

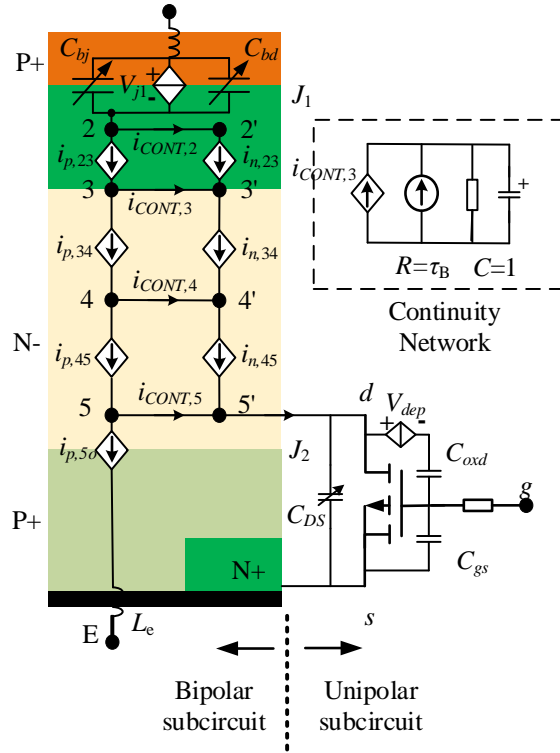


Fig. 4. The lumped-charge model of the SPT-IGBT.

#### B. Parameter extraction

The parameters extraction process of the lumped-charge model proposed in this paper consists of two steps. The first step is the evaluation of the parameters based on the datasheet information and/or switching characteristics, including device structural parameters and circuit parasitic parameters. In the wake of the development of physics-based models, some literature has proposed a series of model parameters extraction methods [18-20]. However, these methods are only suitable for initial parameter estimation.

Then, the second step is using the user-friendly Graphical User Interface (GUI) software MBPI (Model Based Parameter Identifier) presented in [21] to do the optimization of parameters extracted in the first step. Through the optimization, the performance of the physical model will be further improved. The detailed information of the parameter extraction for PSpice

models is discussed in [21].

### C. Model validation

The accuracy of the lumped-charge model for high power SPT-IGBT is proved by experiments of an ABB 3.3kV/1500A. Experimental data have been obtained using a LEMSYS device analyzer for both the static characterization and dynamic characterization. In the way of system integration, the LEMSYS device tester integrates the device test platform, the device protection platform and the power signal measurement platform together, which can control parasitic parameters of the experimental equipment. Thus, the dynamic performance test of high power IGBT under large current application could be efficiently realized.

For the dynamic test, the base plate of the power module is heated to 125°C which is a normal service condition of the device, and then the double-pulse experiment is carried out. The gate voltage  $V_{GE}=15V$ , turn-on gate resistance  $R_{gon}=1.2\Omega$ , turn-off gate resistance  $R_{goff}=3.5\Omega$ .

#### 1) Static characteristics

The developed lumped-charge model has been implemented in PSpice simulator with a user-defined device library. Firstly, use the DC analysis of PSpice to get steady state condition of the model with different temperature and gate voltage. Then, use a LEMSYS device analyzer to obtain the experimental data. It allows you to monitor in the time domain the actual pulsed voltage and current waveforms being applied to the DUT at any point along a measurement curve and the self-heating of the semiconductor could be ignored. The LEMSYS device analyzer gives IGBT current according to a certain step length. When the current reaches the saturation voltage of IGBT at a specific gate voltage,  $V_{ce}$  will be increased rapidly. To protect the IGBT chip, the device analyzer will stop the test. And, from the stop point,  $V_{ce}$  increases with an almost fixed current and IGBT enters the saturated state.

The simulation results compared to the experimental results is shown in Fig. 5. Fig. 5(a) shows the comparison at 25°C and 125°C with gate voltage equals 15 V. Fig. 5(b) shows the comparison at 125°C with different gate voltage. The simulation results are in good agreement with the measured curves, verifying the good quality of the physics-based model for the static characteristics.

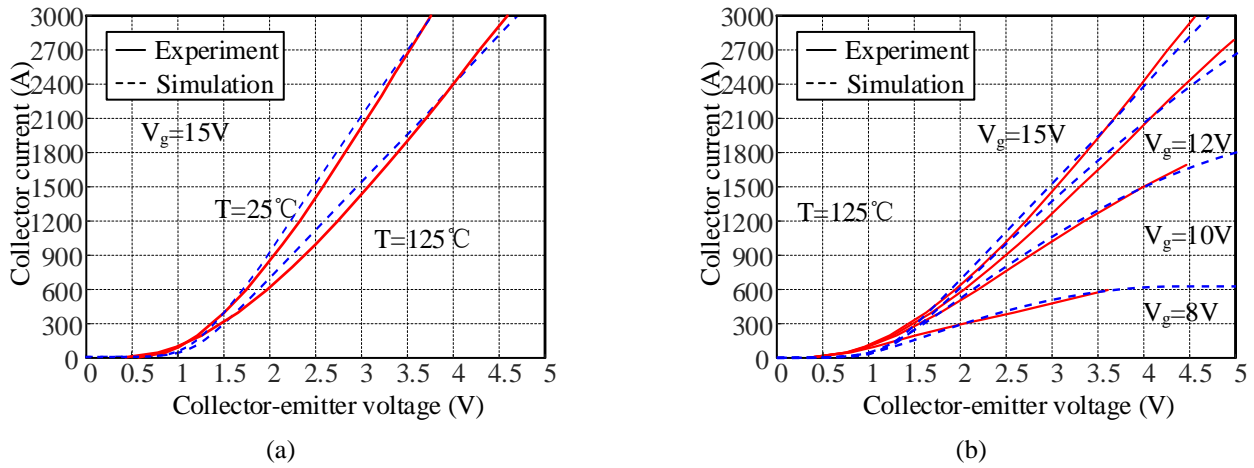
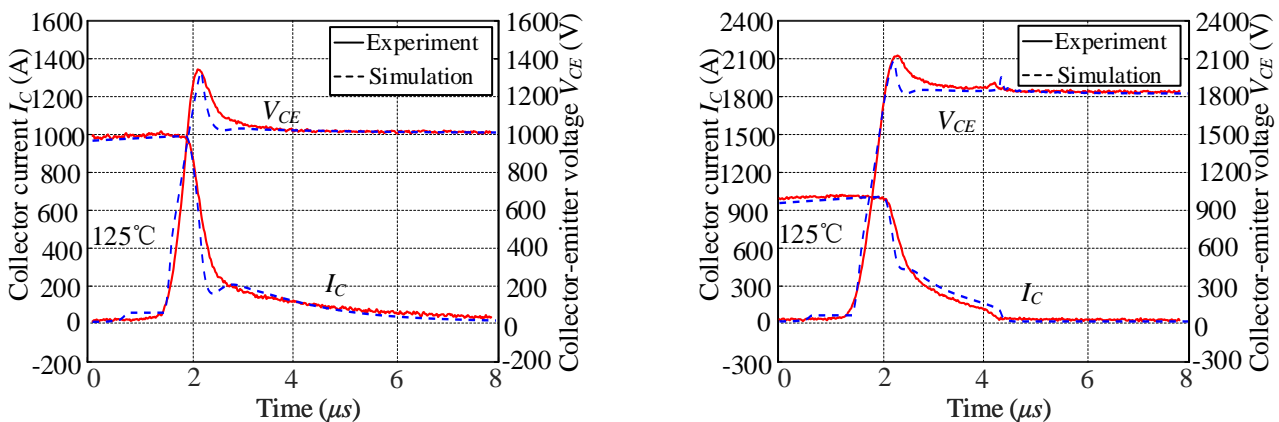


Fig. 5. Comparison between experiment and simulation on static: (a) Static characteristics of IGBT at  $25^{\circ}\text{C}$  and  $125^{\circ}\text{C}$ ; (b) Static characteristics of IGBT under different gate voltage at  $125^{\circ}\text{C}$ .

## 2) Transient characteristics

As we know, IGBT power module comprises two active parts, the IGBT chip and the antiparallel FWD (Fly-Wheel Diode) chip. During the turn-on transient, the switching behavior of the IGBT module is greatly influenced by the FWD, especially for the reverse recovery current, but the turn-off characteristics are mainly depending on the IGBT chip. So, the turn-off transient is firstly used to verify the accuracy of the proposed SPT-IGBT chip model in this paper.

To verify both the NPT and PT condition, we set the block voltage as 1000V (NPT) and 1800V (PT) respectively. Using the proposed model, establish a double pulse tester same with the experiment setup in PSpice and do the AC transient analysis. Comparison results between the experiment and simulation are illustrated in Fig. 6 with three kinds of different collector current (1000 A, 1500 A, 2000 A). 1500 A is the rated current, 1000 A is for the condition smaller than the rated current, 2000 A is for the condition larger than it. Fig. 6(a), Fig. 6(c), and Fig. 6(e) show the NPT condition at  $125^{\circ}\text{C}$ . Fig. 6(b), Fig. 6(d), and Fig. 6(f) indicate the PT condition at  $125^{\circ}\text{C}$ . Simulation results prove that the proposed model in this paper can not only model the NPT condition but also give a precise description of the PT condition.



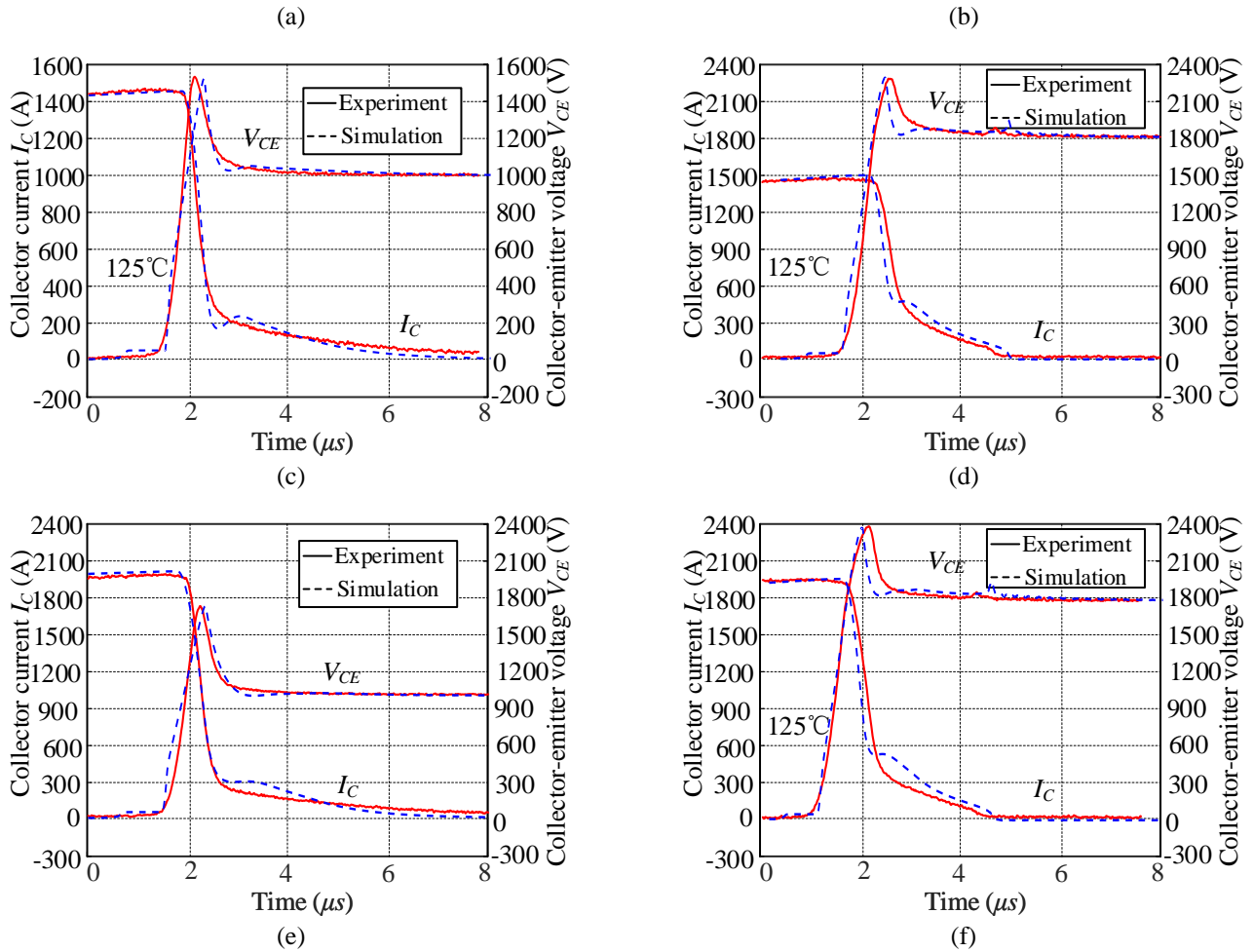


Fig. 6. Comparison between experiment and simulation on turn-off transient at 125°C: (a) NPT condition ( $V_{DC}=1000V$ ,  $I_C=1000A$ ); (b) PT condition ( $V_{DC}=1800V$ ,  $I_C=1000A$ ); (c) NPT condition ( $V_{DC}=1000V$ ,  $I_C=1500A$ ); (d) PT condition ( $V_{DC}=1800V$ ,  $I_C=1500A$ ); (e) NPT condition ( $V_{DC}=1000V$ ,  $I_C=2000A$ ); (f) PT condition ( $V_{DC}=1800V$ ,  $I_C=2000A$ ).

To verify the turn-on transient of the SPT-IGBT and give a full validation of the IGBT model, a lumped-charge PiN diode model presented in [22] is also established in PSpice, and used to do co-simulation with the IGBT model proposed in this paper. For the turn-on transient, there is no apparent difference between NPT condition and PT condition. So, in this paper, only the turn-on curves at 1800V DC voltage condition are illustrated. Fig. 6 shows the comparison results between the experiment and simulation at a different temperature.



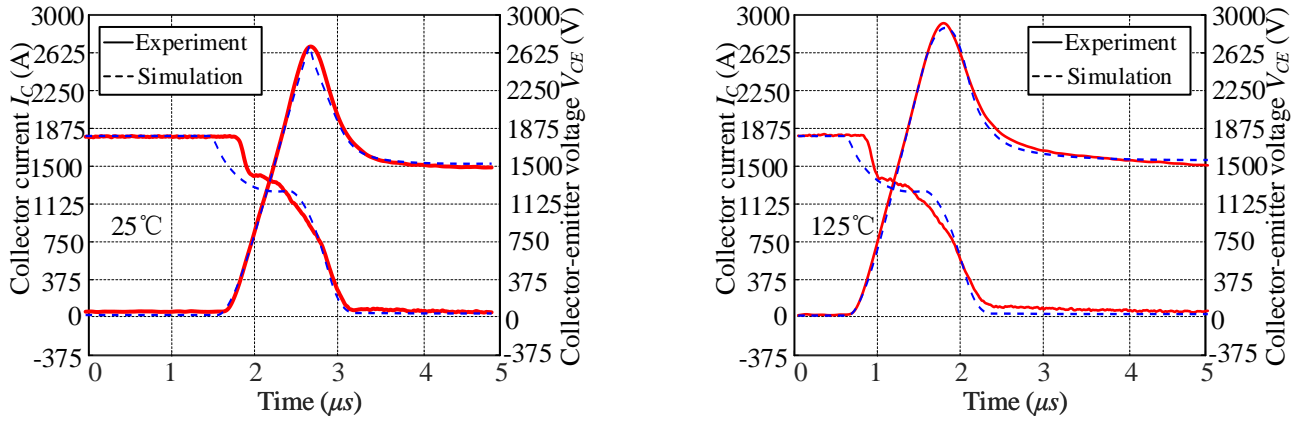


Fig. 7. Comparison between experiment and simulation on turn-on transient at different temperature: (a)  $V_{DC}=1800\text{V}$ ,  $I_C=1500\text{A}$ ,  $T=25^\circ\text{C}$ ; (b)  $V_{DC}=1800\text{V}$ ,  $I_C=1500\text{A}$ ,  $T=125^\circ\text{C}$ .

Fig. 5, Fig. 6 and Fig. 7 show that the IGBT model proposed in this paper could give a good description of the SPT-IGBT. However, there is still some difference between experiments and simulation results. From the perspective of modeling IGBT and parameter optimization, the possible reason comes from two aspects. The first one is the IGBT model itself. Due to the model is established under some certain assumption which is different from the actual IGBT chip, it's hard to give better fitting curves at all conditions. The second one is the stray parameters of the power module and experiment setup. For now, the experiment results are only used to estimate the parasitic inductance, but the parasitic capacitance is ignored in the simulation circuit. Some more research needs to carry on in the future.

#### IV. CONCLUSIONS

This paper has presented a new physical model implemented in the PSpice circuit simulator for high power SPT-IGBT. It is based on the lumped-charge approach to describe carrier distribution in the base region during both the steady state and switching processes. Temperature-dependent physical models, like PN junction model under high-level injection, carrier transportation and recombination, mobility modulation, enhanced planar model during transient are taken into account. The model gives an insight to the internal device variables, such as the base charge, carrier concentration, the voltage drops in different regions, as well as electron and hole current distributions at the collector and emitter edge.

The model has been validated for a 3.3 kV/1500 A SPT-IGBT, proving that it accurately describes both the static and switching behaviour. However, the thermal feedback is not considered. Future research and development on the proposed model expect to be further applied to do the electro-thermal co-simulation to study some complicated conditions that the thermal feedback cannot be ignored, such as short circuit.

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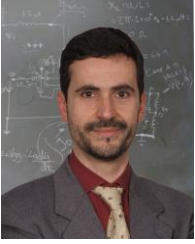
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