Fast Electro-thermal Simulation Strategy for SiC MOSFETs Based on Power Loss Mapping

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Published in:
Proceedings of the 2018 IEEE International Power Electronics and Application Conference and Exposition, PEAC 2018

DOI (link to publication from Publisher):
10.1109/PEAC.2018.8590288

Publication date:
2018

Document Version
Accepted author manuscript, peer reviewed version

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***Abstract* — A fast electro-thermal simulation strategy for SiC power MOSFETs is presented in this paper. This approach features the detailed mapping of the device power losses under a wide range of operating conditions by using a compact electrical model and its experimental validation for a 1.2 kV/ 36 A commercial device. The losses condition map is used in the simplified model of a half-bridge inverter topology. The average device losses per switching period are injected into a multi-layer thermal impedance network obtained via finite-element method (FEM) simulation. The strategy allows the electro-thermal simulation of a simple switching pattern in a very short time (seconds), compared to an equivalent physically-based circuit simulation, without significant accuracy loss, enabling long-timescale simulation and reliable, mission-profile oriented design of power electronic converters.**

Keywords—SiC MOSFET, compact model, electro-thermal simulation, power electronics reliability.

I. INTRODUCTION

As the complexity of power electronic systems and converters increases and new promising devices, like Silicon Carbide (SiC) power MOSFETs [1], are introduced in the market, fast and accurate electro-thermal modeling and simulation is becoming a key factor in the design of applications with optimized electrical and thermal performances [2]. The SiC power MOSFET is now an established device in terms of manufacturing and many off the shelf all-SiC modules are available, rated up to 1.7 kV and 500 A. SiC modules find advantage especially in those applications where high efficiency, more integration and higher power density are prioritized, and can pay off the higher cost of such devices [3]. Nevertheless, despite their inherent advantages, fulfilling the converter design specifications is still a challenge for many applications, with increasing demand for reliability and cost constraints [4]. Higher power density, together with higher thermal conductivity, determine larger temperature stress in SiC devices' packaging materials in comparison to Si devices rated at the same power. Therefore, the lifetime prediction of SiC devices becomes a critical issue in the design of emerging power electronic converters [5].

In particular, the implementation of tools capable of simulating real mission profiles for specific applications enables the study of long-term efficiency and reliability and boosts the design optimization of cooling systems and circuit layout [6]. The major challenge in this field is dealing with very different timescales, ranging from few µs in the case of a semiconductor device switching event to the slow load variations occurring during minutes or hours of the converter normal operation [7]–[9]. Physics-based compact device models, despite being considerably simple and fast, are not realistically suitable for the simulation of billions switching events. This issue can be tackled if a compact electrical model is used offline to map the device losses in a wide range of junction temperatures and operating currents, as already proposed in [10]. Condition mapping allows the creation of lookup tables (LUTs) that can be used in the simulation of a desired switching pattern, providing the device losses without significant loss in accuracy. The power losses are injected into a compact thermal network that accounts for the device and heatsink thermal behavior [11], [12]. The junction temperature can be therefore estimated and fed back to the LUTs, as shown in Fig. 1.

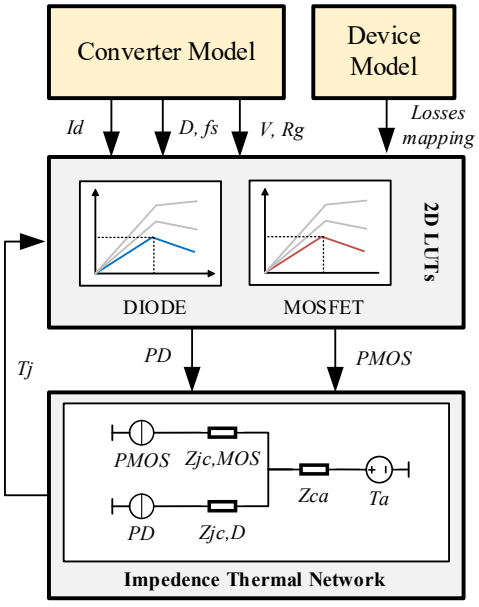

Fig. 1. Fast electro-thermal simulation strategy based on condition mapping.

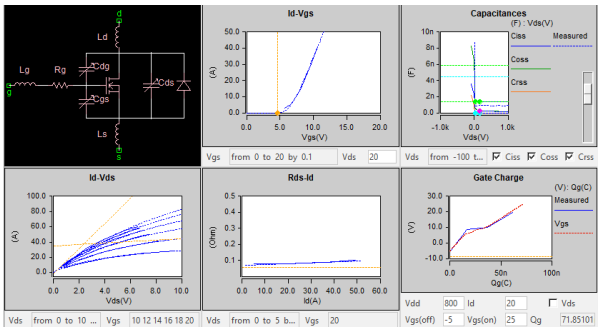

Fig. 2. Snapshot of the Synopsis Power MOSFET tool.

This paper explores the application such a simulation strategy to new-generation SiC power MOSFETs, based on an accurate electrical device model implemented in Saber [13], validated with experimental static and switching measurements, and a thermal model extracted via finite-element method (FEM) analysis of the device and package structure. The fast simulation was implemented in MATLAB/Simulink for a simple converter topology and an AC switching pattern. The performance and results have been compared to an equivalent Saber circuit simulation.

II. Electro-Thermal Model Structure

A. Electrical Device Model

The electrical device model is one of the most essential components for any model-based predictive approach for the lifetime analysis and reliability assessment of any power semiconductor device. The one used for this purpose is based on the SiC compact model published in 2016 and implemented in MAST inside the Saber environment [14]. The Power MOSFET tool inside the Saber environment was used in order to fully characterize the temperature-dependent behavior of the SiC MOSFET and the SiC Schottky barrier diode (SBD). A snapshot of the tool is shown in Fig. 2. The modeled commercial discrete devices are a 1.2 kV SiC Power MOSFETs (C2M0080120D) [15] and a SiC Schottky diode (C4D20120H) [16]. The Power MOSFET and the SiC Schottky diode model parameters are identified and validated by using the measured static characteristics of the device. The model was characterized for DC transfer I-V curves, capacitance/charge and diode forward and reverse characteristics. Fig. 3 shows the large-signal model topology that describes the model formulation approach. The model has 2 internal nodes (namely *Di* and *Si*) that are used to characterize the JFET resistance between the nodes *D* and *Di*, as well as the parasitic source resistance in the path of the channel current. The resistance R_{JFET} is variable and varies during the transition from the linear to the saturation region. The current source Ids represents the channel current and the diode *D* represents the body-diode. The internal device capacitances are C_{GS}, C_{GD}, and C_{DS}. The parasitic inductance and resistance elements for the TO-247 package were included in the device model.

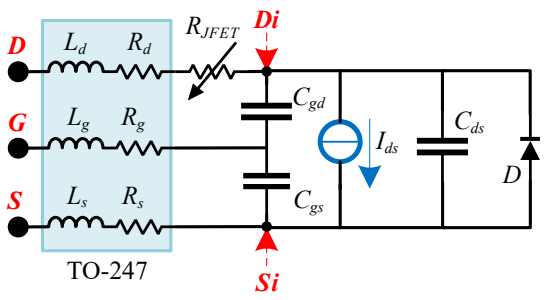

Fig. 3. SiC power MOSFET compact model schematic.

B. Lumped Impedance Thermal Model

The thermal behavior of the device can be described by using a Foster-type impedance thermal network. This equivalent electrical model consists of a multi-layer network of RC elements, like presented in [11]. The main assumption here is the unidirectional heat-flow from the device junction to the heatsink through the thermal stack material. The impedance value can be obtained in several ways: 1) from the module datasheet; 2) from experimental characterization of the heating/cooling response, and 3) from the FEM analysis of the device and its cooling

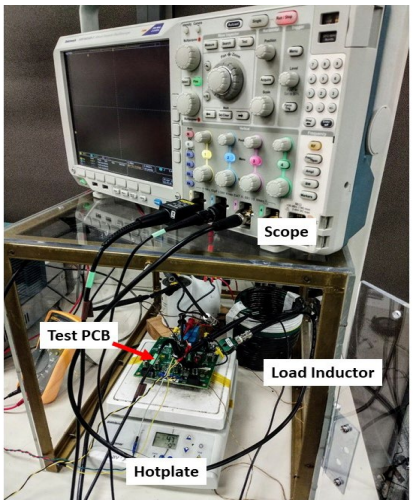

Fig. 4. Laboratory double-pulse test setup used in the device characterization.

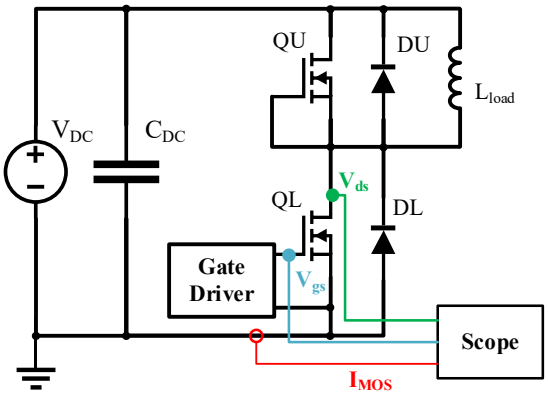

Fig. 5. Laboratory double-pulse test setup electrical schematic.

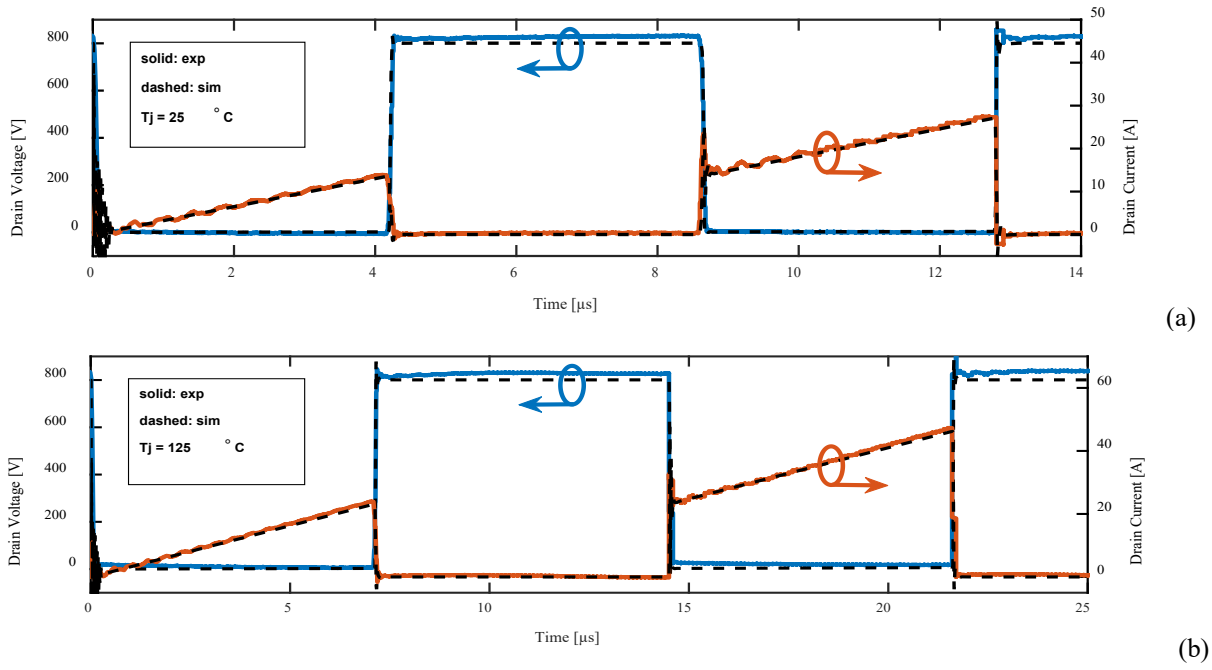

Fig. 6. Comparison of experimental DPT waveforms with simulation results from SABER for T_j=25°C (a) and T_j=125°C (b) with V_{DC}=800 V

system and the fitting of thermal impedance curves, as proposed in [12], [17]. The latter approach was used here for the extraction of the equivalent thermal network, presented in section IV.

III. Experimental Validation

A. Double-pulse Test (DPT) Setup Description

The static characterization of the device under test has been performed using a B1505A Keysight curve tracer/device analyzer. A fixture was connected in order to perform measurements at different temperatures. The double-pulse test (DPT) setup used for the switching characterization and validation of the SiC MOSFET model is shown in Fig. 3, while its circuit schematic is reported in Fig. 4. The setup includes a 800 V DC power supply connected in parallel with the DC-bus capacitors, an air-core load inductor and a test PCB populated with both SiC MOSFETs and SiC SBDs in an half bridge topology. A 20 Ω gate resistance was used in a SiC MOSFET gate drive from CREE. The devices are placed underneath the board, in contact with a hotplate through thermal grease. The hotplate was used to bring the case temperature of the devices up to 125°C, while the load current was measured up to 25 A. The test were conducted assuming that the junction and case temperature were equal at the beginning of the test, given enough time for the heat to spread from the hotplate. The device switching losses were mapped over a wide range of temperature and load current values.

Device Model Validation

Fig. 6 shows the comparison of drain current and drain-source voltage waveforms measured in the DPT with the simulated waveforms obtained in Saber at different junction temperature values, respectively Tj = 25°C (a) and Tj = 125°C (b). The DC-bus voltage in the test was kept at 800 V. It is worth to note that the switching waveform dependency on temperature is not very significant in this

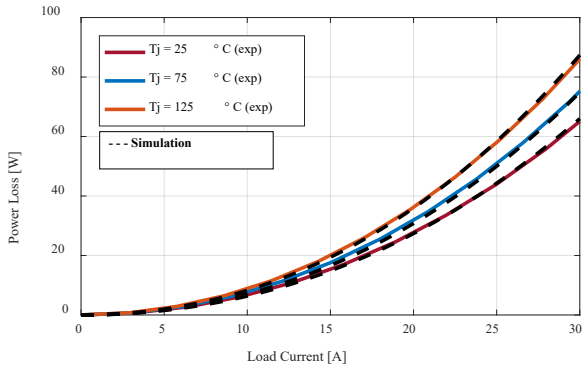

Fig. 7. Validation of MOSFET's conduction power loss vs. load current at different temperatures.

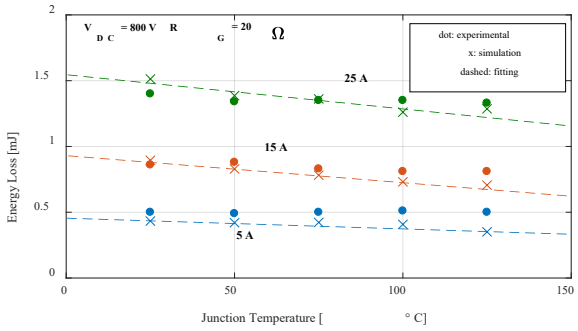

Fig. 8. Validation of MOSFET's total switching energy loss vs. junction temperature for different drain current values – dashed lines: fittings

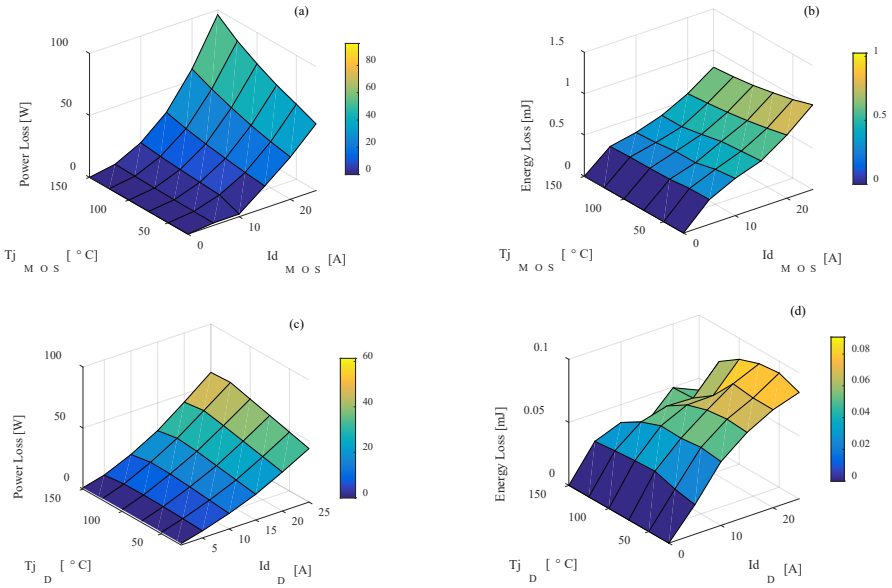

Fig. 9. Condition mapping of: SiC MOSFET conduction power losses (a); SiC MOSFET switching energy losses (b); SiC Schottky diode conduction power losses (c); SiC Schottky diode switching energy losses (d).

range of operation, mostly due to the high-temperature capability of SiC devices. Fig. 7 reports instead the validation of the conduction power loss characteristics for the SiC MOSFET under test considering increasing current and three temperature points. The curves are simulated with outstanding accuracy and less than 2% relative error. The total switching energy loss were calculated from the simulated waveforms by integrating the instantaneous power loss over the turn-on and turn-off time. There is fairly good matching with the experimental results, as shown in Fig. 8. Most of the uncertainty here is given by the parasitic elements in the experimental setup, which contribute to increase the power loss. The simulated topology had to be tuned in order to match such behavior.

Once the model was validated, the power losses were mapped for the same. Fig. 9 reports the condition mapping of the conduction power loss and switching energy loss for both SiC MOSFET and SiC SBD in the considered range of junction temperatures and operating device current at 800 V reverse voltage and 20 Ω gate resistance.

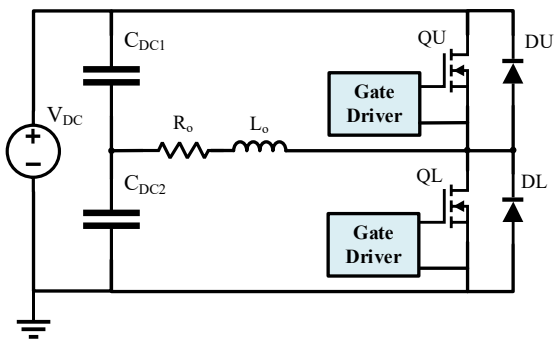

Fig. 10. Schematic of the half-bridge inverter topology used in the simulation.

IV. Fast Electro-Thermal Simulation of a Half-Bridge Inverter Topology

Fig. 10 depicts the half-bridge topology used to compare the circuit simulation in Saber with the proposed fast simulation strategy based on the power loss LUTs, implemented in MATLAB/Simulink. In the simulations, the DC-bus voltage VDC has been set to 800 V and the switching frequency to 10 kHz, with 20 Ω gate resistance. The same thermal network has been used in both the models, since the package is the same for the four devices. It is assumed here that the four devices are all placed on the same heatsink and no thermal coupling takes place between the 4 packages. The thermal network showed in Fig. 11 consists of four branches corresponding to the power losses injection for the 4 half-bridge devices, all converging in the heatsink thermal impedance element. The thermal impedance values used in the simulations are

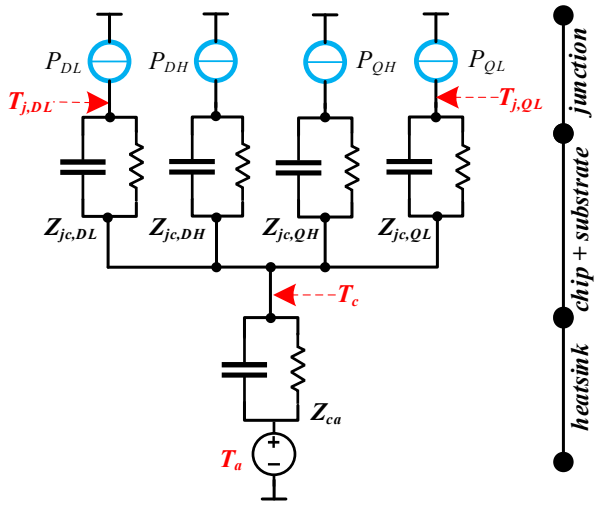

Fig. 11. Multi-layer equivalent thermal network structure.

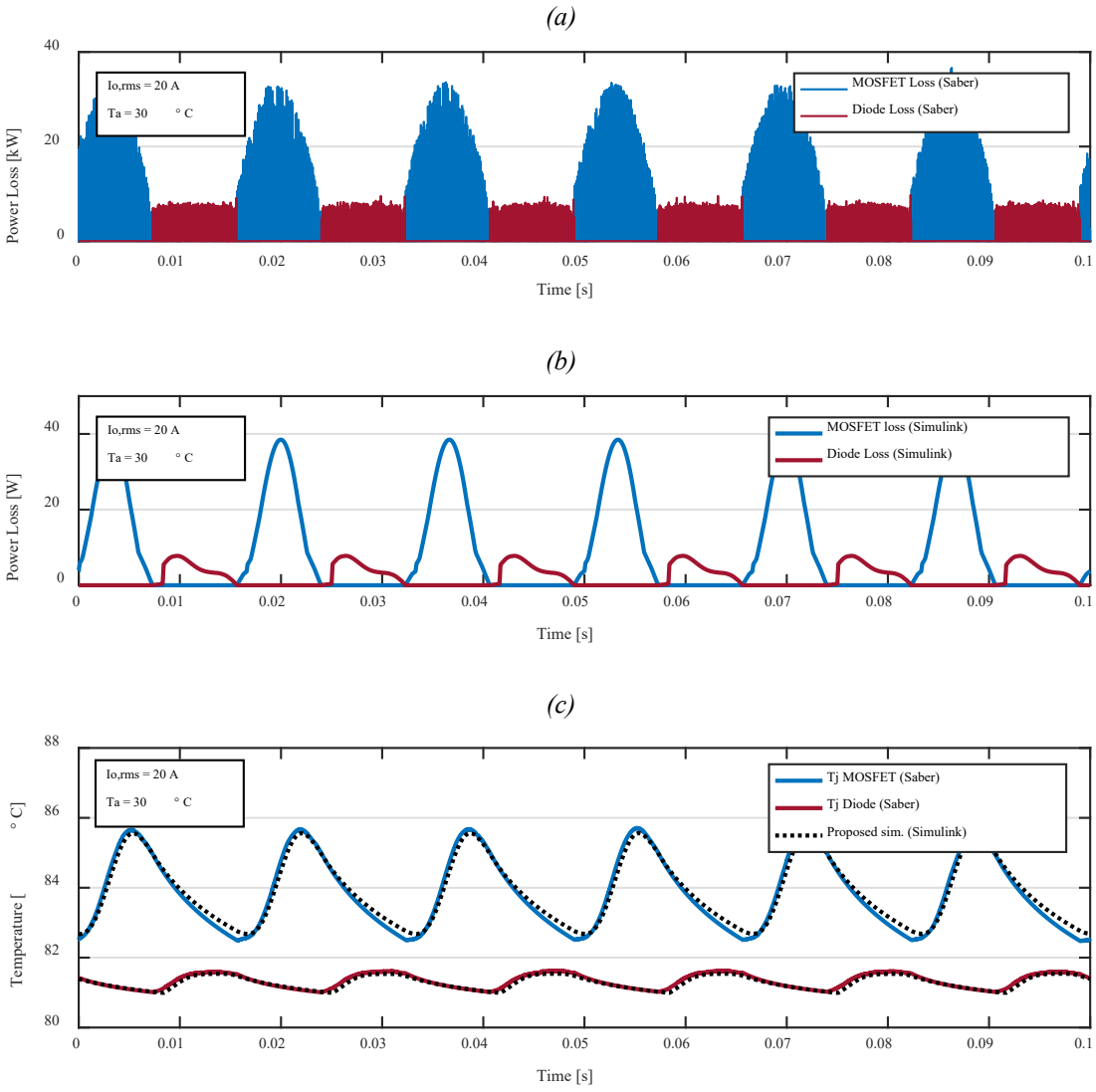

Fig. 12. Simulated power losses in SABER (a) and correspondent averaged power losses in Simulink (b); comparison of the steady state junction temperature simulated in SABER with the proposed fast simulation approach in Simulink (c).

reported in Table I. These were calculated by simulating the thermal structure of the device in ANSYS Icepak and applying power pulses in the junction region to observe its transient thermal response, similar to what was presented in [12].

In Fig. 12.a, one can observe the instantaneous power loss simulated for a MOSFET/SBD couple in the topology. The high spikes – in the range of tens of kW - here represent the switching events, during which the device experiences full voltage and current simultaneously. The power loss waveforms in Fig. 12.b are instead those used in the proposed fast simulation strategy. In this case, the total power loss is averaged on each switching period, resulting in smooth waveforms. Fig. 12.c shows the comparison of the steady-state temperature behavior in the junction of both QL and DL (see Fig. 11). The fast simulation strategy in Simulink can approximate the temperature calculated by the SABER circuit simulation with good accuracy. While the circuit simulation of 0.5 s took approximately 5 min to complete, the proposed strategy completed in just 3 s.

TABLE I – THERMAL NETWORK IMPEDANCES

Layer	R_θ [K/W]	C_θ [J/K]
Z_{jc}	0.7	0.01
Z_{ca}	2.75	0.008

V. CONCLUSIONS

This paper presents an improved electro-thermal simulation strategy for SiC power MOSFETs, which has proven to be extremely fast and accurate and offers several advantages:

- low accuracy loss and considerable reduction of the simulation time in comparison with traditional circuit simulation;
- Easy implementation for a wide range of power electronic devices and converter topologies;

- Can be used for simulating long mission profiles for a given converter application and can significantly boost the optimized design of power converters.

Besides that, the procedure needs a thorough model identification and validation that is strictly dependent on the kind of application and the required range of operational conditions. Overcoming such boundaries would mean obtaining wrong simulation results. For instance, the simulation of abnormal operating conditions has not been considered here. Finally, the further experimental validation of the obtained results, especially temperature estimation, is going to be object of future studies for the authors.

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