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Enabling Junction Temperature Estimation via Collector-Side Thermo-Sensitive Electrical Parameters through Emitter Stray Inductance in High-Power IGBT Modules

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***Abstract*— This paper proposes the adoption of the inherent emitter stray inductance L_{eE} in high-power insulated gate bipolar transistor (IGBT) modules as a new dynamic thermo-sensitive electrical parameter (d-TSEP). Furthermore, a family of 14 derived dynamic TSEP candidates has been extracted and classified in voltage-based, time-based and charge-based TSEPs. Accordingly, the perspectives and the implementation challenges of the proposed method are discussed and summarized. Finally, high-power test platforms are designed and adopted to experimentally verify the theoretical analysis.**

***Index Terms*— High-power IGBT modules, auxiliary parasitic inductance, dynamic thermo-sensitive electrical parameters, junction temperature extraction principles.**

I. Introduction

THE fast-growing pace of high-power conversion systems keep developing high-power Insulated Gate Bipolar Transistors (IGBTs) [1,2]. Thermal performance is currently regarded as one of the most important specifications in high-power modules, since both the short-term characteristics [3] and long-term ones are temperature-dependent [4,5]. In terms of the maximum operating junction temperature T_j, the commercially-available silicon-based power devices are rated up to 175 °C and the expected operation T_j in Wide-Band-Gap devices can reach 300 °C [6]. Hence, the knowledge of T_j has a crucial effect on the safe operation area of IGBTs.

So far, many practical methods have been proposed [7-10]. Generally, the widely-studied T_j estimation methods in practical applications can be classified into three groups: a) sensor-based methods, b) model-based methods, and thermo-sensitive electrical parameter (TSEP)-based methods. Regarding in sensor-based methods, simple temperature-dependent components are soldered on Direct Bond Copper (DBC) substrate as close as possible to the active areas of the module, i.e. the IGBT dies. Nevertheless, the distances of the formers from the latter ones together with the considerable response delays typically lead to a great estimation error. In order to get a faster estimation of T_j, many efforts have been done very recently on model-based methods [11-14]. In such methods, T_j estimation can be achieved as the response of an equivalent thermal RC network to power losses. As a result, the accuracy is strongly dependent on the measurement accuracy of instantaneous power losses and the correct identification of the thermal RC network. However, the thermal RC network is nonlinear at high temperatures and, on top of it, it is also strongly dependent on aging effects [15-17]. Hence, the needed real-time calculations and corrections make model-based methods very complex and time-consuming. Lastly, TSEP-based methods estimate T_j from the variation of physical temperature-dependent electrical parameters which are closely dependent on it. These methods are very promising as they could provide a very fast and cheap estimation of the junction temperature together with great accuracy, but still they require a non-negligible calibration process and computation time at runtime.

In view of the characteristics of fast response (within 100 μs), high accuracy, and low cost, a large numbers of TSEP-based methods have been proposed and applied to MOSFETs, IGBTs, IGCTs, and Wide-Band-Gap devices over past five years [18-20]. Considering the operating status of power devices, the optional TSEP candidates can be classified into the static TSEPs and dynamic TSEPs (d-TSEPs) [21-23]. Since the number of d-TSEPs is larger than that of static TSEPs, more and more d-TSEP methods are being developed for T_j estimation recently [21, 24-26]. Practically, according to the magnitude of electrical parameters, TSEPs can be divided further into gate-related TSEPs and collector-related TSEPs, as depicted in Fig.1.

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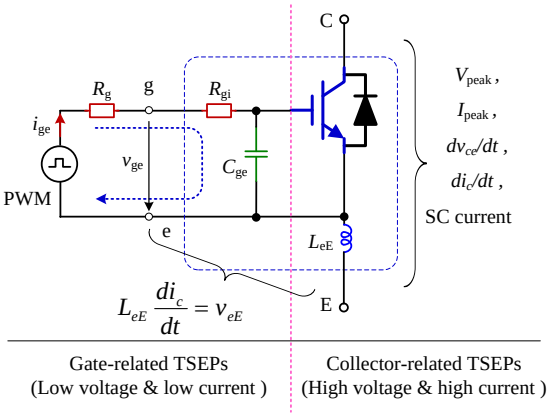


Fig. 1. Gate-related and collector-related TSEP candidates.

Since the electrical parameters in the gate loop are low-voltage quantities, the gate-related TSEPs can be sampled by low-voltage sampling circuits directly. Some key published gate-related TSEPs are based on: peak gate current [8], integration of gate current [20], threshold voltage v_{th} [27], and Miller plateau width [28]. On the other hand, plenty of collector-related TSEPs can be identified, e.g.: di_c/dt, dv_{ce}/dt, maximum turn-off voltage peak V_{peak}, maximum turn-on current peak I_{peak}, etc. Of course, once the collector-related quantities can be measured at a low cost, a lot of new and practical TSEPs candidates can be extracted. However, the sampling circuit should be designed to withstand high voltages and/or large currents during converter operations, making the adoption of such a method not convenient or even not feasible at all.

To overcome the above shortcomings, a new approach for extracting collector-related dynamic TSEPs is proposed in this work. Taking into account the specifications of high-power IGBT module packages, the internal parasitic inductance L_{eE} between the power emitter and Kelvin emitter can be profitably used as an intermediary for the conversion from several hundreds of amperes to tens of volts. A lot of collector-related d-TSEPs can be extracted through the induced voltage v_{eE} across L_{eE}. Moreover, a number of new measurable electrical parameters are proven to be possibly adopted as d-TSEPs. Finally, it is worth to point out that all the v_{eE}-based d-TSEP obtained through the presented method can have a unified evaluation system, which facilitates designers to select the proper d-TSEP candidate for a given application.

II. Proposed Method

A. High-power IGBT module with parasitic parameters

The typical high-power IGBT modules and related circuit diagrams are illustrated in Fig.2, which have been taken from Infineon's portfolio [29]. The depicted high-power multi-chip IGBT modules are characterized by a common gate terminal for the parallel-connected chips.

From the electrical point of view, the high-power IGBT module can be considered as a five-port module, which consists of power collector C (C = C_1, C_2 and C_3 connected together), power emitter E (E = E_1, E_2 and E_3 connected together), auxiliary collector terminal c, Kelvin emitter e and gate terminal g. Its equivalent circuit considering the parasitic

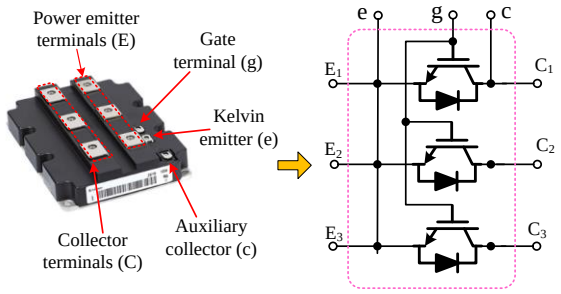


Fig. 2. Typical appearances of high-power IGBT modules and related circuit diagrams for single switch module.

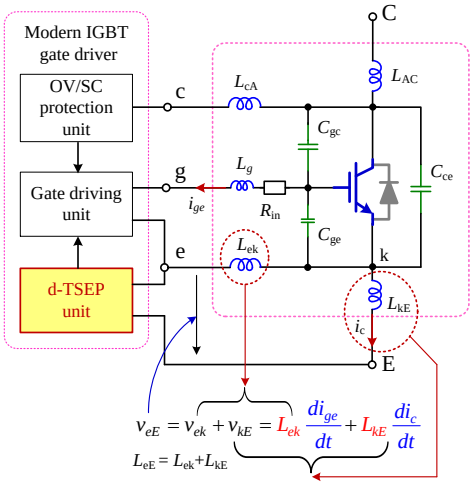


Fig. 3. Equivalent circuit of a high-power IGBT module including parasitic parameters, equipped with a modern gate driver.

inductances is depicted in Fig.3, together with a modern IGBT gate driver [30]. It is worth noting that the inductance L_{eE} can be regarded as a relatively constant for a given part number, and its value can also be extracted during the calibration process.

B. Switching behavior and related v_{eE}

During the switching transitions, an induced voltage v_{eE} is generated. This induced voltage v_{eE} consists of v_{ek} related to di_{ge}/dt and v_{kE} related to di_c/dt, as shown in Fig.3. Moreover, in power IGBTs, gate current i_{ge} is far negligible in respect to the collector current i_c. To better understand the relationship between the hard-switching waveforms and corresponding induced voltage v_{eE} under inductive load, the typical IGBT switching transitions have been reported in Fig.4, which can be divided into four states: on-state, turn-off transition, off-state, and turn-on transition.

Referring to Fig.4, at the beginning of turn-off transition, the rapid decline of v_{ge} causes a negative i_{ge} variation from the gate capacitors C_{gc} and C_{ge}. This variation leads to a positive-going v_{ek} across L_{ek} between t_0 and t_1. For the time period from t_0 to t_1, the collector current i_c can be regarded as constant because the turn-off v_{ge} is still higher than the threshold voltage v_{th}. Therefore, the inductance L_{ek} can be extracted by the voltage spike during Δt_1. Between t_1 and t_2 the Miller plateau takes place. Moreover, with a low di_{ge}/dt and constant collector current i_c, the value of v_{eE} from t_1 to t_3 is approximately zero.

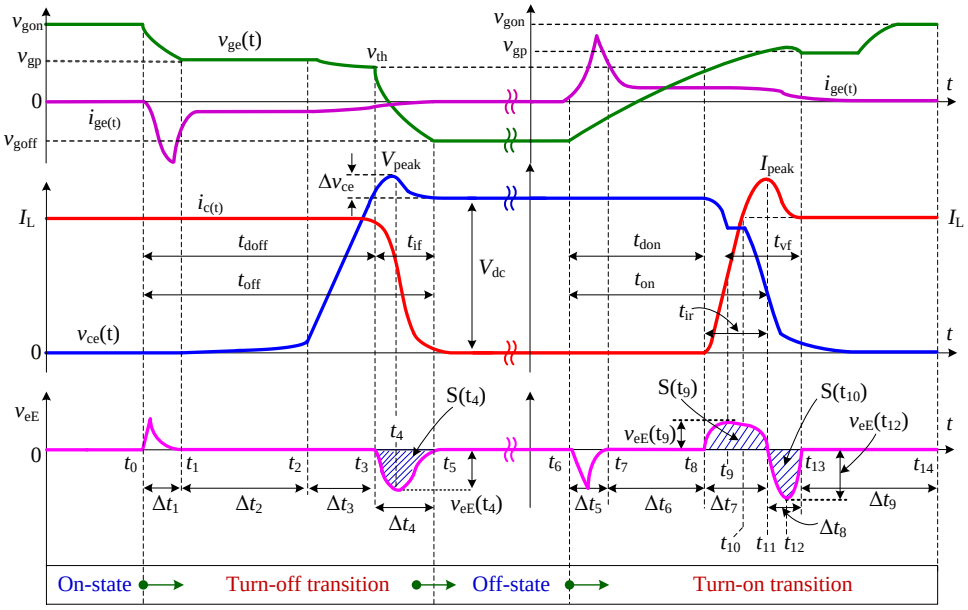


Fig. 4. Hard-switching waveforms of conventional IGBT module under inductive load.

Then, at t_3, the load current begins to fall after v_{ge} reaches v_{th}, and the maximum turn-off di_c/dt can be detected by the negative peak $v_{eE}(t_4)$, whose area is $S(t_4)$. The turn-off process is over at t_5. The rapidly falling i_c is reflected by a synchronous jump of v_{eE}. After t_3, the induced v_{eE} is mainly caused by the collector current variation di_c/dt. Hence, the inductance L_{kE} can be calculated by the second v_{eE} peak value at t_4.

The turn-on transition takes place at t_6. Then, when the gate voltage v_{ge} begins to rise, an induced voltage v_{eK} occurs across L_{ek}, which is mainly due to the rapid gate current i_{ge} variation. Once again, v_{kE} is zero as i_c doesn't vary, so v_{eE} has the same behavior. With respect to the time period from t_6 to t_8, the collector current i_c is zero because the gate voltage v_{ge} is lower than the threshold voltage v_{th}. Moreover, with a low di_{ge}/dt and zero i_c, the value of v_{eE} from t_7 to t_8 is approximately zero. Then, the collector current i_c begins to rise after v_{ge} reaches v_{th}. This rapidly rising i_c is reflected by a synchronous jump of v_{eE}. There, the i_c contains the dynamic characteristics of both diode and IGBT. As a result, the induced v_{eE} during turn-on transition also contains information about the commutated diode. After t_8, the induced v_{eE} is mainly caused by the collector current variation di_c/dt. At t_9, the turn-on collector current slope reaches the maximum value, which can be reflected by the peak value $v_{eE}(t_9)$. At t_{10}, the collector current equals to the load current, and the forward current though commutation diode is decreased to zero and the reverse recovery process begins. When the turn-on i_c reaches its peak value I_{peak}, the induced v_{eE} comes to the zero-crossing point at t_{11}. Then, the negative v_{eE} can reach the negative peak value $v_{eE}(t_{12})$, which can be used for the maximum reverse recovery current slope extraction. From t_{10} to t_{13}, the collector current i_c consists of reverse recovery current i_d and the load inductor current I_L. Therefore, the corresponding induced v_{eE} from t_{10} to t_{13} is affected by the diode characteristics. Accordingly, the enclosed area $S(t_9)$ is caused by the rapid di_c/dt before reaching I_{peak}, and the decreasing collector current after I_{peak} induces the negative area $S(t_{10})$ on the v_{eE} waveform. In summary, the induced v_{eE} during the whole switching period is given by (1).

From Fig.4 and (1), it can be concluded that the effects of the gate current transitions on v_{eE} take place at different time intervals with respect to the effects from the collector current, therefore these latter ones can be separated from the former ones and easily determined.

$$v_{eE}=\begin{cases} v_{ek}=L_{ek}\dfrac{di_{ge}}{dt},(t_0<t\le t_1)\\ v_{ek}\approx v_{kE}=0,(t_1<t\le t_3)\\ v_{kE}=-L_{kE}\dfrac{di_c}{dt},(t_3<t\le t_5)\\ v_{kE}=v_{ek}=0,(t_5<t\le t_6)\\ v_{ek}=-L_{ek}\dfrac{di_{ge}}{dt},(t_6<t\le t_7)\\ v_{ek}\approx v_{kE}=0,(t_7<t\le t_8)\\ v_{kE}=L_{kE}\dfrac{di_c}{dt},(t_8<t\le t_{13}) \end{cases} \quad (1)$$

Nevertheless, the former ones can be also profitably used as a timing reference for the latter ones as will be clarified in the next section. Moreover, with the internal parasitic inductance L_{kE} in a role of intermediary, the low and measurable voltage signal v_{eE} can be straightforwardly converted to the electrical parameter di_c/dt. Last but not least, since the temperature T_j has impact on di_c/dt in several manners, including diode junction temperature T_{jD} at turn on, the induced v_{eE} can be exploited to extract an equal number of d-TSEP methods once the relation between v_{eE} and T_j and T_{jD} has been identified and the related parameters have been calibrated.

III. Collector-side Dynamic TSEPs

According to the waveforms of Fig.4, the collector-side d-TSEPs extracted by means of v_{eE} can be classified into three categories, namely: time-based, voltage-based and charge-based d-TSEPs. Besides, the definitions for electrical parameters are adopted from the standard IEC 60747-9: Semiconductor devices [31].

A. Time-based d-TSEPs

The time-based TSEPs are distributed on the horizontal axis of Fig.4, and are measured in ns/°C. The duration of a given v_{eE} pulse is a function of T_j through a given time-based TSEP. To measure such duration, an analog comparator should be used

with an appropriate threshold voltage, together with a time counter.

(1) Turn-off delay time t_{doff}

The induced voltage v_{eE} consists of v_{ek} introduced by di_{ge}/dt at the beginning of v_{ge} fall and v_{kE} introduced by di_c/dt at t_3. As a result, the starting point of t_{doff} can be determined by $L_{ek}\cdot di_{ge}/dt$, and the ending point is triggered by $L_{kE}\cdot di_c/dt$. Hence, t_{doff} is equal to $(\Delta t_1+\Delta t_2+\Delta t_3)$, as shown in Fig.4. The relationship between T_j and t_{doff} based on the physical mechanisms has been enunciated and discussed in [23].

(2) Current fall time t_{if}

The current fall time t_{if} is usually defined as the falling time of i_c from 90% I_L to 10% I_L. In practice, due to different semiconductor techniques, the 10% I_L limitation for current fall time can be reset according to the practical tail current. In [32], the instantaneous collector current has been extracted by a sophisticated and isolated PCB Rogowski coil. Compared with this solution, t_{if} can be conveniently extracted with the proposed method as the length of the negative pulse of v_{eE}, i.e. Δt_4. This latter duration and corresponding t_{if} can be determined by setting a threshold voltage in an analog comparator.

(3) Turn-off time t_{off}

The turn-off time t_{off} is defined as the sum of the turn-off delay time t_{doff} and the fall time t_{if}, without including the tail current part. The duration of t_{off} can be obtained by the sum of $(\Delta t_1+\Delta t_2+\Delta t_3+\Delta t_4)$. As method (1), a significantly longer time has to be measured in respect to method (2), which is highly beneficial from the measurement accuracy standpoint.

(4) Turn-on delay time t_{don}

The turn-on delay time t_{don} is defined as the duration from the beginning of the v_{ge} transient t_6 to the beginning of the collector current increase t_8. In the v_{eE} waveform, the starting point of t_{don} can be determined as the beginning of the negative peak at t_6, and its ending point can be approximately obtained as the positive voltage jump at t_8. Hence, the duration t_{don} can be extracted by the sum of $(\Delta t_5+\Delta t_6)$.

(5) Voltage fall-time t_{vf}

The collector voltage fall time t_{vf} is defined as the time interval where the collector voltage v_{ce} falls from 90 % to 10 % of the bus voltage V_{dc}. Therefore, t_{vf} can be extracted as $(\Delta t_7+\Delta t_8)$.

(6) Turn-on time t_{on}

The total turn-on time t_{on} can be obtained from the sum of turn-on delay time t_{don} and current rise time t_{ir}., i.e. from t_6 to t_{10}. However, the time t_{10} cannot be extracted by v_{eE} directly. For this reason, time t_{11} must be detected in place of it $(\Delta t_5+\Delta t_6+\Delta t_7)$, which also includes the reverse recovery time of the diode, which is temperature-dependent too. Therefore, in this method the diode T_j should also be determined firstly. Nevertheless, it is worth to point out that, in the likely approximation that IGBT's and diode's junction temperatures are related to each other, this method can be successfully adopted.

B. v_{eE} Voltage-based d-TSEPs

In Fig.4, the v_{eE} voltage-based d-TSEPs are distributed on the v_{eE} vertical axis, and are measured in mV/°C. Accordingly, the v_{eE} voltage-based TSEPs can be measured by means of low-voltage peak detectors [8].

(7) Maximum turn-off di_c/dt

The negative v_{eE} peak occurring at t_4 is proportional to the maximum di_c/dt at turn-off. Therefore, to the extent that such a quantity appreciably depends on T_j, (2) can be adopted

$$\left.\frac{di_c}{dt}\right|_{max\_off} = \frac{v_{eE}(t_4)}{L_{kE}} \quad (2).$$

(8) Maximum turn-on di_c/dt

Similarly to method (7), the maximum turn-on changing rate of di_c/dt induces a positive voltage drop on L_{kE}. Hence, it can be calculated by the peak v_{eE} at t_9, which is given by

$$\left.\frac{di_c}{dt}\right|_{max\_on} = \frac{v_{eE}(t_9)}{L_{kE}} \quad (3).$$

(9) Maximum turn-off reverse recovery di_d/dt

The negative peak voltage of v_{eE} at t_{12} is related to the diode maximum turn-off slope di_d/dt. Besides, the maximum turn-off di_d/dt during the reverse recovery period is studied and developed as a TSEP candidate for T_j extraction of P-i-N diodes [33]. Since the load current I_L can be assumed to be constant in good approximation, the relationship between the induced v_{eE} and di_d/dt from t_{11} to t_{13} is given by

$$\frac{v_{eE}(t_{12})}{L_{kE}} = \frac{di_c}{dt} = \frac{d(I_L - i_d)}{dt} = -\left.\frac{di_d}{dt}\right|_{max} \quad (4).$$

It is worth noting that the changing rate di_c/dt is related to the IGBT characteristics. Therefore, the knowledge of the IGBT T_j is a prerequisite for the diode T_j extraction.

C. Charge-based d-TSEPs

The charge-based d-TSEPs are combined parameters related to both vertical and horizontal information about v_{eE}. By means of an integrator, the enclosed area of v_{eE} waveforms such as $S(t_4)$, $S(t_9)$ and $S(t_{10})$ can be used for the extraction of several TSEP candidates.

(10) IGBT forward storage charge Q_{rrI}

During turn-off transition, I_L can be considered as a constant and the extraction of Δt_4 can be used for the integration limits. The instantaneous collector current i_c can be estimated as the integration of v_{eE} and the initial condition I_L [34].

$$i_c(t) = I_L + \int_{t_3}^{t} \frac{v_{eE}(t)}{L_{kE}} dt, (t_3 < t < t_5) \quad (5).$$

In Fig.5, the estimated instantaneous i_c from (5) during turn-off transition is reported together with the experimental waveforms of an IGBT. In case of fixed T_j, the swept-out charge Q_{rrI} [35] during turn-off transition is related to both I_L and length of Δt_4 and can be obtained as

$$\begin{cases} I_L \approx \Delta i_c = \int_{t_3}^{t_5} \frac{v_{eE}}{L_{kE}} dt = \frac{S(t_4)}{L_{kE}} \\ Q_{rrI} \approx \frac{1}{2}\Delta i_c \Delta t_4 = \frac{S(t_4)\Delta t_4}{2L_{kE}} \end{cases} \quad (6).$$

During the switching transition, the load current I_L can be treated as constant, so the calculated Q_{rrI} is proportional to the extracted Δt_4. Finally, the combination of the derivative effect of the stray inductance L_{kE} and the integrator gives an accurate estimation of the collector current variation Δi_c in the considered interval.

(11) and (12) Diode recovery storage fall charge Q_{rrD} [35] and maximum reverse recovery current I_{rrm}

In [36], the extracted charge during the reverse recovery falling phase of high-voltage P-i-N diodes has been developed as a dynamic TSEP for diode T_j extraction.

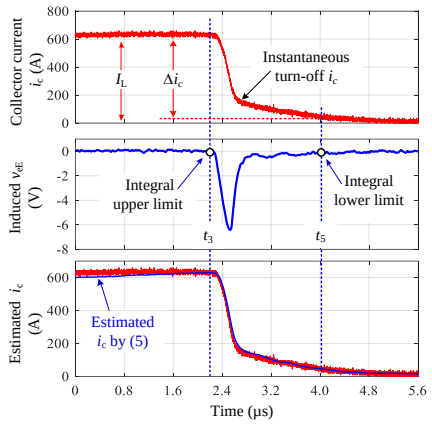


Fig. 5. Collector current estimation using integration of v_{eE} (V_{dc}=1800V, I_L=600A and T_j=25°C) [34].

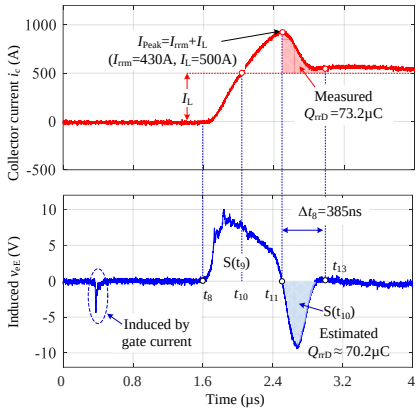


Fig. 6. Waveforms of turn-on i_c and related induced v_{eE}.

In Fig.6, the experimental instantaneous turn-on i_c and the related v_{eE} at V_{dc}=1600 V, I_L=500 A are depicted (IGBT T_j=T_{jD}=25°C). Correspondingly, the duration Δt_8 is around 385 ns and the parasitic L_{eK} is around 6 nH.

According to that approach, the enclosed area S(t_{10}) and recovery storage fall time Δt_8 (t_{11}~t_{13}) can be used for Q_{rrD} calculation. Hence, the Q_{rrD} extraction principle during diode turn-off transition is derived from

$$\begin{cases} I_{rrm} \approx \dfrac{1}{L_{kE}} \int_{t_{13}}^{t_{11}} v_{eE} dt = \dfrac{S(t_{10})}{L_{kE}} \\ Q_{rrD} \approx \dfrac{1}{2} I_{rrm} \Delta t_8 = \dfrac{t_{rrb} S(t_{10})}{2L_{kE}} \end{cases} \quad (7).$$

Compared with the measured charge Q_{rrD} 73.2 μC, the calculated Q_{rrD} by (7) is around 70.2 μC. Therefore, the extracted Q_{rrD} can be predicted by using the negative area S(t_{10}), and the related Δt_8 at given L_{kE}. More importantly, the peak value of reverse recovery current I_{rrm} can also be obtained by S(t_{10}) and L_{kE}.

D. Other electrical parameters extracted by v_{eE}

(13) Turn-on peak collector current I_{peak}

The peak current I_{peak} at turn on can also be extracted in the presented approach. Referring to Fig.6, since i_c after t_{10} consists of the reverse recovery current i_d and the load current I_L, the peak current I_{peak} is the sum of I_L and I_{rrm}: I_{peak}=I_L+I_{rrm}. The turn-on I_{peak} and I_{rrm} can be estimated as

TABLE I
V_{EE}-BASED TSEP CANDIDATES AND RELATED EXTRACTION METHODS FOR IGBT AND DIODE

Description	Identifier	Key parameters	Category
Turn-off delay time	t_{doff}	$\Delta t_1+\Delta t_2+\Delta t_3$	Time-based d-TSEPs
Current fall time	t_{if}	Δt_4	
Turn-off time	t_{off}	$\Delta t_1+\Delta t_2+\Delta t_3+\Delta t_4$	
Turn-on delay time	t_{don}	$\Delta t_5+\Delta t_6$	
Voltage fall time	t_{vf}	$\Delta t_7+\Delta t_8$	
Turn-on time	t_{on}	$\Delta t_5+\Delta t_6+\Delta t_7$	
Maximum turn-off di_c/dt	$di_c/dt_{(max\_off)}$	$v_{eE}(t_4)$	Voltage-based d-TSEPs
Maximum turn-on di_c/dt	$di_c/dt_{(max\_on)}$	$v_{eE}(t_9)$	
Diode reverse recovery di_d/dt	$di_d/dt_{(max)}$	$v_{eE}(t_{11})$	
IGBT forward storage charge	Q_{rrI}	S(t_4) and Δt_4	Charge-based d-TSEPs
Diode recovery storage charge	Q_{rrD}	S(t_{10}) and Δt_8	
Maximum reverse recovery peak current	I_{rrm}	S(t_{10})	Other electrical parameters using induced v_{eE}
Maximum turn-on peak collector current	I_{peak}	S(t_9)	
Maximum turn-off peak collector voltage	V_{peak}	$v_{eE}(t_4)$, V_{dc} and fixed circuit parameters	

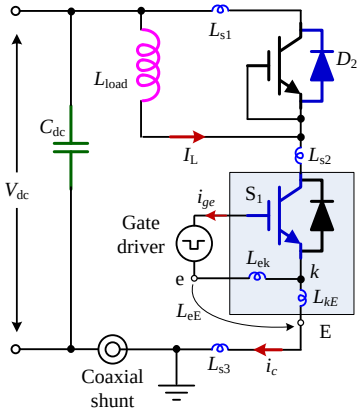


Fig. 7. Half-bridge circuit with inductive load.

$$\begin{cases} I_{peak} \approx i_c(t_{11}) - i_c(t_8) = \int_{t_8}^{t_{11}} \dfrac{v_{eE}}{L_{kE}} dt = \dfrac{S(t_9)}{L_{kE}} \\ I_{rrm} = I_{peak} - I_L \end{cases} \quad (8).$$

Theoretically, through a combination of (7) and (8), the load current I_L during the switching transition can be estimated by subtracting S(t_{10}) from S(t_9).

(14) Turn-off peak collector voltage V_{peak} [37]

The turn-off peak collector voltage V_{peak} cannot be extracted by v_{eE} directly without V_{dc} knowledge. The typical half-bridge circuit with inductive load considering parasitic inductors is depicted in Fig.7. The sum of the stray inductances L_{s1}, L_{s2} and L_{s3} can be conveniently called L_{loop}, whereas the parasitic module inductance is called L_{eE}.

At the beginning of Δt_4, an overshoot Δv_{ce} is induced on the collector voltage by the changing rate of collector current di_c/dt. Therefore, the collector voltage during Δt_4 can be expressed as

$$v_{ce}(t) = V_{dc} + \Delta v_{ce} = V_{dc} + (L_{loop} + L_{kE})\frac{di_c}{dt} \quad (9).$$

Since di_c/dt on the parasitic inductances is the same:

$$\frac{di_c}{dt} = -\frac{v_{eE}}{L_{kE}} = \frac{\Delta v_{ce}}{L_{kE} + L_{loop}} \quad (10).$$

The overshoot Δv_{eE} during Δt_4 can be expressed as

$$v_{ce}(t) = V_{dc} - v_{eE}(t)\frac{L_{kE} + L_{loop}}{L_{kE}}, (t_3 < t < t_5) \quad (11).$$

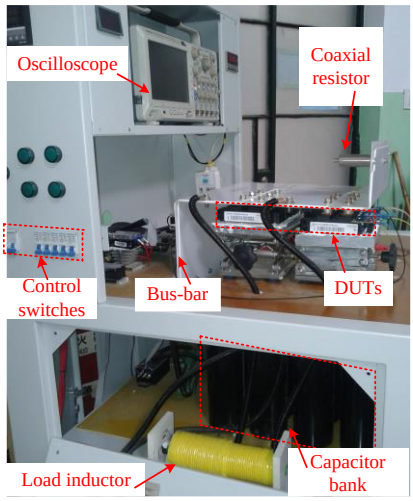
Since the value of L_{loop} and L_{kE} can be determined in advance, the turn-off peak voltage V_{peak} can be obtained as:

$$V_{peak} = V_{dc} - v_{eE}(t_4)\frac{L_{kE} + L_{loop}}{L_{kE}} \quad (12).$$

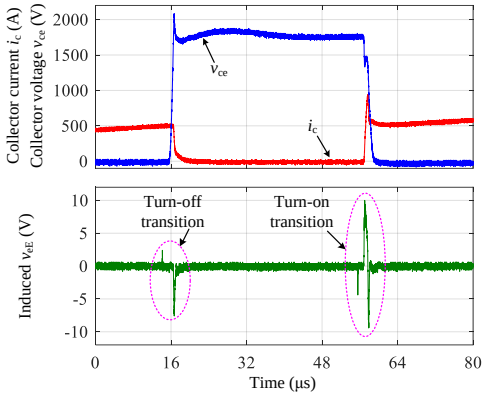
Based on the foregoing analysis, 14 measurable dynamic TSEPs are summarized in Table I and classified according to the above categories. Remarkably, the diode related TSEPs are related to the commutation IGBT characteristics. In terms of the calibration procedure, once the commutation IGBT temperature and related electrical parameters are measured, the corresponding diode T_j can be derived from the multi-dimensional database.

IV. Experimental Validation and Performance Comparison

In order to validate the effectiveness of the discussed dynamic v_{eE}-based TSEP candidates, a high-power double pulse test platform was used, whose picture is reported in Fig.8 (a), and whose specifications are detailed in [38]. The devices under test (DUT) and the related specification of IGBT and gate driver are listed in Table II. Typical double pulse test waveforms obtained from the experimental setup are reported in Fig.8 (b), whose shapes have been comprehensively discussed in the previous sections (see Fig. 4). The relations among d-TSEPs, parasitic parameters and working conditions can be determined by these calibration tests [39]. For higher accuracy of TSEP-based methods during operation, the parasitic parameter L_{eE} can be monitored to make sure it remains approximately constant during measurements. In the following paragraphs the experimental verification and performance comparison is presented separately for time-, v_{eE} voltage- and charge-based d-TSEPs.



(a)



(b)

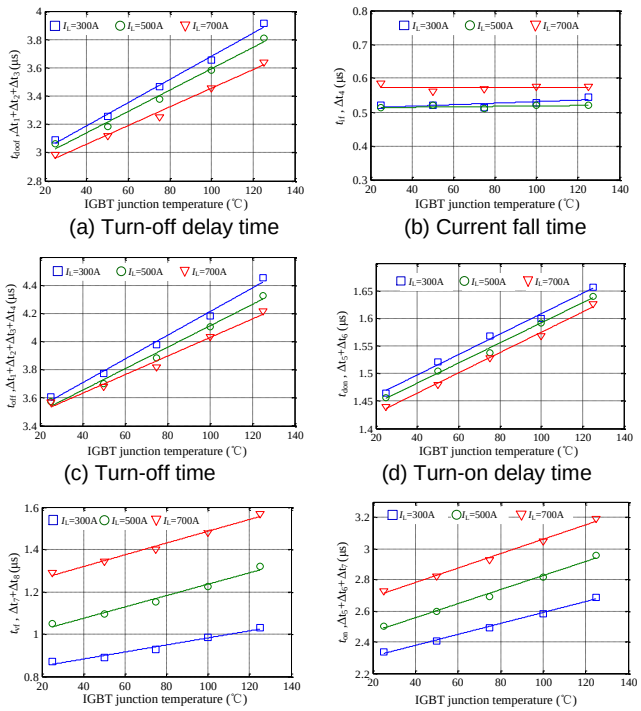
Fig. 8. High-power double pulse test platform. (a) Photograph of test platform; (b) Key test waveforms at V_{dc}=1800 V, I_L=500 A and T_j=25°C.

TABLE II
Specification of IGBT and Gate Driver

Parameters	Value	Parameters	Value
2 x IGBT modules (leg connection)	Fuji 1MBI800UG -330	Gate driver Voltage (v_{ge})	+15V on/ -10V off
Bus voltage (V_{dc})	1400V~ 1800V	Turn-on/off gate river resistor (R_{on}/R_{off})	2.4Ω /3.75Ω
Bus capacitor (C_{dc})	1000μF	P-i-N diode T_j	25ºC to 125ºC
Load current (I_L)	200A~700A	Stray inductance (L_{kE})	≈ 6nH
Load inductance (L_{load})	400μH	Parasitic inductor (L_{loop})	≈ 265nH

(1) Time-based d-TSEPs

In Fig.9, the experimental results concerning the six different time-based TSEPs are plotted. Even though a look-up table can be used in the presented methods, it is worth to point out that the achieved linearity is quite evident. However, the sensitivity of such methods widely varies from one to another. In Table III, the sensitivity comparison among the six time-based TSEPs is reported. From the experimental results in Fig.9 (b), it can be seen that t_{if} based-TSEP was impractical due to too low sensitivity. In fact, because of the current tail during turn-off transitions, the current derivative becomes very small, hence the related induced v_{eE} is not easily detectable. Regarding t_{doff}- and t_{off}-based TSEPs, both linearity and sensitivity are high. Besides, the sensitivity under high current conditions is a bit lower than that at low current. However, their sensitivity is strongly influenced by the junction temperature at fixed bus voltage. For example, in high temperature region such as 125 °C, the sensitivity is higher than that in low temperature region. On the other hand, t_{don}-based TSEP is characterized by fixed sensitivity in a wide T_j range. Concerning t_{vf}- and t_{on}-based methods, both of them have high linearity but lower sensitivity. It is worth noting that t_{vf} and t_{on}-based TSEP methods are also characterized by the approximate fixed sensitivity, like t_{don}-based TSEP. The medium and approximate fixed sensitivity make t_{don}, t_{vf} and t_{on}-based TSEP methods practical and easy to implement.



(a) Turn-off delay time (b) Current fall time

(c) Turn-off time (d) Turn-on delay time

(e) Voltage fall time (f) Turn-on time

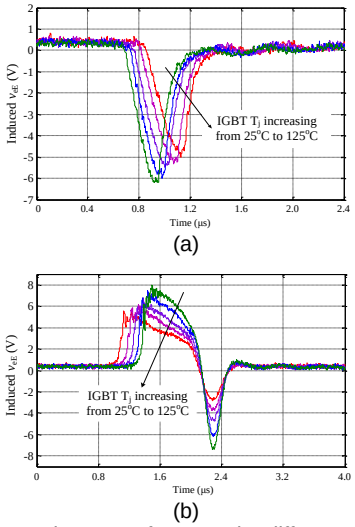
Fig. 9. Comparisons of six Time-based TSEPs under different load currents at fixed V_{dc}=1800 V. (a) turn-off delay time t_{doff}; (b) current fall time t_{if}; (c) turn-off time t_{off}; (d) turn-on delay time t_{don}; (e) voltage fall time t_{vf}; (f) turn-on time t_{on}.

TABLE III
SENSITIVITY COMPARISON AMONG TIME-BASED TSEPS

Identifier	Key Parameters	I_L impact	Maximum sensitivity
t_{doff}	$\Delta t_1+\Delta t_2+\Delta t_3$	Strong	8 ns/℃
t_{off}	$\Delta t_1+\Delta t_2+\Delta t_3+\Delta t_4$	Strong	9 ns/℃
t_{if}	Δt_4	Not applicable	Not applicable
t_{don}	$\Delta t_5+\Delta t_6$	No effect	2 ns/℃
t_{vf}	$\Delta t_7+\Delta t_8$	Weak	2.5 ns/℃
t_{on}	$\Delta t_5+\Delta t_6+\Delta t_7$	Weak	4.5 ns/℃

(2) Experimental results and performance comparison of v_{eE} voltage-based d-TSEPs

There are three voltage-based TSEPs: a) the v_{eE} peak value induced by the maximum turn-off di_c/dt; b) the maximum turn-on di_c/dt and c) the negative peak voltage during turn-on transition. In particular, the latter one is related to the maximum reverse recovery current of the diode, which can be usefully adopted for the diode T_j estimation. In Fig.10 (a) and (b) the induced v_{eE} waveforms at different IGBT junction temperatures are illustrated for the following conditions: V_{dc}=1800 V and I_L=700 A. The diode temperature is purposely kept at T_j=25 °C, to make measurements independent from it. In Fig.10 (a), the negative peak amplitude of v_{eE} shows a negative dependence on IGBT T_j. The induced negative peak v_{eE} is increasing from -6.2 V at 25 °C to -4.9 V at 125 °C, whose sensitivity is +13 mV/°C. A basic explanation is that the carrier lifetime increases with temperature, therefore the switching speed becomes lower at increasing T_j. The turn-on v_{eE} waveforms at different temperatures are depicted in Fig.10 (b). The positive peak v_{eE} also shows a negative trend. The induced peak value of v_{eE} is decreasing from 8 V at 25 °C to 5.5 V at 125 °C. The calculated sensitivity is -25 mV/°C.

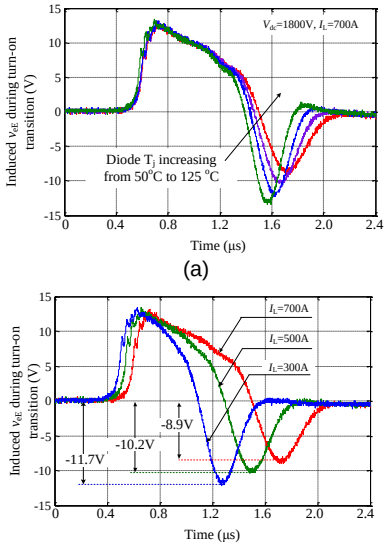


(a)

(b)

Fig. 10. Experimental v_{eE} waveforms under different IGBT T_j (V_{dc}=1800 V, I_L=700 A and diode T_j=25 °C). (a) Turn-off v_{eE} waveform comparison. (b) Turn-on v_{eE} waveform comparison.

In voltage source converters, the reverse recovery current di_d/dt is related to the switching speed of the IGBT, hence the IGBT junction temperature has been kept at T_j=25 °C. Fig.11 (a) shows the turn-on v_{eE} waveforms at different diode junction temperatures ranging from 50 °C to 125 °C, for the same working conditions as before: V_{dc}=1800 V, I_L=700 A. Accordingly, the temperature sensitivity is around +68 mV/°C. Because of the fixed IGBT T_j, the positive peak values of v_{eE} are the same, as they are related to the maximum turn-on di_c/dt of IGBT, as discussed before. The negative peak value of v_{eE} decreases with diode T_j. In Fig.11 (b), the turn-on v_{eE} waveforms at different load currents under the working conditions of V_{dc}=1800 V, diode T_j=125 °C and IGBT T_j=25 °C have been reported. At increasing load currents, the negative peak amplitude decreases from 11.7 V to 8.9 V.



(a)

(b)

Fig. 11. Experimental v_{eE} waveforms comparison under different working conditions with fixed V_{dc}=1800 V. (a) Turn-off v_{eE} comparisons under different diode T_j. (b) Turn-on v_{eE} comparisons under different I_L.

In Table IV, the sensitivity comparisons among the v_{eE}-based d-TSEPs under V_{dc}=1800 V and I_L=700 A are listed. For the v_{eE}-based approach, the sensitivity ratio of the peak value is several tens of millivolts per degree (mV/°C). Moreover, the maximum turn-off di_c/dt and di_d/dt exhibit positive sensitivity coefficient, while the maximum turn-on di_c/dt shows the negative sensitivity coefficient. The effects of positive and negative sensitivity should be taken into account in the peak value detector design.

TABLE IV
SENSITIVITY COMPARISON AMONG V_{eE}-BASED TSEPS

Identifier	Key Parameters	Maximum Sensitivity
$di_c/dt_{(max\_off)}$	$v_{eE}(t_4)$	+13 mV/°C
$di_c/dt_{(max\_on)}$	$v_{eE}(t_9)$	-25 mV/°C
$di_d/dt_{(max)}$	$v_{eE}(t_{11})$	+68 mV/°C

In [33], the dependence between diode T_j and the maximum recovery di_d/dt under different working conditions is analyzed in detail. An experimental mesh plot of the induced negative peak v_{eE} versus diode T_j and I_L at two bus voltages, namely V_{dc}=1600 V and V_{dc}=1200 V is shown in Fig. 12 (a). It is worth to make a comparison of the presented method and the well-established method of forward voltage drop at high current V_F [40]. The comparison between V_F-based method and negative peak v_{eE}-based method on the same device is demonstrated in Fig.12 (b). On the one hand, the maximum sensitivity of negative peak v_{eE}-based method is about 40 times higher than the value of V_F-based TSEP. Furthermore, the proposed method exhibits positive temperature coefficient, which is more convenient from the physical implementation point of view. On the other hand, V_F-based TSEP is independent of V_{dc}.

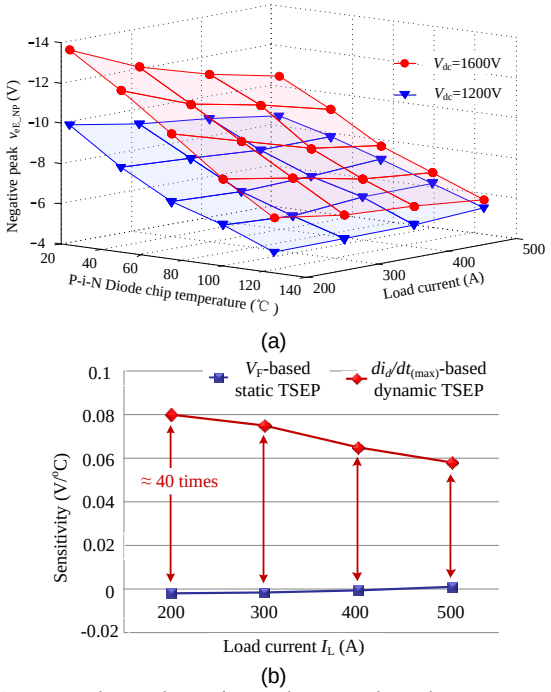


Fig. 12. Experimental results and comparison between V_F-based method and v_{eE_NP} based method. (a) Mesh plot of negative peak v_{eE} at different working conditions [33]. (b) Sensitivity comparison between V_F-based method and v_{eE_NP}-based method.

(3) Charge-based d-TSEPs

The turn-off induced v_{eE} waveforms at different T_j ranging from 25 °C to 125 °C at V_{dc}=1800 V and I_L=700 A are depicted in Fig.13 (a). For the sake of clarity, though, they have not been superimposed. The swept-out charge during turn-off transition has been calculated with (5) and plotted together with a fitting curve in Fig.13 (b). At 25 °C, the charge is about 95 μC. As the junction temperature increases to 125 °C, the charge decreases to 75 μC. Hence, the sensitivity for IGBT Q_{rrI} in Fig. 13(b) is around -0.2 μC/°C. According to theory of semiconductor physics, the stored charge increases with T_j due to the increase in carrier lifetime [41]. However, because the switching speed becomes slower at increasing T_j, more stored charge recombines in the base region, ending up in a reduction in the swept-out charge.

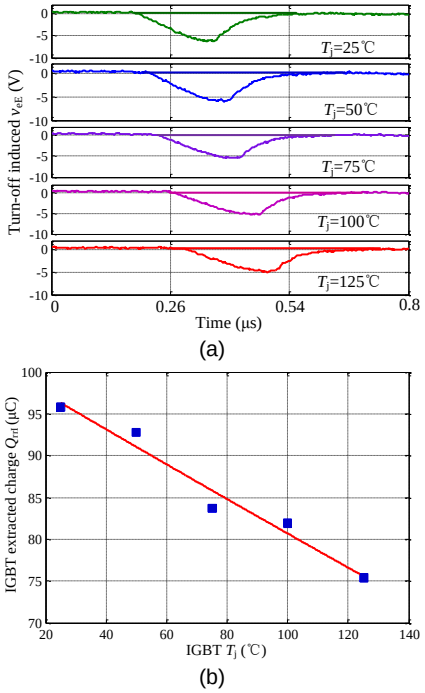


Fig. 13. Turn-off induced v_{eE} waveforms at different IGBT T_j range from 25°C to 125°C and calculated swept-out charge. (a) Turn-off v_{eE} waveform comparisons. (b) Calculated swept-out charge using v_{eE}-based approach.

Regarding the diode related Q_{rrD}, the relations among the extracted charge during the reverse recovery falling, bus voltage, load current and junction temperature have been discussed and experimentally verified in [36]. For the same module Fuji-1MBI800UG-330, the maximum sensitivity for diode related Q_{rrD} is around -0.17 μC/°C at V_{dc}=1600 V, I_L=500 A. As a result, the sensitivity ratio of charge-based d-TSEPs is a few tenths of microcoulomb per degree (μC/°C) with the negative sensitivity coefficient.

V. CHALLENGES AND PERSPECTIVES OF PROPOSED METHODS

Since the switching characteristics depend on gate driver parameters, the proposed dynamic TSEPs are affected by the gate resistances. The experimental comparison between two different gate resistance combinations (1: R_{on}=2.4 Ω / R_{off}= 3.75 Ω and 2: R_{on}= 6.8 Ω / R_{off}=6.8 Ω) at V_{dc}=1600 V, I_L=500 A and T_j=25 °C are shown in Fig.14 (a) and (b). Because of the increased gate resistance, both the turn-on and turn-off

switching speeds get lower. Hence, the maximum turn-off di_c/dt of combination 2 is lower than that of combination 1, as depicted in Fig.14 (a). At the same time, the turn-off time at higher gate resistance toff1 is longer than t_{off2}. On the contrary, the current fall time at higher gate resistance is shorter than that of lower gate resistance. In Fig.14 (b), the turn-on v_{eE} waveform comparison is depicted. Due to the slow switching speed, the voltage-oriented TSEPs tend to lower the values. Besides, time-oriented TSEPs become larger at larger gate resistances. Generally speaking, the selection of gate resistance has an impact on the dynamic TSEPs. Since the power module and external circuit parameters are usually fixed after the hardware design, the gate driver parameters can be treated as fixed values for the assembled converters. As a consequence, the calibration process can be carried out after the determined circuit parameters.

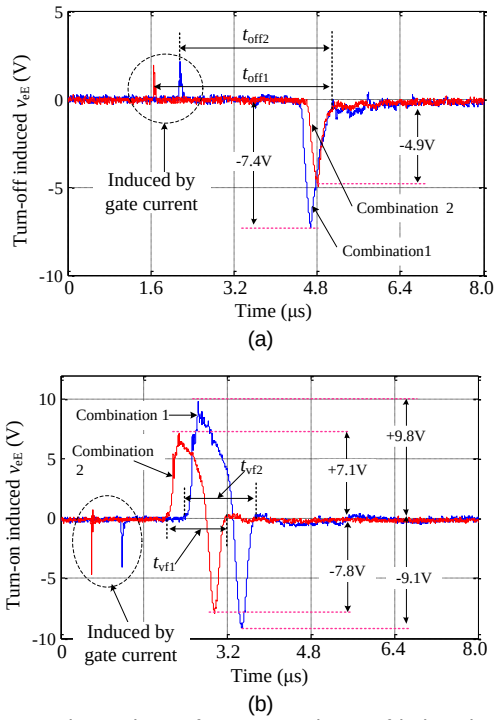


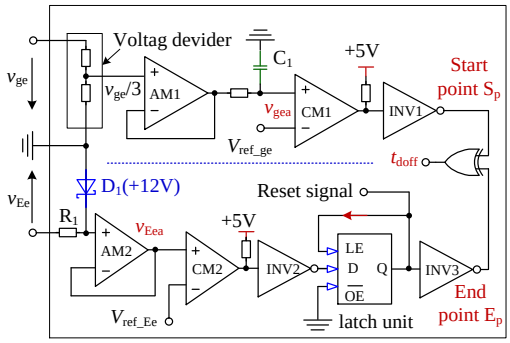
Fig. 14. Experimental waveform comparisons of induced v_{eE} between different gate resistance combinations (V_{dc}=1600 V, I_L=500 A, T_j=25 °C) (a) R_{on}=2.4 Ω / R_{off}=3.75 Ω. (b) R_{on}=6.8 Ω / R_{off}=6.8 Ω.

In terms of generality, it is worth to point out that gate-related dynamic TSEPs only apply to active power devices. Compared with the proposed v_{eE}-based dynamic TSEP methods, they are not applicable to diodes. Indeed, there is no universal solution for particular IGBT modules. Since the operation T_j vary with working conditions, the most suitable TSEP method should be selected from the aforementioned TSEPs with different properties. Compared with the static TSEPs and published dynamic TSEPs without v_{eE}-based approaches, v_{eE}-based approach provides a unified evaluation system for various types of dynamic TSEPs. According to the classification of v_{eE}-based approach, the appropriate TSEP candidate can be reasonably selected for a given module.

VI. A Case Study for On-line Tj Estimation

A. Measurement circuit for t_{doff}

In this section, t_{doff}-based TSEP method is taken as a case study for the on-line T_j variation investigation. The block diagram of the t_{doff} measurement circuit and related circuit appearance are shown in Fig.15. The proposed t_{doff} measurement circuit is mainly composed of operational amplifiers (AM, TL072BCD), high-speed comparators (CM, LM393), inverting Schmitt triggers (INV, 74HC14D), latch unit (SN74HCT573AD) and exclusive-or gate (CD4070B). Besides, the supply voltages for operational amplifies are ±12V, and +5V for the comparators and logic circuits.



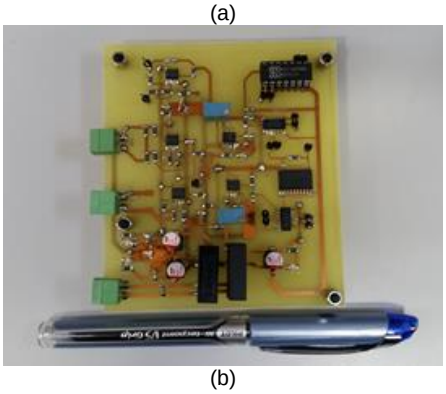


Fig. 15. (a) Turn-off delay time measurement circuit schematic. (b) Measurement circuit appearance.

The key waveforms for the t_{doff} start point S_p capture are depicted in Fig.16 (a). Firstly, S_p pulse is generated from the turn-off gate voltage v_{ge} [42]. By means of the resistor voltage divider, one-third v_{ge} is fed to the comparator CM1 through the voltage follower AM1. Notably, to dampen oscillations at the beginning of turn-off related to the fast voltage transient, a filter capacitor C_1 (18 pF) is inserted into the circuit. The filtered voltage v_{gea} is then compared with the detection threshold levels V_{ref_ge} (+4V). Finally, a positive S_p pulse is obtained via the inverting trigger INV1.

Concerning the end point detection, the second v_{eE} voltage spike induced by di_c/dt is used (see Fig.16 (b)). Firstly, to eliminate the signal interference, Zener diode D_1 and resistor R_1 are used to bypass the first voltage spike of v_{eE}. Another use of +12 V breakdown voltage for Zener diode D_1 is to protect the amplifier AM2. Then, the AM2 output v_{Eea} is compared with the threshold voltage V_{ref_Ee} (+1 V). Then, through an inverter INV2, a negative pulse is generated. It is worth noting that INV2 output negative pulse length varies with the di_c/dt duration Δt_4, which represents the collector current fall time. Considering the t_{doff} end point, only the first falling edge of

negative pulse is useful to determine E_p. In order to latch the first falling edge signal, the latch unit output signal (Q) is connected to the latch enable terminal (LE). As a result, the output low-voltage state can be latched and kept after the first falling edge signal, and this latched pulse represents t_{doff} end point. Finally, a positive pulse is generated by INV3, and this pulse is in accordance with the induced voltage v_{Ee}. Importantly, after the detection of the first falling edge signal, a reset signal is required to reset the latch unit for the next t_{doff} detection.

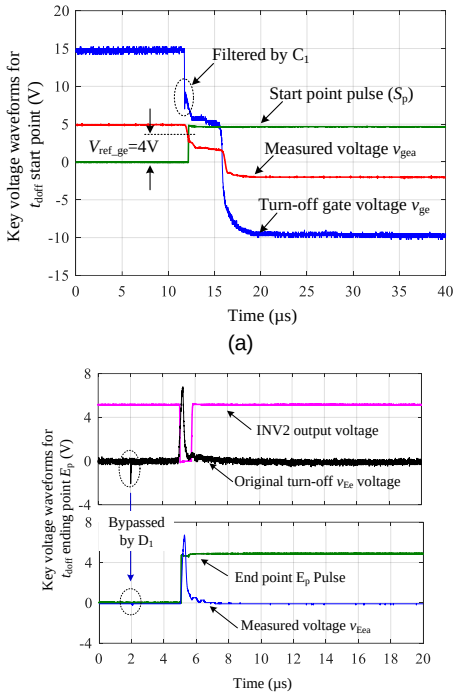


Fig. 16. Experimental tests of turn-off delay time measurement circuit. (a) Start point pulse detection for turn-off delay time. (b) Ending point pulse detection for turn-off delay time.

As a result, by using an exclusive-or gate, a positive pulse related to the turn-off delay time can be extracted. In Fig.17, the key turn-off waveforms and extracted t_{doff} pulse under double pulse test platform are depicted. The extracted t_{doff} is around 2.94 μs, which is consistent with the test results plotted in Fig.9 (a). In practice, the pulse length represents the turn-off delay time and can be applied to the look-up table.

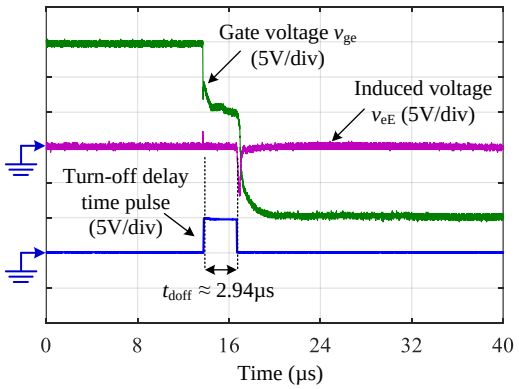


Fig. 17. Experimental turn-off waveforms and extracted turn-off delay time pulse (Fuji 1MBI800UG-330, V_{dc}=1800 V, I_L=700 A and T_j=25 °C).

B. Online T_j variation estimation

In order to verify the effectiveness of the proposed d-TSEP method through inductance L_{eE} for the online T_j estimation, an H-bridge based high-power converter has been used to investigate the high-power IGBT modules rated at 1700 V/1000 A. The appearance of H-bridge converter is shown in Fig.18.

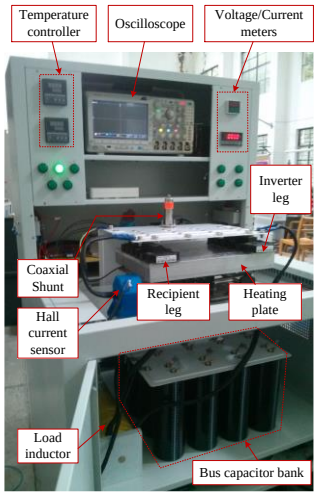


Fig. 18. Appearance of high-power H-bridge converter.

Accordingly, the associated experimental parameters and the platform specifications are given in Table V. The IGBT modules under test are from Infineon (FF1000R17IE4) [29]. Being the module under test used in wind power converters, the bus voltage V_{bus} is controlled at around 1050 V level [43]. Hence, in this study, the bus voltage is fixed at 1050 V by means of a high voltage regulator. At the beginning of tests, a calibration for the given IGBT modules should be carried out on the platform. Then, the turn-off delay time t_{doff} using induced v_{eE} is selected as a d-TSEP candidate for the following on-line T_j estimation. During the turn-off transition, a measurable voltage v_{eE} on parasitic inductance L_{eE} is induced by the variation of gate and collector current. According to the definition of turn-off delay time t_{doff}, the temperature-dependent t_{doff} can be extracted by the synchronous voltage spike on v_{eE}.

TABLE V
SPECIFICATIONS AND PLATFORM TEST CONDITIONS

Parameters	Value	Parameters	Value
IGBT modules	FF1000R17IE4	Gate driver Voltage v_{ge}	+15V on/-10V off
Bus voltage V_{dc}	≈ 1050V	Gate resistances R_{on}/ R_{off}	2 Ω/ 3.75 Ω
Bus capacitance	12 mF	Switch frequency	2.5 kHz
L_{load}	320 μH	Fundamental frequency	50 Hz
R_{th_IGBT}	10.5 °C/kW	Initial case temperature	50 °C

In terms of t_{doff}-based TSEP, a mesh plot is built on the basis of calibration test and depicted in Fig.19. The experimental results are consistent with the theoretical analysis in [23]. By taking the advantage of the good linear dependency between t_{doff} and the working conditions, the real-time IGBT T_j can be estimated by the fitting polynomial

$$T_j = -201.4 + 1.173\times10^{8} t_{doff} - 1.015\times I_L + 7.013\times10^{5} t_{doff} I_L - 5.975\times10^{-5} I_L^2 \quad (13).$$

In T_j estimation procedure, the instantaneous v_{eE} is needed to be recorded along with the load current. In this work, the instantaneous v_{eE} is recorded by means of oscilloscope (Tektronix MDO3034) and the related t_{doff} is extracted in MATLAB. Then, the real-time T_j variation can be calculated by (13).

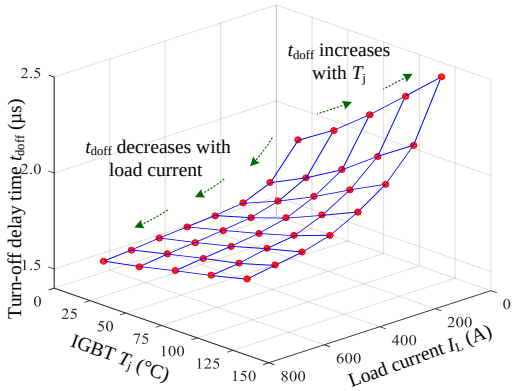


Fig. 19. Mesh plot of t_{doff}-based TSEP at different load current and junction temperature under $V_{dc}\approx$ 1050V.

Before the test, IGBT modules are heated and maintained at 50 °C to emulate the maximum ambient temperature and then the converter is run for 2 seconds. The collector voltage v_{ce} of the lower IGBT in the inverter leg and the related output load current I_L for the last two sinusoidal periods are demonstrated in Fig.20 (a).The root-mean-square of load current I_L is around 533 A. The turn-off peak collector voltage v_{ce} is proportional to the load current. The maximum turn-off peak v_{ce} reaches 1250V due to the parasitic loop inductances. Correspondingly, the extracted t_{doff} and the estimated T_j variations are estimated by the mesh plot and depicted in Fig.20 (b). The maximum T_j reaches 120 °C while the average junction temperature is around 100 °C. The estimated T_j variation is in the range of 79 °C to 120 °C ($\Delta T_j\approx$ 41°C). More importantly, the estimated T_j variation is consistent with the output sinusoidal load current.

Additionally, the simulated junction temperature variation curve in PLECS environment is also plotted in Fig.20 (b). With the aid of 1-D thermal model [43], the relationship between the normal operation and junction temperature of inspected IGBT modules can be simulated. In this work, the thermal impedance parameters and conduction power losses are collected from the IGBT datasheet. Moreover, the practical switching power losses are measured by the calibration tests. According to the simulated T_j variation, the simulation delta T_j is around 39°C, which is in consistent with the results from t_{doff}-based method. It is worth noting that there is temperature difference between estimation and simulation results after the peak T_j. Besides, since there is no switching operation during the cooling stage, the practical IGBT T_j variation cannot be obtained by mean of t_{doff}-based method. Finally, the sensitivity and accuracy of TSEP-based methods will be carried out in the future work.

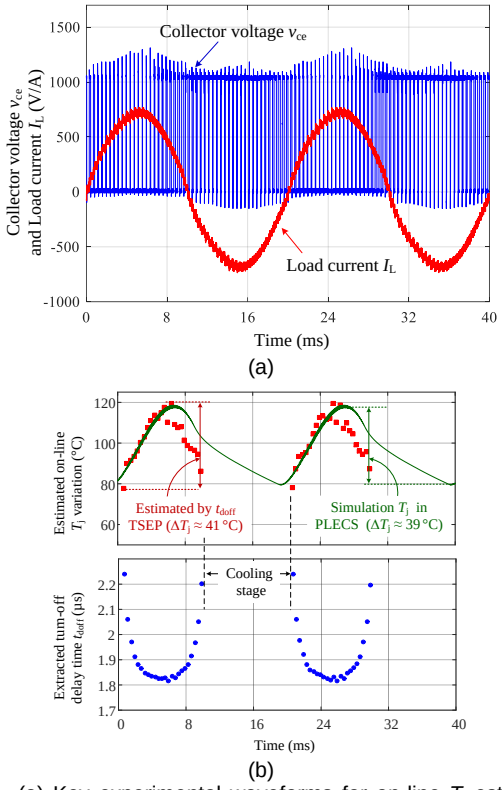


Fig. 20. (a) Key experimental waveforms for on-line T_j estimation in condition of $I_L\approx$ 533 A, power factor PF=-1 and f_s=2.5 kHz. (b) On-line extracted turn-off delay time variation and related estimated T_j variations.

VII. Conclusion

This paper has presented an extraction approach of junction temperature for high-power IGBT modules. By means of the inherent stray inductance L_{eE}, a family of d-TSEP candidates has been extracted and most of them have been proved to be profitably exploited for on-line junction temperature extraction. The advantage of proposed v_{eE}-based extraction approach is that it is intrinsically noninvasive. Another relevant advantage is that measurements on the high-voltage side can be performed at the low-voltage side, which is beneficial both from the cost and simplicity standpoints. The proposed d-TSEP based methods can be applied to IGBT modules and diodes by means of look-up tables or linear functions. A high-power IGBT double pulse test platform has been built to verify the effectiveness of the proposed d-TSEP extraction methods. As a case-study, with the aid of an H-bridge high-power converter, the on-line T_j variation has been extracted and estimated by the turn-off delay based d-TSEP method. Experimental results confirmed that the found d-TSEP based methods are very promising in non-invasive junction temperature estimation for IGBTs and diodes.

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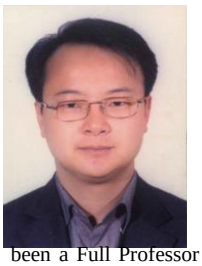

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