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On-line solder layer degradation measurement for SiC-MOSFET modules under accelerated power cycling condition

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Abstract

In order to distinguish die-attach solder layer and bond wire degradation during power cycling tests, a simultaneous on-line measurement method is proposed in this paper. To measure accurately solder layer voltage drop, the intrinsic diode is used as heating source in place of the MOSFET switch. In this way, the measurement method becomes intrinsically insensitive to possible threshold voltage shifts, typical of accelerated test of SiC power MOSFETs. Finally, the experimental results are presented to verify the feasibility of the proposed test method. It is revealed that the solder layer resistance increases linearly with the number of cycles in good approximation.

1. Introduction

Silicon Carbide (SiC) material is characterized by higher critical electric field, higher saturated velocity and higher thermal conductivity in respect to silicon [1]. However, the higher operation temperatures that can be achieved with the SiC technology, brings new reliability issues, especially at package level. By means of accelerated cycling tests, both die and packaging reliability issues can be investigated thoroughly within short time.

According to previous studies, the most vulnerable parts in power modules after long-term accelerated cycling tests are bond wires and die attach solder layer, as shown in Fig.1 [2].

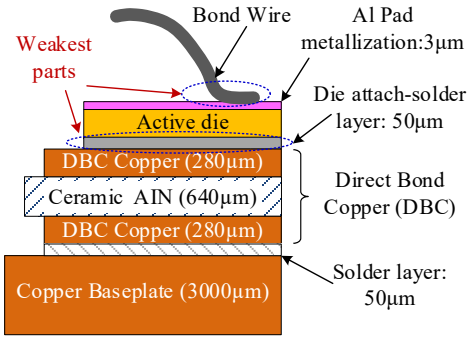

Fig.1. Schematic cross-section of a SiC power module.

Due to the thermal expansion coefficient mismatch among the different materials, the module packages, especially bond wires and solder layer, experience an irreversible degradation over long-term operation. So far, a lot of studies have been devoted to evaluate and monitor the bond wire degradation process [3,4]. The voltage cross the Drain to Source terminal V_{DS} is usually used as an ageing indicator to evaluate the degradation process of package. In power cycling test, the V_{DS} increase mainly consists of the bond wire and solder layer degradations. The solder layer degradation cannot be distinguished from the measured Drain to Source voltage. So far, few of the mentioned studies have addressed the solder layer degradation measurements. Since the die backside is not accessible, there is no possible way to measure the voltage cross the solder layer directly. In practice, the solder layer degradation is usually evaluated by means of thermal impedance measurement and Scanning Acoustic Microscopy (SAM) method after the power cycling tests [5]. However, the test equipment for SAM analysis is very expensive and time-consuming. Moreover, the conventional SAM method cannot be used for on-line measurement and evaluation.

To solve the above problems, an on-line measurement method to detect solder layer

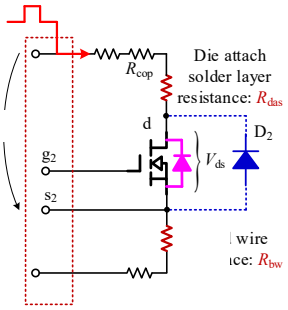

Fig. 2. Equivalent circuit of a SiC power device considering parasitic resistances.

degradation for SiC-MOSFET modules during power cycling test is proposed. Taking the advantage of the auxiliary source terminal, both the solder layer resistance and the bond wire degradation can be measured simultaneously. In order to avoid the SiC die degradation caused by the threshold voltage shift [6], the intrinsic diode is used for load current conduction. More importantly, the intrinsic diode is the first used to monitor solder layer degradation. Finally, the resistance increase of the die attach solder layer can also be distinguished from SiC die degradation itself.

2. Proposed measurement method

2.1. Problem statement in conventional method

The equivalent circuit of a MOSFET power module considering the parasitic resistances and external measurement terminals is shown in Fig.2. R_{Pbw} is the parasitic resistance of positive power terminal, R_{cop} is the parasitic resistance of copper layer, R_{Nbw} is the parasitic resistance of negative power terminal, R_{das} is the die attach solder layer resistance, V_{ds} is the die voltage under load current I_{load}, R_{bw} is the die attach bond wire resistance and R_{Nbw} is the parasitic resistance of negative power terminal. In order to avoid the common source resistances R_{bw} and R_{Nbw}, an additional terminal known as the Kelvin-source (s_2) is used for gating the power device.

According to the independent measurement method proposed in [7], the die attach solder layer resistance increase R_{das} can be measured indirectly by means of the voltage V_{Ds}. Correspondingly, the measurable voltage V_{Ds} consists of the SiC die resistance V_{ds}, R_{das}, R_{cop} and R_{Pbw}. Since the power terminal related bond wire parts are far away from the die during the test, R_{Pbw} and R_{cop} can be considered as constant. However, another additional challenge is the question of threshold voltage shift as the device degrades [8,9].

Under elevated temperature and gate voltage conditions, the gradual threshold voltage shift would lead to SiC die degradation, which causes the die resistance to change significantly. In [10], it is studied that the change in V_{DS} is very fast at the beginning of test in an average variation of 0.81% for 1000 cycles (V_{gs}=15V, T_{min}=175°C and ΔT_j=43°C). Therefore, the conventional measurement method using the on-state voltage of the MOSFET die cannot be applied to monitor the solder layer resistance increase because of the variable die voltage.

2.2. Proposed measurement method

In order to monitor the solder layer resistance increase, the potential threshold voltage shift related to the die degradation should be avoided. Since the MOSFET die contains an intrinsic body diode, this internal diode can also be used as a heating source for the desired T_j swing. More importantly, there is no die degradation mechanism for intrinsic diode such as the threshold voltage shift. Hence, the increased voltage during the test can be attributable to the package degradation rather than the die degradation. A commercial SiC MOSFET module from CREE (CCS020M12CM2) has been selected as a study case, and the internal layout for single phase bridge is depicted in Fig. 3(a). Besides, the related equivalent circuit and measurement principle are depicted in Figure 3(b). In order to bypass the external diode D_2, the two bond wires are cut as shown in Fig. 3(a). As depicted in Fig. 3(b), there are three measurable voltages V_{cD}, V_{sD} and V_{ND} under specific DC load current. Among them, voltages V_{sD} and V_{ND} contain the packaging related degradation information.

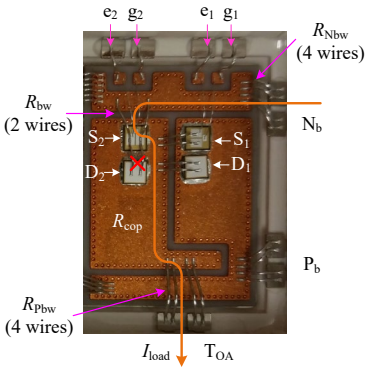

Fig.3 (a) Picture of the internal layout of a SiC power device.

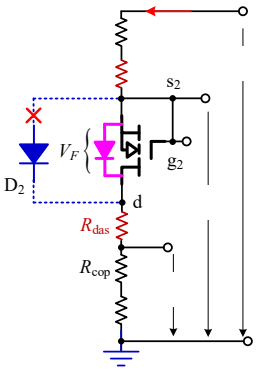

Fig.3 (b) Equivalent circuit considering external measurement terminals.

Considering the voltage V_{sD}, it includes three voltage drops, given by:

$$V_{sD}=V_F+V_{cD}+I_{load}\cdot R_{das} \quad (1)$$

Assuming there is no degradation on the intrinsic diode (V_F), copper layer (R_{cop}) and power terminal bond wires (R_{pbw}), the die attach solder layer resistance increase ΔR_{das} can be calculated by

$$\Delta R_{das}=\Delta V_{sD}/I_{load} \quad (2)$$

In general, the parasitic resistance R_{das} cannot be measured directly, but the resistance increase ΔR_{das} can be monitored.

Another conventional failure case we consider is the bond wire degradation. Since R_{Nbw} can be regarded as constant during the tests, the bond wire resistance can be calculated by

$$V_{ND}= V_{sD} +I_{load}\cdot(R_{bw}+R_{Nbw}) \quad (3)$$

In case of fixed load current, the bond wire resistance increase ΔR_{bw} can be obtained by the voltage difference between V_{ND} and V_{sD}, as expressed by

$$\Delta R_{bw}=\Delta(V_{ND}-V_{sD})/I_{load} \quad (4)$$

3. Test conditions

In order to validate the proposed method to be able to distinguish between solder degradation and bond wire lift off, a power cycling test platform was built. A SiC module from CREE (CCS020M12CM2) has been tested. The test conditions for the SiC modules are listed in Table I. The selected temperature swing is in the range of 25°C to 85°C. The average temperature was adjusted by means of an external heating system. The injected load current was 17 A. The online T_j is measured with isolated optical fiber system from Opsens [10]. Moreover, the measurement positions for the optical fibres as well as the voltage probes are carefully selected to get accurate measurement results.

TABLE I. TEST CONDITIONS FOR CREE MODULE

Parameters	Conditions	Parameters	Conditions
Maximum T_j	85 °C	Period/duration	4s / 8s
Minimum T_j	25 °C	Base plate temperature	≈ 23 °C
Delta T_j	60 °C	Drain current I_{DS}	17 A

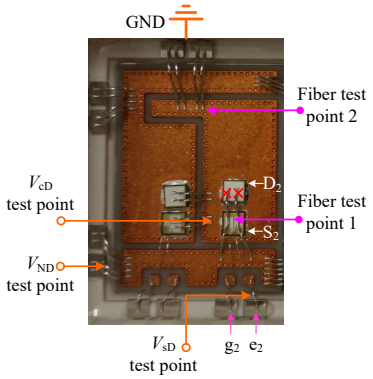

Fig. 4 Selected measurement points for temperature swings monitoring and voltage measurements.

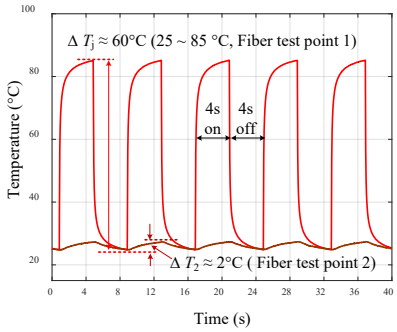

Fig.5 Temperature swings of the junction temperature of the SiC MOSFET and the power terminal bond wires.

In Fig. 4, the implementations of the voltage and temperature measurement are depicted. Considering the T_j swing, one test point is selected at the center of SiC die. In order to investigate the thermal stress for the power terminal bond wires, the fibre test point 2 is selected at the copper area connected to the bond wires. In Fig. 5, the on-line temperature waveforms for the SiC die and power terminal bond wires have been plotted. It is shown that the temperature swing for the power terminal bond wires is around 2 °C. This means that the parasitic resistance R_{Nbw} can be regarded as constant since the temperature stress is negligible.

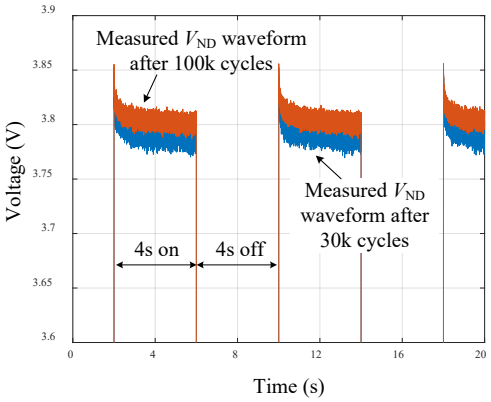

Fig.6 Key waveform comparisons for measured voltage V_{ND} after 30k and 100k cycles.

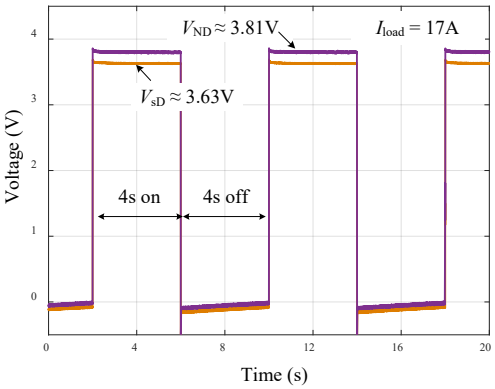

Fig.7 Experimental waveforms of measured V_{ND} and V_{sD} after around 100 k cycles**.**

4. Experimental results

The measured voltage V_{ND} after 30 k and 100 k cycles are depicted in Fig. 6 for the sake of comparison. The increased voltage contains two parts of resistance increase: bond wire resistance increase and solder layer resistance increase. However, based merely on V_{ND}, the solder layer resistance increase cannot be distinguished from the bond wire resistance increase.

In Fig. 7, the key voltage waveforms after 100k cycles are depicted. The final average voltage for V_{ND} is around 3.81 V, which includes the bond wire resistance increase and solder layer resistance increase. Since the resistance R_{cop} and R_{Nbw} are constant, the voltage V_{sD} increase can be attributed to the solder layer resistance increase. Besides, the average V_{sD} during the conduction pulse is around 3.63 V.

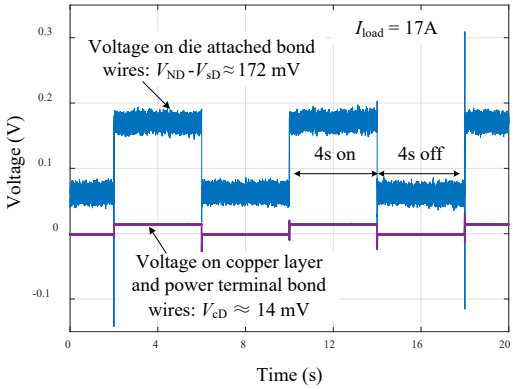

Fig.8 Experimental waveforms of measured (V_{ND}-V_{sD}) and V_{cD} after around 100 k cycles**.**

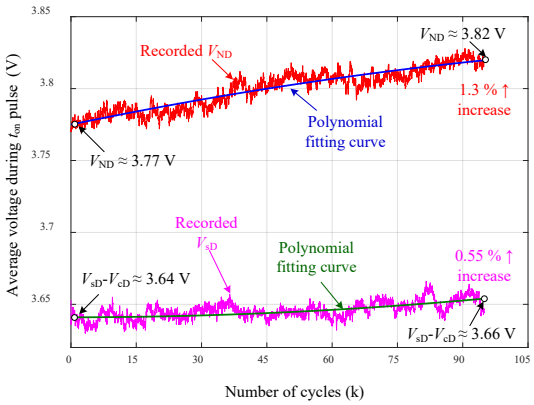

Fig.9 Key waveforms of bond wire and die-attach solder layer degradations.

In Fig. 8, the measured V_{cD} and bond wire voltage are depicted. In case of I_{DS}=17A, the voltage V_{cD} is around 17 mV. In addition, the bond wire voltage can be worked out by subtracting V_{sD} from V_{ND}. After around 100k cycles, the measured average bond wire voltage is 172 mV. Different with the diode die resistance, the measured waveforms on copper layer and power bond wires are independent of the junction temperature variation.

The recorded voltages and related polynomial fitting curves for the device under test are plotted in Fig. 9. According to the polynomial fitting curve for voltage V_{sD}, there is around 0.55% increase after 100k cycles. Correspondingly, the voltage increase is around 20 mV, and the related resistance increase ΔR_{das} is 1.18 mΩ. Meanwhile, the measured voltage V_{ND} increases from 3.77V to 3.82 V after 100k cycles.

The SAM images and comparison between intact SiC die (S_1) and aging die (S_2) after power cycling test are shown in Fig.10. The solder layer damage was investigated in KSI V8 scanning acoustic microscope (SAM) system from IP Holding. Practically, SAM analysis is done by soaking a sample in liquid. Since the SiC die S_1 did not be tested, the SAM image about S_1 shows normal quality of die attach solder layer without any degradation.

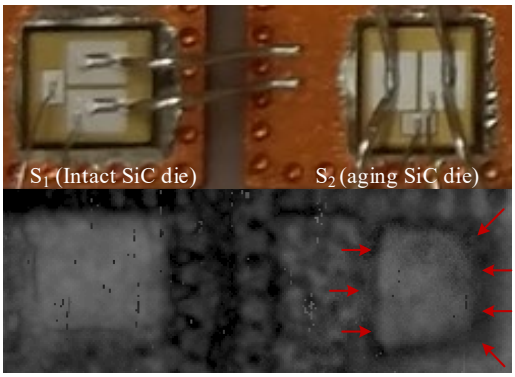

Fig.10 SAM images and comparison for device under test (S_2) and intact SiC die (S_1) after power cycling test.

5. Conclusion

This paper has presented an online measurement method for solder layer degradation monitoring under power cycling tests. By means of the auxiliary source terminal, both the solder layer resistance increase and bond wire resistance increase can be measured separately. In order to avoid the die resistance change due to the threshold voltage shift, the intrinsic diode is not only used as a heating source, but also to get rid of the MOSFET threshold voltage dependence on aging process during the power cycling tests. Experiments were implemented to verify the effectiveness of the proposed method. By using SAM method, the degradation of die attach solder layer is scanned. With the number of cycles, the solder layer resistance increases linearly in good approximation.

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