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Published in:
I E E E Transactions on Power Electronics

DOI (link to publication from Publisher):
10.1109/TPEL.2017.2682114

Publication date:
2018

Document Version
Early version, also known as pre-print

Investigation and Classification of Short-Circuit Failure Modes Based on Three-Dimensional Safe Operating Area for High-Power IGBT Modules

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Abstract –IGBT short-circuit failure modes have been under research for many years, successfully paving the way for device short-circuit ruggedness improvement. The aim of this paper is to classify and discuss the recent contributions about IGBT short-circuit failure modes, in order to establish the current state of the art and trends in this area. First, a 3D-SCSOA is introduced as the IGBT's operational boundary to divide the short-circuit failure modes of device into short-circuit V_{DC}/V_{rated}-I_{SC} SOA limiting and short-circuit endurance time limiting groups. Then, the discussion is centered on currently reported IGBT short-circuit failure modes in terms of their relationships with the 3D-SCSOA characteristics. In addition, further investigation on the interaction of 3D-SCSOA characteristics is implemented to motivate advanced contributions in future dependency research of device short-circuit failure modes on temperature. Consequently, a comprehensive and thoughtful review of where the development of short-circuit failure mode researches of IGBT stands and is heading is provided.

***Index terms*– High power IGBTs, Short-circuit failure mode, 3D-SCSOA, Self-heating, Temperature dependency**

None of the material in this paper has been published or is under consideration for publication elsewhere.

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This work is sponsored by the National Basic Research Program of China (973 Program 2014CB247400) and the National Nature Science Foundation of China (5167716)

I. INTRODUCTION

Nowadays, Insulated-Gate-Bipolar-Transistors (IGBTs) are one of the most important power devices in medium and high power converter applications ranging from few hundred volts to several thousand volts [1-2]. However, recent studies also report that IGBT is the major fragile component for power conversion systems. More specifically, it accounts for nearly 34% of failures in converter systems [3-4]. Especially, in the field of high power converter applications, such as high speed traction systems and megawatt-level renewable energy generation systems, the damage could not be limited in device itself once the failure occurs. There is not so low possibility that the damage would extend to the entire facility or system. Consequently, it would cost both economically and socially expensive. Thus, it is necessary not only to minimize the device power dissipation but also to disclose the failure modes limiting the ruggedness of IGBTs under extreme operating conditions which cannot be avoided in long-term operations.

One of the most common scenarios of the extreme operating conditions for IGBTs is the short-circuit operation, under which the device is unexpectedly turned on or operating at a negligible load inductance [5-6]. As a result, a huge current flows though the IGBT only limited by the device itself, meanwhile the full DC-link voltage is held across it. Due to the large energies normally involved, an IGBT short-circuit failure can have a severe influence if left uncontrolled.

Generally, in terms of the intrinsic thermal limit of IGBTs, manufacturers can guarantee short-circuit withstand capability of commercial devices up to 10μs to

prevent the device from those direct thermal runaway failure types [7-8]. However, besides reaching this thermal limit, additional transient failure modes can occur to instantly destabilize the IGBT under the short-circuit operation, which makes the specification of 10μs short-circuit withstand capability on longer valid. For example, the peak current failure [10-11] and self-turn-off failure [12-13] can drive the device into destruction instantly during the v_{ce}-desaturation process of short-circuit operation. So far, no withstand capability nor safe operating area (SOA) of IGBTs is specified or related to each of these transient short-circuit failure modes. Moreover, some critical operation conditions, such as the DC-link voltage, bus-bar parasitic inductances, and gate driving conditions, can even worsen the impacts of these device failure modes on the entire system. As a result, the requirements concerning short-circuit reliability and ruggedness for IGBTs in practical applications are much higher [14]. Thus, constructing the short-circuit SOA (SCSOA) to prevent the device from as many failure modes as possible is more important than ever before.

However, to enable a wide SCSOA for IGBTs, one key starting point is to fully understand the limiting impacts of different failure modes on the device short-circuit ruggedness. It is of great importance to disclose the detailed relationships between the IGBT short-circuit failure modes and SCSOA boundaries. Therefore, the main focus of this paper is on this topic. More specifically, this paper is structured as follows. In Section II, A three-dimensional SCSOA (3D-SCSOA) is proposed first to classify the device short-circuit failure modes as the short-circuit V_{DC}/V_{rated}-I_{SC} SOA limiting group and short-circuit endurance time limiting group. Basing on it, the present

reported device short-circuit failure modes covered by the upper two groups are respectively reviewed and discussed in Section III and Section IV, in terms of their connections with the 3D-SCSOA characteristics. Moreover, in Section V, the interaction of 3D-SCSOA characteristics is pointed out to motivate further investigation of dependencies of different device short-circuit failure modes on temperature. Finally, some conclusions are drawn in Section VI.

II. 3D-Short-Circuit Safe Operating Area for IGBT Modules

In general, for IGBTs, the traditional SCSOA is specified as the short-circuit endurance time t_w in terms of the device thermal runaway limit induced by the energy accumulation [7-9]. It is usually characterized as an index how long an IGBT can withstand the thermal accumulation until the protection circuit can shut off the unexpected large short-circuit current safely. But, as mentioned in Section I, except those direct thermal runaway failure types, some transient failure modes can still occur to immediately destroy the device. Thus, it is necessary not only to define t_w for those direct thermal runaway failure modes but also to specify SCSOA for those transient failure types, in order to maintain sufficient short-circuit ruggedness for the IGBT.

Therefore, a 3D-SCSOA for IGBTs is proposed and illustrated in Fig.1, of which I_{SC} is the short-circuit current and t stands for the short-circuit operation time. In general, for a given IGBT, the maximum voltage that can be sustained by the device is its rating voltage V_{rated}. Therefore, the full-voltage range that can be applied to the device is approximate to (0V~V_{rated}). Meanwhile, the full-voltage range of the

3D-SCSOA for a given IGBT is also (0V~V_{rated}). In order to describe the voltage sustaining condition across the device within its full-voltage range (0~V_{rated}), the voltage ratio V_{DC}/V_{rated} between the applied DC-link voltage V_{DC} and V_{rated} is used to define the device 3D-SCSOA instead of directly using V_{DC}. Under this scenario, the full-voltage range of the device 3D-SCSOA can be accordingly expressed as (0~1).

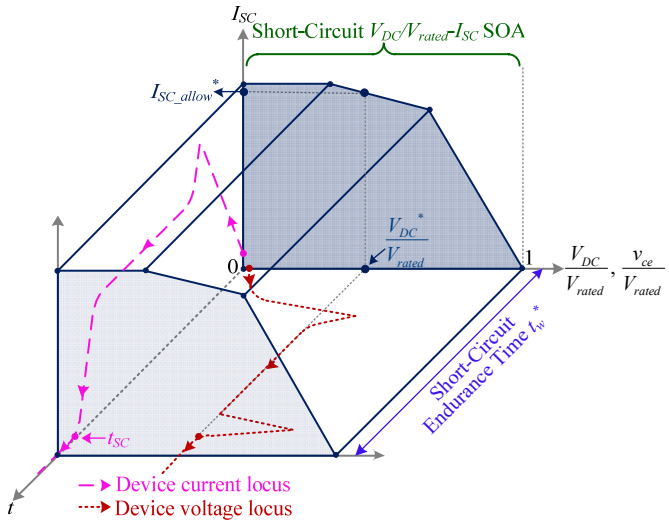

Fig.1. 3D-SCSOA characteristics for IGBT (using short-circuit type II operation of device as an example, v_{ce} is the device collector-emitter voltage, t_{SC} is the short-circuit operation time)

In Fig.1, except for the classical t_w^{*} specified by the direct thermal runaway failure modes, a new short-circuit V_{DC}/V_{rated}-I_{SC} SOA is added for those transient failure types. Thus, the IGBT 3D-SCSOA is made up of two characteristics, namely the short-circuit endurance time and short-circuit V_{DC}/V_{rated}-I_{SC} SOA. Actually, basing on the detailed failure mechanism, for each of those transient short-circuit failures, a V_{DC}/V_{rated}-I_{SC} SOA exists which can guide the device operation to avoid the corresponding failure occurring. Consequently, the overlap region of these individual V_{DC}/V_{rated}-I_{SC} SOAs will form the final short-circuit V_{DC}/V_{rated}-I_{SC} SOA for an IGBT. As shown in Fig.1, for the given DC-link voltage V_{DC}^{*}, the maximum allowable

short-circuit current $I_{SC\_allow}^{*}$ is specified for the device by this final short-circuit V_{DC}/V_{rated}-I_{SC} SOA. Thus, keeping short-circuit current locus of an IGBT lower than $I_{SC\_allowe}^{*}$ can guarantee the device getting rid of all of those transient failures at the V_{DC}^{*} case.

Moreover, in terms of the intrinsic thermal limit of IGBTs, t_w has distinct dependencies on I_{SC} and V_{DC}. Therefore, for each of the individual short-circuit operation condition (V_{DC}/V_{rated}, I_{SC}) located at the boundary of the short-circuit V_{DC}/V_{rated}-I_{SC} SOA, the corresponding value of t_w should be different. For example, in Fig.1, t_w^{*} is the short-circuit endurance time corresponding to the short-circuit operation condition (V_{DC}^{*}/V_{rated}, $I_{SC\_allow}^{*}$). In other words, t_w^{*} represents the maximum allowable short-circuit operation time at the V_{DC}^{*} and $I_{SC\_allow}^{*}$ case, that can guide the protection circuit to activate timely (namely keeping $t_{SC} \leq t_w^{*}$) and avoid driving the device into directly thermal runaway failure types.

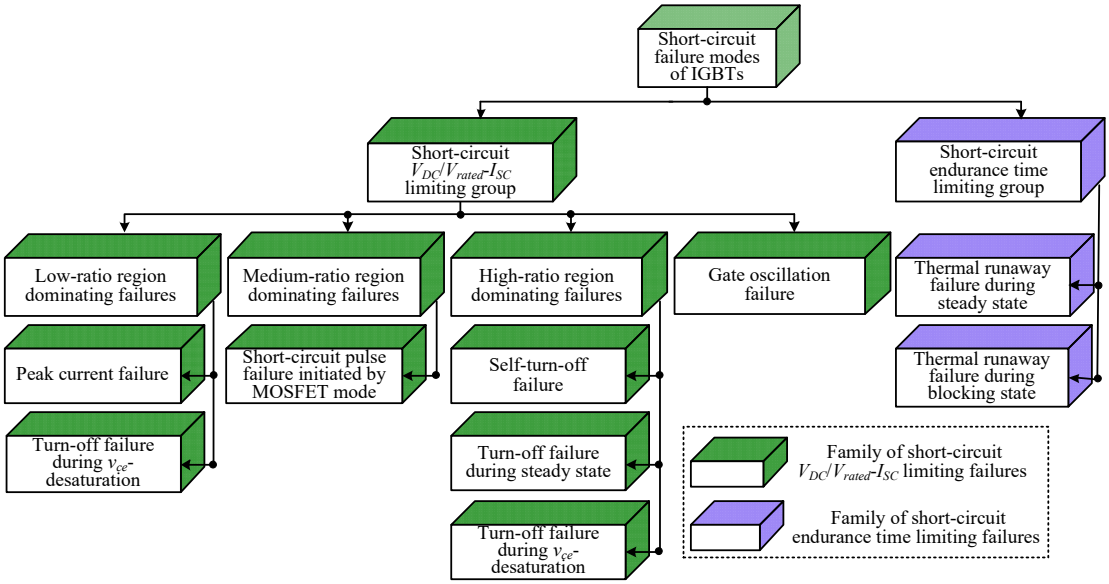

Fig.2. IGBT short-circuit failure modes classification

Consequently, the IGBT short-circuit failure modes can be accordingly classified into the short-circuit V_{DC}/V_{rated}-I_{SC} limiting group and short-circuit endurance time

limiting group. The overview of the present reported short-circuit failure types of IGBTs are summarized and highlighted in Fig.2. The detailed analysis and discussion will be addressed in the following sections.

III. SHORT-CIRCUIT V_{DC}/V_{RATED}-I_{SC} SOA LIMITING GROUP

In this section, a comprehensive survey of short-circuit V_{DC}/V_{rated}-I_{SC} SOA limiting failure modes is presented and discussed. As illustrated in Fig.3, six distinct failure modes of an IGBT may occur to instantly drive the device to destruction at different time during short-circuit type II operation. The same is true for the short-circuit type I operation with a lager parasitic inductance.

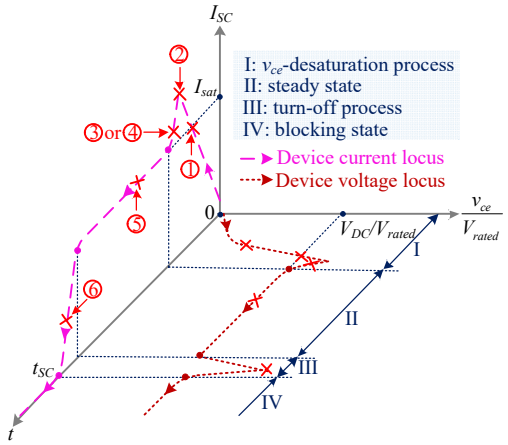

Fig.3. IGBT transient failure modes during short-circuit type II operating (①turn-off failure during v_{ce}-desaturation, ②peak current failure, ③self-turn-off failure, ④gate oscillation failure, ⑤short-circuit pulse failure initiated by MOSFET mode, ⑥turn-off failure during steady state)

However, as limiting factors for the device short-circuit V_{DC}/V_{rated}-I_{SC} SOA, these six transient failures will compete with each other to play the dominating role within the device full-voltage range. As for which one will attract more attentions mainly depends on their dependencies on the voltage sustained by the device during the short-circuit operations [9, 15-20]. In other words, within the device full-voltage

range (0V~V_{rated}), different voltages applied across the device will result in different dominating-failures during the short-circuit operations. As defined in Section II, the voltage ratio V_{DC}/V_{rated} is used to describe the voltage applied condition across the device within the device full-voltage range. Thus, the dependencies of six different transient failures on the applied voltage can be characterized by this voltage ratio.

Consequently, in terms of different voltage-dependent properties of these six transient failures, the full-voltage range (0~1) of the device short-circuit V_{DC}/V_{rated}-I_{SC} SOA can be accordingly divided into three regions, namely: low-ratio, medium-ratio and high-ratio region, seeing Fig.4. Meanwhile, the dominating transient failures corresponding to each region have been classified into the same subgroups, as the low-ratio region dominating failures, medium-ratio region dominating failures, and high-ratio region dominating failures, as displayed in Fig.2. As for the detailed voltage-dependent characteristics of these transient failures, they will be explained in the following parts relating to each subgroup.

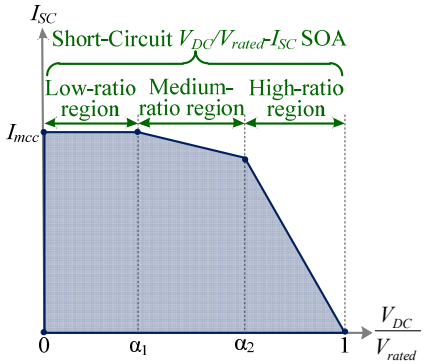

Fig.4. Dependency of IGBT short-circuit V_{DC}/V_{rated}-I_{SC} SOA on V_{DC}

Moreover, as mentioned in Section II, the short-circuit V_{DC}/V_{rated}-I_{SC} SOA of an IGBT is actually the final overlap region of each of the individual V_{DC}/V_{rated}-I_{SC} SOAs corresponding to six different transient failure modes. However, after incorporating

the dependencies of different failure modes on the applied voltage, the device short-circuit V_{DC}/V_{rated}-I_{SC} SOA can be formed by three individual V_{DC}/V_{rated}-I_{SC} SOAs. They are respectively corresponding to the low-ratio region, medium-ratio region and high-ratio region dominating subgroups. More specifically, for each transient-failure subgroup, a maximum allowable short-circuit current I_{SC_allow} at a given V_{DC}/V_{rated} can be predicted to the device. It is the last-past short-circuit current of the device without triggering the corresponding transient failure at the given V_{DC}/V_{rated}. As shown in Fig.4, α_1 and α_2 are respectively the voltage-ratio values of the cross-points between these three V_{DC}/V_{rated}-I_{SC} SOAs. However, the detailed building process of this final short-circuit V_{DC}/V_{rated}-I_{SC} SOA is out of the range of this paper.

A. Low-Ratio Region Dominating Failures

Peak current failure is generally considered as the predominant limiting factor for the short-circuit V_{DC}/V_{rated}-I_{SC} SOA at low V_{DC}/V_{rated} applications [8-9, 15-18]. It means that this peak current failure has the highest possibility to be triggered when the applied V_{DC} across the device is belongs to the low-ratio region of the device full voltage range (0V~V_{rated}). It can be usually connected with the latch up of the intrinsic parasitic thyristor inside the IGBT [9, 21] and expected to occur close to peak current during the short-circuit operation as shown in Fig.3.

As known to all, IGBT is characterized by its MOS channel capability in current self-limiting which can saturate the device short-circuit current [9, 13]. But when the latch up of the internal parasitic thyristor is activated, this current self-limiting capability will be malfunctioned immediately. Then, a continual increase is observed

of the device short-circuit current, eventually resulting in the peak current failure. This is to say, this peak current failure limits the maximum controllable current I_{mcc} of IGBT which is also the upper current boundary of device short-circuit V_{DC}/V_{rated}-I_{SC} SOA at the low-ratio region of the device full-voltage range, seeing Fig. 4.

Actually, for today's commercial IGBTs, they are relatively less sensitive to this failure than those old generations due to the advanced latch-up suppress designs [22]. It is especially the case when the short-circuit current is homogeneously distributed between the cells. Therefore, recent research focus about this latch-up mechanism has gradually transformed to as a subsequent failure mechanism initiated by the current inhomogeneity phenomenon, such as the current filamentation effect [23-24].

However, if the holes sustained by extracting the n^--base region electron-hole plasma take part in the current transport, the IGBT sensitivity to this latch-up mechanism will increase significantly. It is the generally called dynamic latch-up phenomenon, for which the maximum controllable current is much lower comparing with the one determined by the former latch-up effect [21]. Meanwhile, this dynamic latch-up phenomenon can be generally connected with a high-plasma turn-off process, especially at the low V_{DC}/V_{rated} applications [25-26]. As for the short-circuit operation, the turn-off condition during the v_{ce}-desaturation process before v_{ce} reaches V_{DC} is a typical high-plasma turn-off case [27]. Therefore, under this scenario, in combination with a low V_{DC}/V_{rated} application, the impact of the dynamic latch-up mechanism will set in to result in a turn-off failure during the v_{ce}-desaturation process, as displayed in Fig.3. Thus, it generally must be ensured that a hard turn-off is not initiated before v_{ce}

rises to V_{DC}. Otherwise, this turn-off failure during the v_{ce}-desaturation process will severely shrink the low-ratio region boundary of the short-circuit V_{DC}/V_{rated}-I_{SC} SOA defined by the former peak current failure.

B. Medium-Ratio Region Dominating Failures

With the increase of the applied V_{DC}, the maximum allowable short-circuit current I_{SC_allow} for a given V_{DC} specified by the short-circuit V_{DC}/V_{rated}-I_{SC} SOA will be lower than I_{mcc} determined by the former latch-up relating failure types. It is the short-circuit pulse failure initiated by the MOSFET mode that limits I_{SC_allow} at the medium V_{DC}/V_{rated} region of the device full-voltage range [15, 27-28]. It can be generally triggered by a current filamentation effect of the device operating under the MOSFET mode and characterized as a typical failure type for the steady state of short-circuit process (as shown in Fig.3).

As mentioned above, the MOSFET-mode operation of IGBT plays a critical role in activating this failure [14-15, 27, 29-32]. Comparing with the normal-mode operation, the most distinct difference of it is the location of the electric-field peak E_{max} inside the n^--base region. More specifically, under the MOSFET-mode operation, E_{max} can shift from the emitter-side p-well/n^--base junction to collector-side n^--base/field-stop junction with the rising short-circuit saturated current I_{SC_sat}, seeing Fig.6. In contrast, E_{max} is typically located at the emitter-side p-well/n^--base junction for the normal-mode.

Further, under this scenario, the impact of V_{DC} on the operation-mode transformation sets in [15, 27]. Especially, for a medium V_{DC}/V_{rated} application within

the device full-voltage range, a mixed situation with the normal mode operating at the emitter side and MOSFET mode operating at the collector side of n⁻-base region develops, seeing Fig.7. It is the critical condition to accelerate and sustain a current self-constraint process inside the IGBT which can be readily initiated by any potential inhomogeneity due to the manufacturing [27]. As a result, a collector-side current filament will form inside the device and leads to an instant destruction of an IGBT at the short-circuit steady state.

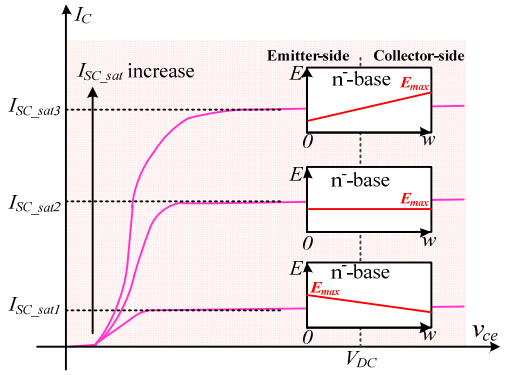

Fig.6. Transformation of n⁻-base region electric-field distribution *E* with increasing current under MOSFET-mode operation (output characteristic is displayed in the background, I_C is the device collector current, *w* is the distance from the emitter side.)

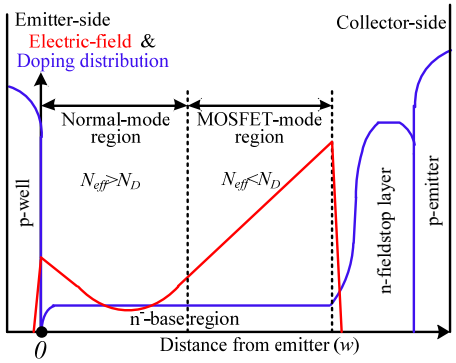

Fig.7. Mixed operation mode of device at medium DC-link voltage application (N_{eff}: effective doping concentration of n⁻-base, N_D: intrinsic doping concentration of n⁻-base)

In contrast, this mixed operation condition would be replaced by a full normal-mode or MOSFET-mode operation inside the n⁻-base region, respectively for the low V_{DC}/V_{rated} and high V_{DC}/V_{rated} applications. Then, the necessary condition for

the self-enhancing formation of current filament is missing. In other words, this collector-side current filament is more possible to form at the medium V_{DC}/V_{rated} application for a given I_{SC_sat} within the device full-voltage range (as displayed in Fig.8) [15, 27]. Therefore, the boundary of short-circuit V_{DC}/V_{rated}-I_{SC} SOA at the medium-ratio region is usually limited by this short-circuit pulse failure.

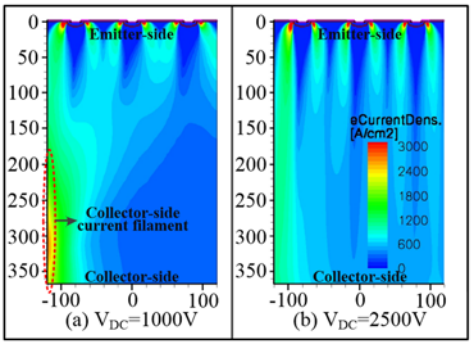

Fig.8. Electron current density of a 3.3kV IGBT for different DC-link voltages during steady-state phase of short-circuit [15]

Moreover, an optimized large bipolar current gain β_{PNP} is pointed out that can enable the device to avoid the MOSFET mode and prevent the device from this short-circuit pulse failure [33]. As for the value of β_{PNP}, it is directly related to the device collector-side design, such as the thickness and doping profile of the field-stop layer and p-emitter layer [34-35].

C. High-Ratio Region Dominating Failures

As explained in Part B, the IGBT ruggedness to resist the upper short-circuit pulse failure increases with the rising V_{DC}. Thus, at high V_{DC}/V_{rated} region of the device full-voltage range, this failure mode is less crucial for restricting I_{SC_allow}, and then there comes the influence of turn-off failures [20, 32, 36]. For an IGBT operating under short-circuit conditions, three different kinds of turn-off failures probably occur to destroy the device. They are respectively the turn-off failure during the

v_{ce}-desaturation process, self-turn-off failure and turn-off failure during the steady state, as presented in Fig.3.

Further, these three turn-off failures can be distinguished by whether a high-concentration electron-hole plasma exists in the n^--base region or not during the initial short-circuit turn-off process. As mentioned in Part A, the turn-off failure during the v_{ce}-desaturation process is generally triggered during a high-plasma turn-off transition. In contrast, the latter two failure modes usually take place without a high-plasma inside the n^--base region [27-28]. Actually, the corresponding turn-off processes for them are initiated after v_{ce} reaches V_{DC}, under which the electron-hole plasma stored in the n^--base region has been exhausted. Therefore, comparing with the turn-off failure during the v_{ce}-desaturation process, the latter two failure modes can all get rid of the impacts of the electron-hole plasma. However, a distinct difference of the initial turn-off mechanism exists between them.

More specifically, for the self-turn-off failure, the negative differential Miller capacitance effect generally sets in to drive the IGBT turning itself off rather than receiving a turn-off signal from the superior control [12, 28]. It is a typical IGBT unstable mechanism for short-circuit types with the v_{ce}-desaturation process, such as the short-circuit type I with large parasitic inductances or short-circuit type II. In general, it can be characterized by a negative displacement current flowing though the device Miller capacitance, which initiates the discharge of the gate-emitter capacitance [37-38]. Consequently, a self-turn-off phenomenon is activated with a drop in the gate voltage v_{ge} after v_{ce} reaches V_{DC} during the v_{ce}-desaturation process, as

illustrated in Fig.9.

Besides, the failure characterization and mechanism of the latter two turn-off failures are almost the same. As for the underlying failure mechanism, another current filamentation effect caused by the negative differential resistance (NDR) region is the necessary destruction precondition [28, 36, 39-40]. Differing from the former collector-side current filament forming under the MOSFET-mode operation, this one appears at the emitter-side of the IGBT. Moreover, the indispensable triggering condition for it is that the device is operating at the NDR branch of the avalanche breakdown curve, initiated by strong avalanche breakdown inside the IGBT (as displayed in Fig.10). Meanwhile, the critical role of the device bipolar current gain β_{PNP} in generating this NDR branch of the device avalanche breakdown curve has been indicated by many researches [28, 34-35]. As presented in Part B, β_{PNP} can be adjusted and optimized by the IGBT collector-side designs.

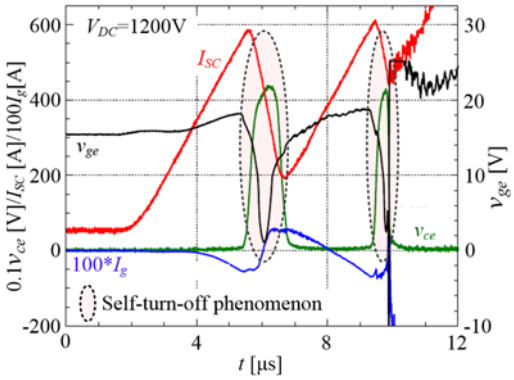

Fig.9. IGBT self-turn-off phenomenon during v_{ce}-desaturation process under short-circuit type II operation [28]

In addition, for this emitter-side filamentary current, two different kinds of current-filament form exist, respectively leading to different subsequent failure mechanisms for the IGBT. More specifically, one is the static current filament which

will directly drive the device into thermal runaway [41]. In contrast, the other one is the hopping current filament, of which the latch up of the corresponding cells is more likely to be triggered as a subsequent failure mechanism [42]. As for the factors that influence the forms of the current filament, both the layout of the chip level and gate drive voltage are of great importance [43-44]. Especially, the chip-level layout, it can be generally connected with an interplay between the device active and termination region. It plays a crucial role in determining the detailed form and location of the current filament inside the device. Meanwhile, in terms of different turn-off voltages applied at the device gate terminal, this interplay between the device active and termination region can be correspondingly weakened or strengthened.

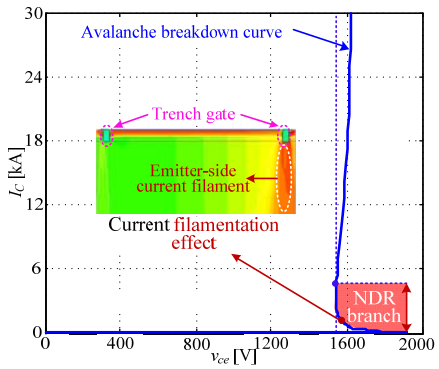

Fig.10. 1700V/1000A IGBT avalanche breakdown curve and current distributing characteristics

Generally, in terms of the avalanche breakdown during the IGBT turn off, no high plasma exists inside the n^--base region will distinctly improve the avalanche ruggedness of the device [45]. As a result, the designed static voltage blocking capability V_{rated} of the IGBT can be more fully utilized under a self-turn-off process or a turn-off process during the steady state. This is to say, the relative values of the triggering voltages for the self-turn-off failure and turn-off failure during the steady

state against V_{rated} are more approaching to 1. In other words, as limiting factors for the IGBT short-circuit V_{DC}/V_{rated}-I_{SC} SOA, these two turn-off failures will play dominating roles in high-ratio region of the device full-voltage range [20, 32, 39].

However, as introduced in Part A, for a high-plasma turn-off process, the holes extracted from the n^--base region plasma will participate in the transport of the I_{SC}. At the high V_{DC}/V_{rated} applications, the avalanche breakdown effect is more sensitive to this hole extraction phenomenon than the latch-up effect, which will weaken the avalanche ruggedness of the device [20, 27]. This is the usually called dynamic avalanche phenomenon. Moreover, at high V_{DC}/V_{rated} cases, it is the major failure mechanism for the turn-off failure during the v_{ce}-desaturation process before v_{ce} reaches V_{DC}. Thus, the high-ratio region boundary specified by the former self-turn-off failure and turn-off failure during the steady state will be further shrunk by this turn-off failure. In combination with the low V_{DC}/V_{rated} case presented in Part A, a short-circuit turn off is generally recommended that should not be initiated before v_{ce} reaches V_{DC}, in order to enable a wide short-circuit V_{DC}/V_{rated}-I_{SC} SOA.

D. Gate Oscillation Failure

Differing from the upper investigated six failure modes, a stability map defined by the gate parasitic inductance and gate resistance is usually specified to the gate oscillation failure mode instead of a V_{DC}/V_{rated}-I_{SC} SOA, as displayed in Fig.11 [46].

In general, this gate oscillation failure is initiated by the gate oscillation phenomenon (illustrated in Fig.12). Due to the fact that this unstable oscillation phenomenon can be usually connected with the negative differential Miller

capacitance effect [48], thus it is also a typical failure mode for the IGBT operating at the short-circuit condition with a v_{ce}-desaturation process.

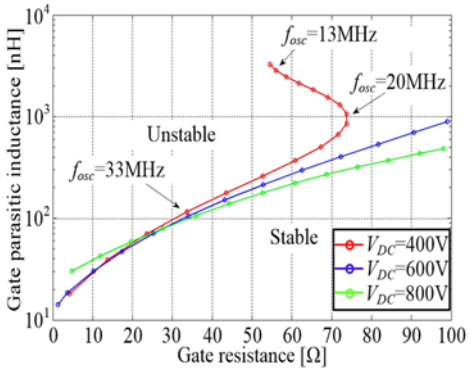

Fig.11. Stability map for device gate oscillation phenomenon at V_{DC}=400V, 600V and 800V; for some point, the oscillation frequency is also reported [46]

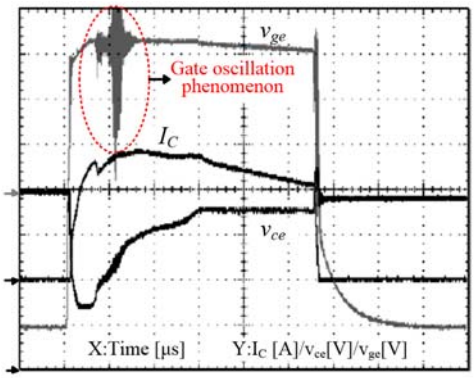

Fig.12. Gate oscillation phenomenon under short-circuit type I with large parasitic inductance [47]

More specifically, this failure mode is intrinsically triggered by the interaction among the equivalent negative Miller capacitance, gate parasitic inductance and gate resistance. Above all, the equivalent negative Miller capacitance can further enable a more readily condition for a diverging and unstable gate oscillation which would finally result in the gate oxide breakdown of the IGBT [49]. However, as mentioned at the beginning of this part, a stability map usually can be specified to help the device avoiding this diverging oscillation phenomenon.

IV. SHORT-CIRCUIT ENDURANCE TIME LIMITING GROUP

In this section, a review of the short-circuit endurance time limiting failure types is explored. More specifically, two potential short-circuit failure modes that limit the device short-circuit endurance time t_w are illustrated in Fig.13. One is the thermal runaway failure during the steady state (⑦), the other one is the thermal runaway failure during the blocking state (⑧) [26, 50-51]. Both of them are initiated by the thermal accumulation during the short-circuit pulse without any other failure mechanism setting in.

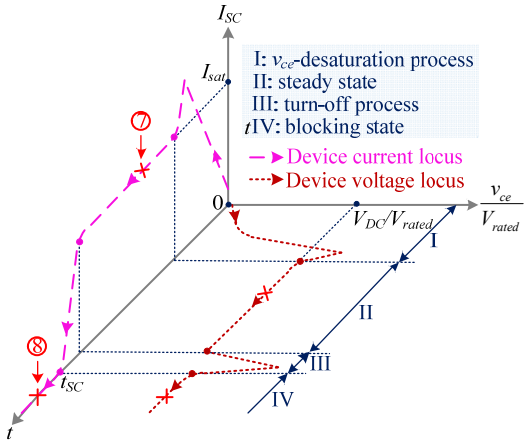

Fig.13. IGBT short-circuit endurance time limiting failure types during short-circuit type 2 operating

A. Thermal Runaway Failure During Steady-state

In general, due to the large current and high voltage characteristics of the short-circuit steady state, a huge amount of energy is deposited in the IGBT which will result in a high rise in the device temperature. Further, without timely shutting off this large short-circuit current, the IGBT temperature would eventually reach the device critical thermal runaway limit. As a result, the doped silicon becomes intrinsic and the IGBT voltage blocking capability deteriorates due to the burn down of the device [52]. This is why and how the traditional SCSOA (namely the short-circuit

endurance time t_w) is specified and defined by the device manufacture. As shown in Fig.13, a 10μs of t_w under specified short-circuit operation conditions (as listed in Table I) is generally guaranteed by the device manufacture. In other words, operating within the specified operation boundary, the IGBT can enable itself at least 10μs withstand capability for the energy accumulation without triggering the thermal runaway failure during the short-circuit pulse.

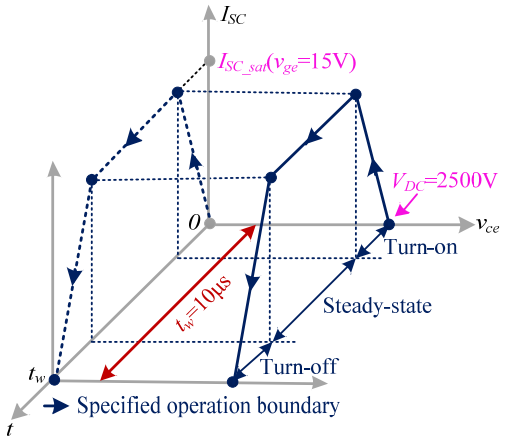

Fig.13. Traditional SCSOA boundary in 3D for INFINEON 3.3kV/1.5kA IGBT

TABLE I. SPECIFIED OPERATION CONDITIONS FOR TRADITIONAL SCSOA DEFINITION OF INFINEON 3.3kV/1.5kA IGBTs

Operation Condition	Value
Gate voltage v_{ge}	15V
DC-link voltage V_{DC}	2500V
Case temperature T_C	125℃
Maximum allowable junction temperature T_{vj}	150℃

Nowadays, the manufactures devote themselves in enlarging t_w for IGBTs. In Fig.13, during the short-circuit pulse, the high amount of energy E_{SC} deposited in the device can be approximately calculated by

$$E_{SC} = V_{DC} \times I_{SC\_sat} \times t_w \tag{1}$$

of which the critical energy E_{SC} accumulated in the device to activate the thermal runaway failure is almost uniquely limited by the silicon material itself [8]; Moreover, V_{DC} is also constant in the general application. Thus, the only solution to extend t_w for

an IGBT is to maintain I_{SC_sat} sufficiently low. In general, this can be realized by the optimized design of the IGBT cell structure, such as the advanced wide cell pitch CSTBTs (carrier stored trench-gate bipolar transistors) from Mitsubishi [8].

B. Thermal Runaway Failure During Blocking-State

As mentioned above, an IGBT can generally avoid the former thermal runaway failure under the guidance of t_w. Nowadays, the device thermal runaway failure is actually more likely to occur during the blocking state rather than during the steady state of short-circuit operation, as illustrated in Fig.14 [26].

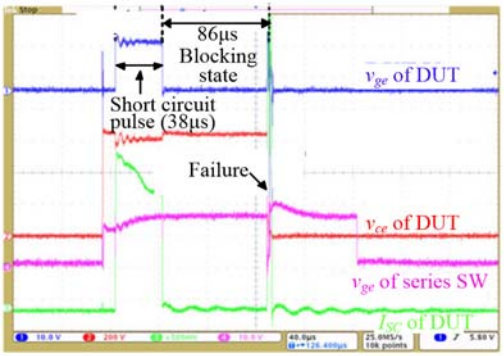

Fig.14. IGBT short-circuit failure by thermal runaway at 86µs after safety turn-off [26]

In Fig.14, after successful withstanding the short-circuit operation of 38µs, the device under test (DUT) is turned off safely. But, this IGBT is still destroyed by a thermal runaway failure after 86µs of the turn off. This type of thermal runaway failure can be usually connected with the high-temperature leakage current caused by the heat spreading from the IGBT p-well/n$^-$-base junction to the collector-side layer after the short-circuit turn-off process [27-28].

More specifically, in the blocking state, the IGBT collector side will be heated up by the energy accumulated during the short-circuit pulse, due to the heat diffusing. Then, the influence of β_{PNP} which is mainly determined by the IGBT collector-side

properties sets in. As a result, in terms of the positive temperature-dependent β_{PNP}, the leakage current $I_{leakage}$ that flows though the IGBT during the blocking state increases with the rising device collector-side temperature [53]. Thus, in this scenario, a high leakage current in combination with the full DC-link voltage across the device would drive the IGBT into a destructive self-heating loop with a thermal runaway failure as a result. Moreover, in practical operations, various factors producing the inhomogeneous operation inside the device definitely exist, which will accelerate this failure occurring [54]. For example, for a multi-cell IGBT chip, considering the possible deviations in the threshold voltage, transconductance and so on, it is obvious that the short-circuit current should have some variations for each unit cell. Thus, the local region in active area, which has the largest applied energy, will obviously more possible to suffer this thermal runaway failure. Besides these electrical-property deviations, the distributions in the thermal parameters of the IGBT module are also important to investigate the cause of the inconsistencies. Consequently, this thermal runaway failure during the blocking state also plays an important role in limiting t_w of the device, as presented in Fig.15 [54].

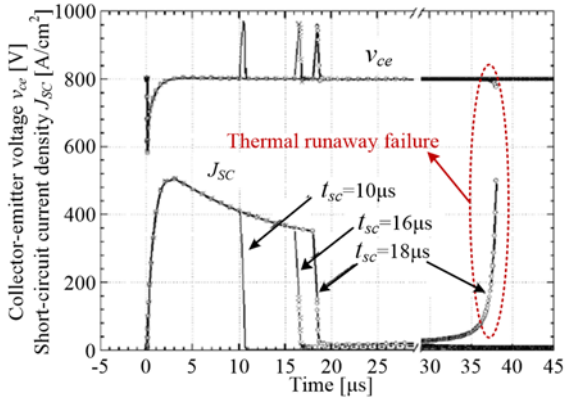

Fig.15. IGBT short-circuit waveforms for different short-circuit operation time t_{SC} [54]

Nowadays, the device manufactures also try to help the IGBT getting rid of this

type of the thermal runaway failure. As explained above, it can be intrinsically ascribed to the positive dependency of β_{PNP} on temperature. Currently, a field-stop layer with a deep-level doping (such as the selenium) is used to mitigate or even eliminate this positive dependency of β_{PNP} on temperature [55-56]. In addition, optimized layout designs of the device chip level and module level are also promising ways to help to improve the device ruggedness for this thermal runaway failure.

V. Interaction Investigation of 3D-SCSOA Characteristics

The evolution of researches on the short-circuit failures over the last two decades has paved the way for several state-of-the-arts in the device ruggedness and reliability improvement. Basing on this well-developed area, as summarized in this paper, some further investigation on future constructing the device 3D-SCSOA can be implemented.

As introduced in Section II, the 3D-SCSOA is made up of two different characteristics, namely the short-circuit V_{DC}/V_{rated}-I_{SC} SOA and short-circuit endurance time t_w. They are respectively specified to guide the IGBT to avoid the two short-circuit failure groups classified above. More specifically, for the two thermal runaway failure modes presented in Section IV, at least 10μs of t_w can be generally guaranteed by the manufactures. In contrast, so far, no available short-circuit V_{DC}/V_{rated}-I_{SC} SOA has been realistically reported for those transient failure modes displayed in Section III. But it is of great importance to guide the IGBT surviving the extreme short-circuit operations. Moreover, the well-investigated connections between those transient failure modes and boundaries of the SOA, as summarized in

Section III, have laid a good foundation for further predicting the short-circuit V_{DC}/V_{rated}-I_{SC} SOA. Therefore, more attention should be paid to the construction of this short-circuit V_{DC}/V_{rated}-I_{SC} SOA.

However, some interactions exist between these two 3D-SCSOA characteristics that would impose some critical impacts on the construction of the short-circuit V_{DC}/V_{rated}-I_{SC} SOA. As mentioned in Section IV, IGBT would be heated up by the deposited energy during the short-circuit pulse. However, considering the thermal diffusing capability of an IGBT module, the 10μs duration of the short-circuit operation is not long enough to propagate the heat from the silicon chip to the baseplate of the IGBT module. Thus, it is the silicon chips that mainly being heated up. Therefore, the temperature rise ΔT_{SC} of the silicon chip during short-circuit pulse can be approximately calculated in terms of the device thermal capacity and regardless of the thermal conduction [6, 28]

$$\Delta T_{SC} = \frac{V_{DC} \times I_{SC\_sat} \times t_w}{c_{th,si} \times \rho \times d \times A} \tag{2}$$

Where $c_{th,si}$ and ρ are the specific heat capacitance and density of the silicon, d and A are the thickness and active area of the chip. Then, form (2), it can be proved that the thin-chip IGBT modules will have a strong temperature rise during the short-circuit operation, seeing Table II [28]. Meanwhile, the collector side of the thin-chip IGBT is also more probable to be heated up during the short-circuit pulse.

Nowadays, the thin-wafer technology has paved its wave for various ratings of IGBT modules with high performance and reliability [57-58]. This is to say such a severe self-heating effect inside the device cannot be ignored any longer under the

short-circuit conditions. Moreover, it can be intensified with the extending of the device short-circuit endurance time t_w. On the other hand, this device self-heating effect would impose strong impacts on operating behaviors of the IGBT during the short-circuit pulse, especially, those device unstable behaviors limited by the short-circuit V_{DC}/V_{rated}-I_{SC} SOA. Whereas, the boundaries of the short-circuit V_{DC}/V_{rated}-I_{SC} SOA should change with the duration of the short-circuit operation, in order to fit those temperature-dependent transient failure modes, as illustrated in Fig.16. As for detailed variation trends of each of these boundaries, further investigations should focus on dependencies of the transient failure modes (investigated in Section III) on temperature.

TABLE II. TEMPERATURE RISE COMPARISON BETWEEN LOW-VOLTAGE IGBT CHIP (INFINEON) AND HIGH VOLTAGE IGBT CHIP (ABB) [28]

Chip Parameter	LV IGBT	HV IGBT
Voltage Rating V_{rated}	600V	4.5V
Current Rating I_{rated}	200A	55A
Short-circuit Endurance Time t_w	10μs	10μs
Short-circuit Saturated Current I_{SC_sat}	730A(360V)	200A(3.4kV)
Chip Thickness d	70μm	530μm
Chip Active Area A	99.5mm^2	205.5mm^2
ΔT_{SC} (T_{start}=400K)	**204K**	**24K**

As described above, the heat is primarily deposited in the IGBT chip during the steady state of the short-circuit operation. Thus, an assumption can be made, namely the self-heating effect doesn't come into play until the beginning of the steady state. Therefore, from Fig.3, the short-circuit pulse failure initiated by the MOSFET mode and turn-off failure during the steady state are more possible to suffer the impact of this self-heating phenomenon than others.

For the short-circuit pulse failure initiated by the MOSFET mode, the

self-heating effect mainly sets in though the temperature-dependent β_{PNP}. As mentioned in Section III, a large β_{PNP} can strengthen the device ruggedness to avoid this failure. Thus, when the self-heating effect is involved, a positive temperature-dependent β_{PNP} can contribute to this device ruggedness improvement. Under this scenario, as shown in Fig.17, the maximum allowable short-circuit current I_{SC_allow} that the device can withstand before this short-circuit pulse failure is activated increases with the rising temperature at a given V_{DC}.

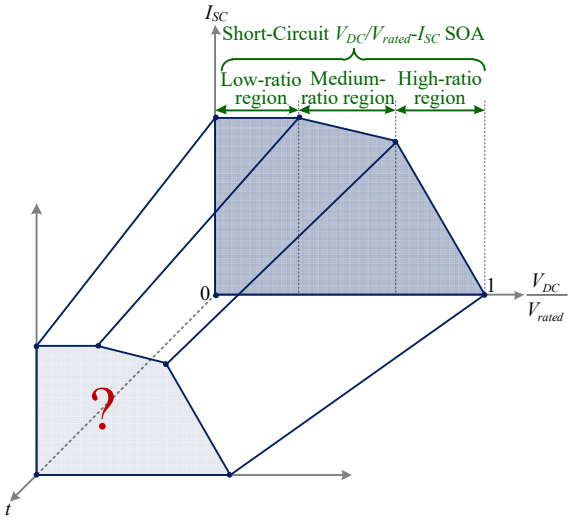

Fig.16. Impacts of device self-heating effect on IGBT short-circuit V_{DC}/V_{rated}-I_{SC} SOA

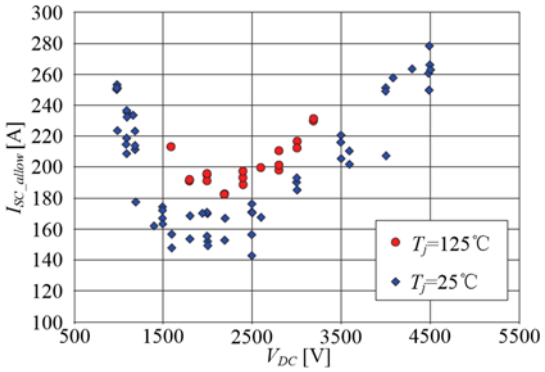

Fig.17. 6.5kV IGBT ruggedness for short-circuit pulse failure induced by MOSFET mode under two different starting temperatures [27]

Thus, the corresponding medium-ratio region boundary of the short-circuit V_{DC}/V_{rated}-I_{SC} SOA should accordingly extend to a higher current level for a given

V_{DC}/V_{rated}, as illustrated in Fig.18.

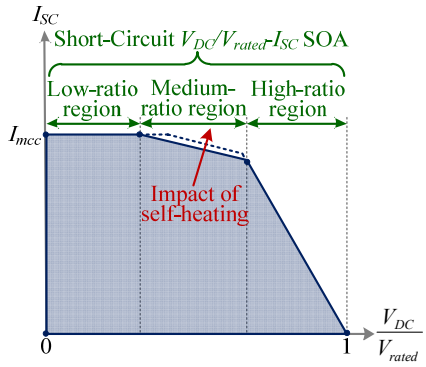

Fig.18. Impact of IGBT self-heating effect on medium-ratio region boundary for positive temperature-dependent β_{PNP} condition

Next, coming to the turn-off failure during the steady state, there has two possible ways for the device self-heating effect to impose its impacts. One is through the temperature-dependent impact ionization coefficient, the other one is still though the temperature-dependent bipolar current gain. As disclosed in Section III, the shape of the device avalanche breakdown curve plays an important role in triggering this turn-off failure. Thus, the dependency of this turn-off failure on temperature is actually determined by the influences of the temperature-dependent impact ionization coefficients and bipolar current gain on the avalanche curve shape, seeing Fig.19.

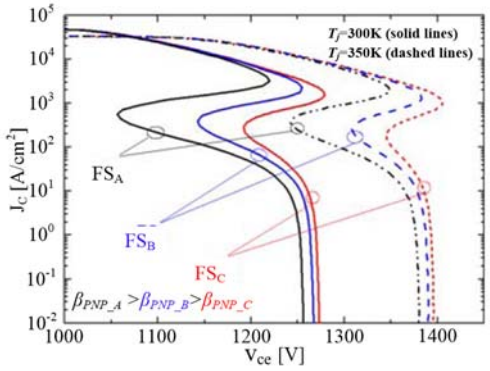

Fig.19. Impacts of temperature on IGBT avalanche breakdown curve for three FS structures [35]

In Fig.19, the IGBT avalanche breakdown curve shifts to a much higher voltage

region with the increasing temperature. It is mainly caused by the negative dependency of the carrier impact ionization coefficients on temperature. Thus, for a high temperature case, IGBT can sustain a much higher voltage level before this turn-off failure is triggered. Consequently, the high-ratio region boundary of the device short-circuit V_{DC}/V_{rated}-I_{SC} SOA should correspondingly shifts to a higher voltage-ratio region for a given short-circuit current, as presented in Fig.20.

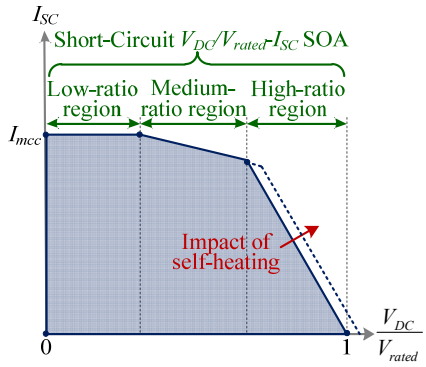

Fig.20. Impact of device self-heating effect on high-ratio region boundary of short-circuit V_{DC}/V_{rated}-I_{SC} SOA

What's more, a negative temperature-dependent β_{PNP} can further improve the device turn-off ruggedness by confining the development of the NDR branch on the device avalanche breakdown curve. In Fig.19, the extension of the NDR branch shrinks with the rising temperature, resulting in a decreasing possibility for the current-filament formation during the short-circuit turn off. Thus, being opposite to the former short-circuit pulse failure, a negative temperature-dependent β_{PNP} would be more preferable for this short-circuit turn-off failure.

However, for currently widespread trench gate/field-stop IGBTs, a positive or negative dependency of β_{PNP} on temperature is actually determined by the field-stop layer design. A field-stop layer with a deep-level doping is more likely to have a

negative temperature dependency, while a shallow-level doped one is more possible to be enabled with a positive temperature dependency [55-56]. Therefore, a careful trade-off between the device medium-ratio and high-ratio region ruggedness under the short-circuit conditions should be considered into the further β_{PNP} design, see Fig.21.

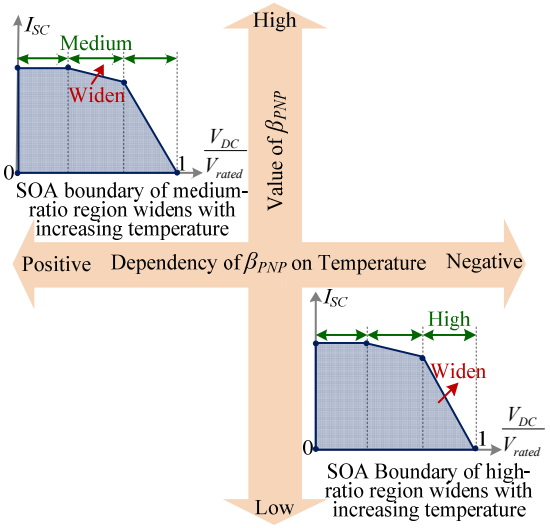

Fig.21. Trade-off between device ruggedness for medium-ratio and high-ratio region dominating failure modes in terms of optimized design of β_{PNP}

VI. CONCLUSION

The present state of the art about the IGBT short-circuit failure modes has been investigated and classified into the short-circuit V_{DC}/V_{rated}-I_{SC} SOA limiting and short-circuit endurance time limiting groups by introducing a 3D-SCSOA for IGBTs. At this point, the detailed relationships between eight short-circuit failure modes and 3D-SCSOA boundaries of the IGBT have been proposed and identified, giving a deep insight into the limiting effects of these failure modes on the device short-circuit ruggedness. Moreover, a self-heating effect during the short-circuit pulse has been discussed. It points out the importance of the dependency investigation of IGBT short-circuit failure modes on temperature for further device short-circuit

V_{DC}/V_{rated}-I_{SC} SOA construction. Meanwhile, the critical roles of β_{PNP} and its temperature-dependency in device short-circuit ruggedness and SOA optimizations have also been disclosed. Consequently, a comprehensive and thoughtful overview of the short-circuit failure modes of the IGBT has been provided, which will drive and shape the future of IGBT short-circuit ruggedness and 3D-SCSOA improvements.

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