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Efficiency Enhancement of Bridgeless Buck-Boost PFC Converter with Unity PF and DC Split to Reduce Voltage Stresses

Zhengge Chen, Bochen Liu, Pooya Davari, and Huai Wang
Department of Energy Technology
Aalborg University, Denmark
E-mail: zgc@et.aau.dk, bli@et.aau.dk, pda@et.aau.dk, hwa@et.aau.dk

***Abstract*—This paper proposes a unity power factor (PF) bridgeless buck-boost power factor correction (PFC) converter to minimize conduction losses caused by the diode bridge. Moreover, compared to the conventional buck-boost PFC converter, the proposed converter has lower voltage stresses across switches, which further improves total efficiency of the proposed converter, especially when converter operates in the light load conditions. Operation modes with inductors working in the discontinuous conduction mode (DCM) is given in detail, and comparative analysis are conducted to show the proposed converter performances regarding the PF, component stresses, and output ripple. The proposed and conventional converter prototypes with load range of 20~100 W are built and tested both in simulation and experiment. The obtained results verify the feasibility of proposed converter and theoretical analysis.**

Keywords—PFC, bridgeless, buck-boost, DCM, low voltage stresses, unity power factor

I. INTRODUCTION

Power factor correction (PFC) converters are widely used in AC-DC converters for its ability to reduce the input line current harmonics and improve the power factor (PF) [1], [2]. For the concerns of energy-saving and environmental impacts [2], Bridgeless topologies have gained interest due to reduced number of the semiconductor components in the line current path which may reduce conduction loss. [2], [3]. Hence, many different bridgeless topologies of boost, buck, Cuk, SEPIC, and buck-boost converters have been proposed [2]-[7].

In single-phase low power applications, e.g., adjustable DC link motor drives and some light emitting diode (LED) applications, boost, buck, and buck-boost PFC converters are usually the preferable candidates for their simplicity in topologies and easily implemented control in the discontinuous conduction mode (DCM) [8]-[11]. However, boost PFC converter is only able to operate in the boost mode, and thus its output voltage will usually be set as 380~400 Vdc to maintain a high PF in the universal input voltage range. The drawbacks are limited DC link voltage range and the requirement of high voltage-rating devices in rear-end converters [8]-[10]. On the other hand, buck PFC converter is only able to work in the buck mode, a poor PF and distorted input line current will be unavoidable unless certain topological modifications or new control strategies applied [4]. For buck-boost PFC converter, it can work in the boost and buck modes without compromising the PF. Hence, buck-boost PFC converter can set a low output voltage for LED applications and electrolytic capacitor can be eliminated by using additional ripple absorption circuits potentially [10].

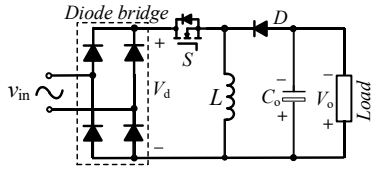


Fig. 1. Conventional (Conv.) buck-boost PFC converter.

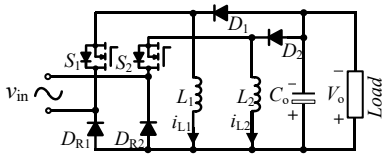


Fig. 2. Dual buck-boost bridgeless (DBBL) PFC converter [9].

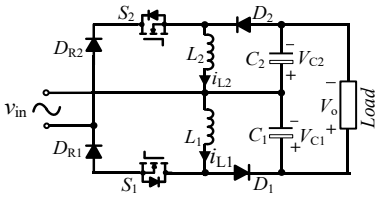


Fig. 3. Proposed (Prop.) bridgeless buck-boost PFC converter.

TABLE I
KEY FEATURE COMPARISON BETWEEN CONVERTERS

Features		Conv.	DBBL	Prop.
No. of devices in topology	*Switch*	1	2	2
	Diode	5	4	4
	Inductor	1	2	2
	Capacitor	1	1	2
	Total	8	9	10
Max. No. of conducting devices in one half line cycle		4	3	3
Reverse voltage across switch		$v_{in}+V_o$	$v_{in}+V_o$	$v_{in}+½V_o$
Reversed output voltage		Yes	Yes	Yes

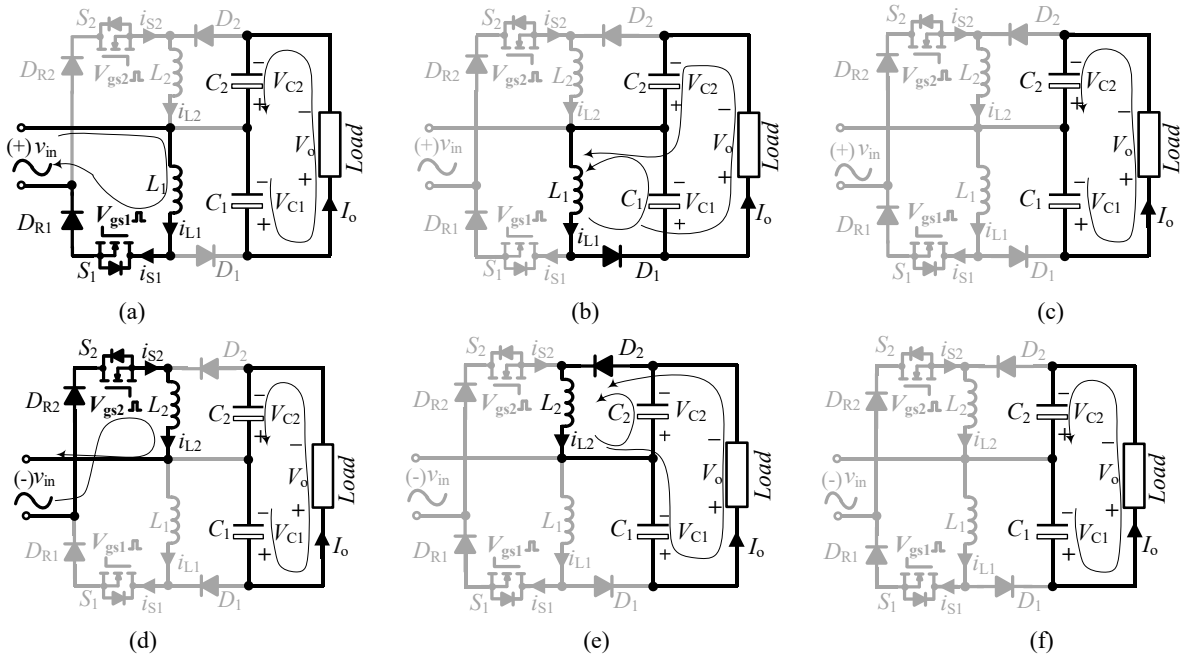


Fig. 4. Operational modes of the proposed topology: (a), (b), (c) in a positive half line cycle, (d), (e), (f) in a negative half line cycle.

Meanwhile, buck-boost PFC converter can also be designed with a variable DC link voltage in motor drives to lower switching losses in rear-end inverter [8], which improves the entire system efficiency.

However, conventional buck-boost PFC converter (see Fig. 1) suffers from several drawbacks, e.g., high voltage stresses across switch and the grounding issue for input and output sources [10]. Driven by reducing the component count and conduction losses, bridgeless buck-boost PFC converters with single tapped inductors were proposed in [7], where it requires snubber capacitors to handle the induced voltage spikes from the tapped inductor leakage inductance, and thus, degrading the efficiency. Ref. [9] has proposed a dual buck-boost bridgeless (DBBL) PFC converter, given in Fig. 2, which has minimized the conduction losses by cancelling the diode bridge, but it still suffers from high voltage stresses across switches.

This paper proposes a novel bridgeless buck-boost PFC converter with reduced voltage stresses across components, as shown in Fig. 3. Table I gives the feature comparisons between the conventional, the DBBL and the proposed converters. Compared to the conventional and DBBL converters, the total component count is increased in the proposed converter. Nevertheless, the voltage stresses are reduced by the DC-split output configuration in the proposed converter, which alleviate switching losses. Besides, the proposed converter has reduced the conducting device number to minimize conduction losses. Hence, compared to the conventional converter, the proposed converter will have higher efficiency, especially in light load conditions.

The rest of paper are organized as follows. In Section II, the operational principle of the proposed converter with inductors working in the DCM is introduced. Then, the PF, voltage stresses across devices, and the output ripple are analyzed. In Section III, specific parameters of converters with brief design criterion are given. Meanwhile, control strategy is introduced, which is applied to the two built prototypes. The obtained results from both simulation and experiment verify the feasibility of the proposed converter and theoretical analysis. Finally, Section IV gives the conclusion of this study.

II. Analysis of The Proposed Converter

A. Topology

Fig. 3 shows the proposed buck-boost PFC converter topology, which consists of two equal inductors L_1, L_2, two equal capacitors C_1, C_2, two rectifier diodes D_{R1}, D_{R2}, two output diodes D_1, D_2, and two power switches S_1, S_2.

For simplicity, the assumptions are as following. (*i*) All components in the topology are ideal. (*ii*) The switching frequency f_{SW} is much higher than the line frequency f_L, so the switching cycle T_S is much small than line cycle T_L. (iii) The ac input voltage v_{in} is considered as a constant during one switching cycle. (iv) Assume that charge duty cycle of inductor L_1 and L_2 are d_{L1_1} and d_{L2_1}, and discharge duty cycle of inductor L_1 and L_2 are d_{L1_2} and d_{L2_2}, respectively. (*v*) When the inductors L_1 and L_2 operate in the DCM, $d_{L1\_1}+d_{L1\_2}<1$, and $d_{L2\_1}+d_{L2\_2}<1$ hold.

B. Operational modes

Fig. 4 illustrates the operational modes of the proposed converter. In a positive half line cycle, Operational mode are shown in (a), (b), (c); in a negative half line cycle, operational modes are shown in (d), (e), (f), respectively.

In a positive line cycle, the switch S_2 is kept in off-state, and the DCM operational modes are as following.

Mode I: In Fig. 4(a), when the switch S_1 is turned on, the inductor L_1 will be charged by the input line voltage v_{in} through S_1 and rectifier diode D_{R1}. The inductor current i_{L1}

will increase linearly during this turning-on duty cycle d_{L1_1}. The capacitors C_1 and C_2 will both support the load.

Mode II: In Fig. 4(b), when the switch S_1 is turned off, the i_{L1} will go through diode D_1 to charge capacitor C_1 and feed the load. The capacitor C_2 will continue to discharge. The inductor current i_{L1} will decrease linearly until to zero during this turning-off duty cycle d_{L1_2}.

Mode III: In Fig. 4(c), switch S_1 stays in off-state. The inductor current i_{L1} keeps in zero until the beginning of the next switching cycle, and the capacitors C_1 and C_2 continue to support the load.

In a negative line cycle, as illustrated in Fig. 4(d), (e), and (f), the switch S_1 keeps turned off, and operational modes are similar to that in a positive line cycle. Switch S_2, inductor L_2, rectifier diode D_{R2} and diode D_2 will operate correspondingly to achieve PFC and output voltage regulation. Hence, this paper will focus only on positive half line cycle. Meanwhile, based on the operational modes analysis, it is obvious that the control signals for both switches can be the same, as even although the switches are on, the existing rectifier diodes D_{R1} and D_{R2} will block the reverse current and to make the operation modes as illustrated above.

Fig. 5 gives the waveforms of inductor current i_{L1}, output diode current i_{D1}, and switching current i_{S1} in the proposed converter, along with the waveforms of i_L, i_D, and i_S in the conventional converter. As can be seen from Fig.5, i_{S1} and i_S are same, but i_{D1} and i_D are not, neither are i_{L1} and i_L. In buck-boost PFC converter, the input average current is the switch current, so the same waveform between i_{S1} and i_S indicates the same PF of the proposed converter and the conventional converter. In contrary, the differences between i_{D1} and i_D actually imply the larger rms value of i_{D1} than that of i_D, and larger rms value of i_{L1} than that of i_L. This feature will increase conduction losses in L_1 and D_1 of proposed converter, which is the penalty of reduced voltage stresses across devices.

C. Unity Power Factor

Knowing that the peak value of input line voltage is V_M, the RMS value of line voltage is V_{in_rms} and the line angle frequency is ω. Then v_{in} can be given as:

$$v_{in}(t) = V_M \sin(\omega t) = \sqrt{2} V_{in\_rms} \sin(\omega t). \quad (1)$$

following (1), the inductor peak current is:

$$I_{L1\_pk}(t) = \frac{V_M \left|\sin(\omega t)\right| d_{L1\_1}}{L_1 f_{SW}} \quad (2)$$

where the absolute value of $\sin(\omega t)$ indicate that it is in positive half line cycle.

The average switch current i_{S1_ave} can be expressed as the input current:

$$i_{in}(t) = i_{S1\_ave}(t) = \frac{V_M \left|\sin(\omega t)\right| d_{L1\_1}^2}{2 L_1 f_{SW}}. \quad (3)$$

Based on (1) and (3), the input power is expressed as:

$$P_{in} = \frac{1}{T_L/2} \int_0^{T_L/2} i_{in}(t) v_{in}(t) d(t) = \frac{(d_{L1\_1} V_M)^2}{4 L_1 f_{SW}}. \quad (4)$$

From (4), the duty cycle d_{L1_1} can be expressed as:

$$d_{L1\_1} = \frac{2\sqrt{L_1 f_{SW} P_{in}}}{V_M}. \quad (5)$$

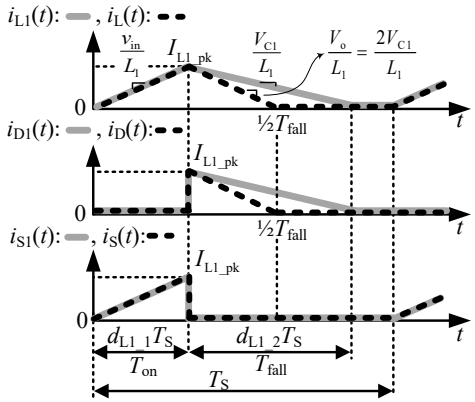


Fig. 5. Waveforms of inductor current i_{L1}, output diode current i_{D1}, and switch current i_{S1} in the proposed converter, along with corresponding waveforms in conventional converter.

Equation (5) indicates that in steady state, the turning-on duty cycle is theoretically fixed and it only relates to L_1, f_{SW}, P_{in}, and V_M. Assume the rms value of the input current is I_{in_rms}. Then, theoretically, using (3) and (4), it can obtain the PF of the proposed converter as:

$$PF = \frac{P_{in}}{V_{in\_rms} I_{in\_rms}} = \frac{(d_{L1\_1} V_M)^2 / 4 L_1 f_S}{\frac{V_M}{\sqrt{2}} \sqrt{\frac{1}{T_L/2} \int_0^{T_L/2} [i_{in}(t)]^2 d(t)}} = 1. \quad (6)$$

Equation (6) indicates that ideally the proposed converter has the unity PF. However, Equation (6) is the theoretical expression of the PF without considering phase shift between input line voltage and current. In practice, phase shift caused by EMI filter network will degrade the PF [13].

D. Voltage stresses

Note that the V_{C1} and V_{C2} will be equal automatically, just as the bridgeless buck PFC converter in [4]. According to Kirchhoff's law and the operational analysis above, there is equation $V_{C1}=V_{C2}=½V_o$. Based on Fig. 4, the reverse voltage across switches S_1 and S_2, as well as the D_1 and D_2 can be easily derived as:

$$v_{re\_X}\Big|_{X=D1,D2,S1,S2} = V_M \left|\sin(\omega t)\right| + V_o/2 \quad (7)$$

where the subscript X in reverse voltage v_{re_X}, represents S_1, S_2, D_1, and D_2. Similarly, for the conventional converter, the reverse voltage across switch S and output diode D can also be derived as:

$$v_{re\_X}\Big|_{X=D,S} = V_M \left|\sin(\omega t)\right| + V_o. \quad (8)$$

Obviously, the maximum reverse voltage $v_{re\_X\_max}$ across these devices in the proposed and the conventional converters are:

$$\begin{cases} v_{re\_X\_max}\Big|_{X=S1,S2,D1,D2} = V_M + V_o/2 & \text{Prop.} \\ v_{re\_X\_max}\Big|_{X=D,S} = V_M + V_o & \text{Conv.} \end{cases} \quad (9)$$

Seen from (9), compared to the conventional converter, the relatively lower voltage stresses of components in the proposed converter allow employing low voltage rating devices, which lower entire cost of converter. Furthermore, it will reduce switching losses of power switches. As in light

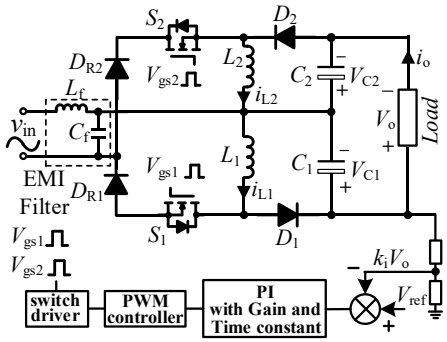


Fig. 6. Control block diagram of the proposed converter.

TABLE II
KEY CIRCUIT PARAMETERS OF CONVERTERS

Symbols	Conventional DCM buck-boost PFC	Symbols	Proposed DCM buck-boost PFC
f_{SW}	50 kHz	f_{SW}	50 kHz
V_{in}	85~135 Vac	V_{in}	85~135 Vac
V_o	160 Vdc	V_o	160 Vdc
P_o	20~100 W	P_o	20~100 W
L	110 μH	L_1, L_2	110 μH
C_o	1500 μF/200 Vdc	C_1, C_2	3300 μF/100 Vdc
C_f	0.1 μF	C_f	0.1 μF
L_f	1.9 mH	L_f	1.9 mH

load conditions, switching losses are usually the dominant segment in the total energy losses. Hence, the proposed converter will be more efficient under light load conditions. Notably, in order to nullify the reverse recovery losses in diodes, inductors are designed to operate in the DCM. Thus, here, switching losses only refer to losses of switches, not including diodes.

E. Voltage ripple

For an AC-DC converter, the output ripple is caused by the unbalanced instantaneous power between input and output. Therefore, capacitors are necessary in AC-DC converters to buffer this unbalanced power. The following equation illustrates the relationship between output voltage ripple v_{o_rip} and output capacitance C [8], as:

$$v_{o\_rip} = -\frac{I_o \sin(2\omega t)}{2\omega C}. \tag{10}$$

The output capacitance C in the proposed and conventional converter are respectively as:

$$\begin{cases} C = C_1 // C_2 = \dfrac{C_1}{2} = \dfrac{C_2}{2} & Prop. \\ C = C_o & Conv. \end{cases} \tag{11}$$

According to (10) and (11), the output voltage ripples of proposed and conventional converter are:

$$\begin{cases} v_{o\_rip} = -\dfrac{I_o \sin(2\omega t)}{\omega C_1} & Prop. \\ v_{o\_rip} = -\dfrac{I_o \sin(2\omega t)}{2\omega C_o} & Conv. \end{cases} \tag{12}$$

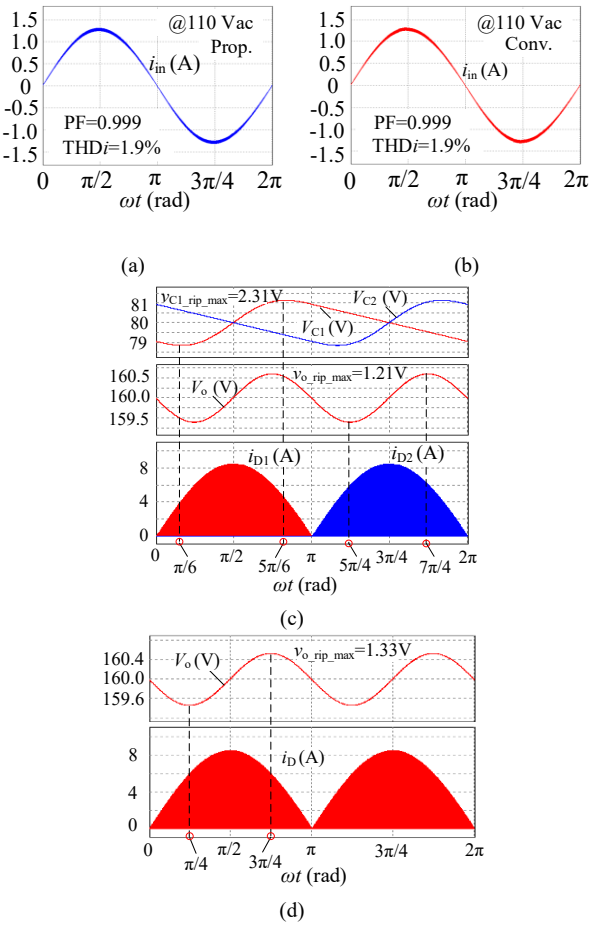


Fig. 7. Simulation waveforms with a 110-Vac input voltage: input line current of the (a) proposed and (b) conventional converters, output voltage ripple of the (c) proposed and the (d) conventional converters.

Seen from (12), if the proposed converter needs to meet the same output ripple requirement as in the conventional converter, Capacitance of C_1 and C_2 in the proposed converter should be twice-larger than that of C_o in the conventional converter. However, the voltage rating of capacitor C_1 and C_2 are only half that of C_o in the conventional converter. This means that the size and cost will not increase so significantly.

III. SIMULATION AND EXPERIMENTAL RESULTS

In order to validate the effectiveness of the proposed topology comparative simulation studies are conducted. Furthermore, hardware prototypes for the proposed and conventional buck-boost PFC are implemented and verified through experiments.

A. Control and circuit parameters

Similar to the conventional converter, the proposed converter can also employ simple single voltage loop control to achieve output regulation and the unity PF. Fig. 6 gives the control schematic of the proposed converter. As seen from Fig. 6, both switches S_1 and S_2 can be driven by the same control signal. The gain and time constant in PI controller are selected as 0.9 and 0.05 respectively.

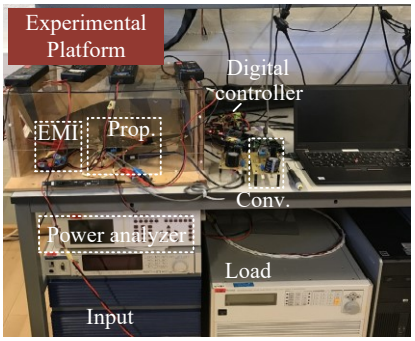
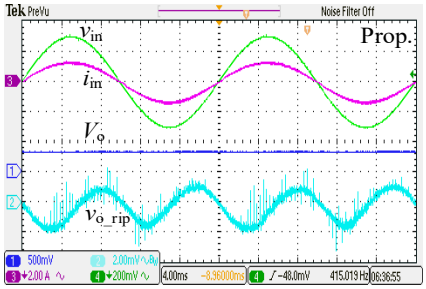
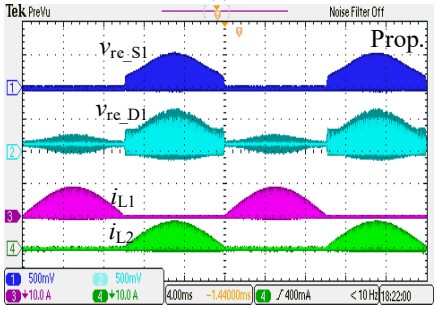


Fig. 8. Experimental test setup.

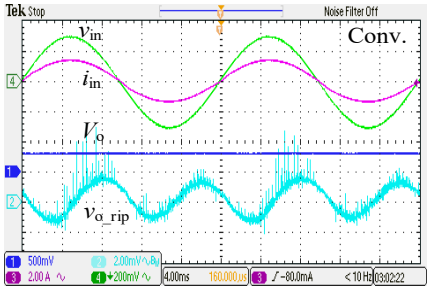


(a)

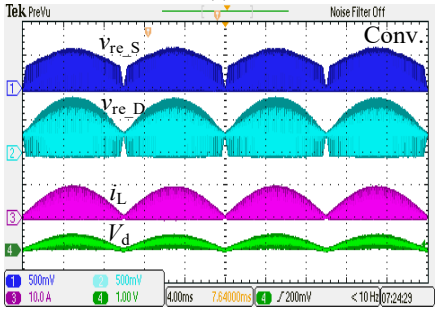


(b)

Fig. 9. Obtained experimental waveforms of proposed converter operating at 100 Watts in a 110-Vac input voltage: (a) input voltage v_{in} [100 V/div], input current i_{in} [2 A/div], output voltage V_o [250 V/div], output voltage ripple v_{o_rip} [1 V/div], and time [4 ms/div], (b) reverse voltages V_{re_S1}, V_{re_D1} [250 V/div], inductor currents i_{L1}, i_{L2} [10 A/div], and time [4 ms/div],



(a)



(b)

Fig. 10. Obtained experimental waveforms of conventional converter operating at 100 Watts in a 110-Vac input: (a) input voltage v_{in} [100 V/div], input current i_{in} [2 A/div], output voltage V_o [250 V/div], output voltage ripple v_{o_rip} [1 V/div], and time [4 ms/div], (b) reverse voltages V_{re_S1}, V_{re_D1} [250 V/div], inductor currents i_{L1}, i_{L2} [10 A/div], and time [4 ms/div].

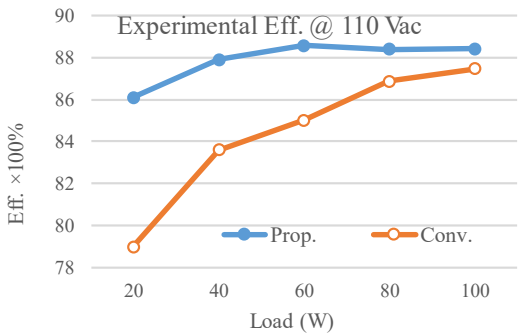


Fig. 11. Measured efficiencies of proposed and conventional converters.

By referring to [12], the inductance of L_1 and L_2 are calculated to guarantee the DCM operations, i.e., $L_1 = L_2 \leq 115.4$ μH. Furthermore, to limit the peak inductor current to 10 A, inductance of L_1 and L_2 are set as 110 μH. On the other hand, the capacitance of C_1, C_2, and C_o are set as 3300 μF and 1500 μF to meet the output voltage ripple requirements, i.e.,$v_{o\_rip} \leq 1.6$ V ($v_{o\_rip}/V_o \leq 1\%$). Table II gives the key circuit parameters of the proposed and the conventional converters.

B. Simulation

Fig. 7 gives the simulation waveforms of proposed and conventional converters operating at 100 W in a 110-Vac input voltage. Seen from Fig. 7(a), (b), the proposed and conventional converters have the same high PF and low THD*i*. The reason why the simulation has the PF less than one is that the used EMI filter at input ac side will cause the phase shift, which will degrade PF and THD*i* [13].

Seen from Fig. 7(c), (d), the voltage ripple of conventional and the proposed converter are 1.33 V and 1.21 V, which are all within the output ripple requirement ($v_{o\_rip}/V_o \leq 1\%$). Meanwhile, the voltage ripple (2.31 V) of capacitor C_1 and C_2 are almost twice larger than that of capacitor C_o. Furthermore, the voltage ripple of C_1 and C_2 will partly cancelled out by each other, but it will not fully cancel out. This is because C_1 and C_2 are charged only in positive and negative half line cycle, separately, and they have to discharge in another complementary half line cycle. Therefore, their peak voltage and valley voltage will never appear at the same time unless different control strategy or topological modification applied.

C. Experimental results

In the experiment, the conventional and the proposed buck-boost PFC converters are built up for validation purpose. Two prototypes use the same PI control system implemented by digital signal processor (DSP) TMS320F28335 and the

same analog-to-digital conversion ship AD7656. The switches, diodes (output and rectifier), and inductor cores are realized by component IXFH22N652, STPSC12065, and CM571026 from Chang Sung. Capacitors are realized by ECOS2AA332DA (3300 μF, 100 Vdc) in the proposed converter and ECOS2DA152EA (1500 μF, 200 Vdc) in the conventional converter. Notably, in order to have a fair comparison STPSC12065 is also used for the diode bridge in conventional converter. Fig. 8 shows the experimental setup. Fig. 9 and 10 show the experimental waveforms of the proposed and the conventional converters. As it is shown in Fig. 9 the proposed converter can use simple voltage control strategy to achieve the output voltage regulation and a near unity PF.

Seen from Fig. 9(a) and 10(a), compared to conventional converter, the proposed converter has the same sinusoidal input current, which indicates that the proposed converter has the same unity PF as that of the conventional converter. The measured PF of the proposed and the conventional converter are the same 0.999, and the corresponding THD*i* are 3.5% (Prop.) and 3.1% (Conv.), respectively.

Besides, observed from Fig. 9(b) and 10(b), compared to the conventional converter (340 V and 420 V across switch and diodes, respectively), the proposed converter has lower reverse voltage across devices (250 V and 340 V across switch and diodes, respectively). The lower reverse voltage across switches actually helps to reduce the switching losses. Consequently, the proposed converter shows a good performance in efficiency aspect compared to the conventional converter, especially in light load conditions.

Fig. 11 gives the measured efficiency of the proposed and conventional converter in output power range of 20~100 W. As can be seen from Fig. 11 for the entire output power range, the proposed converter has better efficiency than conventional one, especially in the light load conditions. Note that RCD snubber circuits are used to suppress the voltage spike across switches during experiments, which decrease the efficiency of both converters given in Fig. 11.

IV. Conclusion

This paper proposes a bridgeless buck-boost PFC converter to minimize the conduction losses by the removal of diode bridge. Furthermore, the proposed converter with a DC-split output structure can lower the voltage stresses across switches, which eases the switching losses. The operation principles of the proposed converter are presented and analyzed in detail. Then, based on the operation principles, this paper analyzes and compare the PF, voltage stresses, and output voltage ripple between the proposed and the conventional converters. Simulation and experiment are verified by two built prototypes with same control system and same load range of 20-100 Watts. The obtained results from simulation and experiment indicate that compared to the conventional converter, the proposed converter can use same simple control strategy to achieve a near unity PF and output regulation. Meanwhile, the proposed converter has higher efficiency in the entire load range, even much better in light load conditions. The major drawback of the proposed converter is that output capacitors with twice-larger capacitance are required to satisfy the output ripple requirement as in the conventional converter. In summary, the proposed converter can be an alternative solution to the conventional buck-boost PFC converter in efficiency-concerned applications, especially suitable in the light load conditions.

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