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# Zero-Voltage Switching PWM Strategy Based Capacitor Current-Balancing Control for Half-Bridge Three-Level DC/DC Converter

Dong Liu, *Student Member, IEEE*, Fujin Deng, *Member, IEEE*, Qi Zhang, and Zhe Chen, *Senior Member, IEEE*

**Abstract**— The current imbalance among the two input capacitors is one of the important issues of the half-bridge three-level (HBTL) DC/DC converter, which would affect system performance and reliability. In this paper, a zero-voltage switching (ZVS) pulse-wide modulation (PWM) strategy including two operation modes is proposed. Based on the proposed ZVS PWM strategy, a capacitor current-balancing control is proposed for the HBTL DC/DC converter, where the currents on the two input capacitors can be kept balanced by alternating the two operation modes of the proposed ZVS PWM strategy. Therefore, the proposed control strategy can improve the performance and reliability of the converter in the aspect of balancing the thermal stresses and lifetimes among the two input capacitors. Finally, simulation and experimental studies are conducted and results verify the proposed control strategy.

**Index Terms**—Capacitor current-balancing control, DC/DC converter, three-level (TL).

## I. INTRODUCTION

Due to the merits of the DC transmission such as no reactive power, no frequency stability, high conversion efficiency, and easy system control [1-3], DC distribution systems and DC micro-grids have been proposed as the promising solution for future smart-grid systems. Furthermore, DC data centers and residential systems have been increasingly developed recently [4], [5]. In DC transmission systems and DC grids, DC/DC converters play an important role in delivering the power and changing voltage levels [6-8].

Generally, in order to reduce the power losses and increase the power capability, a reasonable high DC voltage is preferred for the DC distribution systems and DC micro-grids. So far, a number of studies about the DC/DC converters with high input voltage for the DC distribution systems have been reported in literature. The three-level (TL) DC/DC converter is acknowledged as one of the promising solutions for the DC

distribution system development because the power switches in the TL converter only need to withstand half of the input voltage [9-12]. The TL circuit structure was firstly applied into the DC/DC converter in [13], [14]. Based on the conventional TL DC/DC converter, many other studies about TL DC/DC converters have been presented in [15-29]. Reference [24] proposed a novel four-switch HBTL DC/DC converter with zero-voltage switching (ZVS) control strategy, which only added one DC-blocking capacitor but removed two clamped diodes in comparison with the conventional TL DC/DC converter. Due to the low cost and compact circuit structure, the four-switch HBTL DC/DC converter has become attractive for industrial applications [25-28]. Reference [25] presented new solutions to achieve the wide range soft-switching based on the four-switch HBTL converter, in which four kinds of new pulse-wide modulation PWM TL DC/DC converters were proposed for the industrial application. In [26], a new PWM TL combined DC/DC converter was proposed to achieve wide range soft-switching. A secondary-side phase-shift controlled ZVS DC/DC converter with wide voltage gain and a three-phase DC/DC converter with low voltage stress on the power switches were proposed in [27] and [28] for the high voltage applications. In addition, reference [29] presented a new control strategy to balance the voltages on the two input capacitors for the four-switch HBTL DC/DC converter.

The above literatures mainly focus on the topics about improving the converter's performance by increasing the efficiency or enhancing the converter's reliability by balancing the input capacitor voltages. Unfortunately, there is few studies about the currents flowing through the input capacitors of the four-switch HBTL DC/DC converter, which would make significant influences on the reliability of the converter [30], [31]. In [24], it is analyzed that the currents among the two input capacitors in the four-switch HBTL converter are balanced based on the assumption that the input power supply is regarded as an ideal voltage source, which means that the input current can change abruptly along with the switching actions. However, in the real applications, these abrupt changes of the input current in the switching period are impractical because of the effect from the output inductance of the input power supply and the inductance of the input line on the input current, which would result in the current imbalance

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among the two input capacitors in the four-switch HBTL DC/DC converter. Furthermore, this current imbalance would become larger along with the output power increasing and input voltage increasing, and make influence on the converter's reliability in aspects of the thermal stress imbalance and lifetime imbalance among the two input capacitors.

In this paper, a ZVS PWM strategy and a capacitor current-balancing control are proposed for the four-switch HBTL DC/DC converter. The proposed ZVS PWM strategy is composed of two operation modes. Based on the proposed ZVS PWM strategy, a capacitor current-balancing control is proposed by alternating the two operation modes of the proposed PWM strategy, which can effectively eliminate the current imbalance among the two input capacitors. In addition, the switching losses caused by the hard switching at the light load situation can be distributed evenly among the four power switches by using the proposed control strategy. Therefore, the proposed control can balance the thermal stresses, lifetimes among the two input capacitors and balance the thermal stresses among the four power switches at the light load situation, which thus can improve the converter's performance and reliability. The currents on the two input capacitors of the four-switch HBTL DC/DC converter are analyzed in detail when considering the effect from the output inductance of the input power supply and inductance of the input line on the input current.

This paper is organized as follows. Section II analyzes the current imbalance issue in the four-bridge HBTL DC/DC converter under the conventional control strategy. Section III proposes the ZVS PWM strategy including the two operation modes and analyzes the performances of the four-switch HBTL DC/DC converter under the proposed ZVS PWM strategy. Section IV proposes the capacitor current-balancing control and analyzes the performances of the four-switch HBTL DC/DC converter under the proposed capacitor current-balancing control. Section V presents the simulation and experimental results to verify the proposed control strategy. Finally, the main contributions are summarized in Section VI.

## II. CAPACITOR CURRENT IMBALANCE UNDER CONVENTIONAL CONTROL STRATEGY

### A. Converter Structure and Conventional Control Strategy

Fig. 1(a) shows the structure of the four-switch HBTL DC/DC converter. In the primary side, two input capacitors  $C_1$  and  $C_2$  are used to split the input voltage  $V_{in}$  into two voltages  $V_1$  and  $V_2$ ;  $S_1 - S_4$  and  $D_1 - D_4$  are power switches and diodes;  $T_r$  is the high frequency transformer (HFT);  $L_r$  is the leakage inductance of  $T_r$ ;  $C_{s1} - C_{s4}$  are the parasitic capacitors of  $S_1 - S_4$ ;  $C_b$  is the DC-blocking capacitor. In the secondary side, there are four rectifier diodes  $D_{r1} - D_{r4}$ , one output filter inductor  $L_o$ , and one output filter capacitor  $C_o$ . In Fig. 1(a),  $i_{in}$  is the input current;  $i_{c1}$  and  $i_{c2}$  are the currents flowing through  $C_1$  and  $C_2$ , respectively;  $V_{pri}$  and  $i_p$  are the primary voltage and current of the transformer  $T_r$ ;  $i_{L_o}$  is the current through  $L_o$ ;  $V_{cb}$  is the voltage on the DC-blocking capacitor  $C_b$ ;  $i_o$  and  $V_o$  are

the output current and output voltage;  $V_{ab}$  is the voltage between point a and b;  $n$  is the turns ratio of the transformer  $T_r$ .

Fig. 1(b) shows the conventional control strategy [24] and main waveforms of the four-switch HBTL DC/DC converter. In Fig. 1(b),  $d_{rv1} - d_{rv4}$  are four driving signals of the power switches  $S_1 - S_4$ , where  $(S_1, S_2)$  and  $(S_3, S_4)$  are complementary switch pairs.  $d_1$  and  $d_2$  are duty ratios in one switching period  $T_s$ , where  $d_2$  is bigger than  $d_1$  in the normal operations.

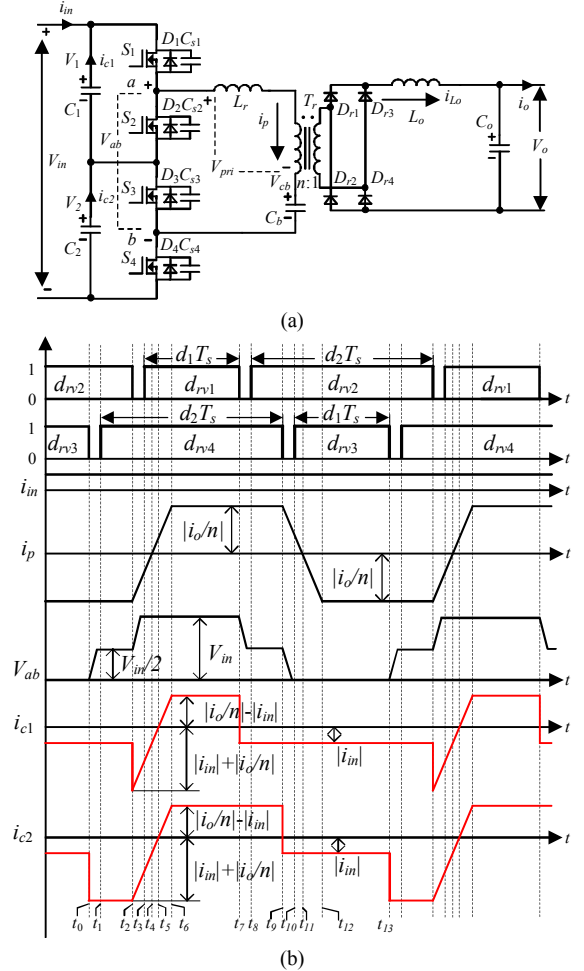


Fig. 1. (a) Structure of four-switch HBTL DC/DC converter. (b) Conventional control strategy with main waveforms.

### B. Capacitor Current Imbalance Analysis

Before discussing about the currents on the two input capacitors of the four-switch HBTL DC/DC converter, several assumptions are made as below to simplify the analysis.

- 1) The inductance of the output filter inductor  $L_o$  is large enough to be considered as a current source;
- 2) The power switches  $S_1 - S_4$  are ideal, which means that the effects of the parasitic capacitors are neglected;
- 3) The input current  $i_{in}$  is considered as a constant in the switching period due to the effect from the output inductance of the input power supply and inductance of the input line on the input current.

According to Fig. 1(b),  $i_{c1}$  and  $i_{c2}$  in one switching period  $T_s$  can be expressed as

$$i_{c1} = \begin{cases} -i_{in} & t_0 \leq t < t_2 \\ i_p - i_{in} & t_2 \leq t < t_7 \\ -i_{in} & t_7 \leq t < t_{13} \end{cases} \quad (1)$$

$$i_{c2} = \begin{cases} i_p - i_{in} & t_0 \leq t < t_9 \\ -i_{in} & t_9 \leq t < t_{13} \end{cases} \quad (2)$$

According to Fig. 1(b), the primary current  $i_p$  in one switching period  $T_s$  can be described as

$$i_p = \begin{cases} -\frac{i_o}{n} & t_0 \leq t < t_2 \\ -\frac{i_o}{n} + \frac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) & t_2 \leq t < t_6 \\ \frac{i_o}{n} & t_6 \leq t < t_9 \\ \frac{i_o}{n} - \frac{V_{in}}{2 \cdot L_r} \cdot (t - t_9) & t_9 \leq t < t_{12} \\ -\frac{i_o}{n} & t_{12} \leq t < t_{13} \end{cases} \quad (3)$$

Substituting (3) into (1) and (2),  $i_{c1}$  and  $i_{c2}$  in one switching period can be rewritten as

$$i_{c1} = \begin{cases} -i_{in} & t_0 \leq t < t_2 \\ \frac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) - \frac{i_o}{n} - i_{in} & t_2 \leq t < t_6 \\ \frac{i_o}{n} - i_{in} & t_6 \leq t < t_7 \\ -i_{in} & t_7 \leq t < t_{13} \end{cases} \quad (4)$$

$$i_{c1\_rms\_con} = \sqrt{i_{in}^2 + \frac{i_o^2 \cdot d_1}{n^2} + \frac{8 \cdot L_r \cdot i_{in} \cdot i_o^2}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{8 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \quad (7)$$

$$i_{c2\_rms\_con} = \sqrt{i_{in}^2 + \frac{i_o^2 \cdot d_2}{n^2} + \frac{8 \cdot L_r \cdot i_{in} \cdot i_o^2}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{8 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \quad (8)$$

$$\Delta i_{c\_rms\_con} = |i_{c1\_rms\_con} - i_{c2\_rms\_con}| = \frac{i_o^2 \cdot (d_2 - d_1)}{n^2 \cdot (i_{c1\_rms\_con} + i_{c2\_rms\_con})} \quad (9)$$

TABLE I  
THEORETICAL CALCULATION FORMULAS OF RMS VALUES OF  $i_{c1}$  AND  $i_{c2}$

Control Strategy	RMS Value	Theoretical Calculation Formula
Conventional Control Strategy	$i_{c1\_rms\_con}$	$\sqrt{i_{in}^2 + \frac{i_o^2 \cdot d_1}{n^2} + \frac{8 \cdot L_r \cdot i_{in} \cdot i_o^2}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{8 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}}$
	$i_{c2\_rms\_con}$	$\sqrt{i_{in}^2 + \frac{i_o^2 \cdot d_2}{n^2} + \frac{8 \cdot L_r \cdot i_{in} \cdot i_o^2}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{8 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}}$
	$\Delta i_{c\_rms\_con}$	$\frac{i_o^2 \cdot (d_2 - d_1)}{n^2 \cdot (i_{c1\_rms\_con} + i_{c2\_rms\_con})}$
Proposed Control Strategy	$i_{c1\_rms\_pro}$ $i_{c2\_rms\_pro}$	$\sqrt{i_{in}^2 + \frac{i_o^2}{2 \cdot n^2} + \frac{8 \cdot L_r \cdot i_{in} \cdot i_o^2}{n^2 \cdot V_{in} \cdot T_s} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{8 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}}$

$$i_{c2} = \begin{cases} -\frac{i_o}{n} - i_{in} & t_0 \leq t < t_2 \\ \frac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) - \frac{i_o}{n} - i_{in} & t_2 \leq t < t_6 \\ \frac{i_o}{n} - i_{in} & t_6 \leq t < t_9 \\ -i_{in} & t_9 \leq t < t_{13} \end{cases} \quad (5)$$

In the steady-state situation, the time intervals  $[t_2-t_6]$  and  $[t_9-t_{12}]$  are the same as shown in Fig. 1(b), which can be calculated by

$$t_6 - t_2 = t_{12} - t_9 = \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in}} \quad (6)$$

According to (4) ~ (6), the root-mean-square (RMS) values of  $i_{c1}$  and  $i_{c2}$  under the conventional control strategy namely  $i_{c1\_rms\_con}$  and  $i_{c2\_rms\_con}$  can be calculated by (7) and (8), which are listed in Table I.

Based on (7) and (8), the difference between  $i_{c1\_rms\_con}$  and  $i_{c2\_rms\_con}$  namely  $\Delta i_{c\_rms\_con}$  can be calculated by (9), which is also listed in Table I.

From (7) and (8), it can be seen that the currents on the two input capacitors  $i_{c1}$  and  $i_{c2}$  are imbalanced under the conventional control strategy and  $i_{c2\_rms\_con}$  is bigger than  $i_{c1\_rms\_con}$  because  $d_2$  is bigger than  $d_1$  in the normal operations. What is worse, this current imbalance issue would result in the thermal stress imbalance and lifetime imbalance among the two input capacitors, which would affect the reliability of the converter.

### III. PROPOSED ZVS PWM STRATEGY

#### A. Proposed ZVS PWM Strategy

Fig. 2 shows the proposed ZVS PWM strategy for the four-switch HBTL DC/DC converter, which includes two operation modes.

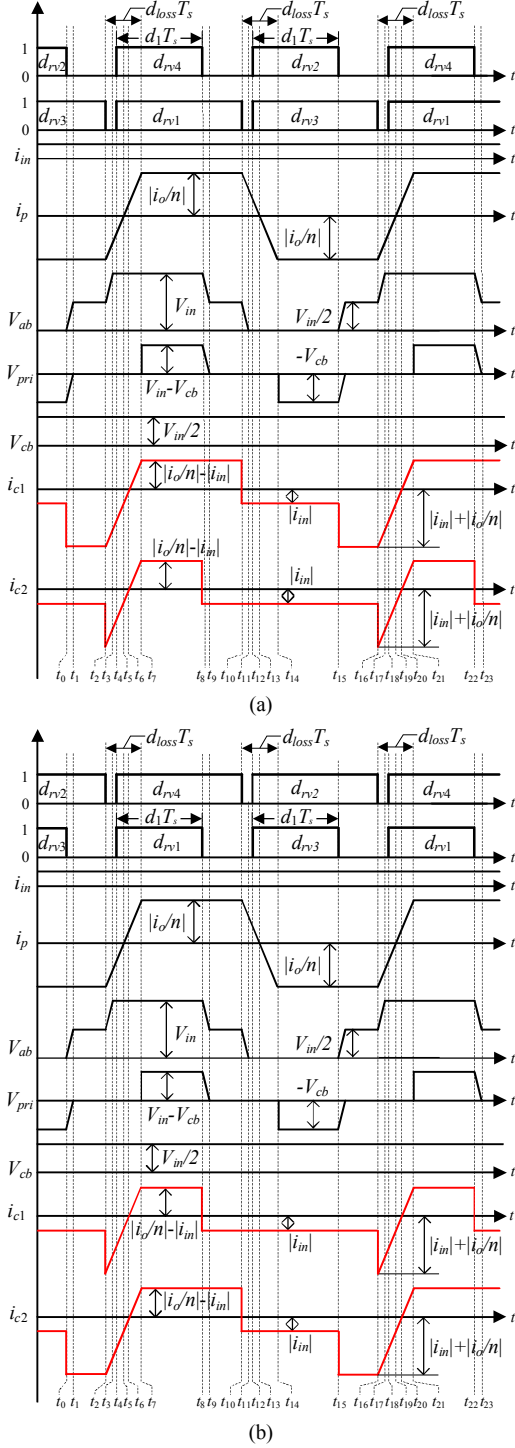


Fig. 2. Proposed ZVS PWM strategy with main waveforms. (a) Operation mode I. (b) Operation mode II.

In Fig. 2,  $d_{rv1}$ - $d_{rv4}$  are four driving signals of the power switches  $S_1$ - $S_4$ ,  $d_1$  is the duty ratio in one switching period, and

$d_{loss}$  is the duty cycle loss. In the operation mode I, the duty ratios of  $d_{rv1}$  and  $d_{rv3}$  are both 0.5, and the duty ratios of  $d_{rv2}$  and  $d_{rv4}$  are both  $d_1$ . Contrarily, in the operation mode II, the duty ratios of  $d_{rv2}$  and  $d_{rv4}$  are both 0.5, and the duty ratios of  $d_{rv1}$  and  $d_{rv3}$  are both  $d_1$ . The maximum value of  $d_1$  is 0.5 in the two operation modes, which avoids the short currents through the switch pairs ( $S_1$ ,  $S_2$ ) and ( $S_3$ ,  $S_4$ ). In addition, the two operation modes have the same output characteristics because the primary currents  $i_p$  and primary voltages  $V_{ab}$  in the two operation modes are the same as shown in Fig. 2.

Fig. 3 shows equivalent circuits to explain the operation principle of the operation mode I.

Stage 0 [before  $t_0$ ] During this stage, both  $S_2$  and  $S_3$  are on-state, therefore the primary current  $i_p$  flows through  $S_2$ ,  $S_3$ , and  $C_b$ , the voltage  $V_{ab}$  is 0 V. The power from  $C_b$  is transferred to the output through  $T_r$ ,  $D_{r2}$ , and  $D_{r3}$ .

Stage 1 [ $t_0$ - $t_1$ ] At  $t_0$ , the switch  $S_2$  is turned off. The capacitor  $C_{s2}$  starts to charge, and the capacitor  $C_{s1}$  begins to discharge. This stage finishes until the voltage on  $C_{s2}$  increases to  $V_{in}/2$  and the voltage on  $C_{s1}$  decreases to 0 V.

Stage 2 [ $t_1$ - $t_2$ ] At  $t_1$ , the voltage on  $C_{s2}$  becomes 0 V and the diode  $D_1$  begins to conduct. The circuit operates in a free-wheeling mode with the primary current  $i_p$  flowing through  $L_r$ ,  $D_1$ ,  $C_1$ ,  $S_3$ ,  $C_b$ , and  $T_r$ . During this stage, the primary current  $i_p$  is kept at  $-i_o/n$ .

Stage 3 [ $t_2$ - $t_3$ ] At  $t_2$ , the switch  $S_3$  is turned off. The capacitor  $C_{s3}$  starts to charge, and the capacitor  $C_{s4}$  begins to discharge. This stage finishes until the voltage on  $C_{s3}$  increases to  $V_{in}/2$  and the voltage on  $C_{s4}$  decreases to 0 V. The primary current  $i_p$  starts to increase, and it is not enough to provide  $i_o$ , so the rectifier diodes  $D_{r1}$ - $D_{r4}$  conduct simultaneously.

Stage 4 [ $t_3$ - $t_4$ ] At  $t_3$ , the voltage on  $C_{s4}$  becomes 0 V and the diode  $D_4$  begins to conduct. The circuit operates in a free-wheeling mode with the primary current  $i_p$  flowing through  $L_r$ ,  $D_1$ ,  $C_1$ ,  $C_2$ ,  $D_4$ ,  $C_b$ , and  $T_r$ .

Stage 5 [ $t_4$ - $t_5$ ] At  $t_4$ , the switches  $S_1$  and  $S_4$  are turned on at zero-voltage. The primary current  $i_p$  flows through  $L_r$ ,  $S_1$ ,  $C_1$ ,  $C_2$ ,  $S_4$ ,  $C_b$ , and  $T_r$ .

Stage 6 [ $t_5$ - $t_6$ ] At  $t_5$ , the primary current  $i_p$  increases to 0 A and continues to increase linearly, which means the direction of  $i_p$  begins to change.

Stage 7 [ $t_6$ - $t_7$ ] At  $t_6$ , the primary currents  $i_{c1}$  and  $i_{c2}$  increases to 0 A, which means the directions of  $i_{c1}$  and  $i_{c2}$  begin to change.

Stage 8 [ $t_7$ - $t_8$ ] At  $t_7$ , the primary current  $i_p$  increases to  $i_o/n$ ,  $D_{r2}$  and  $D_{r3}$  turn off, then the input power begins to be transferred to the output through  $T_r$ ,  $D_{r1}$ , and  $D_{r4}$ . During this stage, the primary current  $i_p$  is kept at  $i_o/n$ .

Stage 9 [ $t_8$ - $t_9$ ] At  $t_8$ , the switch  $S_4$  is turned off. The capacitor  $C_{s4}$  starts to charge, and the capacitor  $C_{s3}$  begins to discharge. This stage finishes until the voltage on  $C_{s4}$  increases to  $V_{in}/2$  and the voltage on  $C_{s3}$  decreases to 0 V.

Stage 10 [ $t_9$ - $t_{10}$ ] At  $t_9$ , the voltage on  $C_{s3}$  decreases to 0 V and diode  $D_3$  begins to conduct. The circuit operates in a free-wheeling mode with the primary current  $i_p$  flowing through  $L_r$ ,  $T_r$ ,  $C_b$ ,  $D_3$ ,  $C_1$ , and  $S_1$ .

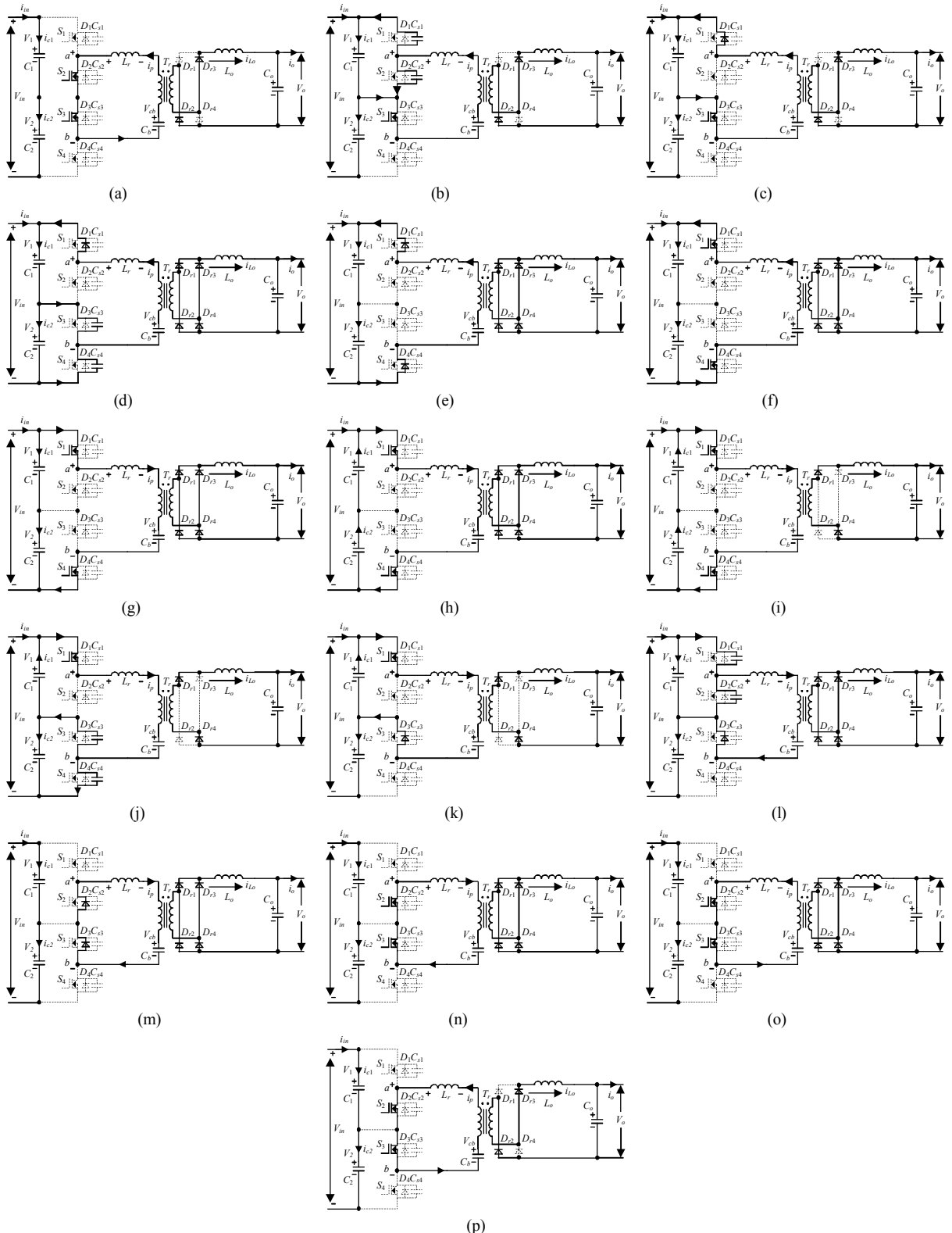


Fig. 3. Equivalent circuits in the operation mode I. (a) [before  $t_0$ ]. (b) [ $t_0 - t_1$ ]. (c) [ $t_1 - t_2$ ]. (d) [ $t_2 - t_3$ ]. (e) [ $t_3 - t_4$ ]. (f) [ $t_4 - t_5$ ]. (g) [ $t_5 - t_6$ ]. (h) [ $t_6 - t_7$ ]. (i) [ $t_7 - t_8$ ]. (j) [ $t_8 - t_9$ ]. (k) [ $t_9 - t_{10}$ ]. (l) [ $t_{10} - t_{11}$ ]. (m) [ $t_{11} - t_{12}$ ]. (n) [ $t_{12} - t_{13}$ ]. (o) [ $t_{13} - t_{14}$ ]. (p) [ $t_{14} - t_{15}$ ].

Stage 11 [ $t_{10}-t_{11}$ ] At  $t_{10}$ , the switch  $S_1$  is turned off. The capacitor  $C_{s1}$  starts to charge, and the capacitor  $C_{s2}$  begins to discharge. This stage finishes until the voltage on  $C_{s1}$  increases to  $V_{in}/2$  and the voltage on  $C_{s2}$  decreases to 0 V. The primary

current  $i_p$  starts to decrease, and it is not enough to provide  $i_o$ , so the rectifier diodes  $D_{r1}-D_{r4}$  conduct simultaneously. The current  $i_{c1}$  decreases to  $-i_{in}$ .

Stage 12 [ $t_{11}$ - $t_{12}$ ] At  $t_{11}$ , the voltage on  $C_{s2}$  becomes 0 V and diode  $D_2$  begins to conduct. The circuit operates in a free-wheeling mode with the primary current  $i_p$  flowing through  $L_r$ ,  $T_r$ ,  $C_b$ ,  $D_3$ , and  $D_2$ . During this stage, both current  $i_{c1}$  and  $i_{c2}$  are  $-i_{in}$ .

Stage 13 [ $t_{12}$ - $t_{13}$ ] At  $t_{12}$ , the switches  $S_2$  and  $S_3$  are turned on at zero-voltage. The primary current  $i_p$  would flow through  $L_r$ ,  $T_r$ ,  $C_b$ ,  $S_3$ , and  $S_2$ .

Stage 14 [ $t_{13}$ - $t_{14}$ ] At  $t_{13}$ , the primary current  $i_p$  decreases to 0 A and continues to decrease linearly, which means the direction of primary current  $i_p$  begins to change.

Stage 15 [ $t_{14}$ - $t_{15}$ ] At  $t_{14}$ , the primary current  $i_p$  decreases to  $-i_o/n$ ,  $D_{r1}$  and  $D_{r4}$  turn off, then the power from  $C_b$  is transferred to the output through  $T_r$ ,  $D_{r2}$ , and  $D_{r3}$ . During this stage, the primary current  $i_p$  is kept at  $-i_o/n$ .

At  $t_{15}$ , the following work operation in the next period starts, which is the same as the first switching period. The main difference between the operation mode I and operation mode II is that the currents  $i_{c1}$  and  $i_{c2}$  shift each other as figured by red color in Fig. 2. The operation principle analysis of the operation mode II is similar to that of the operation mode I, which is not repeated here.

### B. Conditions of ZVS Achievement

Before discussing the conditions of the ZVS achievement, one assumption is made that the four power switches  $S_1$  -  $S_4$  have the same parasitic capacitors namely  $C_s$ .

$$C_{s1} = C_{s2} = C_{s3} = C_{s4} = C_s \quad (10)$$

In the operation mode I, in order to ensure  $S_1$  or  $S_3$  realizing zero-voltage switch-on, the energy  $E_1$  is needed to fully discharge the parasitic capacitor of the in-coming switch and charge the parasitic capacitor of the out-going switch. Taking  $t_8$  in Fig. 2(a) as example,  $E_1$  for the switch  $S_3$  to achieve zero-voltage switch-on can be expressed as (11) according to the energy of these two parasitic capacitors.

$$E_1 = \frac{1}{2} \cdot C_{s3} \cdot \left(\frac{V_{in}}{2}\right)^2 + \frac{1}{2} \cdot C_{s4} \cdot \left(\frac{V_{in}}{2}\right)^2 = \frac{1}{4} \cdot C_s \cdot V_{in}^2 \quad (11)$$

During the time internal [ $t_8$ - $t_{10}$ ] as shown in Fig. 2(a), the output filter inductor is reflected to the primary side and is in series with the leakage inductance of the transformer. Therefore, the energy to achieve zero-voltage switch-on for  $S_1$  and  $S_3$  is provided by both the output filter inductance and the leakage inductance of the transformer. Normally, the output filter inductance is large enough to realize the zero-voltage switch-on for  $S_1$  and  $S_3$  even at light load.

The energy  $E_2$  from the leakage inductance of the transformer is used to achieve zero-voltage switch-on of switches  $S_2$  and  $S_4$ . In order to achieve the zero-voltage switch-on of  $S_2$  or  $S_4$ , the energy  $E_2$  should satisfy the requirement of (12) to fully discharge the parasitic capacitor of the in-coming switch and charge the parasitic capacitor of the out-going switch. The switches  $S_2$  and  $S_4$  are more difficult to achieve zero-voltage switch-on than that of  $S_1$  and  $S_3$  since the leakage inductance  $L_r$  is quite smaller than the reflected output filter inductance.

$$E_2 = \frac{1}{2} \cdot L_r \cdot \left(\frac{I_o}{n}\right)^2 \geq \frac{1}{4} \cdot C_s \cdot V_{in}^2 \quad (12)$$

In the operation mode II, the energy from both the output filter inductance and leakage inductance of the transformer is provided for the switches  $S_2$ ,  $S_4$  to realize the zero-voltage switch-on, and the energy from the leakage inductance of the transformer is provided for the switches  $S_1$ ,  $S_3$  to achieve the zero-voltage switch-on, which is just contrary to the operation mode I. The analysis of the ZVS achievement conditions in the operation mode II is similar to that in the operation mode I, which is not repeated here.

The ZVS achievement conditions under the proposed PWM strategy are almost the same as that under the conventional control strategy. For instance, the needed energy to achieve ZVS for the switch pairs  $S_2$ ,  $S_4$  and  $S_1$ ,  $S_3$  in the operation mode II is the same as that for the switch pairs  $S_2$ ,  $S_4$  and  $S_1$ ,  $S_3$  in the conventional control strategy shown in Fig. 1(b). Therefore, the switching losses under the conventional control strategy and proposed ZVS PWM strategy are almost the same.

### C. Proposed ZVS PWM Strategy Analysis

Assuming that the DC-blocking capacitor is large enough to be considered as a voltage source, the voltage on the DC-blocking capacitor  $V_{cb}$  in the steady states is

$$V_{cb} = \frac{V_{in}}{2} \quad (13)$$

If neglecting the duty cycle loss  $d_{loss}$ , the output voltage  $V_o$  can be obtained by (14) according to Fig. 2.

$$V_o = \frac{1}{n} \cdot [(V_{in} - V_{cb}) \cdot d_1 + V_{cb} \cdot d_1] \quad (14)$$

Substituting (13) into (14), then the output voltage  $V_o$  can be rewritten as

$$V_o = \frac{V_{in}}{n} \cdot d_1 \quad (15)$$

In the real operation, the duty cycle loss  $d_{loss}$  as shown in Fig. 2 would affect the output voltage  $V_o$ , which can be calculated by

$$d_{loss} = \frac{t_7 - t_2}{T_s} = \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s} \quad (16)$$

After considering the effect of the duty cycle loss  $d_{loss}$ , the output voltage  $V_o$  can be further expressed as (17) according to (15) and (16).

$$V_o = \frac{V_{in}}{n} \cdot (d_1 - d_{loss}) = \frac{V_{in}}{n} \cdot \left(d_1 - \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s}\right) \quad (17)$$

## IV. PROPOSED CAPACITOR CURRENT-BALANCING CONTROL

### A. Proposed Capacitor Current-Balancing Control

According to the analysis in the Section III, the main difference between the two operation modes of the proposed ZVS PWM strategy is the currents flowing through the two input capacitors. The RMS value of  $i_{c1}$  is bigger than that of  $i_{c2}$  in the operation mode I, but the RMS value of  $i_{c1}$  is smaller than that of  $i_{c2}$  in the operation mode II. Therefore, based on

this difference between the two operation modes of the proposed ZVS PWM strategy, a capacitor current-balancing control for balancing the two currents  $i_{c1}$  and  $i_{c2}$  is proposed by alternating the two operation modes as shown in Fig. 4.

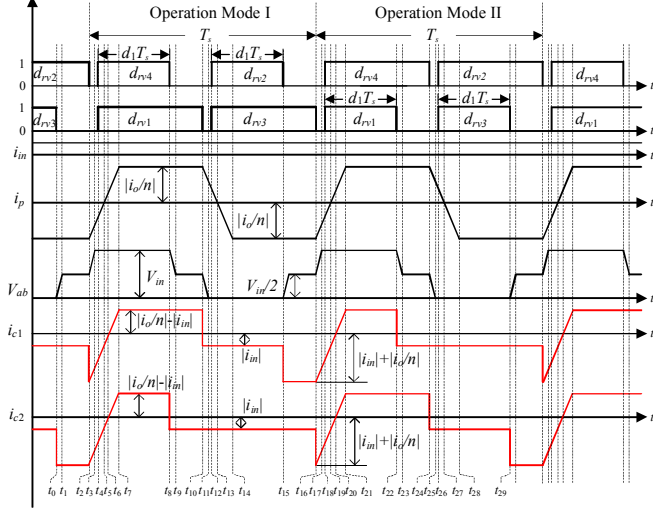


Fig. 4. Proposed capacitor current-balancing control with main waveforms.

In the proposed control, the operation mode I is used in the first switching period and the operation mode II is used in the second switching period, which achieves that the currents on the two input capacitors are the same in every two switching periods as shown in Fig. 4.

The proposed capacitor current-balancing control operates by alternating the two operation modes of the proposed ZVS PWM strategy, so the ZVS achievement conditions of the proposed capacitor current-balancing control are the combination of the ZVS achievement conditions of the two operation modes. In the first switching period, as shown in Fig. 4 (Operation Mode I), the energy from both the output filter inductance and leakage inductance of the transformer is provided for  $S_3, S_4$  to realize the zero-voltage switch-on, and the energy from the leakage inductance of the transformer is provided for  $S_1, S_2$  to achieve the zero-voltage switch-on. In the second switching period, as shown in Fig. 4 (Operation Mode II), the ZVS achievement conditions are just contrary to that in the first switching period, which means the energy from both the output filter inductance and leakage inductance of the transformer is provided for  $S_1, S_2$  to realize the zero-voltage switch-on, and the energy from the leakage inductance of the transformer is provided for  $S_3, S_4$  to achieve the zero-voltage switch-on.

### B. Input Capacitor Current Analysis

In Fig. 4, the currents on the two input capacitors  $i_{c1}$  and  $i_{c2}$  in two switching periods can be expressed as

$$i_{c1} = \begin{cases} -i_{in} & t_0 \leq t < t_2 \\ i_p - i_{in} & t_2 \leq t < t_{10} \\ -i_{in} & t_{10} \leq t < t_{15} \\ i_p - i_{in} & t_{15} \leq t < t_{22} \\ -i_{in} & t_{22} \leq t < t_{29} \end{cases} \quad (18)$$

$$i_{c2} = \begin{cases} i_p - i_{in} & t_0 \leq t < t_8 \\ -i_{in} & t_8 \leq t < t_{16} \\ i_p - i_{in} & t_{16} \leq t < t_{24} \\ -i_{in} & t_{24} \leq t < t_{29} \end{cases} \quad (19)$$

According to Fig. 4, the primary current  $i_p$  in one switching period can be expressed as

$$i_p = \begin{cases} -\frac{i_o}{n} & t_0 \leq t < t_2 \\ -\frac{i_o}{n} + \frac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) & t_2 \leq t < t_7 \\ \frac{i_o}{n} & t_7 \leq t < t_{10} \\ \frac{i_o}{n} - \frac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) & t_{10} \leq t < t_{14} \\ -\frac{i_o}{n} & t_{14} \leq t < t_{15} \end{cases} \quad (20)$$

Substituting (20) into (18) and (19),  $i_{c1}$  and  $i_{c2}$  in two switching periods can be rewritten as

$$i_{c1} = \begin{cases} -i_{in} & t_0 \leq t < t_2 \\ \frac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) - \frac{i_o}{n} - i_{in} & t_2 \leq t < t_7 \\ \frac{i_o}{n} - i_{in} & t_7 \leq t < t_{10} \\ -i_{in} & t_{10} \leq t < t_{15} \\ -\frac{i_o}{n} - i_{in} & t_{15} \leq t < t_{16} \\ \frac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) - \frac{i_o}{n} - i_{in} & t_{16} \leq t < t_{21} \\ \frac{i_o}{n} - i_{in} & t_{21} \leq t < t_{22} \\ -i_{in} & t_{22} \leq t < t_{29} \end{cases} \quad (21)$$

$$i_{c2} = \begin{cases} -\frac{i_o}{n} - i_{in} & t_0 \leq t < t_2 \\ \frac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) - \frac{i_o}{n} - i_{in} & t_2 \leq t < t_7 \\ \frac{i_o}{n} - i_{in} & t_7 \leq t < t_8 \\ -i_{in} & t_8 \leq t < t_{16} \\ \frac{V_{in}}{2 \cdot L_r} \cdot (t - t_2) - \frac{i_o}{n} - i_{in} & t_{16} \leq t < t_{21} \\ \frac{i_o}{n} - i_{in} & t_{21} \leq t < t_{24} \\ -i_{in} & t_{24} \leq t < t_{29} \end{cases} \quad (22)$$

In Fig. 4, the time intervals  $[t_2 - t_7]$  and  $[t_{16} - t_{21}]$  are the same, which can be described as

$$t_7 - t_2 = t_{21} - t_{16} = \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in}} \quad (23)$$

According to (21) ~ (23), the RMS values of  $i_{c1}$  and  $i_{c2}$

under the proposed capacitor current-balancing control namely  $i_{c1\_rms\_pro}$  and  $i_{c2\_rms\_pro}$  can be calculated by (24), which is listed in Table I.

$$i_{c1\_rms\_pro} = i_{c2\_rms\_pro} = \sqrt{\frac{i_{in}^2 + \frac{i_o^2}{2 \cdot n^2} + \frac{8 \cdot L_r \cdot i_{in} \cdot i_o^2}{n^2 \cdot V_{in} \cdot T_s}}{\frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n} - \frac{8 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}}} \quad (24)$$

From Table I, it can be observed that: 1) under the conventional control strategy, the RMS values of  $i_{c1}$  and  $i_{c2}$  are imbalanced, and the RMS value of  $i_{c1}$  is smaller than that of  $i_{c2}$  because  $d_2$  is bigger than  $d_1$  in the normal operations; 2) after utilizing the proposed control, the RMS values of  $i_{c1}$  and  $i_{c2}$  become the same, which means that the current imbalance among the two input capacitors in the four-switch HBTL DC/DC converter is eliminated by utilizing the proposed capacitor current-balancing control. One thing need to be mentioned is that (7), (8), and (24) are derived based on the continuous primary current  $i_p$ , therefore these equations are only suitable for the continuous conduction mode (CCM).

By putting the circuit parameters in the Appendix into (7), (8), and (24), the calculated RMS values of  $i_{c1}$  and  $i_{c2}$  with various output power and output voltages are presented in Fig. 5 when the output voltage is 50 V. In addition, the calculated results by (9) about the difference between the RMS values of  $i_{c1}$  and  $i_{c2}$  under the conventional control strategy  $\Delta i_{c\_rms\_con}$  are shown in Fig. 6.

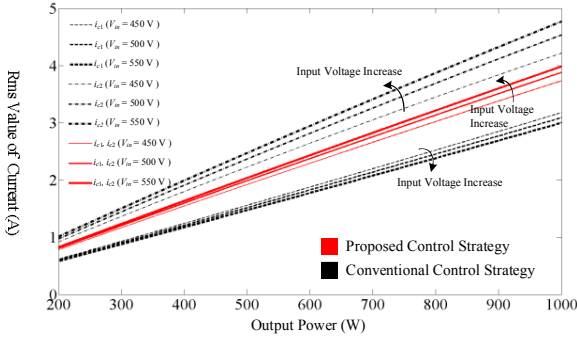


Fig. 5. Calculated RMS values of  $i_{c1}$  and  $i_{c2}$  with various input voltages and output power.

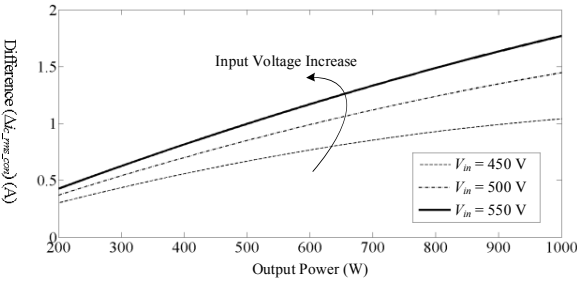


Fig. 6. Calculated difference between the RMS values of  $i_{c1}$  and  $i_{c2}$  with various input voltages and output power under the conventional control strategy.

From Figs. 5 and 6, it can be seen that: 1) under the conventional control strategy, the RMS values of  $i_{c1}$  and  $i_{c2}$  are imbalanced, the RMS value of  $i_{c2}$  is bigger than that of  $i_{c1}$ ; 2) such capacitor current imbalance under the conventional

control strategy becomes larger along with the output power increasing and input voltage increasing as shown in Fig. 6, and the largest difference reaches 1.77 A when the output power increases to 1-kW and the input voltage increases to 550 V; 3) under the proposed control, the RMS values of  $i_{c1}$  and  $i_{c2}$  are kept balanced along with the output power increasing and output voltage increasing, and these RMS values of  $i_{c1}$  and  $i_{c2}$  range between the RMS values of  $i_{c1}$  and  $i_{c2}$  under the conventional control strategy.

### C. Switching Loss Distribution Analysis

Based on the above analysis, it can be observed that the two power switches whose energy to achieve ZVS is from the leakage inductance of the transformer would firstly lose ZVS in comparison with the other two power switches whose energy to achieve ZVS is from the both the output filter inductance and leakage inductance of the transformer at the light load situation. As to the conventional control strategy as shown in Fig. 1(b),  $S_1$  and  $S_3$  would always firstly lose zero-voltage switch-on at the light load while  $S_2$ ,  $S_4$  can still realize zero-voltage switch-on, which means that the switching losses of  $S_1$  and  $S_3$  are more than that of  $S_2$  and  $S_4$ . However, as to the proposed capacitor current-balancing control as show in Fig. 4,  $S_1$ ,  $S_2$  would firstly lose zero-voltage switch-on in the first switching period but  $S_3$ ,  $S_4$  would firstly lose zero-voltage switch-on in the second switching period according to the above theoretical analysis in the Section IV-A, which means the ZVS achievement conditions of ( $S_1$ ,  $S_2$ ) and ( $S_3$ ,  $S_4$ ) are shifted each other in every two switching periods. Therefore, the switching losses caused by the hard switching at the light load situation can be distributed evenly among the four power switches under the proposed capacitor current-balancing control.

In order to simplify the theoretical calculation about the switching losses of the power switches at the light load situation, one assumption is made that the two switches of the four switches would firstly lose zero-voltage switch-on when the energy of the leakage inductance  $E_2$  as (12) decreases to ten percentage of the energy that can fully realize zero-voltage switch-on. Therefore, two switches are not able to realize zero-voltage switch-on when the output power is about 200 W according to (12) and the circuit parameters in the Appendix. Based on [32], the theoretical calculation about the switching losses of the four power switches under the conventional control strategy and proposed control strategy is shown in Fig. 7, where the output power is 200 W. From Fig. 7, it can be observed that: 1) the switching losses of  $S_1$  and  $S_3$  are bigger than that of  $S_2$  and  $S_4$  under the conventional control strategy; 2) the switching loss of each switch is the same under the proposed control. Therefore, the thermal stresses on the four power switches  $S_1$ - $S_4$  would be more balanced under the proposed capacitor current-balancing control than that under the conventional control strategy at the light load situation, which can improve the reliability of the converter.

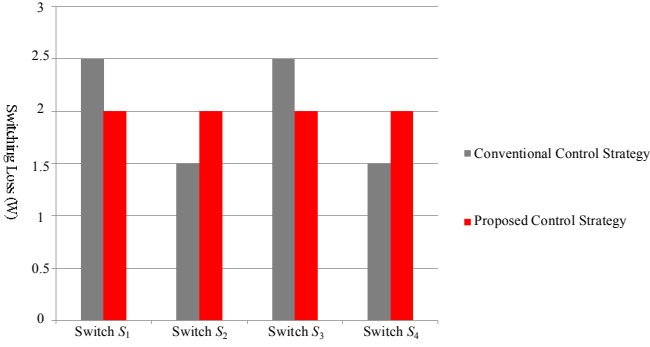


Fig. 7. Calculated switching losses of the four power switches when the output power is 200 W.

## V. SIMULATION AND EXPERIMENTAL VERIFICATION

### A. Simulation Verification

In order to verify the proposed control strategy, a simulation model of the four-switch HBTL DC/DC converter is built in PLECS, whose circuit parameters are listed in the Appendix. In the simulation, the input voltage is 550 V, the output voltage is 50 V, and the output power is 1-kW.

Fig. 8(a) shows the performances under the conventional control strategy, where  $i_{c1}$  and  $i_{c2}$  are imbalanced. Under the conventional control strategy, the RMS values of  $i_{c1}$  and  $i_{c2}$  are 3.05 A and 5.11 A, and their average values are both 0 A. Fig. 8(b) shows the performances under the proposed control strategy, where  $i_{c1}$  and  $i_{c2}$  are kept balanced. Under the proposed control strategy, the RMS values of  $i_{c1}$  and  $i_{c2}$  are both 4.2 A, and their average values are both 0 A. From Fig. 8, it can be also observed that the currents  $i_{c1}$  and  $i_{c2}$  are kept same in every two switching periods as marked in Fig. 8(b), which is consistent with the above theoretical analysis. In summary, the simulation results verify that the current imbalance among the two input capacitors is effectively eliminated with the help of the proposed capacitor current-balancing control.

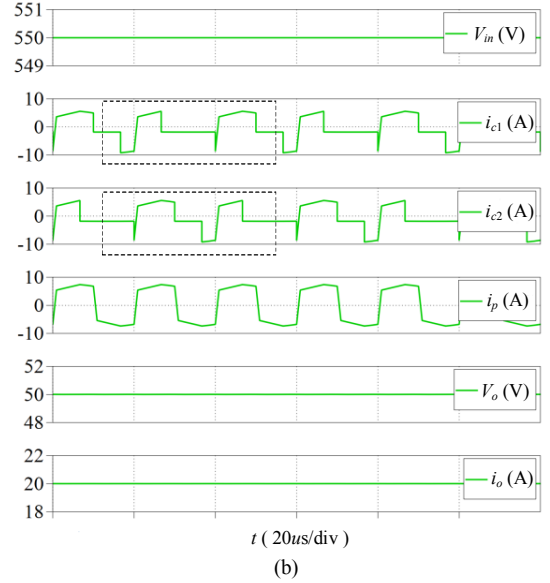
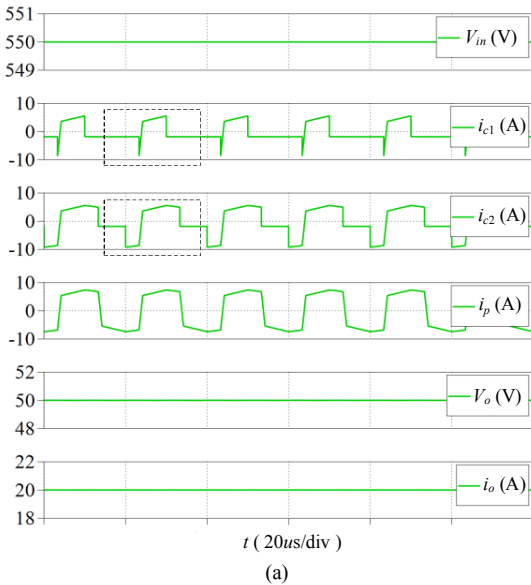
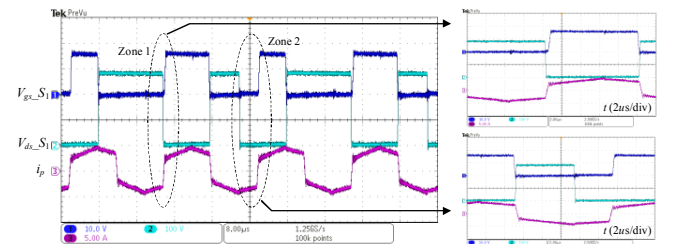


Fig. 8. Simulation results including  $V_{in}$ ,  $V_o$ ,  $i_{c1}$ ,  $i_{c2}$ ,  $i_p$ , and  $i_o$ . (a) Conventional control strategy. (b) Proposed control strategy.

### B. Experimental Verification

A 1-kW four-switch HBTL DC/DC converter prototype is built to verify the proposed control strategy. The specifications of the built prototype are listed in the Appendix. In the experiments, the input voltage is 450 V ~ 550 V, and the output voltage  $V_o$  is 50 V.

Figs. 9 and 10 show the ZVS achievement conditions under the proposed control strategy. Fig. 9 shows the primary current  $i_p$ , driving signal  $V_{gs\_S1}$ , and drain-source voltage  $V_{ds\_S1}$  of the power switch  $S_1$ , which illustrates that  $S_1$  realizes ZVS and its voltage stress is half of the input voltage. Figs. 9(a) and (b) show ZVS of  $S_1$  under 500 W and 1-kW, respectively. In Fig. 9, the energy from the leakage inductance of the transformer is provided for  $S_1$  to achieve the zero-voltage switch-on at zone 1, and the energy from both the output filter inductance and leakage inductance of the transformer is provided for  $S_1$  to realize the zero-voltage switch-on at zone 2. Fig. 10 shows the primary current  $i_p$ , driving signal  $V_{gs\_S3}$ , and drain-source voltage  $V_{ds\_S3}$  of the power switch  $S_3$ , which illustrates that  $S_3$  realizes ZVS and its voltage stress is half of the input voltage. Figs. 10(a) and (b) show ZVS of  $S_3$  under 500 W and 1-kW, respectively. In Fig. 10, the energy from both the output filter inductance and leakage inductance of the transformer is provided for  $S_3$  to achieve the zero-voltage switch-on at zone 1, and the energy from the leakage inductance of the transformer is provided for  $S_3$  to realize the zero-voltage switch-on at zone 2.



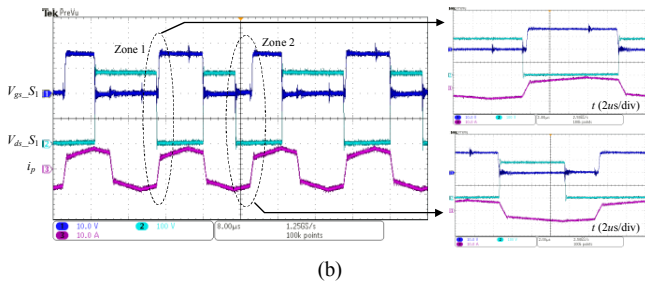


Fig. 9. Driving signal and drain-source voltage of switch  $S_1$ , and primary current  $i_p$ . (a) at  $V_{in} = 550$  V and  $P_o = 500$  W. (b) at  $V_{in} = 550$  V and  $P_o = 1$ -kW.

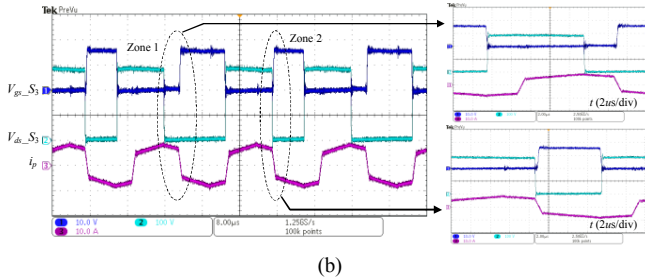
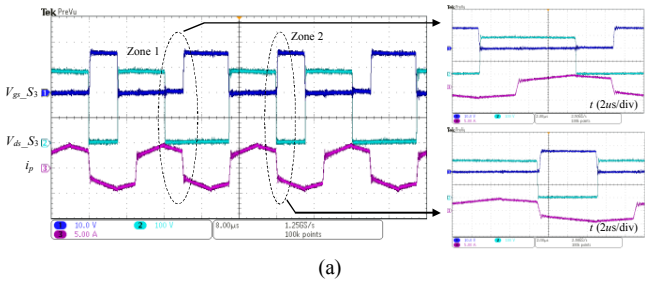


Fig. 10. Driving signal and drain-source voltage of switch  $S_3$ , and primary current  $i_p$ . (a) at  $V_{in} = 550$  V and  $P_o = 500$  W. (b) at  $V_{in} = 550$  V and  $P_o = 1$ -kW.

Figs. 11 - 13 show the performances of the prototype under the working conditions that the input voltage  $V_{in}$  is 550 V and the output power namely  $P_o$  is 1-kW. Figs. 11(a) and (b) show the currents  $i_p$ ,  $i_o$  and voltages  $V_{in}$ ,  $V_o$  under the conventional control strategy and proposed control strategy, respectively. From Fig. 11, it can be seen that the primary currents  $i_p$  are almost the same under the two control strategies. Figs. 12(a) and (b) show the voltages on the two input capacitors  $V_1$ ,  $V_2$ , the voltage on the DC-blocking capacitor  $V_{cb}$ , and current  $i_{c2}$  under the conventional and proposed control strategy, respectively. From Fig. 12, it can be observed that  $V_1$  and  $V_2$  are constant and balanced in the steady states under the two control strategies. The measured average values of the capacitor voltages  $V_1$  and  $V_2$  are both 271 V under the conventional control strategy, and they are both 273 V under the proposed control strategy. Fig. 13(a) shows that the currents through the two input capacitors  $i_{c1}$  and  $i_{c2}$  are imbalanced under the conventional control strategy, whose RMS values are 3.16 A, 5.18 A and average values are 125 mA, 160 mA. Therefore, the difference between the RMS values of  $i_{c1}$  and  $i_{c2}$  is 2.02 A under the conventional control strategy. Fig. 13(b) shows that under the proposed control  $i_{c1}$  and  $i_{c2}$  are kept same in every two switching periods as marked in Fig. 13(b), their RMS values are both 4.37 A and average values are 135 mA, 155 mA, which is consistent with the theoretical analysis in the Section IV.

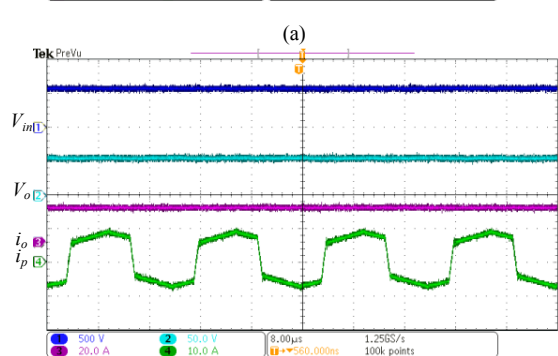
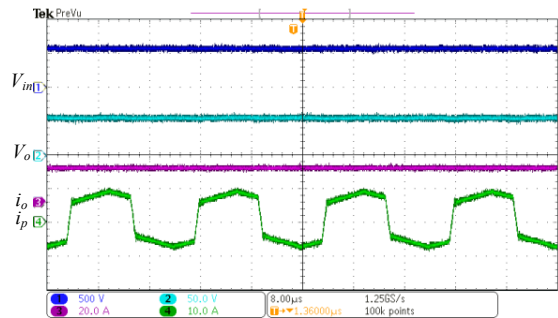


Fig. 11. Experimental results including  $V_{in}$ ,  $V_o$ ,  $i_o$ , and  $i_p$  at  $V_{in} = 550$  V and  $P_o = 1$ -kW. (a) Conventional control strategy. (b) Proposed control strategy.

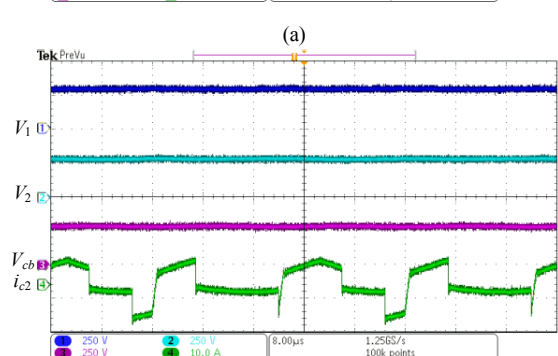
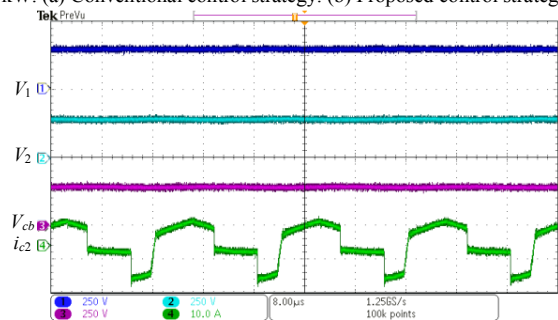


Fig. 12. Experimental results including  $V_1$ ,  $V_2$ ,  $V_{cb}$ , and  $i_{c2}$  at  $V_{in} = 550$  V and  $P_o = 1$ -kW. (a) Conventional control strategy. (b) Proposed control strategy.

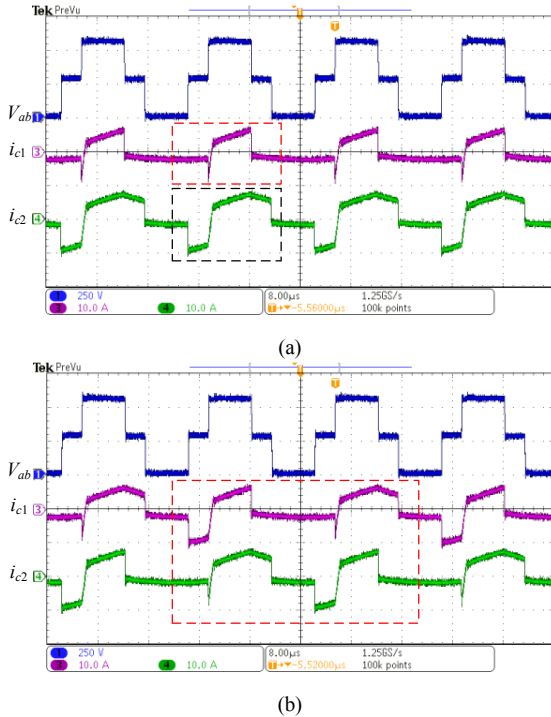


Fig. 13. Experimental results including  $V_{ab}$ ,  $i_{c1}$ , and  $i_{c2}$  at  $V_{in} = 550$  V and  $P_o = 1$ -kW. (a) Conventional control strategy. (b) Proposed control strategy.

Fig. 14 shows the measured RMS values of  $i_{c1}$  and  $i_{c2}$  under various input voltages, where the output voltage is 50 V and the output power  $P_o$  is 1-kW. From Fig. 14, it can be seen that: 1) the RMS values of  $i_{c1}$  and  $i_{c2}$  are imbalanced under the conventional control strategy; 2) with the input voltage increasing, the current imbalance between the RMS values of  $i_{c1}$  and  $i_{c2}$  becomes larger under the conventional control strategy, and the biggest difference reaches 2.02 A while the input voltage increases to 550 V; 3) under the proposed control strategy, the RMS values of  $i_{c1}$  and  $i_{c2}$  are almost the same along with the input voltage increasing and range between the RMS values of  $i_{c1}$  and  $i_{c2}$  under the conventional control strategy; 4) the experimental results about the currents on the two input capacitors are consistent with the theoretical analysis in the Section IV-B. Based on the experimental results shown in Fig. 14, it can be concluded that the current imbalance among the two input capacitors in the four-switch HBTL DC/DC converter can be eliminated by utilizing the proposed control strategy.

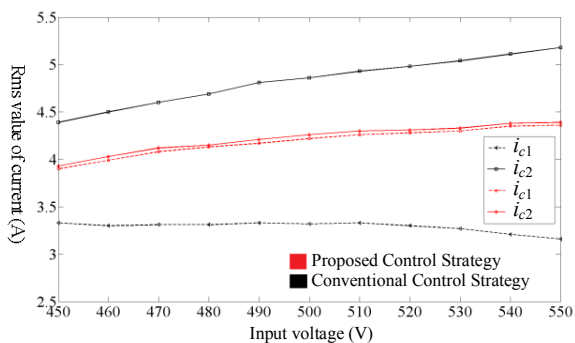


Fig. 14. Measured RMS values of  $i_{c1}$  and  $i_{c2}$  under various input voltages when  $V_o = 50$  V and  $P_o = 1$ -kW.

Fig. 15 shows the dynamic performance of the proposed control strategy. In Fig. 15, the output load changes from 1-kW to 500 W and finally gets back to 1-kW when the input voltage  $V_{in}$  is 550 V and output voltage  $V_o$  is 50 V. From Fig. 15, it can be observed that the voltages on the two input capacitors  $V_1$ ,  $V_2$  and the voltage on the DC-blocking capacitor  $V_{cb}$  are all constant under the proposed control strategy when the load changes.

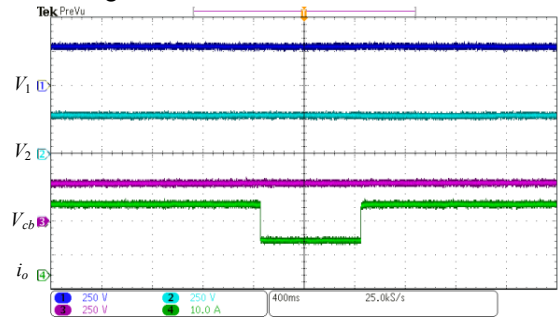


Fig. 15. Dynamic performance under load changes when  $V_{in} = 550$  V and  $V_o = 50$  V.

The measured efficiency curves with various input voltages (450 V, 500 V, and 550 V) are presented in Fig. 16 when the output voltage  $V_o$  is 50 V.

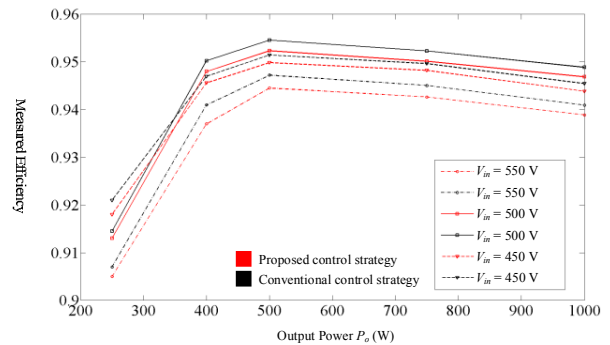


Fig. 16. Measured efficiency curves with various input voltages when  $V_o = 50$  V.

The peak efficiency under the proposed control strategy is over 95%. With the input voltage  $V_{in}$  increasing while the output power is constant, 1) the conduction losses of the primary side would decrease because the input current would decrease; 2) the switching losses would increase because ZVS achievement conditions would become worse. Whether the efficiency of the converter would increase or decrease with the input voltage increasing is decided by the combination of 1) and 2). Therefore, the reason why the efficiency under 500 V is higher than that under 550 V in Fig. 16 is that the value of the increasing switching losses is higher than that of the decreasing conduction losses when the input voltage  $V_{in}$  changes from 500 V to 550 V. In addition, the efficiencies under the proposed control strategy are slightly lower than that under the conventional control strategy, whose reason is that MOSFET is used for the power switches in the built prototype. For MOSFET, the primary current  $i_p$  flows through the body diodes of the power switches instead of the power switches in the free-wheeling time under the proposed control, which would increase the conduction losses comparing with the

conventional control strategy. If the input voltage increases and IGBT is selected for the power switches, the efficiencies under the two control strategies would be almost the same.

## VI. CONCLUSION

This paper proposes a ZVS PWM strategy and a capacitor current-balancing control for the HBTL DC/DC converter. Under the conventional control strategy, there exists a current imbalance among the two input capacitors in the four-switch HBTL DC/DC converter due to the effect from the output inductance of the input power supply and the inductance of the input line on the input current, which would make influence on the converter's reliability. The proposed ZVS PWM strategy is composed of two operation modes. Based on the proposed ZVS PWM strategy, a capacitor current-balancing control is proposed by alternating the two operation modes of the proposed PWM strategy, which can effectively eliminate the current imbalance among the two input capacitors. Therefore, the performance and reliability of the converter can be improved by balancing the thermal stresses and lifetimes among the two input capacitors. Finally, the simulation and experimental results verify the feasibility and effectiveness of the proposed control strategy.

## APPENDIX

See Table II.

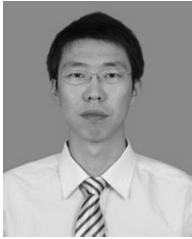
TABLE II  
PARAMETERS OF THE SIMULATION MODEL AND EXPERIMENTAL PROTOTYPE

Description	Parameter
Power Switches $S_1 - S_4$	SPW47N60C3
Rectifier Diodes $D_{r1} - D_{r4}$	MBR40250TG
Turns Ratio of Transformer $T_r$	25 : 8
Leakage Inductance $L_r$ ( $\mu\text{H}$ )	20.7
Output Filter Capacitor $C_o$ ( $\mu\text{F}$ )	470
Output Filter Inductor $L_o$ ( $\mu\text{H}$ )	140
Input Capacitors $C_1$ and $C_2$ ( $\mu\text{F}$ )	14.4
DC-blocking Capacitor $C_b$ ( $\mu\text{F}$ )	12
Switching Frequency (kHz)	50
Dead Time (ns)	400
Input Inductance ( $\mu\text{H}$ ) (Including the output inductance of the input power supply and inductance of the input line)	60

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