Periodically Swapping Modulation (PSM) Strategy for Three-Level (TL) DC/DC Converters With Balanced Switch Currents

Liu, Dong; Deng, Fujin; Zhang, Qi; Chen, Zhe

Published in:
IEEE Transactions on Industrial Electronics

DOI (link to publication from Publisher):
10.1109/TIE.2017.2714125

Publication date:
2018

Document Version
Accepted author manuscript, peer reviewed version

Periodically Swapping Modulation (PSM) Strategy for Three-Level (TL) DC/DC Converters with Balanced Switch Currents

Dong Liu, *Student Member, IEEE*, Fujin Deng, *Member, IEEE*, Qi Zhang, *Member, IEEE* and Zhe Chen, *Senior Member, IEEE*

***Abstract*—The asymmetrical modulation strategy is widely used in various types of three-level (TL) DC/DC converters, while the current imbalance among the power switches is one of the important issues. In this paper, a novel periodically swapping modulation (PSM) strategy is proposed for balancing the power switches' currents in various types of TL DC/DC converters. In the proposed PSM strategy, the driving signals of the switch pairs are swapped periodically, which guarantees that the currents through the power switches are kept balanced in every two switching periods. Therefore, the proposed PSM strategy can effectively improve the reliability of the converter by balancing the power losses and thermal stresses among the power switches. The operation principle and performances of the proposed PSM strategy are analyzed in detail. Finally, the simulation and experimental results are presented to verify the proposed modulation strategy.**

***Index Terms*— DC/DC converter, periodically swapping modulation (PSM), three-level (TL).**

I. INTRODUCTION

The three-level (TL) DC/DC converter is attractive for the high input voltage applications [1-5] because the power switches only need to withstand half of the input voltage in the TL DC/DC converter. In [6], the TL circuit structure was firstly applied into the DC/DC converter. Based on the conventional TL DC/DC converter in [6], many studies about the TL DC/DC converter have been carried out [7-12]. In [7], a zero-voltage and zero-current switching TL DC/DC converter was proposed, in which a flying capacitor in the primary side was added to make the phase-shift control strategy applicable in the TL DC/DC converter. Based on [7], an auxiliary circuit was added in the secondary side to reduce the circulating current [8]. A new TL DC/DC converter composed of one TL leg and one two-level leg was proposed in [9] for the high power applications. Reference [10] proposed a zero-voltage switching (ZVS) DC/DC converter with two TL circuits sharing the same power switches, which can reduce the current stresses on the transformer windings and output rectifiers. In [11], a zero-voltage and zero current-switching TL DC/DC converter combining a TL converter and full-bridge converter was proposed to reduce the output filter inductance. In addition, a hybrid TL DC/DC converter composed of a full-bridge TL converter and a half-bridge TL converter was proposed to extend the ZVS range in [12]. In order to achieve soft switching for the converter's efficiency improvement, the phase-shift control strategy is utilized in the above various types of TL D/DC converters [6-12].

The asymmetrical modulation strategy is another modulation strategy, which is also widely used in various types of TL DC/DC converters [13-16]. In [13], a TL DC/DC converter based on the flying capacitor was proposed, which features with the simple and compact circuit structure. A new TL DC/DC converter with two transformers was proposed in [14] to reduce the current stresses on the transformer windings. Reference [15] proposed a dual half-bridge cascaded TL DC/DC converter, which is composed of two half-bridge cells and two transformers. In addition, a novel four-switch TL DC/DC converter was proposed in [16], which only adds one DC-blocking capacitor but removes two clamped diodes in comparison with the conventional TL DC/DC converter [6]. The asymmetrical modulation strategy realizes the soft switching for the above various types of TL DC/DC converters [13-16]. However, there is one important issue about the conventional asymmetrical modulation strategy that the currents through the primary power switches are imbalanced.

Many studies have been carried recently on the TL DC/DC converters, which mainly focus on the topics of extending the soft switching range [17], [18], reducing the circulating currents [19], and balancing the voltages on the input capacitors [20], [21]. However, until now there are few studies discussing about such current imbalance of the primary power switches in the TL DC/DC converters under the conventional asymmetrical modulation strategy, which would affect the reliability of the converter by causing the power loss

Manuscript received December 22, 2016; revised March 06, 2017, April 06, 2017, and April 25, 2017; accepted May 24, 2017.

Dong Liu, and Zhe Chen are with the Department of Energy Technology, Aalborg University, Aalborg, 9220 Denmark (email: dli@et.aau.dk, zch@et.aau.dk).

Fujin Deng is with the School of Electrical Engineering, Southeast University, Nanjing, 210000 China (email: dfjqfa@163.com).

Qi Zhang is with the Department of Electrical Engineering, Xi'an University of Technology, Xi'an, 710000 China (email: zhangqi_hero@163.com).

imbalance and thermal stress imbalance among the power switches [22], [23].

In this paper, a novel periodically swapping modulation (PSM) strategy is proposed, which can be used for various types of TL DC/DC converter to balance the currents flowing through the power switches. In the proposed modulation strategy, the driving signals of the switch pairs are swapped periodically, which would keep the power switches' currents balanced in every two switching periods. Consequently, the proposed modulation strategy can balance the power losses and thermal stresses among the power switches in the TL DC/DC converter, which can thus improve the reliability of the TL DC/DC converter. In this paper, the four-switch TL DC/DC converter [16] as shown in Fig. 1(a) is selected as a sample to analyze the operation principle and performances of the proposed PSM strategy. The analysis of other types of TL DC/DC converters [13-16] under the proposed modulation strategy is similar to that of the four-switch TL DC/DC converter.

This paper is organized as follows. Section II analyzes the power switches' current imbalance issue under the conventional modulation strategy. Section III introduces the operation principle of the proposed PSM strategy. Section IV analyzes the characteristics and performances of the four-switch TL DC/DC converter under the proposed modulation strategy in detail. Section V presents the simulation and experimental results to verify the effectiveness and feasibility of the proposed modulation strategy. Finally, the main contributions are summarized in Section VI.

II. Current Imbalance Analysis under Conventional Asymmetrical Modulation Strategy

Figs. 1(a) and 1(b) show the circuit structure of the four-switch TL DC/DC converter and conventional asymmetrical modulation strategy with the main operation waveforms, respectively. In Fig. 1(a), two input capacitors C_1 and C_2 are used to split the input voltage V_{in} into two voltages V_1 and V_2; S_1 - S_4 and D_1 - D_4 are primary power switches and diodes; T_r is the high frequency transformer; L_r is the leakage inductance of T_r; C_{s1} - C_{s4} are the parasitic capacitors of S_1 - S_4; C_b is the DC-blocking capacitor in the primary side. In the secondary side, there are four rectifier diodes D_{r1} - D_{r4}, one output filter inductor L_o, and one output filter capacitor C_o. In Fig. 1(a), i_p is the primary current of the transformer T_r; i_1, i_2, i_3, and i_4 are the currents through the primary power devices (S_1, D_1), (S_2, D_2), (S_3, D_3), and (S_4, D_4); i_{in} is the input current; i_{c1} and i_{c2} are the currents flowing through the two input capacitors C_1 and C_2; i_{Lo} is the current through L_o; V_{cb} is the voltage on the DC-blocking capacitor C_b; i_o and V_o are the output current and output voltage; V_{ab} is the voltage between point a and b; n is the turns ratio of the transformer T_r. In Fig. 1(b), d_{rv1} - d_{rv4} are four driving signals of the power switches S_1 - S_4, where (S_1, S_2) and (S_3, S_4) are complementary switch pairs; d_1 and d_2 are duty ratios in one switching period and d_2 is 1 - d_1 if neglecting the dead time. From Fig. 1(b), it can be seen that the currents (i_1, i_3) and (i_2, i_4) are different because d_2 is larger than d_1, which would result in the power loss imbalance and thermal stress imbalance among the primary power switches.

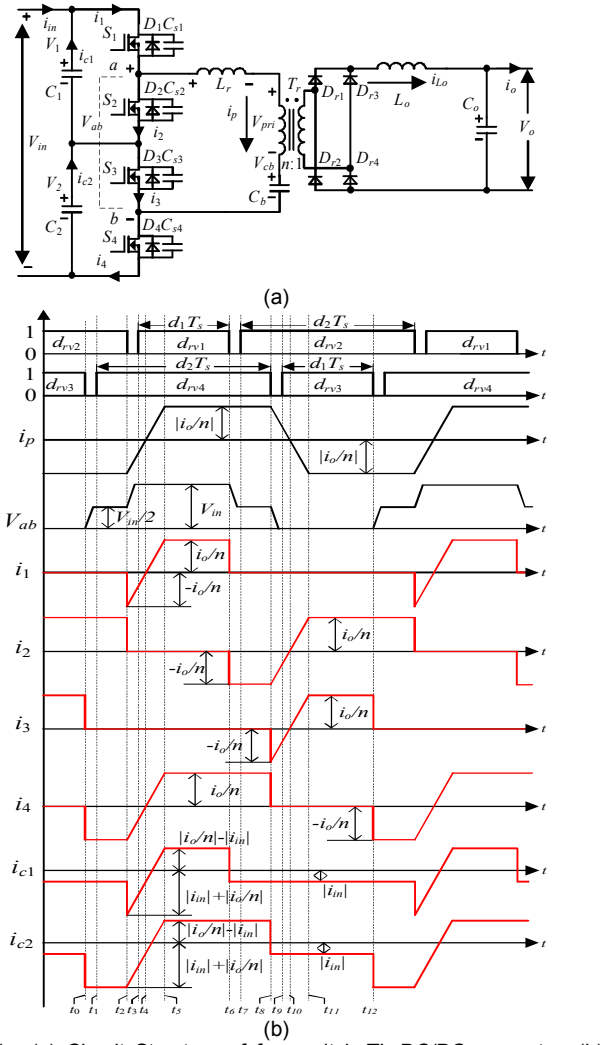


Fig. 1. (a) Circuit Structure of four-switch TL DC/DC converter. (b) Conventional asymmetrical modulation strategy [16] with main operation waveforms.

In order to simplify the analysis about the currents through the four power switches in the four-switch TL DC/DC converter, several assumptions are made that: 1) the inductance of the output filter inductor L_o is large enough to be considered as a current source; 2) the power switches S_1 - S_4 and diodes D_1 - D_4 are ideal; 3) the two input capacitors and DC-blocking capacitor are large enough to be regarded as the constant voltage sources with the value of $V_{in}/2$.

From Fig. 1(b), it can be seen that the current pairs (i_1, i_3) and (i_2, i_4) are the same respectively in every switching period. Therefore, only the expressions of the currents i_1 and i_2 in one switching period are given as

$$i_1 = \begin{cases} -\dfrac{i_o}{n} + \dfrac{V_{in}}{2 \cdot L_r} \cdot t & [t_2 - t_5] \\ \dfrac{i_o}{n} & [t_5 - t_6] \end{cases} \tag{1}$$

$$i_2 = \begin{cases} \dfrac{i_o}{n} & [t_0 - t_2] \\ -\dfrac{i_o}{n} & [t_6 - t_8] \\ -\dfrac{i_o}{n} + \dfrac{V_{in}}{2 \cdot L_r} \cdot t & [t_8 - t_{11}] \\ \dfrac{i_o}{n} & [t_{11} - t_{12}] \end{cases} \quad (2)$$

According to (1) and (2), the root mean square (RMS) values of the currents i_1, i_2, i_3, and i_4 under the conventional asymmetrical modulation strategy namely $i_{1\_rms\_c}$, $i_{2\_rms\_c}$, $i_{3\_rms\_c}$, and $i_{4\_rms\_c}$ can be calculated by

$$i_{1\_rms\_c} = i_{3\_rms\_c} = \sqrt{\frac{i_o^2}{n^2} \cdot d_1 - \frac{8 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \quad (3)$$

$$i_{2\_rms\_c} = i_{4\_rms\_c} = \sqrt{\frac{i_o^2}{n^2} \cdot d_2 - \frac{8 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \quad (4)$$

From (3) and (4), it can be observed that the RMS values of (i_1, i_3) and (i_2, i_4) are different because d_1 and d_2 are normally different in the asymmetrical modulation strategy [24-26]. This current imbalance would result in the power loss imbalance and thermal stress imbalance among the primary power switches, which would thus affect the converter's reliability.

III. Proposed Periodically Swapping Modulation Strategy

The PSM strategy is proposed for various types of TL DC/DC converters, where the driving signals of the switch pairs are swapped periodically in order to balance the power switches' currents. Fig. 2 shows the proposed PSM for the four-switch TL DC/DC converter configuration, where the main operation waveforms are presented.

The proposed PSM strategy operates by swapping the driving signals of the switching pairs (S_1, S_4) and (S_2, S_3) respectively in every switching period to make the currents flowing through the four power switches balanced in every two switching periods as shown in Fig. 2, which means that 1) in the first switching period, the duty ratios of d_{rv1} and d_{rv3} are both 0.5 if neglecting the dead time, the duty ratios of d_{rv2} and d_{rv4} are both d_1; and 2) in the second switching period, the duty ratios of d_{rv2} and d_{rv4} are both 0.5 if neglecting the dead time, the duty ratios of d_{rv1} and d_{rv3} are both d_1. In the real applications, the output voltage V_o is controlled by adjusting the duty ratio d_1. In the first switching period, the calculated d_1 is set for the driving signals of the power switches S_2 and S_4 and duty ratio 0.5 minus the dead time is set for the driving signals of the power switches S_1 and S_3 in the first switching period; contrarily the calculated d_1 is set for the driving signals of the power switches S_1 and S_3 and duty ratio 0.5 minus the dead time is set for the driving signals of the power switches S_2 and S_4 in the second switching period. The duty ratio d_1 calculated by the control loop would be changed in every two switching periods to adjust the output voltage V_o in the steady operations.

Fig. 3 shows the equivalent circuits to explain the operation principle of the proposed PSM strategy presented in Fig. 2.

Stage 1 [before t_2] Before t_2, the circuit works at a free-wheeling mode with the primary current i_p flowing through L_r, S_2, C_2, D_4, C_b, and T_r as shown in Fig. 3(a). During this stage, the primary current i_p is kept at $-i_o/n$. The currents on (S_1, D_1) and (S_3, D_3), which are i_1 and i_3, are both 0 A.

Stage 2 [t_2 - t_3] At t_2, the switch S_2 is turned off. Then, the capacitor C_{s2} starts to charge, and the capacitor C_{s1} begins to discharge. This stage would finish until that the voltage on C_{s2} increases to $V_{in}/2$ and the voltage on C_{s1} decreases to 0 V. In addition, the primary current i_p begins to increase, and there is no enough primary power to provide the output power, so the four output rectifier diodes D_{r1} - D_{r4} conduct simultaneously.

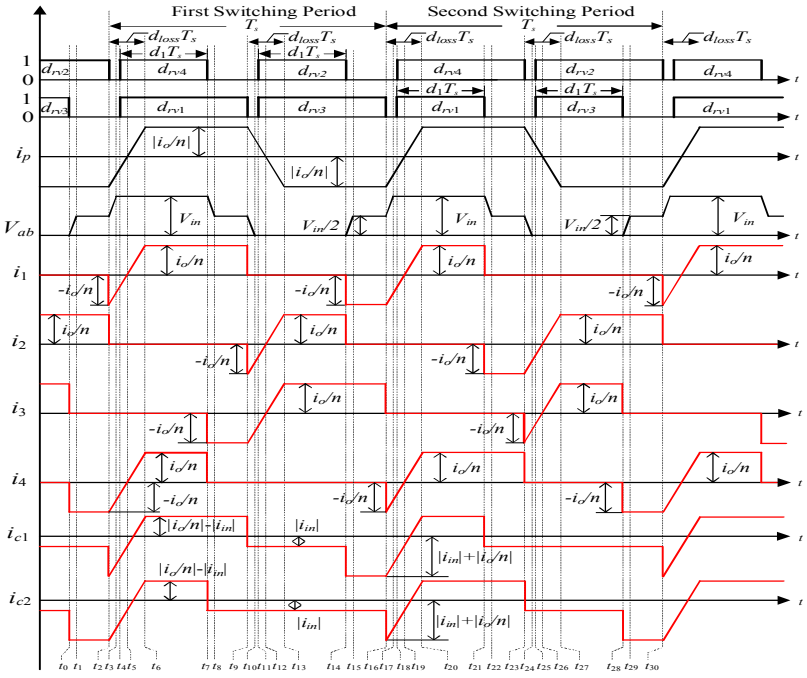


Fig. 2. Proposed periodically swapping modulation (PSM) strategy with main operation waveforms.

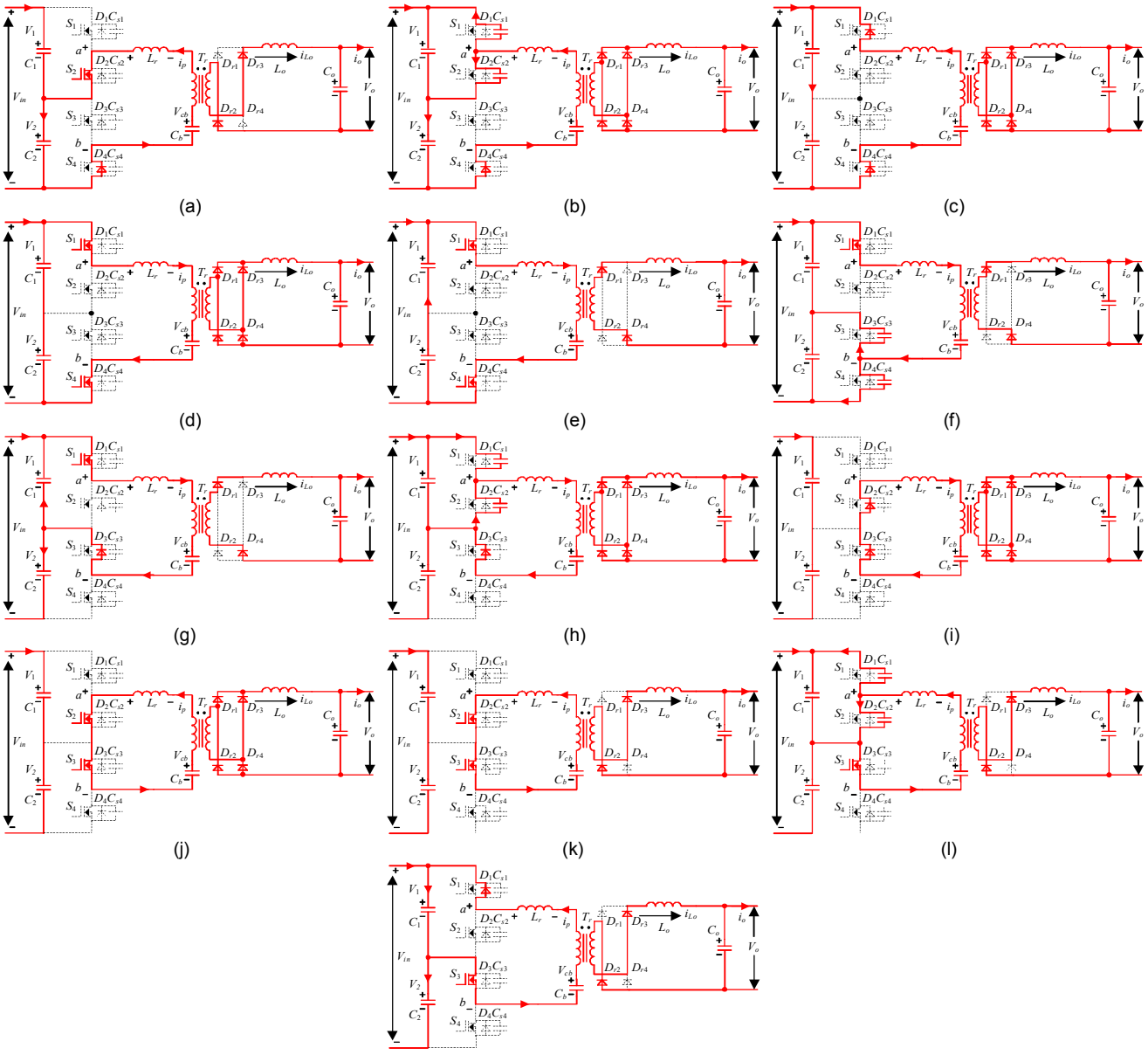


Fig. 3. Equivalent circuits in the first switching period. (a) [before t2]. (b) [t2 - t3]. (c) [t3 - t5]. (d) [t5 - t6]. (e) [t6 - t7]. (f) [t7 - t8]. (g) [t8 - t9]. (h) [t9 - t10]. (i) [t10 - t12]. (j) [t12 - t13]. (k) [t13 - t14]. (l) [t14 - t15]. (m) [t15 - t16].

Stage 3 [t_3 - t_5] At t_3, the voltage on C_{s1} decreases to 0 V, then the diode D_1 begins to conduct. Therefore, the switches S_1 and S_4 can be turned on at zero-voltage at the time t_4. The primary current i_p would flow through L_r, D_1, C_1, C_2, D_4, C_b, and T_r.

Stage 4 [t_5 - t_6] At t_5, the primary current i_p increases to 0 A, then the direction of i_p begins to change. During this stage, the primary current i_p would increase linearly and flow through L_r, T_r, C_b, S_4, C_1, C_2, and S_1 as shown in Fig. 3(d).

Stage 5 [t_6 - t_7] At t_6, the primary current i_p increases to i_o/n, then D_{r2} and D_{r3} turn off and the input power begins to be transferred to the output through T_r, D_{r1}, and D_{r4}. During this stage, the primary current i_p would be kept at i_o/n; the currents i_1 and i_4 are both i_o/n; and the currents i_2 and i_3 are both 0 A.

Stage 6 [t_7 - t_8] At t_7, the switch S_4 is turned off. The capacitor C_{s4} starts to charge, and the capacitor C_{s3} begins to discharge. This stage would finish until the voltage on C_{s4} increases to V_{in}/2 and the voltage on C_{s3} decreases to 0 V.

Stage 7 [t_8 - t_9] At t_8, the voltage on C_{s3} decreases to 0 V, then the diode D_3 begins to conduct. During this stage, the circuit operates at a free-wheeling mode with the primary current i_p flowing through L_r, T_r, C_b, D_3, C_1, and S_1 as shown in Fig. 3(g).

Stage 8 [t_9 - t_{10}] At t_9, the switch S_1 is turned off. Then, the capacitor C_{s1} starts to charge, and the capacitor C_{s2} begins to discharge. This stage would finish until that the voltage on C_{s1} increases to V_{in}/2 and the voltage on C_{s2} decreases to 0 V. The primary current i_p starts to decrease, and there is no enough primary power to provide the output power, so the four output rectifier diodes D_{r1} - D_{r4} conduct simultaneously.

Stage 9 [t_{10} - t_{12}] At t_{10}, the voltage on C_{s2} decreases to 0 V, then the diode D_2 begins to conduct. Therefore, the switches S_2 and S_3 are turned on at zero-voltage at t_{11}. The primary current i_p flows through L_r, T_r, C_b, D_3, and D_2 as shown in Fig. 3(i).

Stage 10 [t_{12} - t_{13}] At t_{12}, the primary current i_p decreases to 0 A, then the direction of primary current i_p begins to change. During this stage, the primary current i_p would decrease linearly and flow through L_r, S_2, S_3, C_b, and T_r.

Stage 11 [t_{13} - t_{14}] At t_{13}, the primary current i_p decreases to -i_o/n, then D_{r1} and D_{r4} turn off and the power from C_b is transferred to the output through T_r, D_{r2}, and D_{r3}. During this stage, the primary current i_p would be kept at -i_o/n; the currents i_2 and i_3 are both i_o/n; and the currents i_1 and i_4 are both 0 A.

Stage 12 [t_{14} - t_{15}] At t_{14}, the switch S_2 is turned off. Then, the capacitor C_{s2} starts to charge, and the capacitor C_{s1} begins to discharge. This stage would finish until that the voltage on C_{s2} increases to V_{in}/2 and the voltage on C_{s1} decreases to 0 V.

Stage 13 [t_{15} - t_{16}] At t_{15}, the voltage on C_{s1} decreases to 0 V, then the diode D_1 begins to conduct. During this stage, the circuit operates at a free-wheeling mode with the primary current i_p flowing through L_r, D_1, C_1, S_3, C_b, and T_r as shown in Fig. 3(m).

At t_{16}, the switch S_3 is turned off, then the second switching period [t_{16} - t_{30}] starts. The following work operations are similar to the fist switching period, which is not repeated here.

IV. Characteristic Analysis of Proposed Modulation Strategy

In the proposed PSM strategy shown in Fig. 2, the driving signals of the power switches in the first switching period and driving signals of the power switches in the second switching period can be regarded as two separate modulation modes named mode I and II. These two modes can be used independently to control the converter, which both have the same characteristics and performances including duty cycle loss, output voltage characteristic, primary voltage, and primary current as that under the conventional modulation strategy. The main difference between these two modes is the power switches' currents i_1 - i_4, so the PSM strategy is proposed to balance the currents i_1 - i_4 by swapping these two modes.

A. Duty Cycle Loss

In Fig. 2, [t_2 - t_6], [t_9 - t_{13}], [t_{16} - t_{20}] and [t_{23} - t_{27}] are the time periods of the duty cycle losses in the two switching periods, which can be calculated by

$$t_6 - t_2 = t_{13} - t_9 = t_{20} - t_{16} = t_{27} - t_{23} = \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in}} \tag{5}$$

According to (5), the duty cycle loss d_{loss} in one switching period as shown in Fig. 2 can be obtained by

$$d_{loss} = \frac{t_6 - t_2}{T_s} = \frac{t_{13} - t_9}{T_s} = \frac{t_{20} - t_{16}}{T_s} = \frac{t_{27} - t_{23}}{T_s} = \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s} \tag{6}$$

B. Output Characteristic

Considering the duty cycle loss, the average output voltage V_o can be calculated by

$$V_o = \frac{V_{in}}{n} \cdot (d_1 - d_{loss}) = \frac{V_{in}}{n} \cdot (d_1 - \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s}) \tag{7}$$

According to (7), the duty ratio d_1 can be given by

$$d_1 = \frac{V_o \cdot n}{V_{in}} + \frac{4 \cdot L_r \cdot i_o}{n \cdot V_{in} \cdot T_s} \tag{8}$$

C. Currents through Primary Power Switches

From Fig. 2, it can be seen that the currents i_1, i_2, i_3, and i_4 are the same in every two switching periods. Therefore, only the expression of the current i_1 in two switching periods is given as (9). According to (9), the RMS values of the currents i_1, i_2, i_3, and i_4 under the proposed PSM strategy namely $i_{1\_rms\_p}$, $i_{2\_rms\_p}$, $i_{3\_rms\_p}$, and $i_{4\_rms\_p}$ can be calculated by (10).

$$i_1 = \begin{cases} -\frac{i_o}{n} + \frac{V_{in}}{2 \cdot L_r} \cdot t & [t_2 - t_6] \\ \frac{i_o}{n} & [t_6 - t_9] \\ -\frac{i_o}{n} & [t_{14} - t_{16}] \\ -\frac{i_o}{n} + \frac{V_{in}}{2 \cdot L_r} \cdot t & [t_{16} - t_{20}] \\ \frac{i_o}{n} & [t_{20} - t_{21}] \end{cases} \tag{9}$$

$$i_{1\_rms\_p} = i_{2\_rms\_p} = i_{3\_rms\_p} = i_{4\_rms\_p} = \sqrt{\frac{i_o^2}{2 \cdot n^2} - \frac{8 \cdot L_r \cdot i_o^3}{3 \cdot n^3 \cdot V_{in} \cdot T_s}} \tag{10}$$

Normally, there are mainly two types of widely used power switches in the industrial applications, which are MOSFET and IGBT for the low power and high power applications respectively. The theoretical waveforms of the currents i_1, i_2, i_3, and i_4 under the conventional and proposed modulation strategy shown in Fig. 1(b) and Fig. 2 would be the same whether MOSFET or IGBT is used. However, there is one major difference between MOSFET and IGBT that: when the current flow from source to drain and there is a driving voltage, the current would flow through the MOSFET itself instead of the body diode, which have been widely applied in the synchronous rectification; but IGBT do not have this characteristic. Take Fig. 1(b) as an instance, during the time period [t_1 - t_2], the primary current i_p would flow through S_4 instead of the body diode D_4 because there is the driving voltage on S_4 if MOSFET is used for S_4; contrarily the primary current i_p could only flow through the body diode (or paralleled diode) D_4 during the time period [t_1 - t_2] even there is the driving voltage on S_4 if IGBT is used for S_4. In addition, the RMS and average value of the currents on the power switches S_1, S_2, S_3, S_4 and average values of the currents on the body diodes (or paralleled diodes) D_1, D_2, D_3, D_4 are imbalanced under the conventional modulation strategy but balanced under the proposed modulation strategy, and they are different between using MOSFET and IGBT, whose related calculation equations are listed in Tables III and IV in the Appendix.

D. Currents and Voltages on Two Input Capacitors

In order to simplify the following analysis, one assumption is made that the input current i_{in} is constant due to the effect

from the output inductance of the input power supplier and inductance of the input line. According to Fig. 2, if neglecting the duty cycle loss, the RMS values of the currents through the two input capacitors under the proposed modulation strategy namely $i_{c1\_rms\_p}$ and $i_{c2\_rms\_p}$ can be obtained by

$$i_{c1\_rms\_p} = i_{c2\_rms\_p} = \sqrt{i_{in}^2 + \frac{i_o^2}{2 \cdot n^2} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n}} \quad (11)$$

According to Fig. 1(b), the RMS values of the currents through the two input capacitors under the conventional modulation strategy namely $i_{c1\_rms\_c}$ and $i_{c2\_rms\_c}$ can be obtained by (12) and (13) if neglecting the duty cycle loss.

$$i_{c1\_rms\_c} = \sqrt{i_{in}^2 + \frac{i_o^2 \cdot d_1}{n^2} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n}} \quad (12)$$

$$i_{c2\_rms\_c} = \sqrt{i_{in}^2 + \frac{i_o^2 \cdot d_2}{n^2} - \frac{2 \cdot i_{in} \cdot i_o \cdot d_1}{n}} \quad (13)$$

From (11) - (13), it can observed that the currents on the two input capacitor are difference because d_1 and d_2 are different under the conventional asymmetrical modulation strategy, but the currents on the two input capacitors would be balanced under the proposed PSM strategy.

If the driving signals of the primary power switches in second switching period (modulation mode II) shown in Fig. 2 is used independently to control the converter, the currents on the power devices (i_1 - i_4) and two input capacitors (i_{c1}, i_{c2}), and the ripple voltages on the two input capacitors (V_1, V_2) would be the same as that under the conventional asymmetrical modulation strategy. Therefore, the maximum voltage ripples on the two input capacitor (V_1, V_2) in the steady operations are the same under the conventional and proposed modulation strategy because the proposed PSM strategy operates by swapping the modulation mode I (first switching period) and II (second switching period).

E. ZVS Achievement Conditions

Before discussing the conditions of the ZVS achievement, one assumption is made that the four power switches S_1 - S_4 have the same parasitic capacitors namely C_s.

$$C_{s1} = C_{s2} = C_{s3} = C_{s4} = C_s \quad (14)$$

In the first switching period, in order to ensure S_3 or S_4 realizing zero-voltage switch-on, the energy E_1 is needed to fully discharge the parasitic capacitor of the in-coming switch and charge the parasitic capacitor of the out-going switch, whose expression can be given by (15). The energy to achieve zero-voltage switch-on for S_3 and S_4 is provided by both the output filter inductance and leakage inductance of the transformer. Normally, the output filter inductance is large enough to realize the zero-voltage switch-on for S_3 and S_4 even at light load.

$$E_1 = \frac{1}{2} \cdot C_{s3} \cdot (\frac{V_{in}}{2})^2 + \frac{1}{2} \cdot C_{s4} \cdot (\frac{V_{in}}{2})^2 = \frac{1}{4} \cdot C_s \cdot V_{in}^2 \quad (15)$$

The energy E_2 from the leakage inductance of the transformer is used to achieve zero-voltage switch-on of switches S_1 and S_2. In order to achieve the zero-voltage switch-on of S_1 or S_2, the energy E_2 should satisfy the requirement (16) to fully discharge the parasitic capacitor of the in-coming switch and charge the parasitic capacitor of the out-going switch. The switches S_1 and S_2 are more difficult to achieve zero-voltage switch-on than the switches S_3 and S_4 since the leakage inductance L_r is quite smaller than the reflected output filter inductance.

$$E_2 = \frac{1}{2} \cdot L_r \cdot \left(\frac{i_o}{n}\right)^2 \geq \frac{1}{2} \cdot C_{s1} \cdot (\frac{V_{in}}{2})^2 + \frac{1}{2} \cdot C_{s2} \cdot (\frac{V_{in}}{2})^2 = \frac{1}{4} \cdot C_s \cdot V_{in}^2 \quad (16)$$

In the second switching period, the energy from both the output filter inductance and leakage inductance of the transformer is provided for the switches S_1 and S_2 to realize the zero-voltage switch-on, and the energy from the leakage inductance of the transformer is provided for the switches S_3 and S_4 to achieve the zero-voltage switch-on, which is just contrary to that in the first switching period. The requirements to achieve ZVS in the second switching period is similar to that in the first switching period, which is not repeated here.

F. Duty Cycle Limitation and Dead time Design

In the proposed PSM strategy, the duty ratio d_1 shown in Fig. 2 should be smaller than 0.5 minus dead time to avoid the short connection of C_1 and C_2 via conducting the switch pairs (S_1, S_2) and (S_3, S_4) simultaneously. In addition, The dead time T_{dead} of the switch pairs (S_1, S_2) and (S_3, S_4) must be also set in the real applications to avoid the short connection of C_1 and C_2 via conducting the switch pairs (S_1, S_2) and (S_3, S_4) simultaneously, whose value can be calculated by (17) if neglecting the parasitic capacitor of the transformer [27].

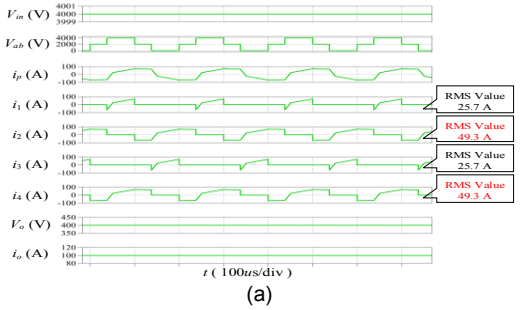
$$T_{dead} \geq \frac{\pi}{2} \cdot \sqrt{2 \cdot L_r \cdot C_{o(tr)}} \quad (17)$$

in which $C_{o(tr)}$ is the effective output capacitance of the switch.

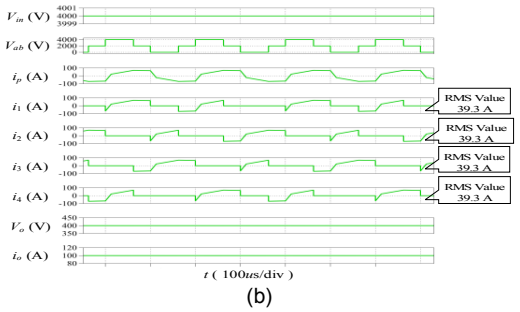
V. Simulation and Experimental Verification

A. Simulation Verification

A simulation model is built in PLECS to verify the proposed PSM strategy, whose circuit parameters are listed in Appendix. In the simulation, the input voltage V_{in} is 4 kV, the output voltage V_o is 400 V, and the output current i_o is 100 A.



(a)



(b)

Fig. 4. Simulation results (V_{in} = 4 kV, V_o = 400 V, and i_o = 100 A). (a) Conventional asymmetrical modulation strategy. (b) Proposed modulation strategy.

Fig. 4 shows the simulation results under the conventional and proposed modulation strategy, respectively. The RMS values of the currents i_1 and i_3 are 25.7 A, and the RMS values of the currents i_2 and i_4 are 49.3 A under the conventional modulation strategy as shown in Fig. 4(a). However, the RMS values of i_1, i_2, i_3, and i_4 are all 39.3 A under the proposed modulation strategy as shown in Fig. 4(b).

B. Experimental Verification

In order to verify the proposed PSM strategy, a 1 kW experimental prototype is established, which is controlled by dSPACE and whose circuit parameters are listed in the Appendix. Fig. 5 shows the hardware of the established experimental prototype. In the following experimental tests, a single proportional-integral (PI) control loop is used to control the output voltage V_o by adjusting the duty ratio d_1 shown in Fig. 2.

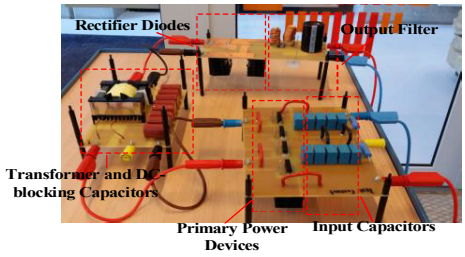


Fig. 5. Hardware of 1 kW established experimental prototype.

Fig. 6 presents the control block, in which V_{ref} is the reference value of the output voltage V_o. Fig. 7 shows the experimental results including V_{ab}, V_o, i_o, and i_p when the output power P_o is 1 kW, the input voltage V_{in} is 550 V, and the output voltage V_o is 50 V. From Fig. 7, it can be observed that primary voltage V_{ab} and primary current i_p are almost the same under the conventional and proposed modulation strategy.

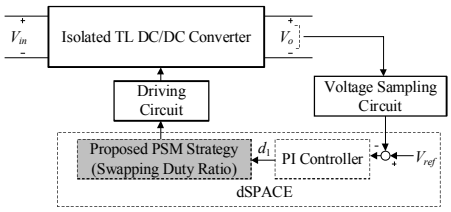
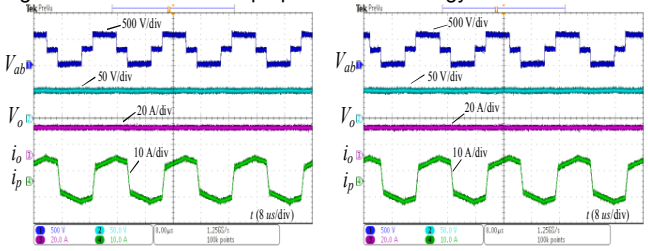


Fig. 6. Control block of the proposed PSM strategy.

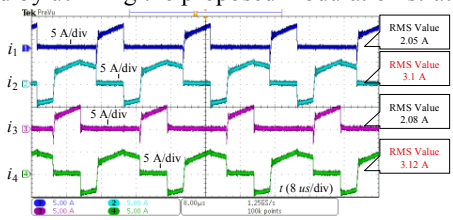


(a) (b)

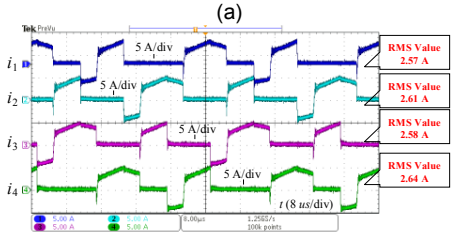
Fig. 7. Experimental results including V_{ab}, V_o, i_o, and i_p (V_{in} = 550 V, V_o = 50 V, and P_o = 1 kW). (a) Conventional asymmetrical modulation strategy. (b) Proposed modulation strategy.

Figs. 8 and 9 show the experimental results about the currents i_1, i_2, i_3, and i_4 under the conventional and proposed modulation strategy. When using the conventional modulation strategy, the RMS values of i_1, i_2, i_3, and i_4 are 2.05 A, 3.10 A, 2.08 A, and 3.12 A under 500 W and 3.86 A, 5.63 A, 3.79 A, and 5.59 A under 1 kW as shown in Figs. 8(a) and 9(a). By utilizing the proposed modulation strategy, the currents flowing through the four power switches are kept balanced in every two switching periods as shown in Figs. 8(b) and 9(b), whose RMS values are 2.57 A, 2.61 A, 2.58 A, and 2.64 A under 500 W and 4.75 A, 4.76 A, 4.68 A, and 4.73 A under 1 kW.

Fig. 10 shows the experimentally measured RMS values of i_1, i_2, i_3, and i_4 under various input voltages when the output voltage V_o is 50 V and output power P_o is 1 kW. From Fig. 10, it can be seen that 1) the RMS values of i_1, i_2, i_3, and i_4 are imbalanced under the conventional asymmetrical modulation strategy; 2) with the input voltage increasing, the RMS values of i_1, i_3 decrease and the RMS values of i_2, i_4 increase. Therefore, the current imbalance between the RMS values of (i_1, i_3), and (i_2, i_4) would become larger under the conventional asymmetrical modulation strategy, and the biggest difference reaches 1.84 A when the input voltage increases to 550 V; 3) under the proposed PSM strategy, the RMS values of i_1, i_2, i_3, and i_4 have a slight increasing along with the input voltage increasing and range between the RMS values of (i_1, i_3), and (i_2, i_4) under the conventional asymmetrical modulation strategy; and 4) the experimental results about the currents i_1 - i_4 are consistent with the above theoretical analysis. Based on the experimental results shown in Fig. 10, it can be concluded that the current imbalance among the power switches caused by the conventional asymmetrical modulation strategy can be eliminated by utilizing the proposed modulation strategy.

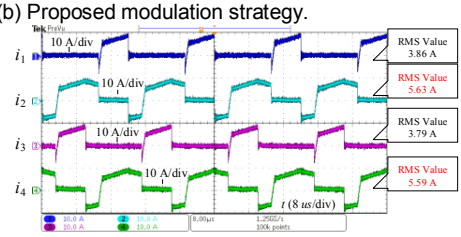


(a)

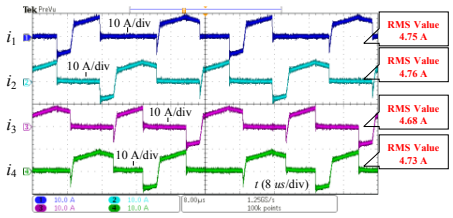


(b)

Fig. 8. Experimental results about currents i_1, i_2, i_3, and i_4 (V_{in} = 550 V, V_o = 50 V, and P_o = 500 W). (a) Conventional asymmetrical modulation strategy. (b) Proposed modulation strategy.



(a)



(b)

Fig. 9. Experimental results currents i_1, i_2, i_3, and i_4 (V_{in} = 550 V, V_o = 50 V, and P_o = 1 kW). (a) Conventional asymmetrical modulation strategy. (b) Proposed modulation strategy.

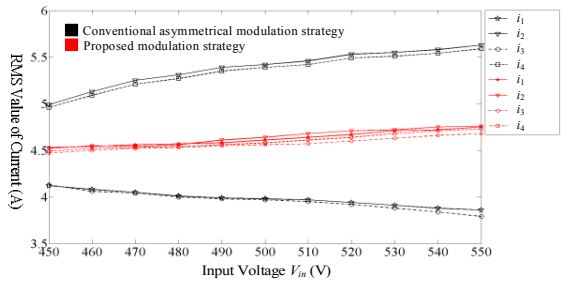
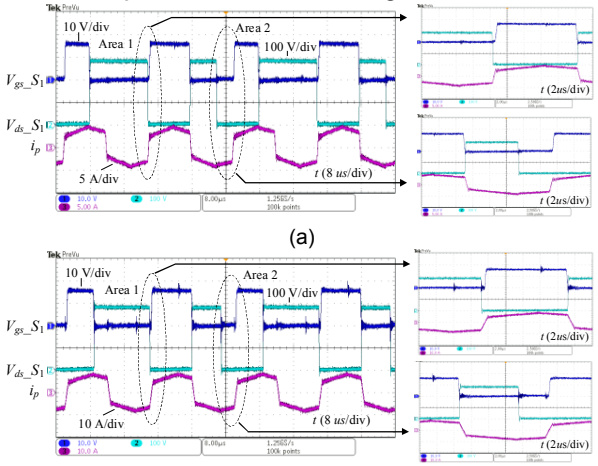


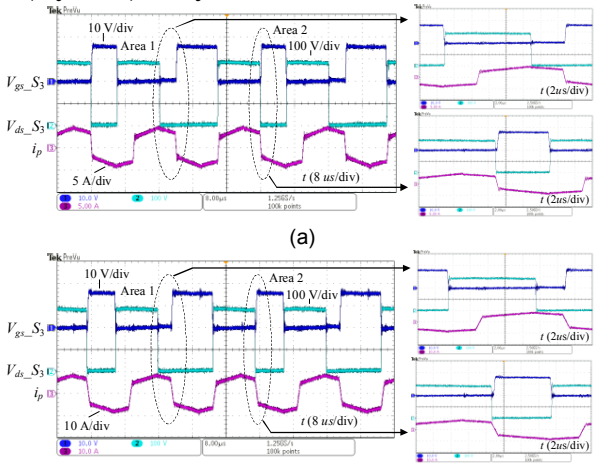
Fig. 10. Experimentally measured RMS values of i_1, i_2, i_3, and i_4 under various input voltages (P_o = 1 kW).

Figs. 11 and 12 show the ZVS achievement conditions under the proposed modulation strategy. Fig. 11 shows the primary current i_p, driving signal $V_{gs}\_S_1$, and drain-source voltage $V_{ds}\_S_1$ of the power switch S_1 under 500 W and 1 kW, which illustrates that S_1 realizes ZVS and its voltage stress is about half of the input voltage. In Fig. 11, the energy from the leakage inductance of the transformer is provided for S_1 to achieve the zero-voltage switch-on at Area 1, the energy from both the output filter inductance and leakage inductance of the transformer is provided for S_1 to realize the zero-voltage switch-on at Area 2. Fig. 12 shows the primary current i_p, driving signal $V_{gs}\_S_3$, and drain-source voltage $V_{ds}\_S_3$ of the power switch S_3 under 500 W and 1 kW, which demonstrates that S_3 realizes ZVS and its voltage stress is about half of the input voltage. In Fig. 12, the energy from both the output filter inductance and leakage inductance of the transformer is provided for S_3 to achieve the zero-voltage switch-on at Area 1, the energy from the leakage inductance of the transformer is provided for S_3 to realize the zero-voltage switch-on at Area 2.



(a) (b)

Fig. 11. Driving signal and drain-source voltage of switch S_1, and primary current i_p. (a) V_{in} = 550 V, V_o = 50 V, and P_o = 500 W. (b) V_{in} = 550 V, V_o = 50 V, and P_o = 1 kW.



(a) (b)

Fig. 12. Driving signal and drain-source voltage of switch S_3, and primary current i_p. (a) V_{in} = 550 V, V_o = 50 V, and P_o = 500 W. (b) V_{in} = 550 V, V_o = 50 V, and P_o = 1 kW.

Figs. 13 and 14 show the dynamic performances, in which the output power changs from 1 kW to 500 W and finally gets back to 1 kW when the input voltage V_{in} is 550 V and output voltage V_o is 50 V. From Fig. 13, it can be seen that the voltages on the two input capacitors V_1, V_2 and the voltage on the DC-blocking capacitor V_{cb} are all constant under the proposed PSM strategy when the load changes. From Fig 14, it can be observed that the dynamic responses of V_o (only including AC component) are almost the same with the load changes under the conventional and proposed modulation strategy when using the same PI control loop.

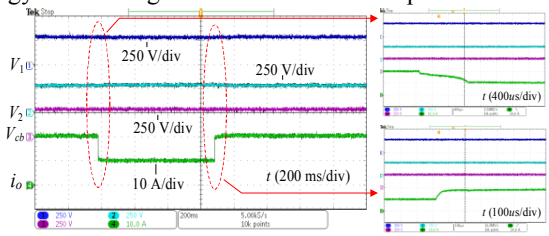
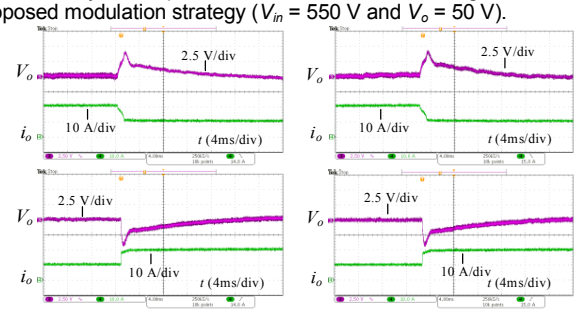


Fig. 13. Dynamic performances under load changes when using proposed modulation strategy (V_{in} = 550 V and V_o = 50 V).

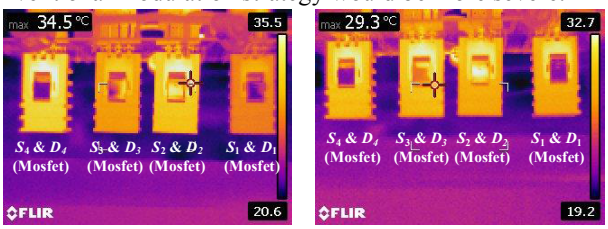


(a) (b)

Fig. 14. Dynamic performances under load changes including V_o and i_o (V_{in} = 550 V and V_o = 50 V). (a) Conventional asymmetrical modulation strategy. (b) Proposed modulation strategy.

Figs. 15 (a) and 15(b) show the experimental comparison results about the thermal stresses on the primary power switches between the conventional and proposed modulation strategy in the established experimental prototype. From Fig.

14, it can be observed obviously that 1) the temperatures on the (S_2, D_2) and (S_4, D_4) are higher than that on the (S_1, D_1) and (S_3, D_3) under the conventional modulation strategy; 2) the temperature on the (S_1, D_1), (S_2, D_2), (S_3, D_3), and (S_4, D_4) are almost the same under the proposed PSM strategy; and 3) the maximum temperature on the primary power switches is 34.5 C under the conventional modulation strategy, but the maximum temperature on the primary power switches can be reduced to 29.3 C by utilizing the proposed PSM strategy. In addition, with the output power increasing, the thermal stress imbalance among the primary power devices under the conventional modulation strategy would be more severe.



(a) (b)

Fig. 15. Experimental comparison results about thermal stresses on the primary power switches (V_{in} = 550 V, V_o = 50 V, and P_o = 1 kW). (a) Conventional asymmetrical modulation strategy. (b) Proposed modulation strategy.

The experimentally measured efficiency curves with various input voltages (450 V, 500 V, and 550 V) are shown in Fig. 16 when the output voltage V_o is 50 V. The peak efficiency under the proposed modulation strategy is over 95%. From Fig. 16, it can be observed that the efficiencies under the proposed modulation strategy are slightly lower than that under the conventional modulation strategy, whose reason is that MOSFET is used for the primary power switches in the established experimental prototype. When using MOSFET, the primary current i_p flows through the body diodes of the power switches instead of the power switches during the free-wheeling time periods under the proposed modulation strategy, which would increase the conduction losses in comparison with the conventional modulation strategy.

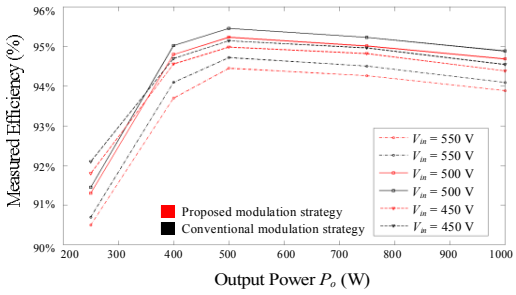


Fig. 16. Efficiency curves with various input voltages (V_o = 50 V).

According to the circuit parameters of the established experimental prototype and calculation equations (Table IV) in the Appendix, the calculated conduction power losses of the primary power switches are shown in Fig. 17. In Fig. 17, the total conduction power losses of the primary switches under the proposed PSM strategy are 8.44 W, which is slightly higher than that under the conventional modulation strategy (7.67 W) because MOSFET is used for the primary power switches in the established experimental prototype. If IGBT is used for the power switches when applied in the high voltage and high power applications, the total conduction power losses of the primary power switches and the efficiencies of the converter under the conventional and proposed modulation strategy would be almost the same.

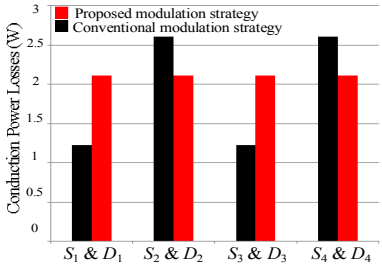


Fig. 17. Calculated conduction power losses of primary power switches (V_{in} = 550 V, V_o = 50 V, and P_o = 1 kW). Note: in the calculation, the turn-on resistor of MOSFET $R_{ds\_on\_Mos}$ is 100 mΩ, the voltage drop on the body diode V_f is 1 V according to the datasheet of SPW47N60C3.

VI. Conclusion

In this paper, a novel periodically swapping modulation strategy (PSM) is proposed for various types of TL DC/DC converters to balance the power switches' currents. The current imbalance issue of the power switches under the conventional asymmetrical modulation strategy is analyzed in detail. After utilizing the proposed modulation strategy, the currents flowing through the power switches can be effectively kept balanced by swapping the driving signals of the switch pairs periodically. Therefore, the proposed modulation strategy can improve the converter's reliability in the aspects of balancing the power losses and thermal stresses among the power switches. Finally, the simulation and experimental results verify the effectiveness and feasibility of the proposed modulation strategy.

Appendix

TABLE I PARAMETERS OF SIMULATION MODEL

Description	Parameter
Turns Ratio of Transformer T_r	15 : 7
Leakage Inductance L_r (uH)	300
Output Filter Capacitor C_o (uF)	4700
Output Filter Inductor L_o (uH)	1500
Input Capacitors C_1 and C_2 (uF)	4700
DC-blocking Capacitor C_b (uF)	100
Switching Frequency (kHz)	5
Dead Time (us)	1

TABLE II PARAMETERS OF EXPERIMENTAL PROTOTYPE

Description	Parameter
Power Switches S_1 - S_4	SPW47N60C3
Rectifier Diodes D_{r1} - D_{r4}	MBR40250TG
Turns Ratio of Transformer T_r	25 : 8
Leakage Inductance L_r of T_r (uH)	20.7
Output Filter Capacitor C_o (uF)	470
Output Filter Inductor L_o (uH)	140
Input Capacitors C_1 and C_2 (uF)	11
DC-blocking Capacitor C_b (uF)	12
Switching Frequency (kHz)	50
Dead Time (ns)	400

According to Fig. 1(b) and Fig. 2, the average values of the currents on S_1, S_2, S_3, S_4 (or RMS values of the currents on S_1, S_2, S_3, S_4) and average values of the currents on D_1, D_2, D_3, D_4

are shown in Tables III and IV when using IGBT and MOSFET respectively if neglecting the effect of the parasitic capacitors and dead time.

TABLE III THEORETICAL CACULATION EQUATIONS ABOUT AVERAGE VALUES OF CURRENTS ON S_1 - S_4 AND D_1 - D_4 (USING IGBT)

IGBT	Conventional modulation strategy	Proposed modulation strategy
Average current of S_1 and S_3 $i_{S1\&S3\_avg\_IGBT}$	$\frac{i_o}{n}\cdot d_1-\frac{3\cdot L_r\cdot i_o^2}{n^2\cdot V_{in}\cdot T_s}$	$\frac{i_o}{2\cdot n}\cdot(0.5+d_1)-\frac{3\cdot L_r\cdot i_o^2}{n^2\cdot V_{in}\cdot T_s}$
Average current of S_2 and S_4 $i_{S2\&S4\_avg\_IGBT}$	$\frac{i_o}{2\cdot n}-\frac{3\cdot L_r\cdot i_o^2}{n^2\cdot V_{in}\cdot T_s}$	
Average current of D_1 and D_3 $i_{D1\&D3\_avg\_IGBT}$	$\frac{L_r\cdot i_o^2}{n^2\cdot V_{in}\cdot T_s}$	$\frac{i_o}{2\cdot n}\cdot(0.5-d_1)+\frac{L_r\cdot i_o^2}{n^2\cdot V_{in}\cdot T_s}$
Average current of D_2 and D_4 $i_{D2\&D4\_avg\_IGBT}$	$\frac{i_o}{2\cdot n}\cdot(d_2-d_1)+\frac{L_r\cdot i_o^2}{n^2\cdot V_{in}\cdot T_s}$	

TABLE IV THEORETICAL CACULATION EQUATIONS ABOUT RMS VALUES OF CURRENTS ON S_1 - S_4 AND AVERAGE VALUES OF CURRENTS ON D_1 - D_4 (USING MOSFET)

MOSFET	Conventional modulation strategy	Proposed modulation strategy
RMS current of S_1 and S_3 $i_{S1\&S3\_rms\_Mos}$	$\sqrt{\frac{i_o^2}{n^2}\cdot d_1-\frac{8\cdot L_r\cdot i_o^3}{3\cdot n^3\cdot V_{in}\cdot T_s}}$	$\sqrt{\frac{i_o^2}{2\cdot n^2}\cdot(0.5+d_1)-\frac{8\cdot L_r\cdot i_o^3}{3\cdot n^3\cdot V_{in}\cdot T_s}}$
RMS current of S_2 and S_4 $i_{S2\&S4\_rms\_Mos}$	$\sqrt{\frac{i_o^2}{n^2}\cdot d_2-\frac{8\cdot L_r\cdot i_o^3}{3\cdot n^3\cdot V_{in}\cdot T_s}}$	
Average current of D_1 and D_3 $i_{D1\&D3\_avg\_Mos}$	0	$\frac{i_o}{2\cdot n}\cdot(0.5-d_1)$
Average current of D_2 and D_4 $i_{D2\&D4\_avg\_Mos}$	0	
Conduction power losses	$R_{ds\_on\_Mos}\cdot(2\cdot i_{S1\&S3\_rms\_Mos}+2\cdot i_{S2\&S4\_rms\_Mos})+V_f\cdot(2\cdot i_{D1\&D3\_avg\_Mos}+2\cdot i_{D2\&D4\_avg\_Mos})$	

Note: $R_{ds\_on\_Mos}$ is the turn-on resistor of MOSFET, and V_f is the voltage drop on the body diode.

REFERENCES

[1] M. Saeedifard, M. Graovac, R. F. Dias, and R. Iravani, "DC power systems: challenges and opportunities," in *Proc. IEEE Power Energy Soc. Gen. Meet*., 2010, pp. 1-7.

[2] Y. Chen, M. Haj-ahmed, and M. S. Illindala, "An MVDC microgrid for a remote area mine site: Protection, operation and control," in *Proc. IEEE IAS Annu. Meet*., Oct. 2014, pp. 1-9.

[3] X. Ruan, B. Li, Q. Chen, S. C. Tan, and C.K. Tse, "Fundamental considerations of three-level dc-dc converters: Topologies, analyses, and control," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 11, pp. 3733-3743, Dec. 2008.

[4] K. Jin and X. Ruan, "Hybrid full-bridge three-level LLC resonant converter-a novel DC-DC converter suitable for fuel-cell power system," *IEEE Trans. Ind. Electron*., vol. 53, no. 5, pp. 1492-1503, 2006.

[5] P. J. Grbovic, P. Delarue, P. Le Moigne, and P. Bartholomeus, "A bi-´ directional three-level DC-DC converter for the ultra-capacitor applications," *IEEE Trans. Ind. Electron*., vol. 57, no. 10, pp. 3415-3430, Oct. 2010.

[6] J. R. Pinheiro and I. Barbi, "The three-level ZVS PWM converter-A new concept in high-voltage DC-to-DC conversion," in *Proc. IEEE Int. Conf. Ind. Electron. Control Instrum. Autom*., 1992, pp. 173-178.

[7] F. Canales, P. Barbosa, M. Burdio, and F. Lee, "A zero-voltage switching three-level DC/DC converter," in *Proc. 22nd Int. Telecommun. Energy Conf*., 2000, pp. 512-517.

[8] F. Canales, P. Barbosa, and F. C. Lee, "A zero-voltage and zero-current switching three-level DC/DC converter," *IEEE Trans. Power Electron*., vol. 17, no. 6, pp. 898-904, Nov. 2002.

[9] X. Ruan, Z. Chen, and W. Chen, "Zero-voltage-switching PWM hybrid full-bridge three-level converter," *IEEE Trans. Power Electron*., vol. 20, no. 2, pp. 395-404, Mar. 2005.

[10] B. R. Lin and C. H. Liu, "ZVS DC/DC converter based on two three-level PWM circuits sharing the same power switches," *IEEE Trans. Ind. Electron*., vol. 60, no. 10, pp. 4191-4200, Oct. 2013.

[11] F. Liu, J. Yan, and X. Ruan, "Zero-voltage and zero-current-switching PWM combined three-level DC/DC converter," *IEEE Trans. Ind. Electron*., vol. 57, no. 5, pp. 1644-1654, May 2010.

[12] Y. Shi and X. Yang, "Zero-voltage switching PWM three-level full-bridge DC-DC converter with wide ZVS load range," *IEEE Trans. Power Electron*., vol. 28, no. 10, pp. 4511-4524, Oct. 2013.

[13] J. S. Lai and F. Z. Peng, "Multilevel converters-A new breed of power converters," *IEEE Trans. Ind. Appl*., vol. 32, no. 3, pp. 509-517, May/ Jun. 1996.

[14] E. Deschamps and I. Barbi, "A flying-capacitor ZVS PWM 1.5 kW DC-to-DC converter with half of the input voltage across the switches," *IEEE Trans. Power Electron*., vol. 15, no. 5, pp. 855-860, Sep. 2000.

[15] E. Deschamps, and I. Barbi, "A comparison among three-level ZVS-PWM isolated DC-to-DC converters," in *Proc. IEEE IECON*, 1998, pp.1024-1029.

[16] I. Barbi, R. Gules, R. Redl, and N. O. Sokal, "DC/DC converter: Four switches $V_{pk} = V_{in}$ /2, capacitive turn-off snubbing, ZV turn-on," *IEEE Trans. Power Electron*., vol. 19, no. 4, pp. 918-927, Jul. 2004.

[17] Y. Shi, and X. Yang, "Wide range soft switching PWM three-level DC-DC converters suitable for industrial applications," *IEEE Trans. Power Electron*., vol. 29, no. 2, pp. 603-616, Feb. 2014.

[18] Y. Shi, and X. Yang, "Wide load range ZVS three-level dc-dc converter: four primary switches, capacitor clamped, two secondary switches, and smaller output filter volume," *IEEE Trans. Power Electron*., vol. 31, No. 5, pp. 3431-3443, May. 2016.

[19] Z. Guo, K. Sun, and D. Sha, "Improved ZVS three-level DC-DC converter with reduced circulating loss," *IEEE Trans. Power Electron*., vol. 31, no. 9, pp. 6394-6404, Dec. 2015.

[20] X. Yu, K. Jin, and Z. Liu, "Capacitor voltage control strategy for half-bridge three-level DC/DC converter," *IEEE Trans. Power Electron*., vol. 29, no. 4, pp. 1557-1561, Apr. 2014.

[21] B. Lin and S. Zhang, "Analysis and implementation of a three-level hybrid DC-DC converter with the balanced capacitor voltages," *IET Power Electron*., vol. 9, no. 3, pp. 457-465, Mar. 2016.

[22] T. Bruckner, S. Bernet, and H. Guldner, "The active NPC converter and its loss-balancing control," *IEEE Trans. Ind. Electron*., vol. 52, no. 3, pp. 855-867, Jun. 2005.

[23] H. Wang, M. Liserre, and F. Blaabjerg, "Toward reliable power electronics: Challenges, design tools, and opportunities," *IEEE Ind. Electron. Mag*., vol. 7, no. 2, pp. 17-26, Jun. 2013.

[24] P. K. Jain, A. Martin, and G. Edwards, "Asymmetrical pulse-width modulated resonant DC/DC converter topologies," *IEEE Trans. Power Electron*., vol. 11, no. 3, pp. 413-422, May 1996.

[25] B. R. Lin and C. H. Tseng, "Analysis of parallel-connected asymmetrical soft-switching converter," *IEEE Trans. Ind. Electron*., vol. 54, no. 3, pp. 1642-1653, May 2009.

[26] S. Zong, H. Luo, W. Li, Y. Deng, and X. He, "Asymmetrical duty cycle controlled LLC resonant converter with equivalent switching frequency doubler," *IEEE Trans. Power Electron*., vol. 31, no. 7, pp. 4963-4973, Jul. 2016.

[27] Sam A. Rahman, "Design of phase shifted full-bridge converter with current doubler rectifier," Infineon Technol., North America, Jan. 2013, Appl. note.