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Five-Level Active-Neutral-Point-Clamped DC/DC Converter

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***Abstract*—Multi-level converters are getting more and more attentions because of their obvious merits such as lower voltage stress and harmonic, smaller size of output filters, and so on. In this paper, a five-level active-neutral-point-clamped (5L-ANPC) dc/dc converter is proposed for power transfer in the applications of the medium voltage dc (MVDC) grids. A modulation strategy is also proposed to achieve five-level voltages generating, which can effectively reduce the high voltage change rate *dv*/*dt* and voltage stress on the transformer, thus decrease the electromagnetic interference (EMI) and increase reliability. Furthermore, a capacitor voltage control strategy by alternating two operation modes of the proposed modulation strategy is proposed to balance the voltage of the flying capacitor, which ensures multi-level voltages producing. Finally, the performance of the proposed converter and control strategy is verified by both simulation results and experimental results from a down-scaled prototype.**

Keywords—dc/dc converter; five-level active-neutral-point-clamped; medium voltage.

I. INTRODUCTION

DC-based distributions and dc-based micro-grids have been proposed as promising solutions for future smart-grid systems because of their clear merits, such as no reactive power, no frequency stability, high conversion efficiency, and easy system control [1], [2]. Furthermore, dc-based data centers and residential systems have also been increasingly developed recently [3], [4]. The performances of the dc-based systems highly depend on dc/dc converters because these converters are responsible for delivering power and changing voltage grades among dc-based systems. Accordingly, a dc/dc converter with high performance and high reliability is desired for the dc grids.

So far, a number of dc/dc converters for the dc grids have been designed in the existing literatures. Generally, they can be classified into two types, namely non-isolated converters and isolated converters. The non-isolated converters cannot achieve high voltage gain and has no galvanic isolation between the input side and output side, which makes it not fit to the dc-based applications which require wide voltage ranges and high reliability. Hence, this work focuses on the study of the isolated dc/dc converter. Normally, three types of isolated dc/dc converters can be identified which are namely two-level based converters, three-level (TL) based converters, and modular multi-level converters (MMC). Specifically, two-level based converters have the least quantity of power switches, while the power switches need to sustain a high dc bus voltage, which results in high conduction losses and high voltage change rate *dv*/dt. The high *dv*/*dt* is risky as it would cause large electromagnetic interference (EMI). MMC distinguish themselves from others due to their low switches' voltage stress, low EMI, and good power quality arising from the increasing amount of voltage levels [5]. However, MMC need more switches accompanying cost increasing, which also increases the needs for voltage sensors, complicates the circuit structure and the voltage balancing control strategy [6]. Given the above analysis, two-level based converters and MMC are more suitable for power transfer in low voltage and high voltage dc-based distributions respectively. For TL based converters, the main feature is that their switches only sustain half of the input voltage. In addition, TL based converters [7-13] perform better in the aspects of EMI, power quality and filter size in comparison with two-level based converters and have easier circuit structure and control strategy in comparison with MMC. These advantages of TL based converters make them preferable for MVDC grids [8] with several thousand volts dc bus voltage [14], [15].

Many studies on the isolated TL based converters have been conducted. For instance, a hybrid isolated FBTL dc/dc converter with a chopping phase-shift (CPS) control and an isolated FBTL dc/dc converter with a double phase-shift (DPS) control are presented in [9] and [11] respectively. These two convers both have high voltage change rate *dv*/*dt* on the primary side voltage of the transformer, which would cause large EMI and thus lead them not suitable for the high voltage applications. In [13], an improved FBTL dc/dc converter with a voltage balance control strategy is proposed to reduce the *dv*/*dt*, but a passive filter is inserted into the primary side of the transformer, which reduces voltage conversion rate and efficiency.

In this paper, a 5L-ANPC dc/dc converter with a corresponding modulation strategy is proposed for power transfer in MVDC grids. The proposed converter is suitable to be applied into the medium voltage dc-based distributions because the proposed converter has similar TL structure whose switches only sustain half of the input voltage. In addition, due

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to multi-level voltage generating, the voltage change rate dv/dt and voltage stress on the transformer can be effectively reduced, and thus both EMI and reliability can be improved. A capacitor voltage control strategy for balancing the voltage of the flying capacitor, which can ensure producing five-level voltages, is also proposed. The 5L-ANPC dc/dc converter and capacitor voltage control strategy is validated by simulation results and experimentation results from a down-scale prototype.

This paper is organized as follows. Section II introduces the circuit structure of the 5L-ANPC dc/dc converter, modulation strategy of the proposed converter, and the operational principle of the proposed modulation strategy. In section III, a capacitor voltage control strategy by alternating two operation modes of the proposed modulation strategy is proposed. Section IV presents the simulation and experimental results to verify the theoretical analysis. Finally, the main contributions of this paper are summarized in Section V.

II. PROPSED 5L-ANPC DC/DC CONVERTER

A. Circuit Structure of the Proposed Converter

Fig. 1 shows the circuit structure of the proposed 5L-ANPC dc/dc converter. In the primary side, two input capacitors C_1, C_2 are used to split the input voltage V_{in} into two voltages, V_{c1} and V_{c2}. S_1-S_8 and D_1-D_8 are power switches and power diodes of the proposed converter. C_3 is a flying capacitor. T_r is a media frequency transformer (MFT) to obtain voltage gain and galvanic isolation. In the secondary side, there are four rectifier diodes D_{r1}-D_{r4}, an output filter inductor L_o, and an output filter capacitor C_o. In Fig. 1, i_{c3} and i_{Lo} are the current flowing through the flying capacitor C_3 and output filter inductor L_o; V_{c3} is the voltage on the flying capacitor C_3; V_{out} and i_o are the output voltage and output current respectively; V_{ab} and i_p are the primary voltage and current of the transformer.

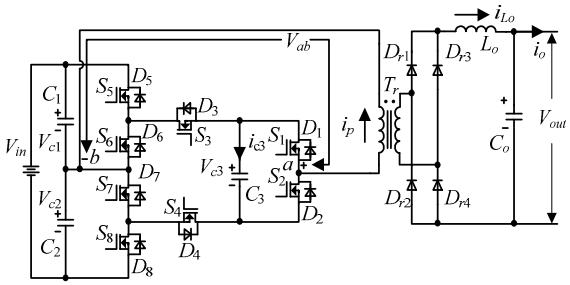


Fig. 1. Circuit structure of the proposed 5L-ANPC dc/dc converter.

B. Proposed Modulation Strategy

As shown in Fig. 2, a modulation strategy including the two operation modes is proposed to realize five-level voltages producing, in which (S_1, S_2), (S_3, S_4), (S_5, S_6), (S_7, S_8) are complementary switch pairs, D_1 and D_2 are duty ratios in one cycle, and T_s is the time of one cycle. In normal operation condition, $V_{c1} = V_{c2} = V_{in}/2$ and $V_{c3} = V_{in}/4$. The voltage stresses of S_5-S_8 and S_1-S_4 are $V_{in}/2$ and $V_{in}/4$ respectively.

- Operation mode I: Fig. 2(a) illustrates the operation mode I in one cycle. In the first half cycle, the switching function for S_1 lags behind that for S_3 by $(D_2\text{-}D_1)T_s/2$; S_5, S_7 keep on-state and S_6, S_7 keep off-state during first half cycle. In the second half cycle, the switching function for S_2 lags behind that for S_4 by $(D_2\text{-}D_1)T_s/2$; S_6, S_8 keep on-state and S_5, S_7 keep off-state during second half cycle. In the operation mode I, there are six kinds of switching states namely $V0$, $V2$, $V3$, $V4$, $V5$, and $V7$ as listed in Table I. In addition, the flying capacitor is charged in switching states $V2$ and $V5$, which in turn means the current flowing through the flying capacitor i_{c3} is positive in such two switching states as showed in Fig. 2(a).
- Operation mode II: The operation mode II is similar as the operation mode I, which is showed in Fig. 2(b). Different from the operation mode I, the switching functions for S_1 and S_3 are shifted with each other in the operation mode II, which is the same for S_2 and S_4. In the operation mode II, there are also six kinds of switching states namely $V0$, $V1$, $V3$, $V4$, $V6$, and $V7$ as listed in Table I. In addition, the flying capacitor is charged in switching states $V1$ and $V6$, which in turn means the current flowing through the flying capacitor i_{c3} is negative in such two switching states as showed in Fig. 2(b).

C. Operational Principle of Propsoed Modulation Strategy

Fig. 3 shows the equivalent circuits to explain the operational principle in the operation mode I as shown in Fig. 2(a).

Stage 1 [t_0-t_1]: During this stage, the switches S_2, S_4, S_5, and S_7 are in on-state as shown in Fig. 3(a). Therefore, the voltage of V_{ab} is kept at $0V$.

Stage 2 [t_1-t_2]: During this stage, the switches S_2, S_3, S_5, and S_7 are in on-state. The current i_p will go through S_5, S_3, C_3, and S_2 (or D_2), which makes the V_{ab} equals to $V_{in}/4$.

Stage 3 [t_2-t_3]: During this stage, the switches S_1, S_3, S_5, and S_7 are in on-state. The current i_p will go through S_5, S_3, and S_1, which leads the V_{ab} equals to $V_{in}/2$.

The switching states in the time intervals [t_0-t_1] and [t_1-t_2] are the same as the above time intervals [t_3-t_4] and [t_4-t_5] respectively. Therefore, the analysis about them is not repeated here.

Stage 4 [t_5-t_6]: During this stage, the switches S_1, S_3, S_6, and S_8 are in on-state as shown in Fig. 3(d). Therefore, the voltage of V_{ab} is kept at $0V$.

Stage 5 [t_6-t_7]: During this stage, the switches S_1, S_4, S_6, and S_8 are in on-state. The current i_p will go through S_1 (or D_1), C_3, S_4, and S_8, which makes the V_{ab} equals to $-V_{in}/4$.

Stage 6 [t_7-t_8]: During this stage, the switches S_2, S_4, S_6, and S_8 are in on-state. The current i_p will go through S_2, S_4, and S_8, which leads the V_{ab} equals to $-V_{in}/2$.

The switching states in the time intervals [t_5-t_6] and [t_6-t_7] are the same as the above time intervals [t_8-t_9] and [t_9-t_{10}] respectively. Therefore, the analysis about them is not repeated here.

The analysis about the operation mode II is similar to that in the operation mode I, which is not repeated here.

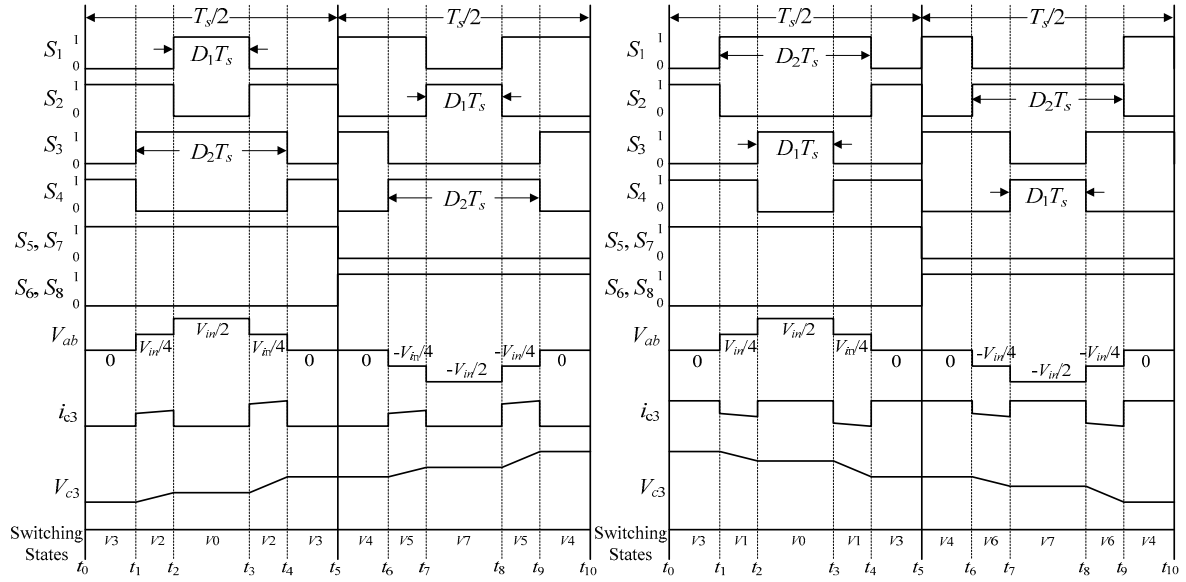
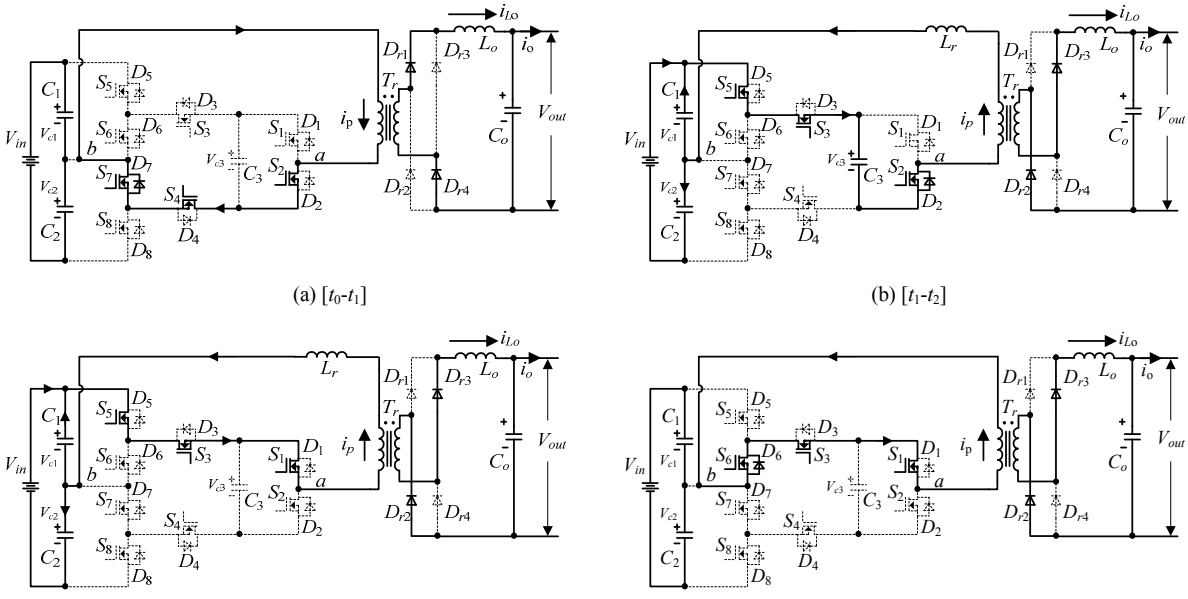


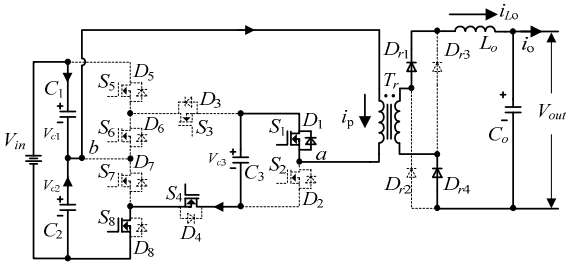
Fig. 2. Proposed modulation strategy. (a) the operation mode I. (b) the operation mode II.

TABLE I. SWITCHING STATES AND CIRCUIT OPERATION STATUSES OF THE 5L-ANPC CONVERTER

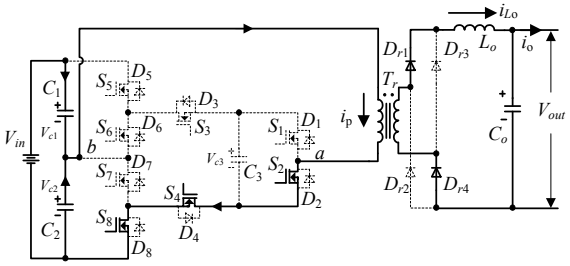
Switching State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V_{ab}	i_{c3}
$V0$	1	0	1	0	1	0	1	0	V_{c1} (V_{in}/2)	0
$V1$	1	0	0	1	1	0	1	0	V_{c3} (V_{in}/4)	-|i_{ab}|
$V2$	0	1	1	0	1	0	1	0	V_{c1}-V_{c3} (V_{in}/4)	+|i_{ab}|
$V3$	0	1	0	1	1	0	1	0	0	0
$V4$	1	0	1	0	0	1	0	1	0	0
$V5$	1	0	0	1	0	1	0	1	-(V_{c2}-V_{c3}) (-V_{in}/4)	+|i_{ab}|
$V6$	0	1	1	0	0	1	0	1	-V_{c3} (-V_{in}/4)	-|i_{ab}|
$V7$	0	1	0	1	0	1	0	1	-V_{c2} (V_{in}/2)	0



(a) [t_0-t_1]
(b) [t_1-t_2]
(c) [t_2-t_3]
(d) [t_5-t_6]



(e) [t_6-t_7]



(f) [t_7-t_8]

Fig. 3. Equivalent circuits in the operation mode I.

III. Proposed Capacitor Voltage Control Strategy

A voltage control strategy is proposed for balancing the flying capacitor's voltage by alternating the operation modes I and II of the proposed modulation strategy because the main difference between the operation mode I and II is the charge and discharge issue of the flying capacitor C_3.

A. Operation Mode I

From Fig. 2 (a), in the first half cycle, it can be observed that the input voltage of MFT V_{ab} is positive and the switching states are:

$$V3 \rightarrow V2 \rightarrow V0 \rightarrow V2 \rightarrow V3 \quad (1)$$

In addition, the switching state is $V2$ when V_{ab} equals $V_{in}/4$. According to Table I, the charge or discharge situation of the flying capacitor C_3 only occurs when the input voltage of MFT V_{ab} equals $V_{in}/4$ or $-V_{in}/4$, and the flying capacitor is charged on switching states $V2$, $V5$ and discharged on switching states $V1$, $V6$ respectively. Therefore, the flying capacitor C_3 is charged and not discharged in the first half cycle.

In the second half cycle, the switching states are:

$$V4 \rightarrow V5 \rightarrow V7 \rightarrow V5 \rightarrow V4 \quad (2)$$

Similar to the first half cycle, the flying capacitor C_3 is also charged and not discharged in the second half cycle because the switching state is $V5$ when V_{ab} equals $-V_{in}/4$. In summary, the flying capacitor C_3 is charged and not discharged, which in turn means the voltage of the flying capacitor increase and not decrease in the operation mode I as showed in Fig. 2(a).

B. Operation Mode II

Similar to the analysis about the operation mode I, in the operation mode II, it can also be seen that the switching states in the first half cycle is:

$$V3 \rightarrow V1 \rightarrow V0 \rightarrow V1 \rightarrow V3 \quad (3)$$

The switching state is $V1$ when V_{ab} equals $V_{in}/4$. According to Table I, the flying capacitor C_3 is discharged and not charged in the first half cycle.

In the second half cycle, the switching states are:

$$V4 \rightarrow V6 \rightarrow V7 \rightarrow V6 \rightarrow V4 \quad (4)$$

When V_{ab} is $-V_{in}/4$, the switching state is $V6$, which means the flying capacitor C_3 is discharged and not charged in the second half cycle according to Table I. Base on the above analysis, it can be concluded that the flying capacitor C_3 is discharged and not charged in the operation mode II, which means the voltage of the flying capacitor decrease but not increase in the operation mode I as showed in Fig. 2(b).

C. Proposed Capacitor Voltage Control Strategy

Based on the above analysis, the voltage of flying capacitor C_3 would increase in the operation mode I and decrease in the operation mode II. Consequently, a capacitor voltage control strategy is proposed for balancing the voltage of the flying capacitor C_3 as showed in Fig. 4, where a comparator is used with two input voltages V_{c3} and V_{ref_c3}. V_{ref_c3} is the reference voltage of the flying capacitor C_3, which is normally set to $V_{in}/4$. If V_{c3} is less than V_{ref_c3}, the operation mode I is selected in the next cycle. On the contrary, the operation mode II is selected in the next cycle.

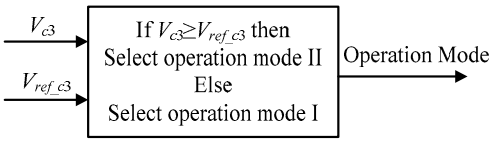


Fig. 4. Block diagram of the proposed voltage control strategy for the flying capacitor C_3.

IV. Simulation And Experimental Verification

A simulation model is built in PLECS to validate the above theoretical analysis, whose parameters are listed in Table II.

TABLE II. Parameters of the Simulation Model

Components	Description
Turns Ratio of the Transformer	2:1
Input Capacitors C_1, and C_2 (uF)	6800
Flying Capacitor C_3 (uF)	3500
Input Voltage V_{in} (kV)	4
Output Voltage V_{out} (V)	800
Voltage Reference of Flying Capacitor V_{ref_c3} (kV)	1
Switching Frequency (kHz)	5

The simulation results in steady state are showed in Fig. 5 and Fig. 6, which include voltages V_{in}, V_{ab}, V_{c3}, V_{out} and currents i_p, i_{Lo}, and i_o. It can be observed that five-level voltages are produced on the primary side of the transformer, which can effectively reduce the voltage change rate dv/dt and

voltage stress on the transformer, and the voltage of the flying capacitor V_{c3} is balanced at 1-kV constantly, which is a quarter of input voltage 4-kV, by the proposed voltage control strategy. The output voltage V_{out} is 800V stably.

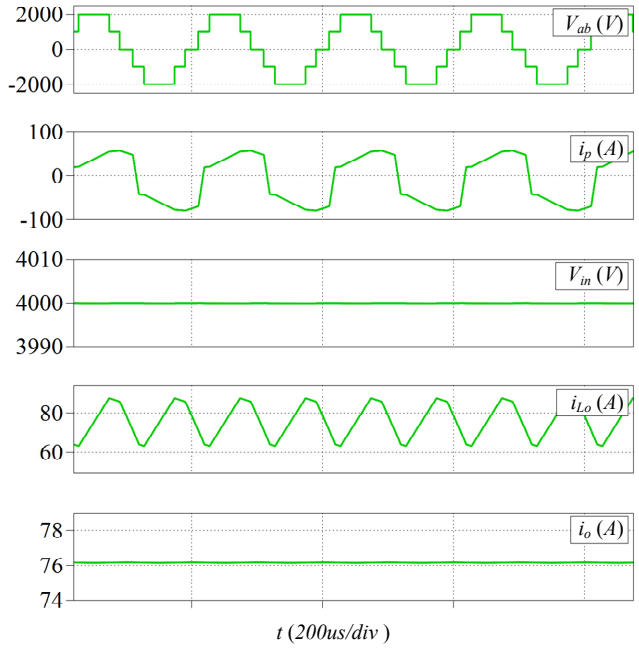


Fig. 5. Simulation results including V_{ab}, i_p, V_{in}, i_{Lo}, and i_o.

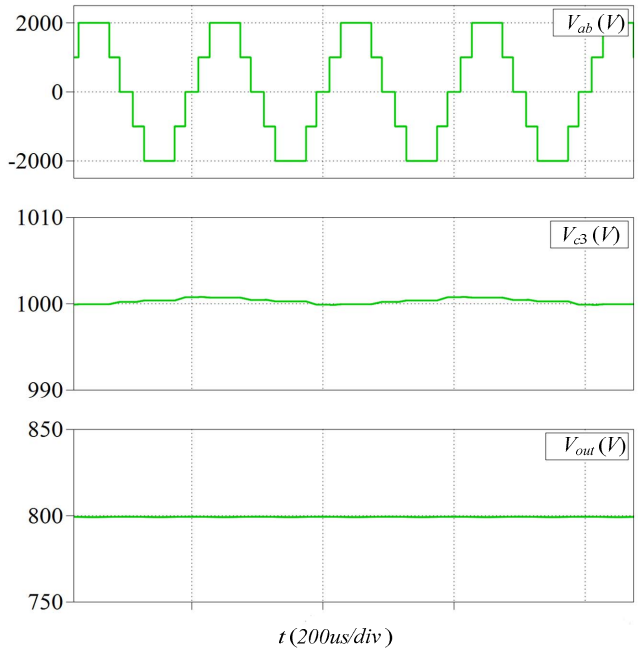


Fig. 6. Simulation results including V_{ab}, V_{c3}, and V_{out}.

In order to verify the above theoretical analysis, a down-scaled prototype is built, whose parameters are listed in Table III.

TABLE III. PARAMETERS OF THE EXPERIMENTAL SETUP

Components	Description
Mosfets S_1/D_1-S_4/D_4	IRFP4137PBF
Mosfets S_5/D_5-S_8/D_8	SPW47N60C3
Rectifier Diodes D_{r1}-D_{r4}	FFA60UP30DNTU
Turns Ratio of the Transformer	1:2
Input Capacitors C_1 and C_2 (uF)	1500
Flying Capacitor C_3 (uF)	1500
Input Voltage V_{in} (V)	240
Output Voltage V_{out} (V)	100
Voltage Reference of Flying Capacitor $V_{ref\ c3}$ (V)	60
Switching Frequency (kHz)	5
Dead Time (us)	1.5

Fig. 7 shows the experimental results under 250W, which include voltages V_{out}, V_{c3}, and V_{ab}. It can be observed that five-level voltages are produced on the transformer and the voltage of the flying capacitor V_{c3} is balanced at 60V constantly which is a quarter of V_{in} (240V) by using the proposed capacitor voltage control strategy.

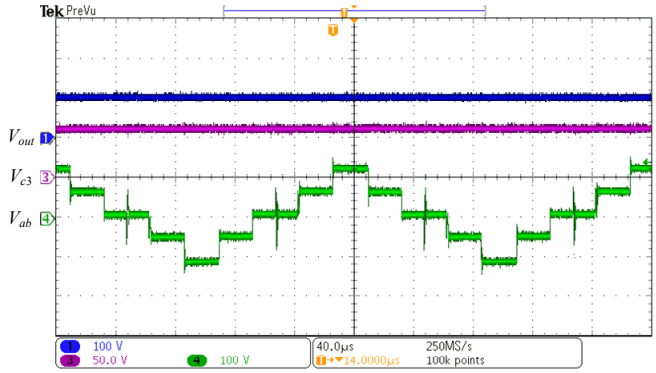


Fig. 7. Experimental results under 250W including V_{out}, V_{c3}, and V_{ab}.

V. CONCLUSION

This paper has proposed a 5L-ANPC dc/dc converter with a corresponding modulation strategy for the applications of MVDC grids. Due to multi-level voltages generating, the proposed converter can effectively reduce the voltage change rate dv/dt and voltage stress on the transformer, and thus reduces EMI and increases reliability of the converter. Furthermore, a capacitor voltage control strategy is proposed for balancing the voltage of the flying capacitor, which ensures five-level voltages producing. Finally, a simulation model and a down-scaled laboratory prototype of the proposed converter have been built. The simulation and experimental results validate the feasibility of the proposed converter and voltage control strategy.

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