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Published in:
Proceedings of the 2017 IEEE Applied Power Electronics Conference and Exposition (APEC)

DOI (link to publication from Publisher):
10.1109/APEC.2017.7930710

Publication date:
2017

Document Version
Accepted author manuscript, peer reviewed version

Link to publication from Aalborg University

Citation for published version (APA):

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A ZVS PWM Control Strategy with Balanced Capacitor Current for Half-Bridge Three-Level DC/DC Converter

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Abstract—The capacitor current would be imbalanced under the conventional control strategy in the half-bridge three-level (HBTL) DC/DC converter due to the effect of the output inductance of the power supply and the input line inductance, which would affect the converter’s reliability. This paper proposes a pulse-wide modulation (PWM) strategy composed of two operation modes for the HBTL DC/DC converter, which can realize the zero-voltage switching (ZVS) for the efficiency improvement. In addition, a capacitor current balancing control is proposed by alternating the two operation modes of the proposed ZVS PWM strategy, which can eliminate the current imbalance among the two input capacitors. Therefore, the proposed control strategy can improve the converter’s performance and reliability in: 1) reducing the switching losses and noises of the power switches; 2) balancing the thermal stresses and lifetimes among the two input capacitors. Finally, the simulation and experimental results are presented to verify the proposed control strategy.

Keywords—Capacitor current balance; DC/DC three-level converter; zero-voltage-switching (ZVS).

I. INTRODUCTION

More and more researches focus on the high voltage DC/DC converter with high performance and high reliability. The three-level (TL) DC/DC converter is one of the most attractive choices for the DC distribution systems with the high DC bus voltage [1-3] because the power switches in the TL converter only have to withstand half of the input voltage. The TL circuit structure was first applied into the DC/DC converter in [4], [5]. So far, many studies have been done based on the conventional TL circuit structure [6-9]. Reference [10] proposed a novel four-switch half-bridge three-level (HBT) DC/DC converter with zero-voltage-switching (ZVS) control strategy as shown in Fig. 1(a). In comparison with the conventional TL DC/DC converter, the four-switch HBT converter only adds one DC-blocking capacitor but removes two clamped diodes. Therefore, the four-switch HBT converter features with lower cost and more compact circuit structure, which makes it more suitable for the industrial applications. Due to these advantages, many studies have been done based on the four-switch HBTL converter [11-14]. In [10], the currents through the two input capacitors in the four-switch HBTL converter are analyzed with the assumption that the input power supply is regarded as an ideal voltage source, which means that the input current can change abruptly in the switching period. However, in the real applications, there exist the output inductance of the input power supply and the inductance of the input line, which would avoid the abrupt changes of the input current in the switching period and thus result in the current imbalance among the two input capacitors in the four-switch HBTL converter. The capacitor current imbalance issue would affect the reliability of the converter in aspects of the imbalance of the thermal stresses and lifetimes among the two input capacitors.

In this paper, a ZVS PWM strategy and a capacitor current balance control are proposed for the four-switch HBTL DC/DC converter. The proposed ZVS PWM strategy is composed of two operation modes with the same output performance, which can effectively achieve the ZVS for improving the converter’s efficiency. What is more, a capacitor current balancing control is proposed by alternating the two operation modes of the proposed ZVS PWM strategy to eliminate the current imbalance among the two input capacitors. Therefore, the proposed control strategy can reduce the switching losses and noises, balance the thermal stresses and lifetimes among the two input capacitors, and thus greatly improve the performance and reliability of the converter. Finally, the simulation and experimental results are presented to validate the proposed control strategy.

The organization of this paper is as follows. Section II analyzes the capacitor current imbalance under the conventional control strategy. Section III presents the operation principles of the proposed ZVS PWM strategy and capacitor current balancing control. Section IV analyzes the characteristics and performances of the HBTL DC/DC converter under the proposed control strategy. Section V shows the simulation and experimental results to validate the proposed control strategy. Finally, Section VI summarizes the main contributions of this paper.
II. ANALYSIS OF CAPACITOR CURRENT IMBALANCE

Fig. 1 shows the circuit structure of the four-switch HBTL DC/DC converter and main operation waveforms under the conventional control strategy [10]. In the primary side, two input capacitors $C_1$ and $C_2$ are used to split the input voltage $V_{in}$ into two voltages $V_1$ and $V_2$; $S_1 - S_4$ and $D_1 - D_4$ are power switches and diodes; $T_r$ is the high frequency transformer (HFT); $L_r$ is the leakage inductance of $T_r$; $C_{a1} - C_{a4}$ are the parasitic capacitors of $S_1 - S_4$; $C_b$ is the DC-blocking capacitor. In the secondary side, there are four rectifier diodes $D_{1a} - D_{4a}$, one output filter inductor $L_o$, and one output filter capacitor $C_o$. In Fig. 1(a), $i_{in}$ is the input current; $i_{c1}$ and $i_{c2}$ are the currents flowing through $C_1$ and $C_2$, respectively; $i_p$ is the current of the transformer $T_r$; $i_{in}$ is the current through $L_o$; $V_{sb}$ is the voltage on $C_b$; $i_o$ and $V_o$ are the output current and output voltage; $V_{in}$ is the voltage between point $a$ and $b$; $n$ is the turns ratio of the transformer $T_r$.

According to Fig. 1(b), $i_{c1}$ and $i_{c2}$ in one switching period namely $T_r$, can be expressed as

$$i_{c1} = \begin{cases} -i_{in} & t_0 \leq t < t_2 \\ \frac{i_p - i_{in}}{n} & t_2 \leq t < t_7 \\ -i_{in} & t_7 \leq t < t_{13} \end{cases}$$  \hspace{1cm} (1)

$$i_{c2} = \begin{cases} \frac{i_p - i_{in}}{n} & t_0 \leq t < t_9 \\ -i_{in} & t_9 \leq t < t_{13} \end{cases}$$  \hspace{1cm} (2)

According to Fig. 1(b), the primary current $i_p$ in one switching period $T_r$ can be described as

$$i_p = \begin{cases} -\frac{i_o}{n} & t_0 \leq t < t_2 \\ -\frac{i_o}{n} + \frac{V_o}{2 \cdot L_r} (t - t_2) & t_2 \leq t < t_6 \\ \frac{i_o}{n} - \frac{V_o}{2 \cdot L_r} (t - t_6) & t_6 \leq t < t_9 \\ -\frac{i_o}{n} & t_9 \leq t < t_{12} \end{cases}$$  \hspace{1cm} (3)

Substituting (3) into (1) and (2), $i_{c1}$ and $i_{c2}$ in one switching period can be rewritten as

$$i_{c1} = \begin{cases} -i_{in} & t_0 \leq t < t_2 \\ \frac{V_o}{2 \cdot L_r} \cdot (t - t_2) - \frac{i_o}{n} - i_{in} & t_2 \leq t < t_6 \\ \frac{i_o}{n} - i_{in} & t_6 \leq t < t_7 \\ -i_{in} & t_7 \leq t < t_{13} \end{cases}$$  \hspace{1cm} (4)

$$i_{c2} = \begin{cases} -\frac{i_o}{n} & t_0 \leq t < t_2 \\ \frac{V_o}{2 \cdot L_r} \cdot (t - t_2) - \frac{i_o}{n} + i_{in} & t_2 \leq t < t_6 \\ \frac{i_o}{n} - i_{in} & t_6 \leq t < t_9 \\ -i_{in} & t_9 \leq t < t_{13} \end{cases}$$  \hspace{1cm} (5)

In the steady-state situation, the time intervals $[t_2 - t_6]$ and $[t_0 - t_12]$ are the same as shown in Fig. 1(b), which can be calculated by

$$t_6 - t_2 = t_{12} - t_0 = \frac{4 \cdot L_r \cdot i_o}{n \cdot V_o}$$  \hspace{1cm} (6)

According to (4) - (6), the root-mean-square (RMS) values of $i_{c1}$ and $i_{c2}$ under the conventional control strategy namely $i_{c1, rms}$ and $i_{c2, rms}$ can be calculated by (7) and (8).
\[ i_{c,1_{rms,e}} = \sqrt[2]{\frac{i_{s,1}^2 \cdot d_1}{n^2} + \frac{8 \cdot L_s \cdot i_{s,1} \cdot i_{s,2}}{n \cdot V_{in} \cdot T_s} + \frac{2 \cdot i_{s,1} \cdot i_{s,2} \cdot d_1}{n} + \frac{8 \cdot L_s \cdot i_{s,2}^3}{3 \cdot n \cdot V_{in} \cdot T_s}} \tag{7} \]

\[ i_{c,2_{rms,e}} = \sqrt[2]{\frac{i_{s,2}^2 \cdot d_2}{n^2} + \frac{8 \cdot L_s \cdot i_{s,1} \cdot i_{s,2}}{n \cdot V_{in} \cdot T_s} + \frac{2 \cdot i_{s,1} \cdot i_{s,2} \cdot d_1}{n} + \frac{8 \cdot L_s \cdot i_{s,2}^3}{3 \cdot n \cdot V_{in} \cdot T_s}} \tag{8} \]

From (7) and (8), it can be observed that \( i_{c,1_{rms,e}} \) and \( i_{c,2_{rms,e}} \) are different and \( i_{c,2_{rms,e}} \) is bigger than \( i_{c,1_{rms,e}} \) because \( d_2 \) is bigger than \( d_1 \) as shown in Fig. 1(b). This current imbalance among the two input capacitors could result in the different thermal stresses and lifetimes between the two input capacitors, which would affect the converter's reliability.

III. PROPOSED CAPACITOR CURRENT BALANCE CONTROL

In this section, a capacitor current balancing control is proposed, which can not only achieve ZVS for the power switches but also eliminate the current imbalance among the two input capacitors.

A. Proposed ZVS PWM Strategy

Fig. 2 shows the proposed ZVS PWM strategy including two operation modes with same output characteristics, in which \( d_{on} - d_{off} \) are four driving signals of the power switches \( S_1 - S_4 \) and \( d_1 \) is the duty ratio in one switching period. In the operation mode I, the duty ratios of \( d_{on} \) and \( d_{off} \) are 0.5 and duty ratios of \( d_{on} \) and \( d_{off} \) are \( d_1 \). On the contrary, the duty ratios of \( d_{on} \) and \( d_{off} \) are 0.5 and duty ratios of \( d_{on} \) and \( d_{off} \) are \( d_1 \) in the operation mode II.

Fig. 3 shows equivalent circuits to explain the operation principle of the operation mode I shown in Fig. 2(a).

Stage 0 [before \( t_0 \)] During this stage, both \( S_2 \) and \( S_3 \) are on-state, therefore the current \( i_p \) flows through \( S_2, S_3, \) and \( C_h \), the voltage \( V_{in} \) is 0 V. The power from \( C_h \) is transferred to the output through \( T_c, D_{c2}, \) and \( D_{c3} \).

Stage 1 [\( t_0 - t_1 \)] At \( t_0 \), the switch \( S_2 \) is turned off. The capacitor \( C_{cs} \) starts to charge, and the capacitor \( C_1 \) begins to discharge. This stage finishes until \( V_{cs} \) increases \( V_{in}/2 \) and \( V_{cs} \) decreases 0 V.

Stage 2 [\( t_1 - t_2 \)] At \( t_1 \), the voltage on \( C_2 \) becomes zero and the diode \( D_1 \) begins to conduct. The circuit operates in a free-wheeling mode with the current \( i_p \) flowing through \( L_2, D_1, C_1, S_1, C_h, \) and \( T_r \). During this stage, the current \( i_p \) is kept at \( i_p/n \).

Stage 3 [\( t_2 - t_3 \)] At \( t_2 \), the switch \( S_3 \) is turned off. The capacitor \( C_{cs} \) starts to charge, and the capacitor \( C_4 \) begins to discharge. This stage finishes until \( V_{cs} \) increases to \( V_{in}/2 \) and \( V_{cs} \) decreases 0 V. The current \( i_p \) starts to increase.

Stage 4 [\( t_3 - t_4 \)] At \( t_3 \), the voltage on \( C_4 \) becomes zero and the diode \( D_2 \) begins to conduct. The circuit operates in a freewheeling mode with the current \( i_p \) flowing through \( L_4, D_3, C_3, S_2, C_h, \) and \( T_r \).

Stage 5 [\( t_4 - t_5 \)] At \( t_4 \), the switches \( S_1 \) and \( S_3 \) are turned on at zero voltage. The current \( i_p \) flows through \( L_2, S_1, C_1, C_2, S_2, C_h, \) and \( T_r \).

Stage 6 [\( t_5 - t_6 \)] At \( t_5 \), the current \( i_p \) increases to 0 A and continues to increase linearly, which means the direction of \( i_p \) begins to change.

Stage 7 [\( t_6 - t_7 \)] At \( t_6 \), the currents \( i_{c1} \) and \( i_{c2} \) increases to 0 A, which means the directions of \( i_{c1} \) and \( i_{c2} \) begin to change.

Stage 8 [\( t_7 - t_8 \)] At \( t_7 \), the current \( i_p \) increases to \( i_p/n \), then the input power \( V_{in} \) begins to be transferred to the output through \( T_r, D_{c1}, \) and \( D_{c3} \). This stage, \( i_p \) is kept at \( i_p/n \).

Stage 9 [\( t_8 - t_9 \)] At \( t_8 \), the switch \( S_4 \) is turned off. The capacitor \( C_{cs} \) starts to charge, and the capacitor \( C_3 \) begins to discharge. This stage finishes until \( V_{cs} \) increases to \( V_{in}/2 \) and \( V_{cs} \) decreases to 0 V.
Stage 10 $[t_9-t_{10}]$ At $t_9$, $V_{c2}$ decreases to 0 V and diode $D_3$ begins to conduct. The circuit operates in a free-wheeling mode with the current $i_p$ flowing through $D_3$, $C_1$, $S_1$, $L_s$, $T_r$, and $C_b$.

Stage 11 $[t_{10}-t_{11}]$ At $t_{10}$, the switch $S_1$ is turned off. The capacitor $C_1$ starts to charge, and the capacitor $C_{c2}$ begins to discharge. This stage finishes when $V_{c2}$ increases to $V_{b2}/2$ and $V_{c2}$ decreases to 0 V. The current $i_p$ starts to decrease, and the current $i_{c1}$ decreases to $-i_{in}$.

Stage 12 $[t_{11}-t_{12}]$ At $t_{11}$, the voltage on $C_{c2}$ becomes zero and diode $D_2$ begins to conduct. The circuit operates in a free-wheeling mode with the current $i_p$ flowing through $D_3$, $D_2$, $L_s$, $T_r$, and $C_b$. Both current $i_{c1}$ and $i_{c2}$ are $-i_{in}$.

Stage 13 $[t_{12}-t_{13}]$ At $t_{12}$, the switches $S_1$ and $S_3$ are turned on at zero voltage. The current $i_p$ would flow through $S_3$, $S_2$, $L_s$, $T_r$, and $C_b$.

Stage 14 $[t_{13}-t_{14}]$ At $t_{13}$, the current $i_p$ decreases to 0 A and continues to decrease linearly, which means the direction of $i_p$ begins to change.

Stage 15 $[t_{14}-t_{15}]$ At $t_{14}$, the current $i_p$ decreases to $-i_{in}/n$, then the power is transferred from $C_b$ to the output through $T_r$, $D_2$, and $D_3$. During this stage, the current $i_p$ is kept at $-i_{in}/n$.

At $t_{15}$, the following work operation in the next cycle starts, which is same as the first switching period. The analysis of the operation mode II is similar as that of the operation mode I, which is not repeated here.
B. Proposed Capacitor Current Balance Control

Based on the above analysis, the main difference between the operation mode I and II is that the RMS value of $i_{c1}$ is bigger than that of $i_{c2}$ in the operation mode I but the RMS value of $i_{c2}$ is smaller than that of $i_{c1}$ in the operation mode II. In order to balance these two currents $i_{c1}$ and $i_{c2}$, a capacitor current balance control is proposed by alternating the two operation modes. Fig. 4 shows the proposed control for balancing the currents on the two input capacitors, in which $d_{i1}$ - $d_{i4}$ are four driving signals of the power switches $S_1$ - $S_4$ and $d_i$ is duty ratio in one switching period. In the proposed capacitor current balancing control, the operation mode I is used for the first switching period and the operation mode II is used for the second switching period, which makes the currents on the two input capacitors are the same in every two switching periods as shown in Fig. 4.

Assuming that the DC-blocking capacitor is large enough to be considered as a voltage source, the voltage on the DC-blocking capacitor is

$$V_{cb} = \frac{V_m}{2}$$

(10)

Substituting (10) into (9), then the output voltage can be expressed by

$$V_o = \frac{V_m}{n} \cdot d_i$$

(11)

The duty cycle loss in one switching period as shown in Fig. 4 can be given by

$$d_{loss} = 2 \cdot \frac{(t_1-t_2)}{T_s} = \frac{8 \cdot L_s \cdot i_s}{n \cdot V_m \cdot T_s}$$

(12)

where $d_{loss}$ is the duty cycle loss.

After considering the effect of duty cycle loss, the output voltage can be calculated by

$$V_o = \frac{V_m}{n} \cdot (d_i - d_{loss}) = \frac{V_m}{n} \cdot (d_i - \frac{4 \cdot L_s \cdot i_s}{n \cdot V_m \cdot T_s})$$

(13)

B. ZVS Achievement Conditions

Before discussing the ZVS achievement conditions under the proposed control strategy, one assumption is made that the parasitic capacitors of $S_1$ - $S_4$ are the same namely $C_v$.

In the operation mode I, the energy $E_i$ calculated by (14) is needed to ensure the switches $S_1$ and $S_3$ realizing zero-voltage switch-on. The energy to achieve zero-voltage switch-on for $S_1$ and $S_3$ is provided by both the output filter inductance and the leakage inductance.

$$E_i = \frac{1}{2} \cdot C_v \cdot \left(\frac{V_m}{2}\right)^2 = \frac{1}{2} \cdot C_v \cdot \left(\frac{V_o}{2}\right)^2 = \frac{1}{4} \cdot C_v \cdot V_o^2$$

(14)

The energy of the leakage inductance of the transformer is used to achieve zero-voltage switch-on of switches $S_2$ and $S_4$. Therefore, in order to achieve the zero-voltage switch-on of switches $S_2$ and $S_4$ (15) should be satisfied.

$$\frac{1}{2} \cdot L_c \cdot \left(\frac{I_n}{n}\right)^2 \geq \frac{1}{2} \cdot C_v \cdot \left(\frac{V_o}{2}\right)^2 + \frac{1}{2} \cdot C_s \cdot \left(\frac{V_o}{2}\right)^2 = \frac{1}{4} \cdot C_v \cdot V_o^2$$

(15)

IV. CHARACTERISTICS AND PERFORMANCES UNDER THE PROPOSED CONTROL STRATEGY

A. Output Characteristic

If neglecting the duty ratio loss, the average output voltage $V_o$ is

$$V_o = \frac{1}{n} \left[ (V_m - V_{cb}) \cdot d_i + V_{cb} \cdot d_i \right]$$

(9)
In the operation mode II, the analysis of the ZVS achievement conditions is similar to that in the operation mode I as above, which is not repeated here.

The proposed capacitor current balance control operates by alternating the operation mode I and II, therefore the ZVS achievement conditions of the proposed capacitor current balance control is the combination of the ZVS achievement conditions of the operation mode I and II. In the first switching period, the energy from both the output filter inductance and leakage inductance of the transformer is provided for $S_1$, $S_2$ to realize the zero-voltage switch-on and the energy from the leakage inductance is provided for $S_3$, $S_4$ to achieve the zero-voltage switch-on. In the second switching period, the ZVS achievement conditions are just contrary to that in the first switching period, which means the energy from both the output filter inductance and leakage inductance of the transformer is provided for $S_3$, $S_4$ to realize the zero-voltage switch-on and the energy from the leakage inductance is provided for $S_1$, $S_2$ to achieve the zero-voltage switch-on.

C. Analysis of Input Capacitor Currents

According to Fig. 4, the expressions of $i_{c1}$ and $i_{c2}$ in two switching periods can be given by

\[
i_{c1} = \begin{cases} 
-i_n, & [t_0 - t_2] \\
-i_n + \frac{V_m}{2 \cdot L_v} \cdot (t - t_2), & [t_2 - t_{10}] \\
-i_n, & [t_{10} - t_{11}] \\
-i_n, & [t_{11} - t_{22}] \\
-i_n, & [t_{22} - t_{29}] \\
\end{cases}
\]

\[
i_{c2} = \begin{cases} 
-i_n, & [t_0 - t_2] \\
-i_n, & [t_2 - t_{13}] \\
-i_n, & [t_{13} - t_{18}] \\
-i_n + \frac{V_m}{2 \cdot L_v} \cdot (t - t_{12}) \cdot i_n, & [t_{18} - t_2] \\
-i_n, & [t_2 - t_{28}] \\
\end{cases}
\]

The time intervals $[t_2 - t_3]$, $[t_{10} - t_{11}]$, $[t_{16} - t_{22}]$, and $[t_{24} - t_{28}]$ as shown in Fig. 4 can be described as

\[
t_3 - t_2 = t_{14} - t_{10} = t_{21} - t_{16} = t_{28} - t_{24} = \frac{4 \cdot L_v \cdot i_n}{n \cdot V_m}
\]

According to (19), (20) and (21), the RMS values of $i_{c1}$ and $i_{c2}$ under the proposed control namely $i_{c1_{rms}}$ and $i_{c2_{rms}}$ can be calculated as (22).

\[
i_{c1_{rms}} = \frac{i_{c1_{rms}}}{n} - \frac{i_{c2_{rms}}}{n} = \sqrt{\frac{\int_{t_0}^{t_3} [i_{c1} - i_{c2}]^2 dt}{t_3 - t_0}} \approx \sqrt{\frac{2 \cdot i_n^2 \cdot V_m^2 \cdot T}{n \cdot L_v}}
\]

V. SIMULATION AND EXPERIMENTAL VERIFICATION

A. Simulation Verification

In order to verify the proposed control strategy, a simulation model is built, whose parameters are listed in Appendix. In the simulation, the input voltage $V_{in}$ is 550 V, the output voltage $V_o$ is 50 V, and the output power namely $P_o$ is 1-kW. Figs. 5(a) and (b) show simulation results under the conventional control strategy and the proposed control strategy, respectively.
Fig. 5. Simulation results including \( V_{in}, i_{c1}, i_{c2}, i_p, V_o, \) and \( i_o \). (a) Conventional control strategy. (b) Proposed control strategy. In summary, the simulation results verify that the current imbalance among the two input capacitors \( C_1 \) and \( C_2 \) are effectively eliminated by utilizing the proposed control strategy.

**B. Experimental Verification**

A 1-kW 50 kHz prototype is built to verify the above theoretical analysis. The specifications of the built prototype are listed in Appendix. In the experiments, the output voltage \( V_o \) is 50 V, and the input voltage is 450 V - 550 V. The turns ratio of the transformer \( T_r \) is 25:8. SPW47N60C3 is adopted as the primary power switches. MBR40250TG is selected for the output rectifier diodes. The performances of the established prototype are shown in Figs. 6 and 7 under the working conditions that the input voltage \( V_{in} \) is 550 V and the output power \( P_o \) is 1-kW.

Figs. 6(a) and (b) show the currents \( i_p, i_o \) and voltages \( V_{in}, V_o, \) \( V_{o} \) under the conventional and proposed control strategy, respectively. It can be seen that the primary currents \( i_p \) are almost the same under the two control strategies. The frequencies of \( i_{c1} \) and \( i_{c2} \) under the proposed control strategy are twice of that under the conventional control strategy as marked in Fig. 7, which is consistent with the theoretical analysis. In addition, \( i_{c1} \) and \( i_{c2} \) are different under the conventional control strategy, whose RMS values are 3.16 A and 5.18 A respectively, as shown in Fig. 7(a). Therefore, the difference between \( i_{c1\_rms}, i_{c2\_rms} \) are 2.02 A. After using the proposed control strategy, \( i_{c1} \) and \( i_{c2} \) are almost the same and their RMS values are 4.36 A and 4.39 A, respectively, as shown in Fig. 7(b).

Fig. 6. Experimental results including \( V_{in}, V_o, i_p, \) and \( i_o \) at \( V_{in} = 550 \) V and \( P_o = 1\)-kW. (a) Conventional control strategy. (b) Proposed control strategy.
In this paper, a ZVS PWM strategy and a capacitor current balancing control is proposed for the four-switch HBTL DC/DC converter. The proposed ZVS PWM strategy composed of two operation modes can achieve the ZVS for the efficiency improvement. In addition, a capacitor current balance control is proposed by alternating the two operation modes of the proposed ZVS PWM strategy to eliminate the current imbalance among the two input capacitors. Therefore, the proposed control strategy can reduce the switching losses and noises, balance the thermal stresses and lifetimes among the two input capacitors, and thus improve the performance and reliability of the converter. Finally, the simulation and experimental results verify the proposed control strategy.

APPENDIX

TABLE I. PARAMETERS OF THE SIMULATION MODEL AND EXPERIMENTAL PROTOTYPE

<table>
<thead>
<tr>
<th>Description</th>
<th>Parameter</th>
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<tr>
<td>Turns Ratio of Transformer $T_l$</td>
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<td>Leakage Inductances $L_a$ (µH)</td>
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<td>Output Filter Capacitor $C_1$ (µF)</td>
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<tr>
<td>Output Filter Inductors $L_m$ (µH)</td>
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<td>Input Capacitors $C_i$ and $C_o$ (µF)</td>
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<td>DC-blocking Capacitors $C_k$ (µF)</td>
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<td>Switching Frequency (kHz)</td>
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<td>Dead Time (ns)</td>
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REFERENCES