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Liu, Dong; Wang, Yanbo; Chen, Zhe; Deng, Fujin

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A Zero-Voltage Switching Control Strategy for Dual Half-Bridge Cascaded Three-Level DC/DC Converter with Balanced Capacitor Voltages

Dong Liu, Yanbo Wang, Zhe Chen
Department of Energy Technology
Aalborg University
Aalborg, Denmark
dli@et.aau.dk, ywa@et.aau.dk, zch@et.aau.dk

Fujin Deng
School of Electrical Engineering
Southeast University
Nanjing, China
dfjqfa@163.com

***Abstract*— The input capacitors' voltages are unbalanced under the conventional control strategy in a dual half-bridge cascaded three-level (TL) DC/DC converter, which would affect the high voltage stresses on the capacitors. This paper proposes a pulse-wide modulation (PWM) strategy with two working modes for the dual half-bridge cascaded TL DC/DC converter, which can realize the zero-voltage switching (ZVS). More significantly, a capacitor voltage balance control is proposed by alternating the two working modes of the proposed ZVS PWM strategy, which can eliminate the voltage unbalance on the four input capacitors. Therefore, the proposed control strategy can improve the converter's performances in: 1) reducing the switching losses and noises of the power switches; and 2) reducing the voltage stresses on the input capacitors. Finally, the simulation results are conducted to verify the proposed control strategy.**

Keywords—Capacitor voltage balance; DC/DC converter; three-level (TL).

I. INTRODUCTION

Although AC grids and AC distribution systems are widely used for transmitting the electrical power currently [1-3], DC distribution system is regarded as one of promising solutions for the future power distribution system [4-6] because the increasing applications of renewable energy. Many studies pay attention on the high voltage DC/DC converters with high performance and high reliability [7], [8] because they play very importance role in delivering the electrical power in DC distribution systems. Due to low voltage stress on the power switch, the three-level (TL) DC/DC converter is one of most suitable choices for the DC distribution systems with high DC bus voltage [9], [10]. The TL circuit structure was first proposed for the DC/DC converter in [11]. Then many studies have been carried on the TL DC/DC converter [12-15]. Improving the power density and efficiency is one of the hot topics about the TL DC/DC converters. In [16], a dual half-bridge cascaded TL DC/DC converter, which is composed of two transformers and two half-bridge cells, was proposed. The two half-bridge cells are connected in series without the clamping diodes and flying capacitors to keep the voltage stresses on the power switches only half of the input voltage. Therefore, the dual half-bridge cascaded TL DC/DC converter have more compact circuit structure in comparison with the conventional TL DC/DC converter. However, the voltages among the input capacitors in the dual half-bridge cascaded TL DC/DC converter are unbalanced under the conventional control strategy, which would cause high voltage stresses on the input capacitors. In addition, this capacitor voltage unbalance would become severe with the output voltage decreasing or the input voltage increasing.

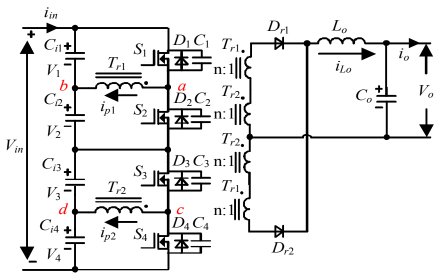
In this paper, a zero-voltage switching (ZVS) pulse-wide modulation (PWM) strategy and a capacitor voltage balance control are proposed for the dual half-bridge cascaded TL DC/DC converter. The proposed ZVS PWM strategy is composed of two working modes, which have the same output performance and can both realize the ZVS for the power switches. More significantly, a capacitor voltage balance control is proposed by alternating the two working modes of the proposed ZVS PWM strategy to eliminate the voltage unbalance among the four input capacitors. Consequently, the proposed control strategy can improve the performances of the converter in aspects of reducing the switching losses and noises, and reducing the voltage stresses on the input capacitors. Finally, the simulation results are presented to verify the proposed control strategy.

The organization of this paper is as follows. Section II analyzes the voltage unbalance among the input capacitors under the conventional control strategy. Section III illustrates the operation principles of the proposed ZVS PWM strategy and proposed capacitor voltage balance control. Section IV analyzes the characteristics of the dual half-bridge cascaded TL DC/DC converter under the proposed control strategy. Section V presents the simulation results to verify the proposed control strategy. Finally, the main contributions of this paper are summarized in Section VI.

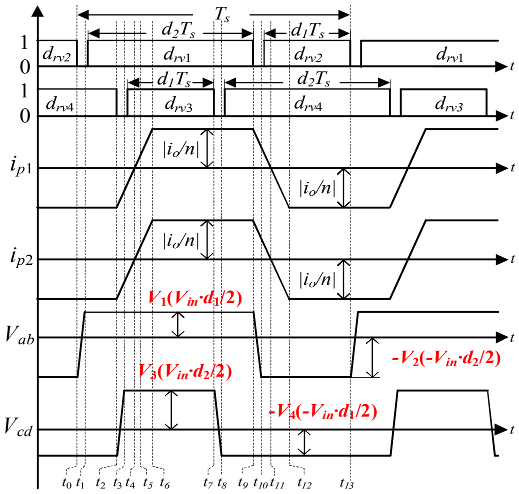
II. CAPCITOR VOLTAGE UNBALANCE ANALYSIS

Fig. 1 shows the circuit structure of the dual half-bridge cascaded TL DC/DC converter with main operation waveforms under the conventional control strategy [16]. In the primary side, four input capacitors C_{i1} - C_{i4} are used to split the input voltage V_{in} into four voltages V_1 - V_4; S_1 - S_4 and D_1 - D_4 are power switches and diodes; T_{r1} and T_{r2} are two high frequency transformers; C_1 - C_4 are the parasitic capacitors of S_1 - S_4. In the secondary side, there are two rectifier diodes D_{r1} and D_{r2}, one output filter inductor L_o, and one output filter capacitor C_o.

In Fig. 1(a), i_{p1} and i_{p2} is the current of the transformer T_{r1} and T_{r2}; i_o and V_o are the output current and voltage; n is turns ratio of the transformers T_{r1} and T_{r2}; V_{ab} is the voltage between point a and b; V_{cd} is the voltage between point c and d. In Fig. 1(b), d_{rv1} - d_{rv4} are the driving signals for the power switches S_1 - S_4; d_1 and d_2 are the duty cycles in one switching period. If neglecting the dead time, d_2 would equal to 1 - d_1.



(a)



(b)

Fig. 1. (a) Circuit structure of dual half-bridge cascaded TL DC/DC converter. (b) Main operation waveforms.

Before discussing about the voltage unbalance among the input capacitors in the dual half-bridge cascaded TL DC/DC converter, some assumptions are made as below: 1) the output filter inductor L_o is large enough to be considered as the current source; 2) the switches S_1 - S_4 and diodes D_1 - D_4 are ideal; 3) the input capacitors C_{i1} - C_{i4} have the same capacitance and are large enough to be considered as the voltage sources.

According to Fig. 1(a), the relations between the voltages on the input capacitors are

$$V_1 + V_2 = V_{in} / 2 \tag{1}$$

$$V_3 + V_4 = V_{in} / 2 \tag{2}$$

Based on the volt-second principle, if neglect the dead time, the voltages on the transformers T_{r1} and T_{r2} multiplied by the time periods in one switching period can be expressed by

$$V_1 \cdot d_2 \cdot T_s = V_2 \cdot d_1 \cdot T_s \tag{3}$$

$$V_4 \cdot d_2 \cdot T_s = V_3 \cdot d_1 \cdot T_s \tag{4}$$

According to (1) - (4), the voltages on the input capacitors can be obtained

$$V_1 = V_4 = \frac{V_{in} \cdot d_1}{2} \tag{5}$$

$$V_2 = V_3 = \frac{V_{in} \cdot d_2}{2} \tag{6}$$

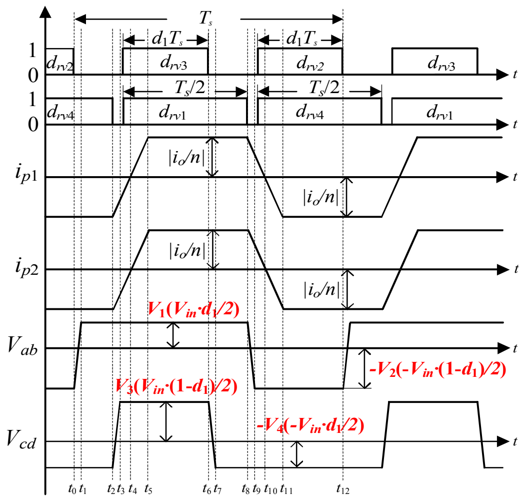
Normally, d_2 is larger than d_1 under the conventional control strategy. Therefore, the voltages on the four input capacitors C_{i1} - C_{i4} (V_1 - V_4) would be unbalanced, which means that the voltages on C_{i2} and C_{i3} (V_2 and V_3) are higher than that on C_{i1} and C_{i4} (V_1 and V_4).

III. Proposed Capacitor Voltage Balance Control

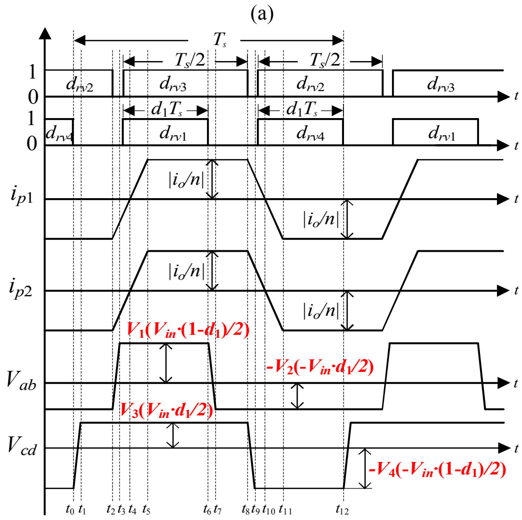
In this section, a capacitor voltage balance control is proposed, which can not only realize ZVS but also eliminate the voltage unbalance on the four input capacitors.

A. Proposed ZVS PWM Strategy

Fig. 2 presents the proposed ZVS PWM strategy including the two working modes with the same output performances.



(a)



(b)

Fig. 2. Operation principle of the proposed ZVS PWM strategy. (a) Working mode I. (b) Working mode II.

In Fig. 2, d_{rv1} - d_{rv4} are the driving signals of S_1 - S_4 and d_1 is the duty cycle in one switching period. In the working mode I, the duty cycles of d_{rv1} and d_{rv4} are 0.5 and duty cycles of d_{rv2} and d_{rv3} are d_1. On the contrary, the duty cycles of d_{rv2} and d_{rv3} are 0.5 and duty cycles of d_{rv1} and d_{rv4} are d_1 in the working mode II.

Fig. 3 presents the equivalent circuits to illustrate the operation principle of the working mode I presented in Fig. 2(a).

Stage 0 [before t_0] During this stage, the power switches S_2 and S_4 are on-state, so the primary currents i_{p1} and i_{p2} flow through S_2 and S_4 respectively. During this stage, the primary voltages V_{ab} and V_{cd} are -V_2 and -V_4 respectively; and the primary power is transferred to the output through T_{r2}, T_{r1}, and D_{r2}.

Stage 1 [t_0 - t_1] At t_0, the switch S_2 is turned off. The capacitor C_2 begins to charge, and the capacitor C_1 starts to discharge. This stage would finish until the voltage on C_2 increases $V_{in}/2$ and the voltage on C_1 decreases 0 V.

Stage 2 [t_1 - t_2] At t_1, the voltage on C_1 becomes 0 V and the diode D_1 begins to conduct. The circuit works in a free-wheeling mode. During this stage, the primary current i_{p1} flows through D_1, C_{i1}, T_{r1}; the primary current i_{p2} flows through S_4, C_{i4}, T_{r2}; and the primary voltages V_{ab} and V_{cd} are V_1 and -V_4 respectively.

Stage 3 [t_2 - t_3] At t_2, the switch S_4 is turned off. The capacitor C_4 begins to charge, and the capacitor C_3 starts to discharge. This stage would finish until the voltage on C_4 increases to $V_{in}/2$ and the voltage on C_3 decreases 0 V. During this stage, there is no enough primary power to be transferred to the output, so the output rectifier diodes D_{r1} and D_{r2} would turn on simultaneously, which clamps the primary voltage and secondary both at 0 V. In addition, the primary currents i_{p1} and i_{p2} start to increase.

Stage 4 [t_3 - t_4] At t_3, the voltage on C_3 becomes 0 V and the diode D_3 begins to conduct. Therefore, the power switches S_1 and S_3 can be turned on at zero voltage. During this stage, the primary voltages V_{ab} and V_{cd} are V_1 and V_3 respectively.

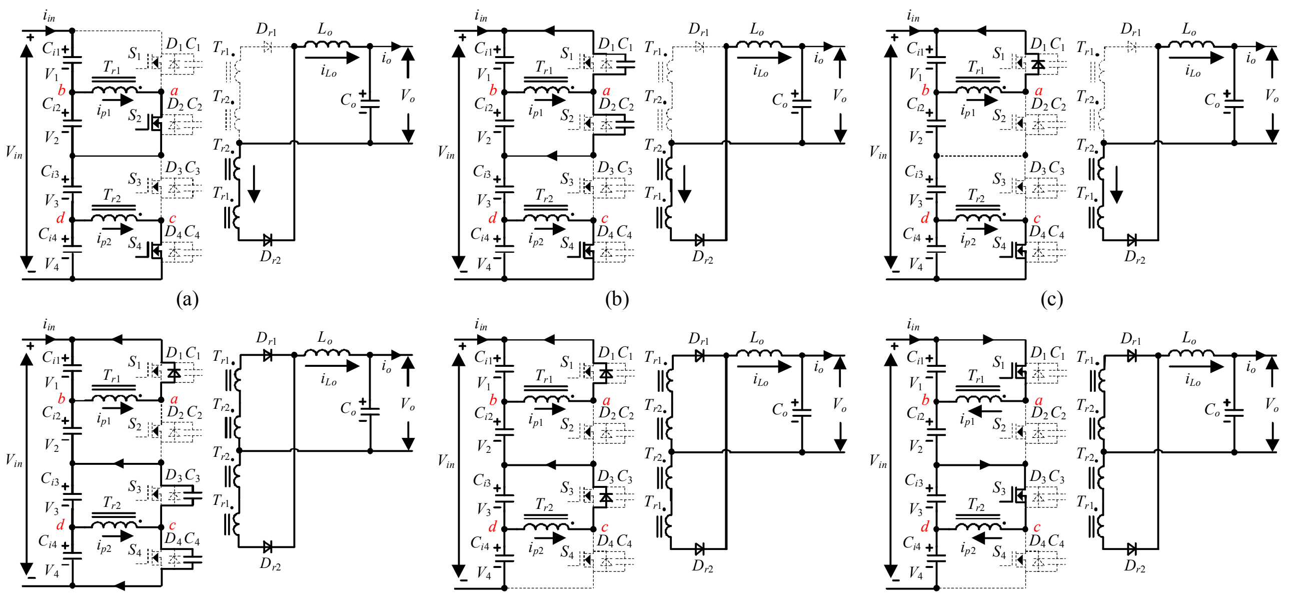
Stage 5 [t_4 - t_5] At t_4, the primary currents i_{p1} and i_{p2} increase to 0 A and continues to increase linearly, which means that the directions of i_{p1} and i_{p2} start to change. The primary voltages V_{ab} and V_{cd} remain V_1 and V_3 respectively.

Stage 6 [t_5 - t_6] At t_5, the primary currents i_{p1} and i_{p2} increase to i_o/n, then the output rectifier diode D_{r2} turn off and the input power begins to be transferred to the output through T_{r1}, T_{r2}, and D_{r1}. During this stage, the primary currents i_{p1} and i_{p2} are both kept at i_o/n; and the primary voltages V_{ab} and V_{cd} are still V_1 and V_3 respectively.

At t_6, the power switch S_3 is turned off, then the next half switching period starts. The analysis about this half switching period is similar to that in the last half switching period, which is not repeated here.

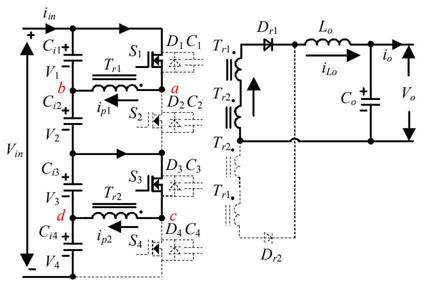
The operation principle of the working mode II is similar to that of the working mode I. The main difference between the working mode I and II in the first half switching period is the time period [t_0 - t_3], whose equivalent circuits are presented in Fig. 4. The analysis of the working mode II is similar to that of the working mode II, which is not repeated here.

The main difference between the working mode I and II is the voltages V_{ab} and V_{cd} as shown in Fig. 2. On the other words, the voltages on the capacitors C_{i2} and C_{i3} (V_2 and V_3) are higher than the voltages on the capacitors C_{i1} and C_{i4} (V_1 and V_4) in the working mode I, contrarily the voltages on the capacitors C_{i2} and C_{i3} (V_2 and V_3) are lower than the voltages on the capacitors C_{i1} and C_{i4} (V_1 and V_4) in the working mode II.



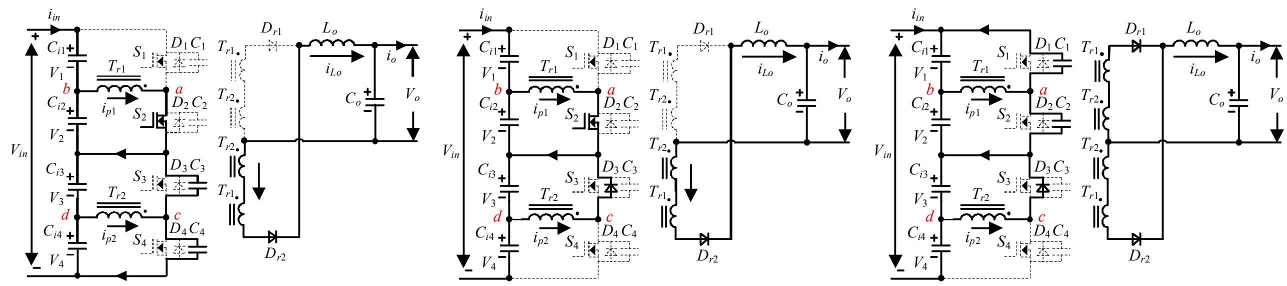
(a) (b) (c)

(d) (e) (f)



(g)

Fig. 3. Equivalent circuits of the working mode I. (a) [before t_0]. (b) [t_0 - t_1]. (c) [t_1 - t_2]. (d) [t_2 - t_3]. (e) [t_3 - t_4]. (f) [t_4 - t_5]. (g) [t_5 - t_6].



(a) (b) (c)

Fig. 4. Main equivalent circuits of the working mode II. (a) [t_0 - t_1]. (b) [t_1 - t_2]. (c) [t_2 - t_3].

B. Proposed Capacitor Voltage Balance Control

Based on the above analysis, the major difference between the working mode I and II is the voltages on the input capacitors (V_1 - V_4). Therefore, a capacitor voltage balance control is proposed by alternating the two working modes to balance these four capacitor voltages V_1 - V_4. Fig. 5 shows the proposed control to balance the voltages among the four input capacitors, in which d_{rv1} - d_{rv4} are four driving signals of the power switches S_1 - S_4 and d_1 is duty cycle in one switching period. In the proposed capacitor voltage balance control, the working mode I is utilized for the first switching period and the working mode II is utilized for the second switching period, which can lead that the voltages on the four input capacitors are the same in every two switching periods.

Based on the volt-second principle, the voltages on the transformers T_{r1} and T_{r2} multiplied by the time periods in two switching periods can be expressed by (7) and (8) under the proposed control.

$$\underbrace{V_1\cdot[\frac{T_s}{2}+(\frac{1}{2}-d_1)\cdot T_s]}_{\text{First Switching Period}}+\underbrace{V_1\cdot d_1\cdot T_s}_{\text{Second Switching Period}}=\underbrace{V_2\cdot d_1\cdot T_s}_{\text{First Switching Period}}+\underbrace{V_2\cdot[\frac{T_s}{2}+(\frac{1}{2}-d_1)\cdot T_s]}_{\text{Second Switching Period}} \tag{7}$$

$$\underbrace{V_3\cdot d_1\cdot T_s}_{\text{First Switching Period}}+\underbrace{V_3\cdot[\frac{T_s}{2}+(\frac{1}{2}-d_1)\cdot T_s]}_{\text{Second Switching Period}}=\underbrace{V_4\cdot[\frac{T_s}{2}+(\frac{1}{2}-d_1)\cdot T_s]}_{\text{First Switching Period}}+\underbrace{V_4\cdot d_1\cdot T_s}_{\text{Second Switching Period}} \tag{8}$$

According to (7) and (8), it can be obtained

$$V_1 = V_2 \tag{9}$$

$$V_3 = V_4 \tag{10}$$

According to (1), (2) and (9), (10), it can be obtained

$$V_1 = V_2 = V_3 = V_4 = V_{in}/2 \tag{11}$$

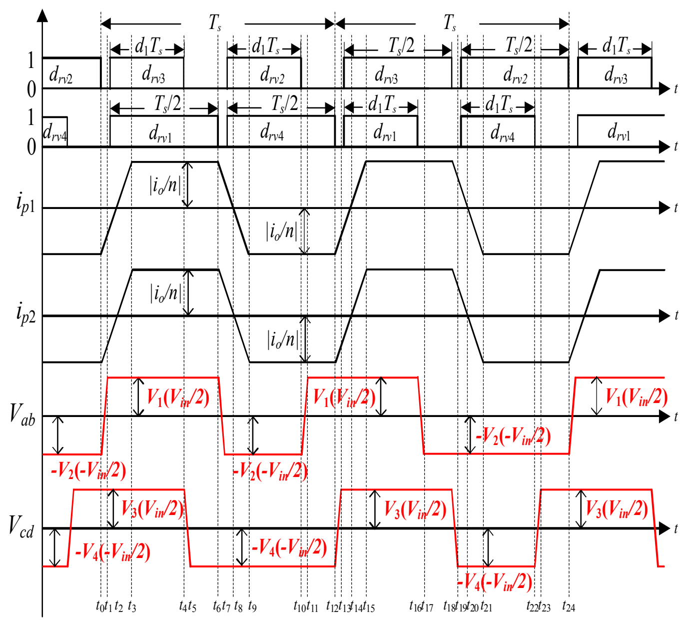


Fig. 5. Proposed capacitor voltage balance control.

IV. CHARACTERISTICS UNDER PROPOSED CONTROL STRATEGY

A. Output Characteristic

If neglecting the duty cycle loss, the average output voltage V_o is

$$V_o = \frac{1}{n}\cdot\left[\frac{V_1\cdot d_1 + V_2\cdot d_1 + V_3\cdot d_1 + V_4\cdot d_1}{2}\right] \tag{12}$$

Substituting (11) in (12), the average output voltage V_o is

$$V_o = \frac{V_{in}}{n}\cdot d_1 \tag{13}$$

Assume the leakage inductances of the two transformers T_{r1} and T_{r2} are the same, which are both L_r. The duty cycle loss namely d_{loss} in one switching period as shown in Fig. 5 ([t_0 - t_3] and [t_6 - t_9]) can be given by

$$d_{loss} = \frac{(t_3 - t_0) + (t_9 - t_6)}{T_s} = \frac{16\cdot L_r\cdot i_o}{n\cdot V_{in}\cdot T_s} \tag{14}$$

After considering the effect of the duty cycle loss, the output voltage V_o can be calculated by

$$V_o = \frac{V_{in}}{n}\cdot(d_1 - \frac{d_{loss}}{2}) = \frac{V_{in}}{n}\cdot(d_1 - \frac{8\cdot L_r\cdot i_o}{n\cdot V_{in}\cdot T_s}) \tag{15}$$

B. ZVS Achievement Conditions

Before discussing the ZVS achievement conditions under the proposed control strategy, one assumption is made that the parasitic capacitors of S_1 - S_4 (C_1 - C_4) are the same, which is named as C_p.

Under the working mode I, the energy E_1 calculated by (16) is needed to ensure the switches S_1 and S_4 achieving zero-voltage switch-on. The energy to realize the zero-voltage switch-on for S_1 and S_4 is provided by both the output filter inductance and the leakage inductance.

$$E_1 = \frac{1}{2}\cdot C_1\cdot(\frac{V_{in}}{2})^2 + \frac{1}{2}\cdot C_2\cdot(\frac{V_{in}}{2})^2 = \frac{1}{4}\cdot C_p\cdot V_{in}^2 \tag{16}$$

The energy of the leakage inductance of the transformer is utilized to achieve zero-voltage switch-on of switches S_2 and S_3. Therefore, in order to achieve the zero-voltage switch-on of switches S_2 and S_3, (17) should be satisfied.

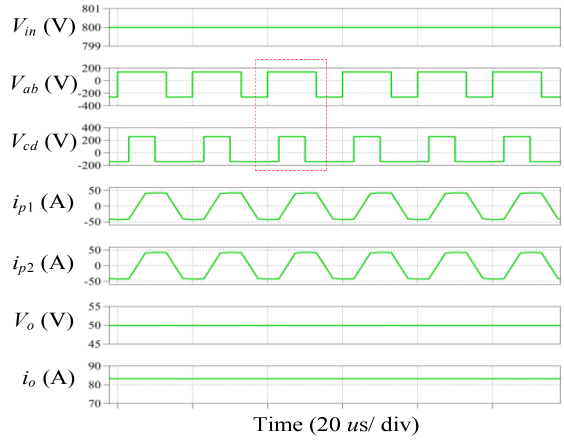
$$\frac{1}{2}\cdot L_r\cdot\left(\frac{i_o}{n}\right)^2 \geq \frac{1}{2}\cdot C_3\cdot(\frac{V_{in}}{2})^2 + \frac{1}{2}\cdot C_4\cdot(\frac{V_{in}}{2})^2 = \frac{1}{4}\cdot C_p\cdot V_{in}^2 \tag{17}$$

Under the working mode II, the analysis of the ZVS achievement conditions is similar to that under the working mode I as above, which is not repeated here.

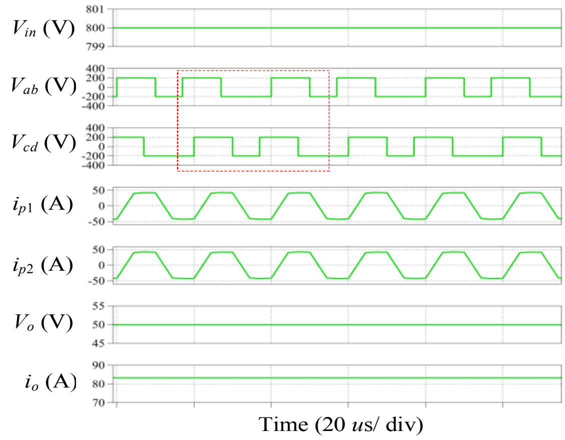
The proposed capacitor voltage balance control works by alternating the working mode I and II, so the ZVS achievement conditions of the proposed capacitor voltage balance control is the combination of the ZVS achievement conditions of the working mode I and II. As shown in Fig. 5, in the first switching period, the energy from both the output filter inductance and leakage inductance of the transformer is provided for S_3, S_4 to realize the zero-voltage switch-on and the energy from the leakage inductance is provided for S_1, S_2 to achieve the zero-voltage switch-on. In the second switching period, the ZVS achievement conditions are just contrary to that in the first switching period, which means the energy from both the output filter inductance and leakage inductance of the transformer is provided for S_1, S_2 to realize the zero-voltage switch-on and the energy from the leakage inductance is provided for S_3, S_4 to achieve the zero-voltage switch-on.

V. Simulation Verification

In order to verify the proposed control strategy, a simulation model is established in PLECS, whose circuit parameters are list in Appendix. In the simulation, the input voltage V_{in} is 800 V, the output voltage V_o is 50 V, and the output power namely P_o is 4.2 kW. The simulation results are presented in Fig. 6.



(a)

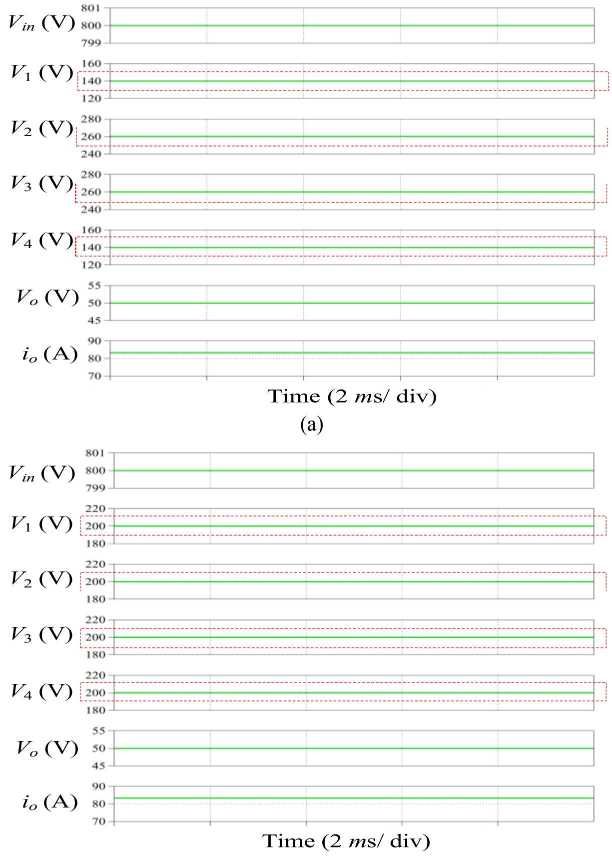


(b)

Fig. 6. Simulation results including V_{in}, V_{ab}, V_{cd}, V_o, i_{p1}, i_{p2}, and i_o when V_{in} = 800 V, V_o = 50 V, and P_o = 4.2 kW. (a) Conventional control strategy. (b) Proposed control strategy.

From Fig. 6, it can be observed that the primary currents i_{p1} and i_{p2} are the same under the conventional and proposed control strategy but the primary voltages V_{ab} and V_{cd} are different between the conventional control strategy and proposed control strategy as marked in Fig. 6.

Figs. 7(a) and (b) presents the four capacitor voltages V_1 - V_4 under the conventional and proposed control strategy respectively. From Fig. 7, it can be observed that: 1) under the conventional control strategy, the four capacitor voltages are unbalanced, in which the average value of V_1 and V_4 are both 140 V and the average value of V_2 and V_3 are both 260 V as marked in Fig. 7(a); 2) by utilizing the proposed capacitor voltage balance control, the four capacitor voltages become balanced, whose average values are all 200 V (V_{in}/4) as marked in Fig. 7(b); and 3) the simulation results are consistent with the above theoretical analysis.



(b)

Fig. 7. Simulation results including V_{in}, V_1, V_2, V_3, V_4, V_o, and i_o when V_{in} = 800 V, V_o = 50 V, and P_o = 4.2 kW. (a) Conventional control strategy. (b) Proposed control strategy.

Finally, based on the simulation results, it can be concluded that the proposed capacitor voltage balance control can effectively balance the voltages among the input capacitors, which can thus reduce the voltage stresses on the input capacitors in the dual half-bridge cascaded TL DC/DC converter.

VI. Conclusion

In this paper, a ZVS PWM strategy with a capacitor voltage balance control is proposed for the dual half-bridge cascaded TL DC/DC converter. The proposed ZVS PWM strategy is composed of two working modes, which can both realize the ZVS. More importantly, a capacitor voltage balance control is proposed by alternating the two working modes of the proposed ZVS PWM strategy to eliminate the voltage unbalance among the input capacitors. Consequently, the proposed control strategy can effectively reduce the switching losses and noises, reduce the voltage stresses on the input capacitors, and thus improve the performances of the converter. Finally, the simulation results validate the effectiveness of the proposed control strategy.

Appendix

TABLE I. PARAMETERS OF THE SIMULATION MODEL

Turns Ratio of Transformers T_{r1} and T_{r1}	2:1:1
Leakage Inductance of T_{r1} and T_{r1} (uH)	10.7
Magnetizing Inductance of T_{r1} and T_{r1} (uH)	2000
Input Capacitors C_{i1} - C_{i4} (uF)	470
Output Filter Capacitor C_o (uF)	470
Output Filter Inductors L_o (uH)	100
Switching Frequency (kHz)	50

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