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Published in:
Microelectronics Reliability

DOI (link to publication from Publisher):
10.1016/j.microrel.2018.07.144

Publication date:
2018

Document Version
Accepted author manuscript, peer reviewed version

Citation for published version (APA):
Reigosa, P. D., Iannuzzo, F., & Ceccarelli, L. (2018). Effect of short-circuit stress on the degradation of the SiO_2 dielectric in SiC power MOSFETs. *Microelectronics Reliability*, *88-90*, 577-583. https://doi.org/10.1016/j.microrel.2018.07.144

Effect of Short-Circuit Stress on the Degradation of the SiO_2 Dielectric in SiC power MOSFETs

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Abstract

This paper presents the impact of a short-circuit event on the gate reliability in planar SiC MOSFETs, which becomes more critical with increased junction temperature and higher bias voltages. The electrical waveforms indicate that a gate degradation mechanism takes place, showing a large gate leakage current that increases as the gate degrades more and more. A failure analysis has been performed on the degraded SiC MOSFET and then compared to the structure of a new device to identify possible defects/abnormalities. A Focused Ion Beam cut is performed showing a number of differences in comparison to the new device: (i) cracks between the poly-silicon gate and aluminium source, (ii) metal particles near the source contact, and (iii) alterations in the top surface of the aluminium source. The defects have been correlated with the increase in gate-leakage current and drain-leakage current.

I. Introduction

Silicon Carbide MOSFETs have evolved into a more mature technology and nowadays several manufacturers provide a wide variety of products at different voltage and current levels. SiC MOSFETs have an improved performance compared to silicon MOSFETs, especially for voltage classes above 600 V where the traditional silicon MOSFETs exhibit an on-state voltage drop that is too high for efficient operation [1]. However, the reliability of the SiC MOSFET needs to be further assessed [2], especially for applications requiring short-circuit proof devices such in the case of motor drive applications. Many efforts have been devoted to the short-circuit robustness testing of SiC MOSFETs under non-destructive operations; while some of them investigated the ageing of the device with a Repetitive Short Circuit testing approach [3]–[5], other identified degradation mechanisms with a stressful single short-circuit event [6]–[8].

A number of challenges have been found in SiC MOSFETs when they are tested under short-circuit conditions [9], mainly attributed to the gate-oxide reliability, namely (i) threshold voltage instabilities [10], [11] and (ii) gate-oxide breakdown [6]. The threshold voltage instabilities are associated to trapping and de-trapping of carriers, more likely to occur under high temperatures [12]. An increase in the net positive charge (i.e., hole trapping) will result in a negative shift of the threshold voltage, whereas an increase in the net negative charge (i.e., electron trapping) will result in a positive shift of the threshold voltage. The threshold voltage shift has been observed under normal turn-on/turn-off operations [12]–[14], but also under short circuit events [3].

In SiC MOSFETs, the most common failure mechanism seems to be the gate-oxide breakdown, as the experimental results in Fig. 1 demonstrate so. Two degradation mechanisms are typically observed: (1) gate-voltage reduction at the end of the short circuit pulse, for example, the short circuit waveforms in Fig. 1 when the device is tested up to 6 μs, and (2) permanent gate-voltage reduction, for example, the short

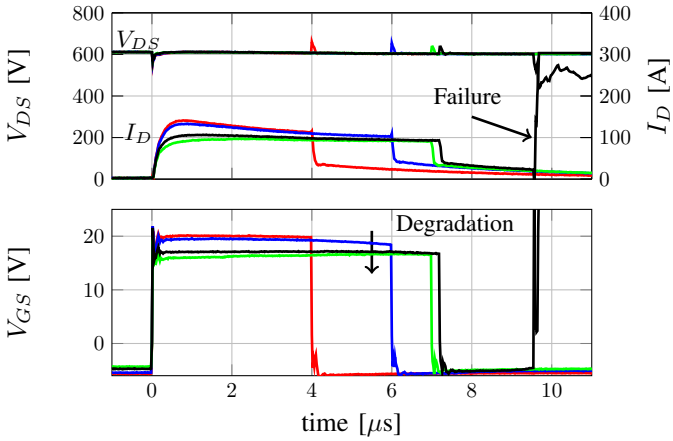


Fig. 1: Short-circuit tests with increasing time of a 1.2-kV/36-A SiC MOSFET: V_{DC} = 600 V T_j = 150°C.

circuit waveforms in Fig. 1 when the device is tested up to 7 μs. Therefore, it is worth to note that the failure indicator is the on-state gate-source voltage reduction due to the increase in the gate leakage current, which eventually causes a permanent gate damage and ends up in a gate-oxide breakdown failure. This failure mode has been attributed to the high temperature and high electric field withstood across the thin gate oxide [7], [15], [16], combined with the much higher defect density of SiC MOSFET structures (i.e., substrate defects, particles and metallic contaminations). Recently, it has been discussed that robust short-circuit devices can be designed if the thickness of the oxide is increased or the cell pitch is increased, while on the other hand, the on-state resistance becomes compromised leading to greater power losses [17], [18]. Despite of this trade-off curve, cracks across the thin gate-oxide have not been reported in the literature, as discussed in [19], therefore this assumption needs to be further validated.

The aim of this paper is to perform failure analysis on 1.2-kV planar SiC MOSFETs, which have been degraded under

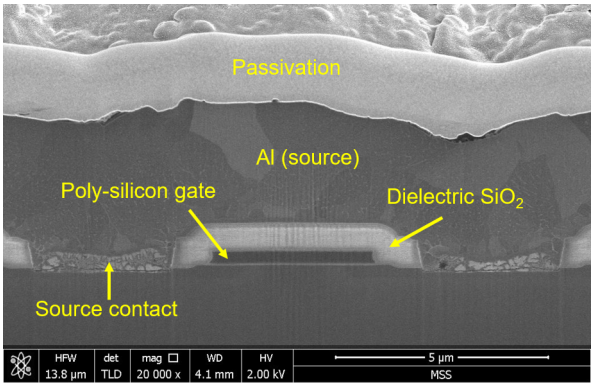


Fig. 2: Focused Ion Beam (FIB) cross section of the new 1.2-kV/90-A SiC MOSFET showing one cell.

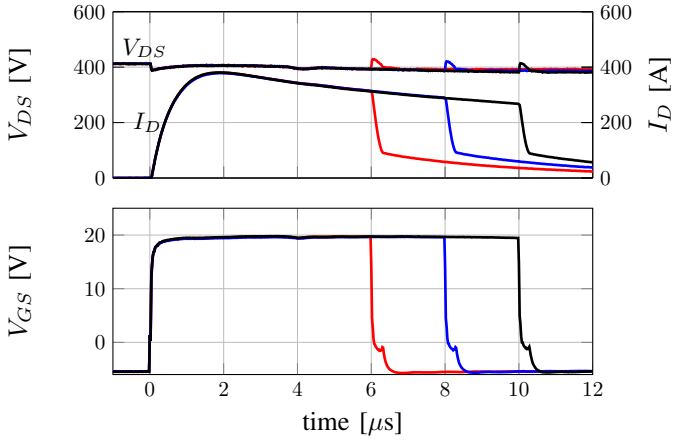


Fig. 3: Short-circuit tests with increasing time of a 1.2-kV/90-A SiC MOSFET: V_{DC} = 400 V T_j = 150°C.

single-stress short circuit operations at high temperatures and nominal voltage. The results will help to understand the root cause of the gate-oxide degradation mechanism by comparing a new device with a degraded one.

This paper is organized as follows: Section II presents the results from the experimental short-circuit tests at different DC-link voltages and initial junction temperatures. Section III and IV demonstrates the root cause of the observed gate-oxide breakdown failure through the failure analysis of the stressed SiC MOSFET, where the resistive paths increasing the gate and drain leakage current can be observed. Finally, concluding remarks are given.

II. Short-Circuit Experimental Results

A. The Device Under Test

The experimental investigations have been conducted on a commercial 1.2-kV/ 90-A SiC MOSFET having a TO-247 package and a planar technology (C2M0025120D). A Focused-Ion Beam (FIB) cut has been performed on the new SiC MOSFET first, which serves as a reference for later comparing the cell differences between the new and the degraded SiC MOSFET after applying the short circuit stress. The vertical cross section of the new device is presented in Fig. 2, where the gate structure of a single cell is observed. The cut has been performed on an arbitrary region of the device active area, showing no abnormalities or process defects.

B. Short Circuit Experiments at Low Bias Voltage

In this section, the waveforms of a typical short circuit test are presented at a low bias voltage of 400 V and at a high initial junction temperature of T_j = 150 °C. The experiments have been performed at V_{GS} = -5 V/ 20 V with a gate resistance of R_g= 10 Ω. The pulse duration has been increased until reaching 10 μs, which is the typical short-circuit withstanding time according to the industrial standard. Fig. 3 shows the drain voltage, drain current and gate-source voltage waveforms of the short circuit tests. The drain current peak is 380 A and then decreases according to the junction temperature increase, which is a well-known phenomenon related to the negative thermal coefficient of MOSFETs. The results at low bias voltage and high temperature do not show any degradation on the gate voltage, and therefore, it can be concluded that the SiC MOSFET is able to survive this condition.

C. Effect of Initial Junction Temperature under a Short Circuit Event

Fig. 4 shows the short-circuit voltage and current waveforms of the 1.2-kV/ 90-A SiC MOSFET for a bias voltage of 600 V and initial junction temperature T_j = 25°C. Furthermore, Fig. 5 shows the same waveforms for a bias voltage of 600 V and T_j = 150°C. In this work it has been assumed a 600 V application to be the nominal. The results at high temperature and nominal voltage show a significant reduction of the gate-source voltage V_{GS}, while the results at room temperature do not show such a degradation. In Fig. 5, the V_{GS} reduces from 19.7 V to 18.7 V while the short circuit pulse has been increased from 3 μs to 4 μs. This leads to a ΔV_{GS} = 1 V, which means that the gate current increases 100 mA (R_g = 10 Ω). The gate leakage current for a fresh device is in the nA-level, and then gradually increases with the short circuit pulse duration up to 100 mA, which is considered as the critical point. The gate leakage current now flows through a new path between gate and source, which demonstrates that the gate electrode is no longer isolated.

After the last test, the damage on the gate side is permanent but the device is still able to turn-on/turn-off. With the aim of performing a physical structural analysis of the device, the short-circuit experiments are stopped before observing a gate breakdown failure, as pointed out in Fig. 1. Thanks to the physical analysis, the assumption that a new resistive path has been originated will be validated.

Finally, it is also worth to note that the gate voltage shows a voltage decay with increasing short circuit pulses. In Fig. 4, the V_{GS} reduces from 19.8 V to 19.4 V when the applied short circuit pulse is increased from 3 μs to 5.5 μs at T_j = 25°C. This leads to a ΔV_{GS} = 0.36 V, which means that the gate leakage current is only 36 mA, and therefore, the device

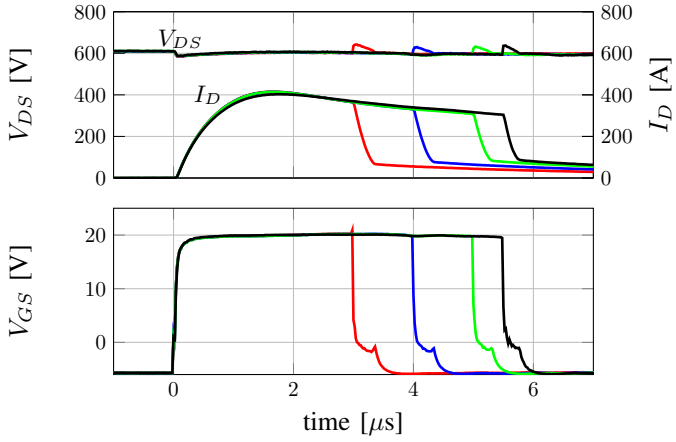


Fig. 4: Short-circuit tests with increasing time of a 1.2-kV/90-A SiC MOSFET: V_{DC} = 600 V T_j = 25°C.

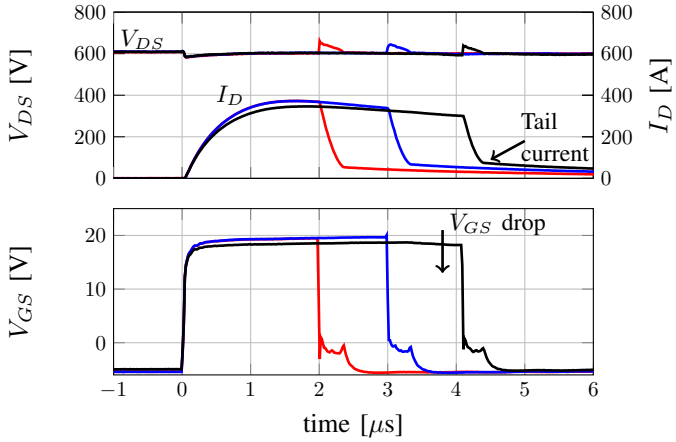


Fig. 5: Short-circuit tests with increasing time of a 1.2-kV/90-A SiC MOSFET: V_{DC} = 600 V T_j = 150°C.

is not permanently degraded as in the previous case when the short circuit test was performed at higher temperature (T_j = 150°C).

D. Short-Circuit Energy Calculation

The calculated short-circuit energies from the short circuit current and drain-source voltage waveforms have been plotted in Fig. 6. The short-circuit energy causing a permanent damage on the SiC MOSFET is 0.8 J, which can be considered as the critical energy when the device is tested at T_j = 150 °C and V_{DC} = 600 V. Furthermore, the calculated short-circuit energy for a bias voltage of 600 V and T_j = 25 °C is about 1.14 J, which is above the one that lead to a permanent degradation in the previous case. The calculated short-circuit energies when the device is tested under a bias voltage of 400 V and T_j = 150 °C show that the value is also above the one leading to the permanent damage of the device, even though the initial junciton temperature was the same (T_j = 150 °C). These results prove that in planar SiC MOSFETs, the gate reliability is not only related to the critical energy, but bias voltage plays a significant role, too.

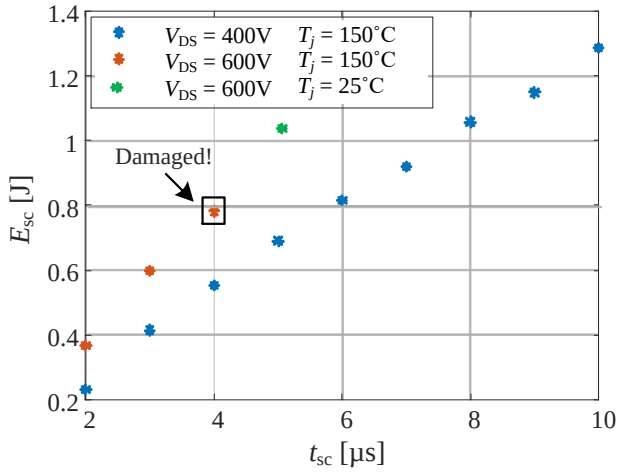


Fig. 6: Calculated short-circuit energy for two bias voltage (V_{DC} = 400 V and 600 V) and initial junction temperatures (T_j = 25 °C and 150 °C).

III. Failure Analysis of the SiC Gate-Oxide

A. Infra-red camera hot spot localization

After the last short circuit test under bias voltage of 600 V and initial junction temperature T_j = 150°C, where we have observed a clear damage on the gate side (Fig. 5), a physical failure analysis on the 1.2-kV/ 90-A SiC MOSFET has been performed. First, the package material has been removed by high-temperature etching, and then, an Indium Gallium Arsenide (InGaAs) infra-red camera has been used to find possible hot spots. The principle is to apply a voltage on the drain terminal and connect the gate and the source terminals to ground. If the SiC MOSFET has a damage, a leakage current will appear from drain to source or drain to gate, which can be detected with a very sensitive infra-red camera. The results can be observed in Fig. 7, where a hot spot in the device active area is revealed. The location of the hot-spot is highlighted in Fig. 7.

B. Focused-Ion Beam Analysis

A Focused Ion Beam (FIB) micro-section at the hot spot location is applied to find possible damages on the gate oxide. Fig. 8 reveals the image of the FIB cut, where the vertical structure corresponding to three cells is observed. It is worth to note that one of the cells appears to be cracked, therefore, this particular cell is further magnified in Fig. 9. It is interesting to compare the image between the new (Fig. 2) and the degraded SiC MOSFET (Fig. 9), which proves that three major degradations have been found:

1) A crack in the dielectric between the poly-silicon gate and the aluminium source.
2) Metal particles accumulated near the source contact (salicide).

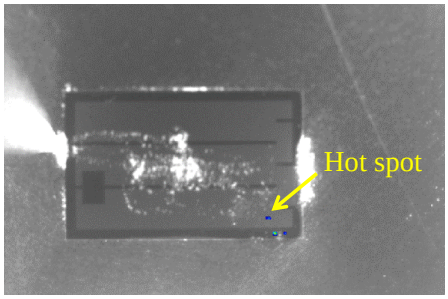


Fig. 7: InGaAs infra-red image of the degraded 1.2-kV/ 90-A SiC MOSFET under short circuit.

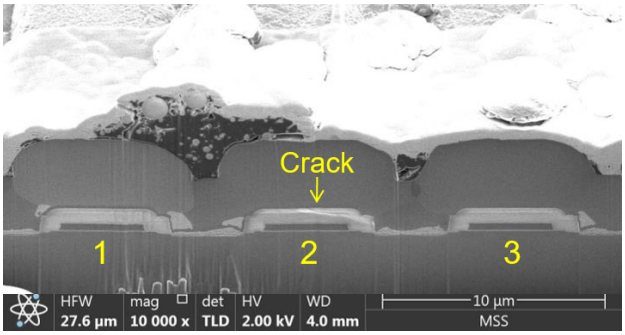


Fig. 8: Focused Ion Beam (FIB) cross-section of three cells at the hot spot location, where one of the cells presents a crack.

3) Alterations in the top surface of the aluminium source.

Each of the three degradations are analysed in more detail in the following. First, the cracks found in the degraded device between the poly-silicon gate and the aluminium source cannot be found for the new device, which proves that have been

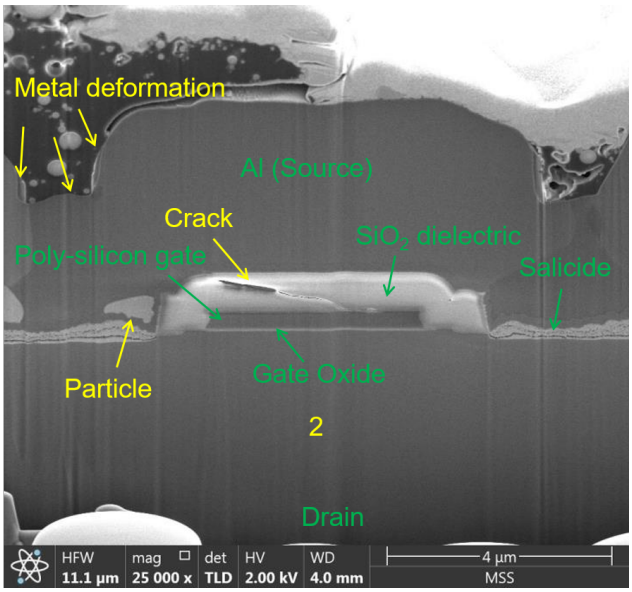


Fig. 9: Magnified Focused Ion Beam (FIB) cross-section of the damaged cell.

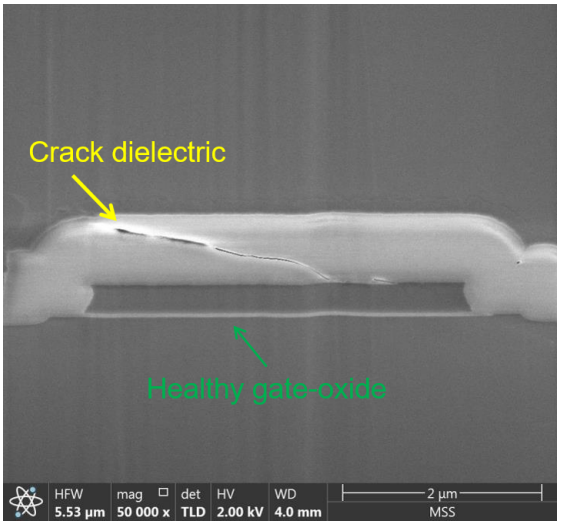


Fig. 10: Image of the gate-oxide region.

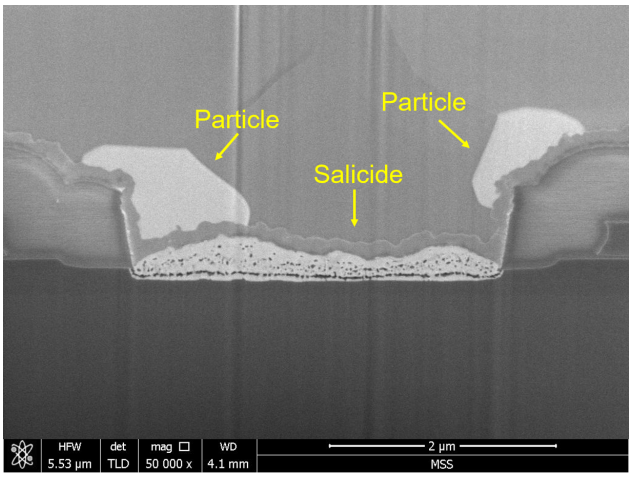


Fig. 11: Magnified Focused Ion Beam (FIB) of the salicide region of the degraded SiC MOSFET.

formed after the short circuit stress. Furthermore, Fig. 10 shows a magnified image where the gate-oxide layer appears to be intact in this cell. This observation demonstrates that the high electric field and high temperature sustained across the thin gate-oxide was not the root cause of the gate damage. A more in-depth analysis has been performed on adjacent cells, showing that not only one cell but several ones have cracks on the inter-level dielectric (between poly-silicon gate and aluminium source).

The salicide which is the technology that is used to form the electrical contact between the semiconductor substrate and the source terminal appears to be severely degraded, which can be observed in Fig. 11. First, the source contact thickness is not homogeneous and second, particles can be observed near the salicide which are not seen for the new device. This indicates that they could have originated as a consequence of the short-circuit stress and not from device process defects. Although a material analysis has not been performed on the particle itself,

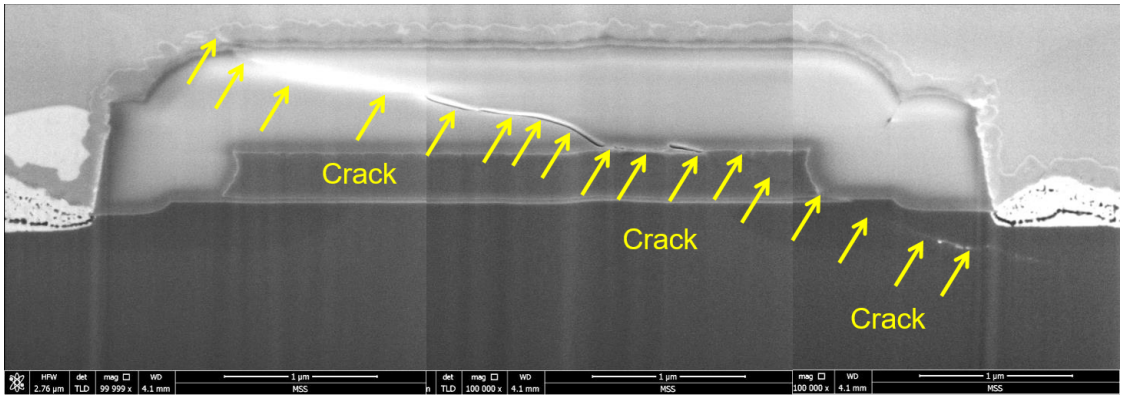


Fig. 12: Focused Ion Beam (FIB) microsection showing a crack between the source metallization and the SiC substrate.

it can be said that the material must be a metal because of the image light color.

Finally, the shape of the interface between the upper aluminium source and the passivation layer shows a significant degradation when compared with the new device, since this layer appears to be deformed. From these results, we can conclude that the temperature reached during short circuit provokes the deformation of the cells. This effect could lead to the formation of cracks in the inter-level dielectric, large enough to deteriorate the gate structure and destroy the device.

IV. Analysis of Degraded SiC MOSFETs in Previous Literature

The following structural analyses of degraded SiC MOSFET cells have been collected from previous research in the literature. The SiC MOSFETs have been stressed until a sign of degradation is observed and then post-failure analysis is performed with special focus on the gate structure. The image of the SiC MOSFET structure in Fig. 13a [20] confirms that the dielectric around the poly-silicon gate has cracked, in a similar way as the results presented in this work. Some of these cracks show signs of metal diffusion, however the root cause of these cracks is still not well understood. The health of the gate oxide has not been assessed in [20], on the other hand, the results presented in our work prove that the gate oxide is intact and no defects have been found. Furthermore, the image found in Fig. 13b [21] shows cracks in the poly-silicon gate for a degraded SiC MOSFET under accelerated aging tests, however the dielectric around the poly-silicon gate seems to be intact. Finally, the results in Fig. 13c [4] detected by using a Photon Emission Microscope (PEM), confirms a structural defect on the poly-silicon gate after the short circuit aging. Overall, it seems that the SiC MOSFET is prone to gate-oxide breakdown failures either related to cracks in the dielectric around the poly-silicon gate, the poly-silicon gate itself or defects in the gate structure. Nevertheless, the particles near the source contact that have been found in our work have never been reported before.

V. Failure Analysis of the SiC Substrate

A. IV Characterization

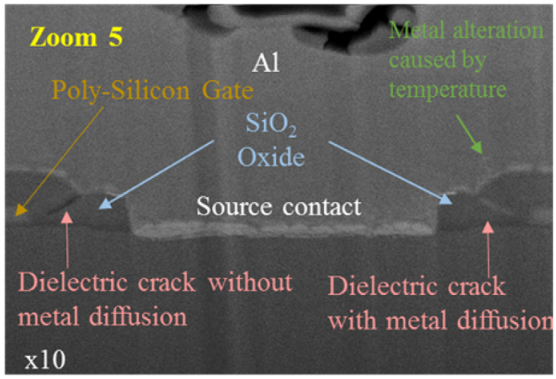
The degradation of the 1.2-kV/ 90-A SiC MOSFET has been attributed to the change in gate leakage current and gate damage due to the formation of cracks in the SiO_2 dielectric. Nevertheless, it is worth to discuss that the drain leakage current significantly increases between the fresh and the damaged device, as observed in Fig. 14, where the typical $I-V$ curve is presented. The aim is now to find out through the physical inspection of the device, whether there are further cracks or defects that allow the drain leakage current to flow from drain to source through a new path.

B. Focused-Ion Beam Analysis

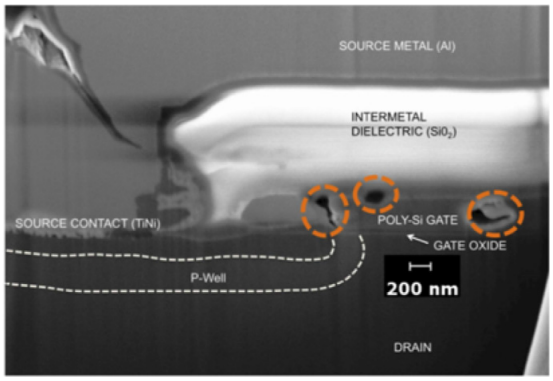
The damaged SiC MOSFET die has been further analysed with the aim of finding defects that could explain the drain leakage current increase. A FIB micro-section has been performed at different locations in the vicinity of the hot spot. In Fig. 12, it can be recognized that the crack between the poly-silicon gate and the aluminum source has propagated towards the SiC substrate through the poly-silicon gate and gate-oxide probably in the third dimension and therefore not clearly visible in Fig. 12. This crack allows for a conductive path between the drain and source generating a drain leakage increase consequently.

VI. Conclusions

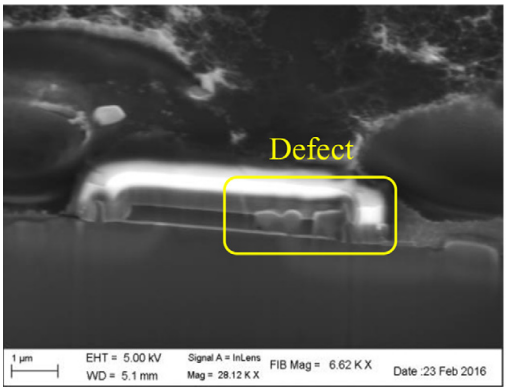
This paper provides a better understanding of the physical root cause of the permanent gate-leakage current and drain-leakage current after a few non-destructive short circuit tests. The SiC MOSFET is tested until an obvious degradation is observed, for example V_{GS} reduction, but keeping the device operational to perform post-failure analysis and allowing for the visual inspection of the die. It has been found that the gate reliability is compromised by the combination of high junction temperature and high bias voltage. More in particular, it has been observed that in planar SiC MOSFETs, the gate reliability is not only related to the critical energy, but bias voltage plays a significant role.



(a) Scanning Electron Microscope (SEM) image showing cracks in the dielectric around the poly-silicon gate electrode of a 1.2 kV/ 36 A SiC MOSFET [20].



(b) SEM image showing defects in the poly-silicon gate electrode of a 1.2 kV SiC MOSFET [21].



(c) SEM image of the degraded 1.2 kV/ 24 A SiC MOSFET cell showing defects in the poly-silicon gate electrode [4].

Fig. 13: Structural analysis of 1.2-kV SiC MOSFETs from previous research in the literature.

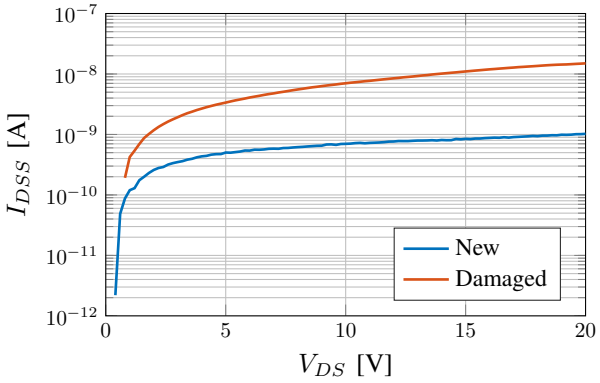


Fig. 14: Short-circuit tests with increasing time of a new and a degraded 1.2-kV/90-A SiC MOSFET: V_{DC} = 600 V T_j = 150°C.

The Focused-Ion Beam (FIB) micro-sections and Scanning Electronic Microscopy (SEM) images on the degraded SiC MOSFET show three major degradations: (1) a crack between the poly-silicon gate and the source metallization, which explains the gate-leakage current increase, (2) the presence of silicide particles near the salicide and at the corners of the SiO_2 dielectric, which are not observed for the fresh SiC MOSFET and (3) alterations on the aluminium source above the oxide and under the passivation layer that are not visible for the fresh device. Additionally, it has been found that one of the cracks in the inter-level dielectric propagates down to the drain the the third dimension, which could be the cause of the drain-leakage current increase.

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