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Performance Analysis of a Single-phase GaN-based 3L-ANPC Inverter for Photovoltaic Applications

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***Abstract*—Nowadays, the power electronics converter design is challenged with a request of high efficiency a nd compactness for various applications. To tackle this, the research community and the industry have almost fully exploited the Silicon technology, leading to the development of new power transistors. The Gallium-Nitride (GaN) HEMTs can be promising power devices to replace the traditional power devices. Therefore, the performances of converters based on such a technology should be assessed to validate the effectiveness in terms of efficiency and compactness. Moreover, among the available converter topologies , the performance of the three-level Neutral Point Clamped (NPC) family can be enhanced with the GaN HEMTs. In light of the above, in this paper, the performance of a GaN-based three-level Active NPC (3L-ANPC) converter is assessed in terms of power losses, volume impact of passive components, and output distortions. Simulations and experiments have been performed.**

I. Introduction

Wide-Band Gap (WBG) devices can be the future alternative to Silicon (Si) transistors. The Silicon Carbide (SiC) and Gallium Nitride (GaN) WBG devices, are the most promising solution to overcome today's challenges in power electronic converters. The key features that can be achieved using the WBG devices are: 1) increased switching frequency with low power losses and 2) operation at higher junction temperature. In particularly, the GaN has a high electric field w hich means that the volume of the transistor can be greatly reduced, when compared to Si and SiC.

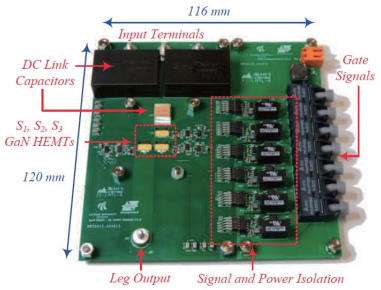
In case of low voltage applications, such as residential photovoltaic (PV) systems, the best candidates are the GaN HEMTs in term of power density. So far, such devices have been introduced on the market by Panasonic and GaN Systems with a maximum blocking voltage of 600 V and 650 V, respectively. For grid-connected application, the required DC-link voltage should be above $650\ V$ in order to connect to the $230\ V_{ph_RMS}$ three-phase grid. Thus, for grid-connected systems, this would lead the transistors to operate at the boundaries of the Safe Operating Area (SOA). To overcome this issue, a solution might be the connection of two transistors in series and, in two-level single-phase converters, it will imply the use of eight switches in full-bridge configuration, increasing the overall cost and complexity of the gate drivers. Another solution is the use of multi-level converters. The most widespread multi-level topology in PV applications is the three-level NPC, which requires only six switches and allows to halve the voltage across the devices. However, this topology has poor stress distribution among the transistors. To overcome the limitation, the diodes are replaced by transistors, being the 3L-ANPC configuration. In addition to the halved drain-source voltage, the three-level inverter allows to reduce the filter size as well. This is possibly due to the multi-level output voltage, reducing the output distortions and consequently the inductor size. Additionally, if a proper modulation technique is used, the isolation transformer can be removed, further contributing to a size reduction of the overall converter [1].

TABLE I
Nominal parameters of the considered inverter.

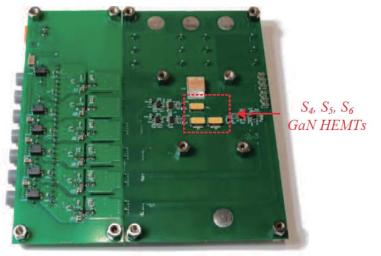
$P_{out,max}$	$5\ kW$
V_{DC}	$700\ V$
V_{line}	$230\ V_{RMS}$
f_{line}	$50\ Hz$
f_{sw}	$50\ kHz$ to $200\ kHz$

Combining the performances of the GaN HEMT with the benefits of the 3L-ANPC, Gurpinar *et al* have proposed a GaN-based 3L-ANPC converter. The proposed solution is a $5\ kW$ single-phase system for PV applications, with a DC-link voltage of $700\ V$. In [2], an ultra-low inductance commutation loop has been proposed along with a validation of the outstanding switching performances. However, there is a need to estimate and validate the performances of such a converter. Therefore, in this paper, the performances in terms of thermal stress, efficiency, and overall volume are presented. This work presented in this paper has been done on the hardware design in [2], as shown in Fig. 1. The nominal parameters are summarized in Table. I.

The rest of the paper is composed as follows. Section II presents the analysis and the design of the converter. In Section III, the hardware system proposed in [2] is described and the proposed modification is highlighted. Simulations and experimental tests are provided to assess the inverter, and the results are shown in Section IV, before the conclusion.



(a)



(b)

Fig. 1. Photos of the 3L-ANPC converter: *(a)* the top-side view and *(b)* bottom-side [2].

II. Topology Analysis and Design

A. 3L-ANPC Converter

The 3L-ANPC belongs to the half-bridge family of multi-level converters and it is shown in Fig. 2. It consists of six switches, which allow to generate three voltage level: positive (P), neutral (O), and negative (N). The current paths for each state depends on the modulation technique. In this paper, the modulation proposed in [3] is used, which features two neutral states with two different current paths, respectively. The positive state is generated by the connection in series of S_1 and S_3, which are carrying the output current, while S_4 is commutated in order to guarantee that the voltage across the low-side switches S_5 and S_6 is kept as $\frac{V_{DC}}{2}$. In a similar manner, the negative state is generated by commutating S_4 and S_6, S_5 is kept on and S_2 is commutated to keep the voltage across the upper switches as half of the DC-link voltage. Regarding the neutral state, two possible configuration are available, depending on which state precedes the neutral one. In both cases, the current is split between S_2 and S_3 in the upper neutral state, or between S_4 and S_5 in the lower neutral state. This particular connection allows to split the conduction losses between these branches, improving the conduction losses during the neutral states.

B. DC-link Capacitors Design

As known, the power pulsation leads to voltage oscillations on the DC-link of the inverters. To address this issue, a DC-link buffer is necessary to keep the voltage within the boundaries, usually $\pm 5\%$ as a rule of thumb. In the 3L-ANPC inverter, the DC-link buffer is composed of two capacitors.

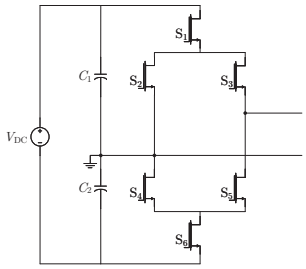


Fig. 2. Single-phase leg of a 3L-ANPC inverter.

Following the procedure described in [4], the DC-link capacitor value can be calculated. Assuming that the converter losses are negligible, the input power should be balanced as

$$p_{in}(t) = p_{out}(t) = \frac{\widehat{V}\widehat{I}}{2} + \frac{\widehat{V}\widehat{I}}{2} \cdot cos(2\omega t) = P + Pcos(2\omega t) \tag{1}$$

where $\widehat{V}$ and $\widehat{I}$ are the peaks of the output voltage and current, respectively, and $\omega = 2\pi f$ is the grid voltage angular frequency with f being the fundamental frequency. Given that the DC power is provided by the DC supply, the power that needs to be provided by the capacitors is expressed as $Pcos(2\omega t)$, which is related to the energy stored in the capacitor $\frac{1}{2}C_{dc}\frac{d(v_c(t)^2)}{dt}$. Accordingly, the capacitance can be approximated as

$$C_{dc} = \frac{\widehat{I}V_{dc}}{4V_{pp}^2\omega} \cdot [1 - cos^2(2\pi\omega)] \tag{2}$$

where V_{pp} is the peak-to-peak voltage on the DC-link and V_{dc} is the nominal DC-link voltage. From Eq. 2, it can concluded that the capacitance depends on the output power. Therefore, using the nominal parameters given in Table I, the capacitance value is $5\ mF$ with an RMS current of $7.5\ A$. Since the CeraLink capacitors shown in Fig. 1(a) have a total capacitance of $21\ \mu F$, an additional capacitor bank is needed. For such a capacitor, the electrolytic technology is the most compact [5]. To have an indication about the capacitance size and characteristic, the EPCOS B43513 has been selected. Moreover, a bank of five $1 - mF$ capacitors is considered, reducing the total Equivalent Series Resistance (ESR) to 20 $m\Omega$ and the Equivalent Series Inductance (ESL) $4\ nH$. The latter is relatively important in high $\frac{di}{dt}$ applications, since a high ESL would introduce unwanted voltage spikes, which can potentially damage the devices. Considering that two banks of this kind are necessary in the 3L-ANPC topology, the overall volume is $1000\ cm^3$.

C. Output Filter

Since the switching frequency of this GaN-based converter is expected to be high enough to reach a low Total Harmonic Distortion level, a second-order filter is designed. Indeed, an LC filter is sufficient to filter-out the switching-frequency harmonics. A step-by-step procedure proposed in [6] is used

to calculate the converter side inductance and the filter capacitance. The inductance is calculated as

$$L_f = \frac{V_{DC}}{8 \cdot f_{sw} \cdot \Delta i} \tag{3}$$

where V_{DC} is the full DC-link voltage, f_{sw} is the switching frequency, and Δi is the current ripple, e.g. 20% of the nominal output current. Regarding the capacitance, it is dependent on the converter-side inductance L_1 and the harmonic attenuation capability as:

$$C_f = \frac{1}{(2\pi \cdot f_{sw})^2 \cdot L_f \cdot k_{att}} \tag{4}$$

where k_{att} is set as 0.01 in order to provide an adequate damping of the resonance frequency magnitude peak and to ensure that the switching frequency and the resonance one do not coincide.

Obviously, the output filter has a great dependency on the switching frequency. Thus, beyond the interest in varying the switching frequency, the output filter has been calculated for the frequency range considered in this paper. The inductance volume has been calculated considering:

$$Vol_L = k_L \cdot A_p^{\frac{3}{4}} \tag{5}$$

where k_L is the volume constant and A_p is the area-product, given as [7]

$$A_p = \left[\frac{\sqrt{1+\gamma} \cdot K_i \cdot L_f \cdot \widehat{I^2}}{B_{max} \cdot K_t \cdot \sqrt{k_u \Delta T}} \right]^{\frac{8}{7}} \tag{6}$$

in which γ is the ratio between the core and the copper losses, which is usually zero if the flux ripple is negligible. Furthermore, B_{max} is the maximum flux density, $\widehat{I^2}$ is the square of the peak current, L_f is the inductance, and ΔT is the temperature rise in the windings. All the constants are given in Table II. Regarding B_{max}, it can be approximated as [6]

$$B_{max} = |1.111 \cdot 10^4 \cdot f_{sw}^{-0.3104} - 132.3| \cdot 10^{-3} \tag{7}$$

which is valid for switching frequencies between 25 and 200 kHz.

Regarding the capacitance value, its value can be calculated using the following:

$$Vol_C = k_c \cdot C_f \cdot V_{nom}^2 \tag{8}$$

where C_f is the calculated capacitance according to 4, V_{nom} is the nominal voltage, and k_c is the capacitor volume constant, which is extracted from data-sheets. For line filter applications, the most suitable capacitors are the X capacitors. As suggested in [6], the EPCOS MKP339-X2 series is the one with a low k_c of 60.

With the calculated LC filter elements by varying the switching frequency, the overall volume is calculated, as shown in 3. Additionally, it is worth mentioning that the capacitance impact on the overall volume is small when compared to the volume occupied by the inductor. This means that with an irrelevant increase in the volume, the filtering performances can be significantly increased compared with a simple L filter.

TABLE II
CONSTANTS USED TO CALCULATE THE AREA-PRODUCT OF AN INDUCTOR.

γ	K_i	K_t	k_u	$\Delta T\ [^\circ C]$
0.03	$\sqrt{2}$	$48.2 \cdot 10^3$	0.8	60

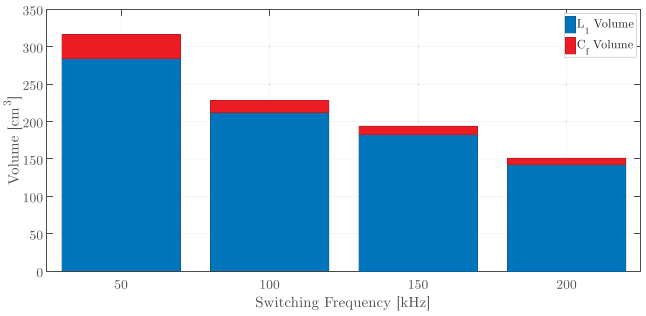


Fig. 3. Comparison of total volume and the capacitance impact with switching frequencies considered for single-phase systems.

D. Cooling System

For the power converter, a cooling system is needed to enhance its performance. In fact, because of the relevant conduction losses, the junction temperature will reach above 150 °C. Additionally, the reason for keeping the junction temperature is twofold. Firstly, the higher the junction temperature is, the higher is the on-state resistance, leading to higher conduction losses. Secondly, according to the Coffin-Manson law, the number of cycles to failure is inversely proportional to the mean junction temperature. Therefore, a high mean junction temperature leads to a premature failure of the switching devices.

The required thermal resistance can be calculated with the total transistor losses and the desired junction temperature. The former is calculated according to the GaN GS66508T data-sheet and the LTSpice model provided by GaN System, while the junction temperature is set as 80 °C, in order to limit the stress on the device. According to the equivalent thermal circuit shown in Fig. 4, the total thermal resistance can be calculated as

$$R_h = \frac{T_c - T_a}{P_{loss}} \tag{9}$$

where T_c is the desired case temperature, T_a is the ambient temperature, and P_{loss} is the total power loss that needs to be dissipated by the heat-sink.

When the required thermal resistance is obtained, the volume in cm^3 of a naturally cooled heat-sink can be calculated approximately as [6]

$$Vol_{hs} = 286.71 \cdot R_{th}^{-1.468} \tag{10}$$

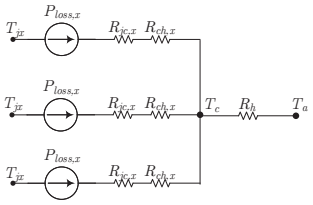


Fig. 4. Equivalent thermal circuit for one heat-sink. The subscript x indicates the number of the power switch.

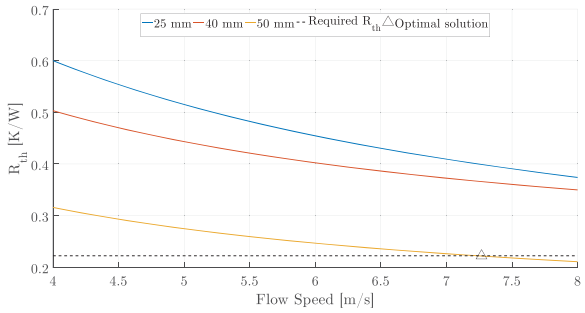


Fig. 5. Selection of the heat-sink height and the fan. The solid lines indicates the curves thermal resistance vs. the flow speed, while the dashed line represents the minimum thermal resistance required for $P_{out} = 5\ kW$.

Notably, the volume of the cooling system can be reduced by means of the forced convection, which can additionally improve the cooling performance. In order to select the proper combination of heat-sink and fan, a market survey has been done. The heat-sink is selected with a base area of $50 \times 50\ mm$ and three different heights: 25, 40, and 50 mm. The thermal resistance variation when changing the air speed is plotted in Fig. 5. Regarding the fan, different models have been selected. Additionally, in this case, different heights have been selected: 10, 15, and 28 mm. By comparing the fan characteristics and the thermal performance of the combination of them with the heat-sink, the feasible solution for the power of 5 kW is the combination of a $50-mm$ heat-sink with a $28-mm$ fan and a flow rate of 54 $\frac{m^3}{h}$. When comparing the proposed forced convection solution with the naturally cooled method, there is a reduction in the overall cooling system of 30% (in height), suggesting the forced one as the best.

Regarding the overall volume occupied by the passive components, the obtained results are summarized in Fig. 6. As can be seen in Fig. 6, the most cumbersome element is the DC-link capacitive buffer, while varying the switching frequency, the volume of the output filter can be halved. In respect to the cooling system, its volume is not varying with the variation of the switching frequency, due to the slight contribution of the switching losses on the overall power devices.

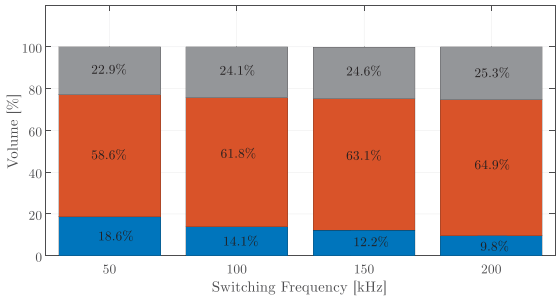


Fig. 6. Overall volume comparison under different switching frequencies. The grey bars indicated the volume occupied by the heatsink, the orange the one occupied by the DC-link capacitors and the blue is the output filter.

III. Hardware Description

As discussed, the converter in this paper is based on the $650-V$ GaN HEMT from GaN System Inc., which features a maximum drain current of 30 A allowing this converter to deliver the power 5 kW per phase. According to the device parameters listed in Table III, the suggested gate-source voltage at the on-state is 6 V, while the threshold one is less than 2 V. Thus, the gate driver should be carefully designed, to avoid any unwanted ringing that may turn-on involuntarily the devices. The gate driver design proposed in [2], in addition to an ultra-low commutation loop inductance, features an unipolar gate-driver with an improved false turn-on capability.

Furthermore, in [2], the cross-talking issue has been discussed through the common-mode current analysis. It has been identify that the capacitive coupling between the overlapped gate-driver ground planes is the main origin of common-mode currents. In this paper, the layer stack has thus been increased with respect to the one used previously in [2], reducing the coupling capacitance and thus improving the cross-talking immunity of the converter. It is worth mentioning that in the provided design, the isolated DC/DC converters the gate driver show a fairly high coupling capacitance which makes the common-mode current flowing from the isolated to the non-isolated side of the gate driver circuitry easily. On the other hand, solutions should be developed with a lower capacitance, improving the decoupling between the non-isolated and the isolated side.

Regarding the commutation loop inductance, a four-layer PCB arrangement with CeraLink capacitors and the GaN HEMTs, allows reducing the loop inductance. The overall PCB arrangement, as shown in Fig. 7, introduces two different commutation loops: 1) the positive state as shown in Fig. 8(a) and 2) the upper negative state as shown in Fig. 8(b). In [8], a new and more accurate method to calculate the commutation loop inductance was proposed. The total loop inductance can be calculated as

$$L_\sigma = \mu_0 \frac{e}{w} l \left(\frac{1}{1 + \frac{e}{w}} + 0.024 \right) \tag{11}$$

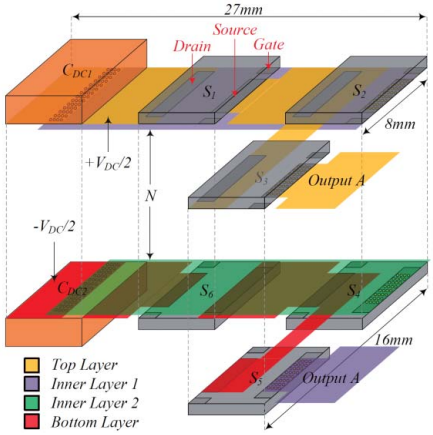


Fig. 7. PCB arrangement of the GaN HEMT and the decoupling capacitors [2].

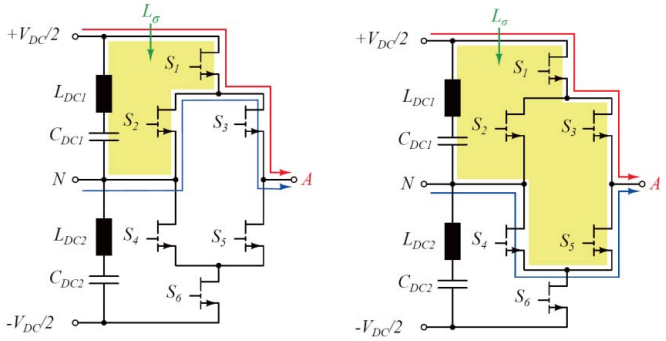
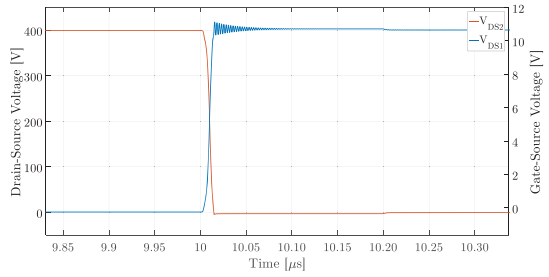
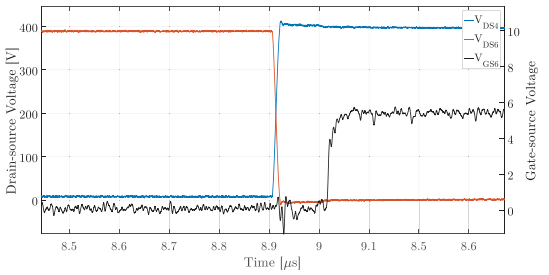


Fig. 8. Two commutation loops: *(a)* from positive to upper neutral state and *(b)* from positive to lower neutral state [2].

where μ_0 is the free space permeability, l and w are length and width, respectively, and e is the distance between the two copper traces. By applying (11) to the commutation paths in Fig. 8, the loop inductance can be calculated. Additionally, the contributions of the CeraLink capacitor ESL ($2.5\ nH$) and the stray inductance of the GaN HEMTs ($0.4\ nH$ each) are included in the calculation, which leads to $3.8\ nH$ for the path of Fig. 8(a) and $6.41\ nH$ for the path of Fig. 8(b). Compared to the values presented in [2] there are small deviations, but the good switching performances are preserved. With the calculated values, a simulation model has been built up in LTspice, for further analysis of the converter behaviour. In Fig. 9(a), a step change from 0 to $400\ V$ has been simulated, with a rise time of $10.3\ ns$ and an overshoot in the drain-source voltage of $18.5\ V$. The ringing present on the peak is due to the resonant tank that is created between the stray inductance and the low capacitance C_{oss} of the GaN HEMT. The frequency of such ringing is around $400\ MHz$, and therefore, it is not expected to be seen in experiments, as shown in Fig. 9(b).



(a)



(b)

Fig. 9. Result of the switching test in the DC/DC operation: *(a)* from the LTSpice model and *(b)* from the experimental setup.

TABLE III
GS66508T GAN HEMT PARAMETERS.

Drain-Source Voltage (V_{DS})	$650\ V$
Continuous Drain Current (I_{DS})	$30\ A$ @ $100°C$
Drain-Source On-State Resistance ($R_{DS,on}$)	$55\ m\Omega$ @ $25°C$ $129\ m\Omega$ @ $100°C$
Input Capacitance (C_{ISS})	$260\ pF$
Output Capacitance (C_{OSS})	$65\ pF$
Reverse Transfer (C_{RSS})	$2\ pF$
Gate Charge (Q_G)	$5.8\ nC$
Min. Gate Threshold Voltage (V_{th})	$1.7\ V$
Gate-Source Voltage (V_{GS})	$-10\ to +7\ V$
Maximum Junction Temperature (T_j)	$150C$
Reverse Recovery Charge (Q_{RR})	$0\ nC$
Package Stray Inductance (L_σ)	$0.4\ nH$
Device Package	GaN_{PX}

IV. PERFORMANCE EVALUATION

A. Simulation Assessment

Simulations have been performed first to evaluate the converter. The conduction losses have been calculated according to the device data-sheet [9]. During the dead-time, the GaN HEMTs involved in the specific transitions are in the reverse conduction mode. Since the conduction losses in the reverse conduction mode are higher [6], the same procedure has been adopted to calculate the losses. Regarding the switching losses, the LTspice simulation model is employed to assist the calculation. In this model, a model of the GS66508T has been used in the buck configuration with hard switching. From this simulation, the switching energies have been calculated for different drain-source voltages, different drain currents, and junction temperatures. Afterwards, the data have been

implemented in a Plexim PLECS open-loop model, which contains a simplified model of the cooling system as well. Consequently, the power losses have been calculated.

The modulation described in Section II has been implemented along with the dead-time open-loop compensation. The compensation has been implemented by modifying the expression of the modulation index m_i for the proposed level-shifted Sinusoidal Pulse-Width Modulation (SPWM) as

$$m_{i,comp} = \frac{2 \cdot \widehat{V}_{line} \cdot \left(1 + 2 \cdot \frac{t_d}{T_{sw}}\right)}{V_{DC}} \cdot cos(\omega t) \qquad (12)$$

Fig. 10 shows the performance of the system with a switching frequency of 50 kHz. Increasing the switching frequency up to 200 kHz has been registered that the open-loop dead-time compensation of Eq. (12) is no longer valid for switching frequencies above the 150 kHz, leading to over-modulation and consequently increased output distortions and conduction losses.

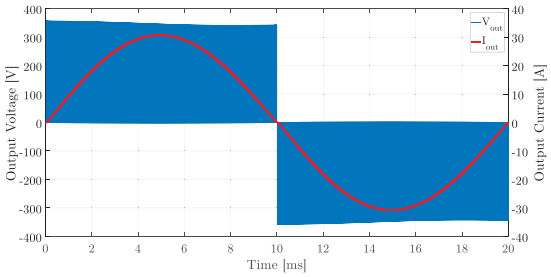


Fig. 10. Output voltage and current in single-phase operation at the nominal power of 5 kW and $f_{sw} = 50$ kHz.

However, the efficiency of the converter has been calculated for different power levels and plotted as shown in Fig. 11. For a power level of 1 kW, the efficiency is around 99% and drops to around 95% when the output power is the rated one. As it is shown in Fig. 12, the main responsible of this efficiency degradation are the conduction losses. In fact, they are dominant and the switching losses are negligible.

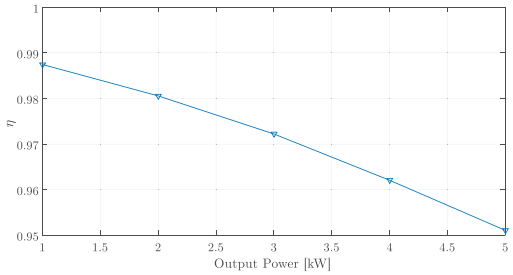


Fig. 11. Inverter efficiency in respect to the output power. The switching frequency is 50 kHz

Regarding the loss distribution among the switches, in Fig. 13, the total losses for the upper switches S_1, S_2 and S_3 are shown. While there is a slight difference between S_1 and S_3, S_2 is generating fewer losses. This reveals a poor stress distribution among the switches, and it is confirmed by the average junction temperature profile, presented in Fig. 14. This is due to the modulation strategy, which presents good performances in lowering the losses. The analysis can be easily extended to the lower switches and thus to the overall topology, due to the symmetry.

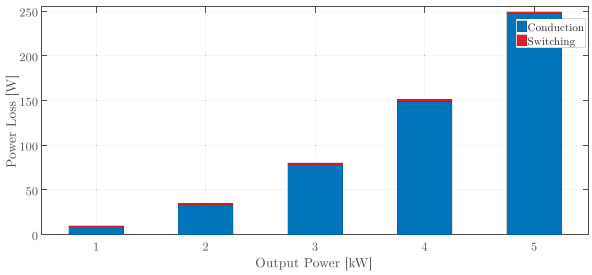


Fig. 12. Power losses at different power levels.

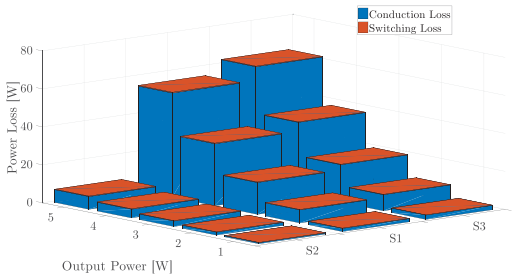


Fig. 13. Power losses distribution among the upper switches S_1, S_2, and S_3.

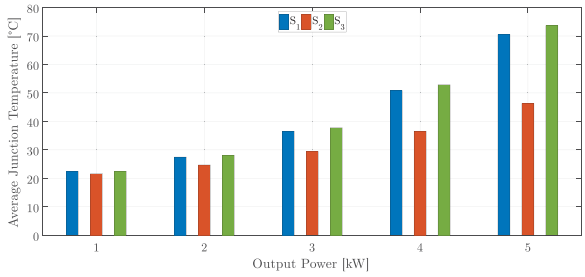


Fig. 14. Average junction temperature of the upper switches S_1, S_2, and S_3 of the inverter.

B. Experimental Results

In order to validate the above performance assessment, a test-rig has been built up. Firstly, the switching performances are evaluated. The converter has been operated in the DC/DC buck configuration. The DC-link voltage has been set as 400 V, the switching frequency to 50 kHz, and the output power to 1 kW. Experimental results are shown in Fig. 15. A close examination of the turn-on switching transients, as shown in Fig. 9(b), reveals that the calculation of the

commutation loop inductances and the simulation model are validated, with a rise time of 11 ns and a voltage overshoot of 13.2 V. The lower voltage overshoot with respect to the simulation is a result of the low bandwidth of the differential probes, which are not able to capture the ringing on the peak. The case temperatures have been measured by means of an optical transducer. Before applying the cooling system, a low power test have been conducted and temperatures are collected, as shown in Fig. 16. It can be observed that there is a sensible temperature difference between the two switches, even though the duty cycle is 0.5 for the equally distributed stress. This difference is due to the size of the copper planes, where the two switches are. That is, the copper plane of S_6 is bigger than that of S_4. This difference is confirmed in the temperature measured with the output power of 1 kW, as summarised in Table IV.

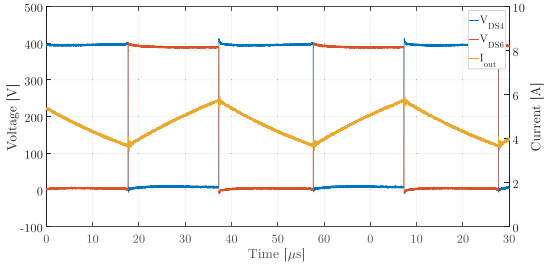


Fig. 15. Experimental results of the synchronous buck configuration test of the GaN 3L-APNC converter.

TABLE IV
COMPARISON OF THE TEMPERATURE MEASUREMENT FROM THE SIMULATION MODEL AND EXPERIMENTS IN DC/DC CONFIGURATION.

	S_4	S_6
Simulation	$26.10°C$	$26.10°C$
Experiment	$25.50°C$	$26.75°C$

During such tests, several problem haves been encountered, mostly related to the measurement equipment. The first reported issue is related to the addition of a small LC load to the gate-source pin of the GaN HEMTs. As it can be seen in Fig. 17(a), the gate-source voltage of the non-floating switch has large oscillations with an overshoot that goes above the maximum allowed gate voltage of $+10$ V. This overshoot has led to several failures, as exemplified in Fig. 18, where a burnt spot can be easily seen corresponding to the gate layer of the GaN HEMT. The issue has been tackled by using an optically isolated differential probe, which gave the clean waveform of Fig. 17(b).

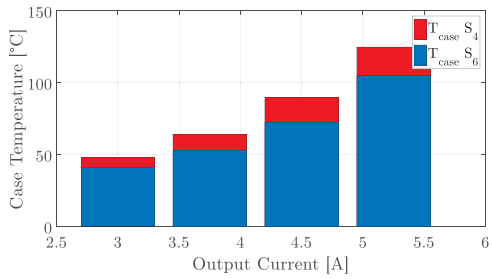


Fig. 16. Temperatures under various output currents in the synchronous buck configuration. The DC-link voltage is 100 V and the switching frequency is 50 kHz.

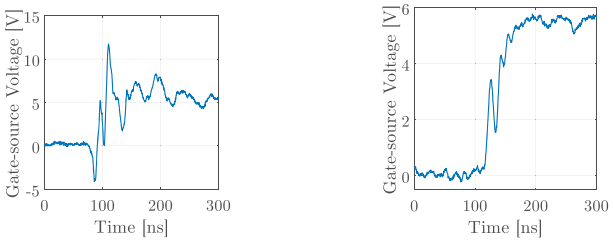


Fig. 17. Gate-source voltages measured with *(a)* a non-isolated differential probe Tektronix P5200A and *(b)* isolated differential probe LeCroy HVFO103.

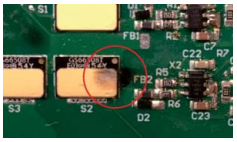
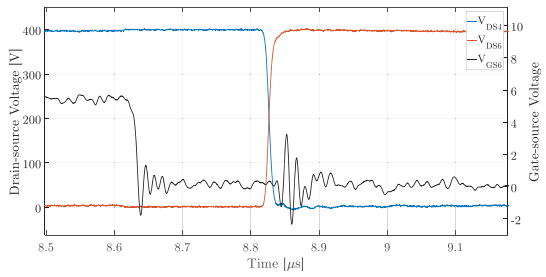


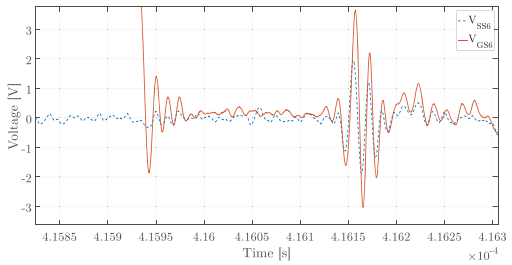
Fig. 18. Picture of the failed device due to the inappropriate probe selection.

Another issue related to the measurement equipment is shown in Fig. 19, which apparently shows a Miller effect oscillation on the gate-source voltage during the turn-off. Increasing the turn-off resistance and adding capacitances across the gate-source in order to give a low impedance path for the Miller current has been ineffective. A further investigation, which involved the measurement across the same point (i.e., source pin voltage in the dashed blue line in Fig. 19) with the differential probe, has revealed that the oscillation is introduced by the radiated EMI concatenated with the probe tips. Therefore, it can concluded that such oscillations represent a false Miller effect, where indeed there is no real oscillation in the gate voltage and the device can work properly.

Lastly, the converter has been tested in its natural configuration of the 3L-ANPC inverter. The DC-link voltage has been increased up to 400 V . The converter-side current along with the output voltage is depicted in Fig. 20, with a switching frequency of 50 kHz and output power of 950 W. In this case, the temperature of the upper switches have been recorded, as listed in Table V. Once again, the simulation model can be validated also from the thermal point of view. Regarding the failure, it can be associated with the damaging of the CeraLink capacitor, as shown in Fig. 21. In fact, when all the failures occurred, the capacitor cracked, leading to the failure of the entire switching cell. By analysing the picture, it seems that



(a)



(b)

Fig. 19. Experimental measurement of the gate-source voltage during turn-off. In *(a)* the oscillations resemble the Miller effect. In *(b)*, the source-source voltage has been measured (blue dashed line) and the oscillations compared with the one seen on the gate-source voltage (orange solid line).

the capacitor failed due to a crack in the dielectric. It may be possible that, due to a bended board or overheating of the capacitor during the soldering procedure, the capacitor has presented such a crack which could not withstand the high DC-link voltage and consequently failed.

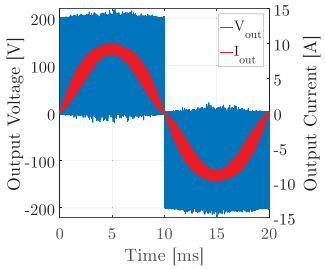


Fig. 20. Experimental results of the output voltage and pre-filter current in the DC/AC configuration with a switching frequency of 50 kHz and $V_{DC} = 400\ V$.

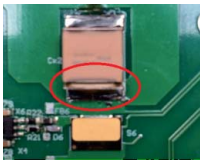


Fig. 21. Picture of the capacitor failure when the DC-link voltage has been increased to 600 V.

TABLE V
COMPARISON OF THE TEMPERATURE MEASUREMENT FROM THE SIMULATION MODEL AND EXPERIMENTS IN AC/DC CONFIGURATION.

	S_1	S_2	S_3
Simulation	$28.8°C$	$28.3°C$	$29°C$
Experiment	$29.15°C$	$28.7°C$	$29.3°C$

V. CONCLUSION

In this paper, the performance assessment of an already designed GaN-based 3L-ANPC single-phase inverter has been presented. During this work, the topology and the previous work have been analysed and a qualitative design of the passive components was proposed. Additionally, simulation have revealed the good performances in terms of efficiency for the GaN inverter, especially from the switching losses point of view. On the other hand, the modulation technique is unable to provide an equal stress distribution among the GaN devices. From the experimental results, two issues related to the measurement equipment have been highlighted, leading to suggestions of the use of isolated differential probes when measuring the gate-source voltage in GaN applications. Lastly, the converter has been tested in DC/AC configuration with a limited DC-link voltage and output power. This limitation has been imposed by several failures on the CeraLink capacitor, when increasing the DC-link voltage.

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