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A Fast-Switching Integrated Full-Bridge Power Module Based on GaN eHEMT Devices

Asger Bjørn Jørgensen, Szymon Bęczkowski, Christian Uhrenfeldt, Niels Høgholt Petersen, Søren Jørgensen, and Stig Munk-Nielsen

***Abstract*—New packaging solutions and power module structures are required to fully utilize the benefits of emerging commercially available wide bandgap semiconductor devices. Conventional packaging solutions for power levels of a few kW are bulky, meaning important gate driver and measurement circuitry is not properly integrated. This paper presents a fast-switching, integrated power module based on gallium nitride enhancement-mode high-electron-mobility transistors, which is easier to manufacture compared with other hybrid structures. The structure of the proposed power module is presented, and the design of its gate driver circuit and board layout structure is discussed. The thermal characteristics of the designed power module are evaluated using COMSOL Multiphysics. ANSYS Q3D Extractor is used to extract the parasitics of the designed power module, and is included in simulation models of various complexity. The simulation model includes the SPICE model of the gallium nitride devices and parasitics of components are included by experimentally characterizing them up to 2 GHz. Finally, the designed power module is tested experimentally, and its switching characteristics cohere with the results of the simulation model. The experimental results show a maximum achieved switching transient of 64 V/ns and verifies the power loop inductance of 2.65 nH.**

***Index Terms*—Semiconductor device packaging, power semiconductor switches, Circuit simulation.**

I. Introduction

POWER electronics is an ever growing industry, used to handle and treat electrical energy in every aspect from production to consumption. Power electronics are used for all power levels, whether it be in wind turbines, solar panels, industry motor drives, pumps, kitchen appliances or artificial lighting. In many cases the electrical energy is handled by switch mode power supplies, in which the semiconductor die is the core unit. Typically at lower power levels <1 kW, the semiconductor device is directly integrated with other components to form a power supply as a single unit [1]. For higher power levels or systems of higher complexity, the semiconductor devices are often packaged as a power module, which is then just seen as a component of the total power electronic system. In either case, the performance of the semiconductor device is dependent on the interconnection it has with critical components of the circuit such as gate driver integrated circuits (ICs), capacitors, sensors and other auxiliary circuitry. Furthermore, to ensure reliable and robust operation, it must be ensured that the device is properly cooled, enclosed and interconnected with other peripherals. New wide band gap (WBG) semiconductor materials, such as silicon carbide (SiC) and gallium nitride (GaN), offer potential size, efficiency and performance improvements of power modules used in switch mode power supplies. These materials offer higher breakdown voltage, faster switching speeds, lowered on-resistance and increased operating temperatures, when compared to silicon [2], [3]. The fast switching speed of WBG devices produces high $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ which may induce ringings and electromagnetic interference issues due to parasitic elements in the packaging [4]. Current power module packaging design for power levels in the kilowatt range is still bulky, which causes difficulty in integration and minimization of parasitic elements in both power and gate driver loop simultanously [5], [6]. To harvest the benefits of WBG devices new designs and integration of parts must be studied and tested.

Silicon power modules with base plates is currently the most dominant design, used in approximately 70 to 80 % of all power modules [7]. A typical sectional view of the conventional power module structure is shown in Fig. 1(a). At the bottom is the baseplate, which is mounted to a heat sink to ensure low thermal resistance. A direct bonded copper (DBC) is soldered to the baseplate. The DBC is a sandwich structure with copper on either side of ceramic substrate which is an electrically insulating material yet capable of transferring heat efficiently [8]. Encapsulation such as epoxy or silicone gel is used to ensure high electric breakdown strength and protect the semiconductor dies from humidity and contaminants. The entire assembly is enclosed in a plastic housing to mechanically protect the internal structures of the power module. Terminals are mounted on the copper planes, and used to connect the semiconductor with electrical circuits outside the power module. Typically this control circuitry is soldered on a printed circuit board (PCB) and connected outside of the power module. The benefits of this structure is its high voltage blocking capabilities and high power dissipation [9]. The conventional structure is challenged by the emergence of new WBG devices. Due to the terminals and copper planes a parasitic inductance of typically 10-30 nH [10]–[13] limits the utilization of the increased switching speeds of the WBG semiconductors.

A solution is to assemble every part of the switching device into a multilayer PCB, as shown in Fig. 1(b). In this way the semiconductor die is directly embedded into the PCB, and has copper planes connecting to its peripheral units [14]. This eliminates the use of bond wires. The concept reduces the parasitic inductance in the power loop, reported at 2.8 nH [12].

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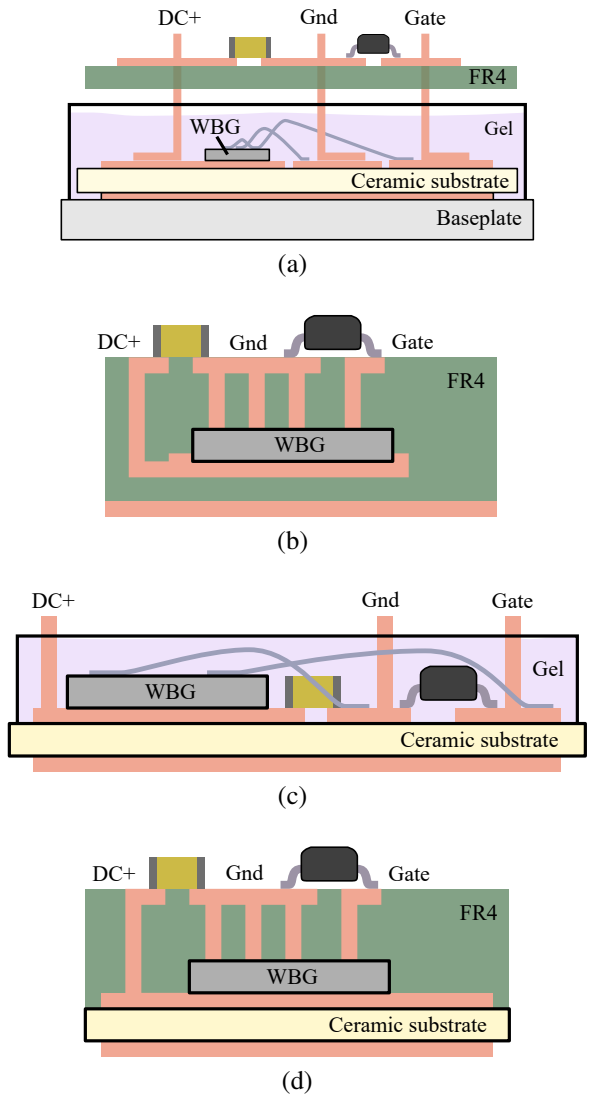

Fig. 1. Packaging technologies (a) conventional power module structure (b) PCB embedded die technology (c) integrated DBC power module structure (d) PCB/DBC hybrid power module structure.

But it is hard to achieve both good thermal and electrostatic performance simultanously [15]. An issue is to dissipate the heat, due to the high thermal resistance of the FR4 material. For high power dissipation levels larger copper planes and vias reduce thermal impedance by more effectively conducting the heat to the outer layers of the PCB. To further reduce thermal impedance the FR4 layer is minimized in thickness, which, in turn, causes issues related to high electric field stress. Too high electric field stress cause partial discharges or sparking [16]. Modifications to the geometry allows for some reduction in electric field stress [17], but still restrictions on spacing have to be maintained. In conclusion embedding everything in a PCB enables low parasitic design, but requires strict compromise between thermal and electrostatic performance.

To improve the heat dissipation of the semiconductor device, it is preferred to mount it on a DBC. An idea is to utilize the DBC as much as possible. The most important components such as semiconductor device, gate drivers and capacitors are

TABLE I
COMPARISON OF POWER MODULE STRUCTURES

	Inductance	Thermal	E-field	Manufacture
(a) Conventional	− −	+ +	+ +	+ +
(b) PCB embedded	+ +	−	−	−
(c) DBC integrated	+	+ +	+ +	+
(d) PCB/DBC	+ +	+ +	+	− −

soldered directly onto the DBC [6]. The structure is depicted in Fig. 1(c). The power module has good heat dissipation through the ceramic, and high electrostatic performance is maintained by encapsulating the module in silicone gel. The power loop layout is restricted to a single copper layer and achieves loop inductances of 7-11 nH [18]. This technology does not introduce any new steps in terms of manufacturing when compared to conventional power module. It mainly requires etching of more tracks and soldering of more components. However, as the DBC is limited to only a single layer, it reduces the complexity of circuits which can be incorporated. An attempt to mitigate this issue is to use printed copper thick-film technology on the DBC [13], [19]. This increases the level of integration of the gate driver circuitry, but it is still not as compact as what is achievable using PCB technology.

Power modules using both DBC and PCB technology reduces the issue of poor heat dissipation, while maintaning the low inductive design. A state of the art power loop inductance of 1.5 nH including current measurement is reported [20]. The solution is to mold the PCB directly on top of the DBC, by which no bond wires are used [21]–[23]. A diagram of the structure is shown in Fig. 1(d). This structure shows very fast switching speeds of both gate and power loops. However, this solution significantly increases the manufacturing complexity, as the PCB molding is done directly on the DBC. A summary of the four packaging structures of Fig. 1 is given in Table I, where positive metrics are given for technologies allowing low inductance, low thermal resistance, high electric field breakdown strength and low manufacturing complexity.

In this paper a power module hybrid structure of DBC and PCB is proposed for use with commercially available lateral GaN enhancement-mode high-electron-mobility transistor (eHEMT), which reduces the manufacturing complexity as only soldering is required for assembly. The structure is used to design a fast-switching integrated GaN eHEMT power module, which focuses on a board layout to simultaneously achieve both fast $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ switching, as described in section II. This also requires that the parameters of the gate driver circuit are properly designed. Thermal characteristics of the module are evaluated in section III. The switching behaviour of the designed power module is simulated prior to testing. Due to the compactness of the designed board, it is difficult to measure and verify the operation. Thus efforts are made to construct a simulation model of high accuracy, to get knowledge of voltage/currents internally on the board. A simulation framework is discussed in section IV, which includes three different levels of simulation complexity and its influence on the resulting waveforms. Finally in section V,

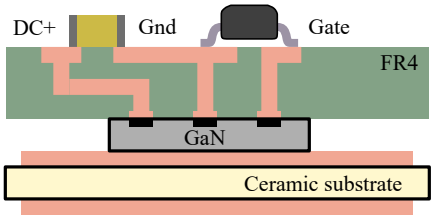

Fig. 2. Proposed DBC/PCB hybrid power module structure for lateral GaN eHEMT devices.

the power module is built and its switching behaviour is experimentally validated and compared with the simulation. The paper is concluded in section VI.

II. Design of Integrated GaN Power Module

New commercially available lateral GaN eHEMT devices have all electrical connections on the top surface, and a solderable bottom surface for heat dissipation [24]. This enables the use of a premanufactured PCB to be stacked on top of the GaN device. A power module structure as shown in Fig. 2 is proposed. This solution offers very low inductance, high power dissipation and low capacitive coupling. The air gap to the DBC, means that traces and planes on the PCB have limited electrical coupling to the DBC and heat sink. A three dimensional model of the stack to be assembled is shown in Fig. 3. At the bottom is a Al_2O_3 DBC substrate. The GaN eHEMT has an exposed metal backside as a heatsink, but is internally connected to source potential. Thus, a pattern is etched on the DBC to isolate each GaN eHEMT device. Additionally, holes are etched underneath each pin for safety, to avoid shorting of the different press fit pins to DBC. The PCB with all the control and measurement circuitry is soldered on top of the GaN eHEMT. At last, a plastic housing is used to enclose and mechanically protect the power module.

A. Gate driver

A schematic of the gate driver circuit used for a single half-bridge is shown in Fig. 4. A bootstrap gate driver configuration is used, due to its simplicity and compactness. Using a bootstrap configuration removes the requirement of isolated power supplies, which can be relatively bulky and adds additional parasitic capacitance between switching output and ground. However, the disadvantage is that there is some limit to the achievable duty cycle range, switching frequency and it requires a start-up procedure to power the high side gate driver circuitry. The ADUM4121 gate driver is used, which provides 5 kV voltage isolation between the input and output side. It has a coupling capacitance of 2 pF between input and output side. It has a 5 V supply on the input side, and is provided with a 6 V supply on the output. Thus the gate-source voltages supplied to the GaN eHEMT are 6 V and 0 V for high and low, respectively. For the high side, a low dropout (LDO) linear regulator is used to stabilize the 6 V supply. The ADUM4121 also has a Miller clamp functionality, but, for the tests shown in this paper, the Miller clamp connection is left unconnected. A 20 nH ferrite bead is inserted in the gate

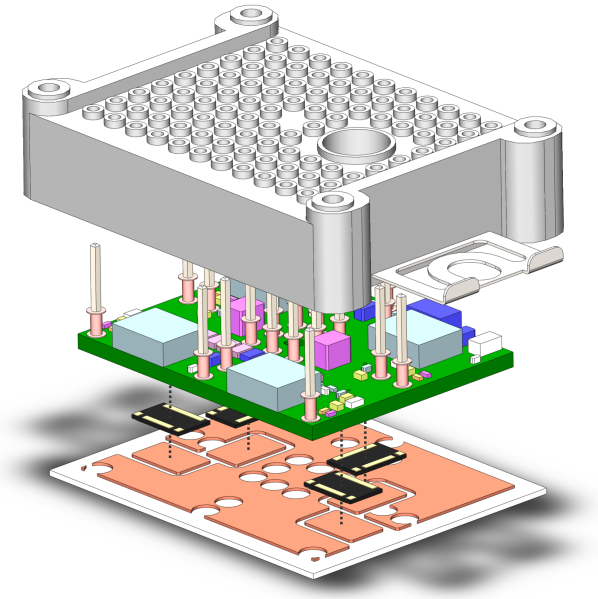

Fig. 3. Three dimensional rendering of the GaN eHEMT power module stack assembly. DBC dimensions are 36x28 mm.

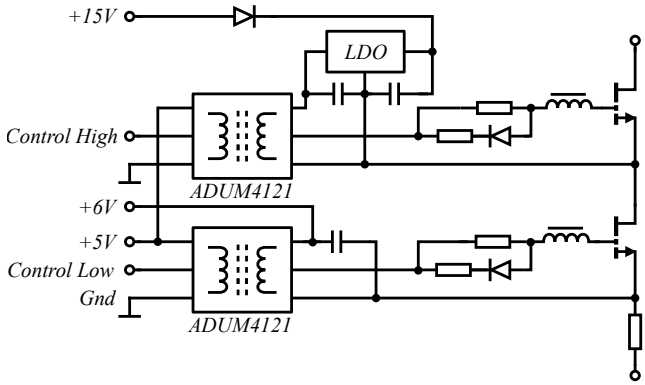

Fig. 4. Schematic of the gate driver and switching circuit for a single half-bridge.

driver path to suppress high frequency ringing originating from the source inductance of the power circuit, and it shifts the resonance frequency of the gate driver loop away from the power loop resonance frequency [25]–[27].

There is a small operation margin of the gate-source voltage of the GaN eHEMT, as its recommended drive voltage is 6 V and maximum limit is 7 V. Thus, the turn-on gate resistance is chosen such that gate-source voltage oscillations are kept low, yet without slowing down the switching speed [21]. The gate-source loop schematic shown in Fig. 5 is analyzed to obtain such dynamics, including the gate loop inductance L_g, turn-on gate resistance $R_{g,on}$ and gate-source capacitance C_{gs}. By applying Kirchoffs voltage law

$$v_{in}(t) = i(t)R_{g,on} + L_g\frac{\mathrm{d}i(t)}{\mathrm{d}t} + v_{gs}(t) \tag{1}$$

The expression $i(t) = C_{gs}\frac{\mathrm{d}v_{gs}(t)}{\mathrm{d}t}$ is inserted, and the

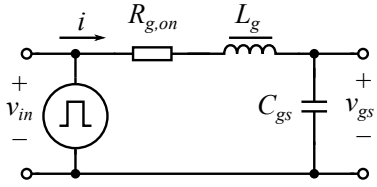

Fig. 5. Schematic used to analyze the dynamics of the gate-source voltage.

Laplace transform of (1) becomes

$$\frac{V_{gs}(s)}{V_{in}(s)} = \frac{\frac{1}{L_g C_{gs}}}{s^2 + \frac{R_{g,on}}{L_g} s + \frac{1}{L_g C_{gs}}} \tag{2}$$

Equation (2) describes the dynamics from the gate driver to the gate-source voltage on the GaN eHEMT. It is compared to the standard form of a second order system [28], given by

$$G(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3}$$

where ζ is the damping ratio and ω_n the natural frequency. By comparing (2) to the standard form in (3) an expression for the gate turn-on resistance is found as

$$R_{g,on} = 2 \cdot \zeta \cdot \sqrt{\frac{L_g}{C_{gs}}} \tag{4}$$

A damping of $\zeta = 0.707$ is chosen to achieve fast rise time, yet limited oscillation of gate-source voltage. Inserting the gate-source capacitance of the GS66508T, and assuming that the gate inductance is dominated by the ferrite bead, the required gate resistance is calculated from (5).

$$R_{g,on} = 2 \cdot 0.707 \cdot \sqrt{\frac{20\,\text{nH}}{258\,\text{pF}}} = 12.4\Omega \tag{5}$$

The ADUM4121 gate driver and internal gate resistance of the GS66508T GaN device contributes with approximately 1.7-2.7 Ω, and thus the external gate resistor is chosen as 10 Ω. According to the design guidelines for the GS66508T GaN eHEMT [29], the turn-off gate resistance should be 5-10x lower to avoid Miller latch up. Due to the resistance contributions from the ADUM4121 and GS66508T internal gate, external turn-off gate resistance is chosen as 0 Ω. This results in a slight overshoot during turn-off, but as the minimum gate-source voltage is rated at $-10\,\text{V}$, a slight overshoot during turn-off does not pose a threat for safe operation of the module.

B. Board layout

The board layout is designed to have both low parasitic capacitance and low inductance in the power loop, to push the capability of both high $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$. However, maintaining both low parasitic capacitance and low inductance is often a compromise between the two. For instance, the inductance can be kept small by decreasing the loop area, and use parallel planes on the PCB to cancel the magnetic fields generated. However, parallel planes have a large capacitive coupling, and results in increased common mode current during voltage transients [30]. Likewise, to have low capacitive coupling between planes they should be spaced far apart, but this will increase the loop area and thus increase the inductance. For this board layout, the parasitic capacitance is kept low by ensuring that switching outputs are not overlapping with other planes, as shown in Fig. 6. Inductance is then kept low by placing the GaN eHEMT devices close to one another, reducing the effective loop area. DC-link capacitors are placed on the top side of the board, directly above the GaN eHEMT devices and multiple vias are used to connect the top and bottom plane.

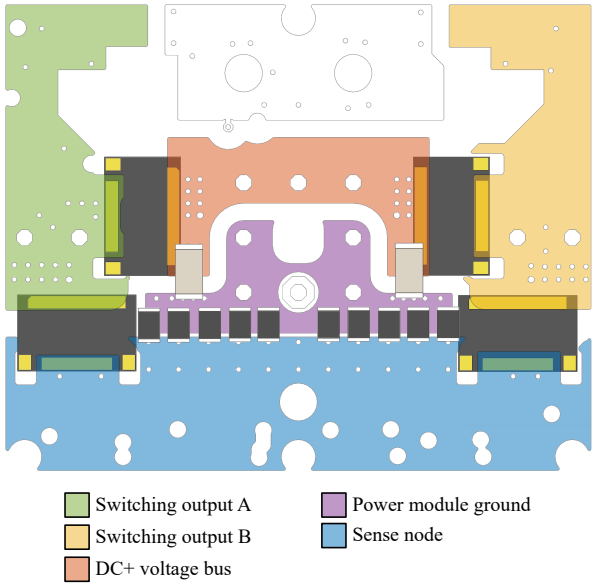

Fig. 6. PCB layout of main power planes, and positioning of GaN eHEMT devices (bottom side), decoupling capacitors (top side) and current shunt resistors (top side).

A current measurement circuit must be integrated for control and safety purposes. For current measurements Hall-effect, Rogowski or similar are often used, but they all require a winding around a current carrying conductor. The inductance introduced by such a solution could compromise the desired fast switching. Instead, it is decided to measure the current through the low GaN eHEMT devices by inserting current shunts resistors in the power loop path. The current shunt resistor array has relatively low insertion inductance compared with other current measurement techniques [31]. The current shunt layout is based on the design presented in [32], [33]. In total ten current shunt resistors are inserted to minimize the parasitic inductance, which improves measurement bandwidth [34]. The issue of this solution is that the measurement is not isolated, and thus it is influenced by parasitics in the circuit. Thus it is important to accurately model the parasitics of the board, as further studied in Section IV, to know their influence on the measured shunt resistor voltage. Two half bridges are placed in the same power module, and by symmetrical placement they share both the same current shunt resistors and decoupling capacitors.

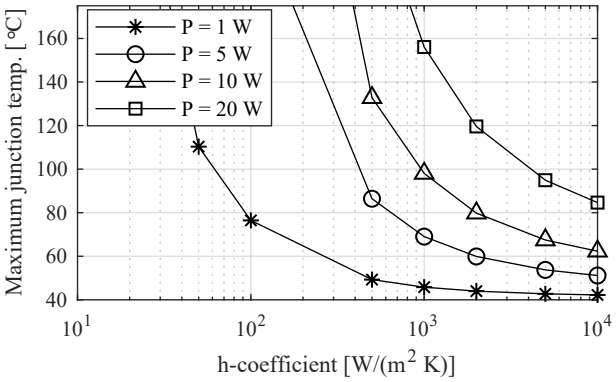

Fig. 7. Maximum junction temperature for different power inputs and heat transfer coefficient. Exterior temperature is T_{ext} = 40 °C.

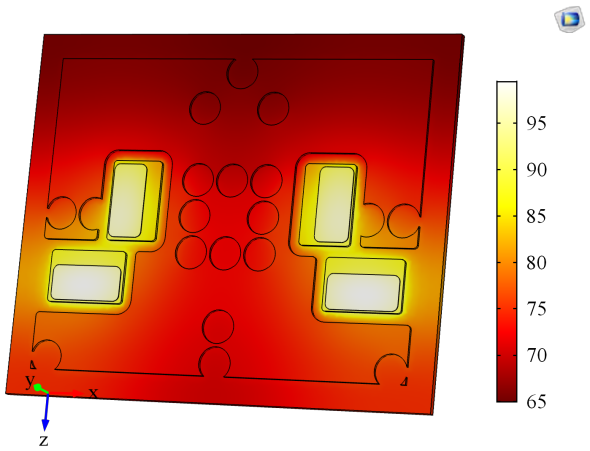

Fig. 8. Temperature distribution simulated in COMSOL Multiphysics, for conditions P = 10 W per device, h = 1000 $\frac{\mathrm{W}}{\mathrm{m^2K}}$ and T_{ext} = 40 °C.

III. Thermal Characteristics

The chosen GaN eHEMT device is a prepackaged device and has a thermal resistance from junction to case, Θ_{jc}, of 0.5 K/W. In comparison the CPM2-1200-0040B SiC MOSFET bare die of similar dimensions has Θ_{jc} = 0.38 K/W [35]. However, the additional 0.12 K/W must be compared to the total thermal resistance from junction to heatsink of the final power module. The thermal performance of the power module is analyzed using a steady state finite element simulation. The 3D model of Fig. 3 is imported to COMSOL Multiphysics.

The DBC stack has a 0.3 mm thick copper layer with thermal conductivity k = 380 $\frac{\mathrm{W}}{\mathrm{mK}}$, on either side of 0.63 mm Al_2O_3 ceramic substrate of k = 25 $\frac{\mathrm{W}}{\mathrm{mK}}$. A thin solder layer of 60 μm thickness having thermal conductivity, k = 60 $\frac{\mathrm{W}}{\mathrm{mK}}$, is included to the heat pad of the GaN eHEMT device. The backside of the power module is cooled by the heat flux

$$q = h \cdot (T_{ext} - T) \tag{6}$$

where q is the heat flux, h is the heat transfer coefficient and T_{ext} is the exterior temperature. The heat transfer coefficient changes greatly depending on how the power module is cooled. Typically the h-coefficient is up to 100-300 $\frac{\mathrm{W}}{\mathrm{m^2K}}$ for forced convection of air, 500-2000 $\frac{\mathrm{W}}{\mathrm{m^2K}}$ for modules mounted on heatsink and 10000 $\frac{\mathrm{W}}{\mathrm{m^2K}}$ or more for direct water cooling [15], [23], [36]–[38]. Shown in Fig. 7 is the maximum junction temperature of the power module, when subjected to different power inputs per device and heat transfer coefficients. In all cases the exterior temperature is kept at 40 °C.

A case where each GaN eHEMT device is subjected to a power loss, P of 10 W, the exterior temperature, T_{ext} = 40 °C and h = 1000 $\frac{\mathrm{W}}{\mathrm{m^2K}}$, is shown in Fig. 8. The thermal resistances from junction to heatsink, Θ_{jh}, are evaluated as 2.4 $\frac{\mathrm{K}}{\mathrm{W}}$ and 2.1 $\frac{\mathrm{K}}{\mathrm{W}}$ for low and high side, respectively. This is comparable with power modules on similar DBC material, thickness and semiconductor die area [5], [13]. The difference in thermal resistance between high and low side devices is 12 %. Compared to other integrated power modules the difference between devices is found as 18-19 % [15], [23]. It is concluded that the thermal performance, measured in terms of thermal resistance Θ_{jh} and mismatch between devices is within range of similar integrated solutions. Based on the total thermal resistance of the power module, the prepackaged GaN eHEMT device is not regarded as the bottleneck. It is concluded as suitable for use in the power module without modifications to its proposed structure.

IV. Electrical Simulation Model

Due to the compactness of the design, there is only a limited amount of measurement points available from the power module: switching output voltages and the current sense measurement. Thus, during development and testing, an accurate simulation model is a necessary tool to gain insight in other nodes of interest, i.e. gate voltages. Secondly, to further improve the design, it is required to know the contribution different board parasitics have on the switching performance and measurements. A simplified schematic of the parasitics and the components of one half-bridge is shown in Fig. 9. As an example, due to the location of the grounding on the board, and if assuming that trace impedances are mainly inductive, the sense voltage measured is given by

$$v_{sense}(t) = i_1(t) \cdot R_{\mathrm{sense}} + L_{\mathrm{De}} \frac{\mathrm{d}i_1(t)}{\mathrm{d}t} + L_{\mathrm{DC-}} \frac{\mathrm{d}i_2(t)}{\mathrm{d}t} \tag{7}$$

where i_1 is the power loop current, i_2 is the circulating current between distributed DC-links, R_{sense} is the resistance of the shunt array and L_{De}, $L_{\mathrm{DC-}}$ are trace self-inductances. When achieving fast switching speed, there is a significant contribution from the parasitic inductances L_{De} and $L_{\mathrm{DC-}}$ and thus their value are important to know, to validate that the experimental measurements are correct.

To extract the board parasitics the ANSYS Q3D Extractor simulation software is used. ANSYS Q3D Extractor uses finite element method and methods of moments to solve electromagnetic field simulations [39]. A three dimensional model of the board is imported to the software, and inputs/outputs of each net are defined. A literature review reveals that different simulation approaches are used with the ANSYS Q3D Extractor software, which might result in different accuracy, simulation time and ease of convergence when later implemented in a SPICE solver. In the following section, three different

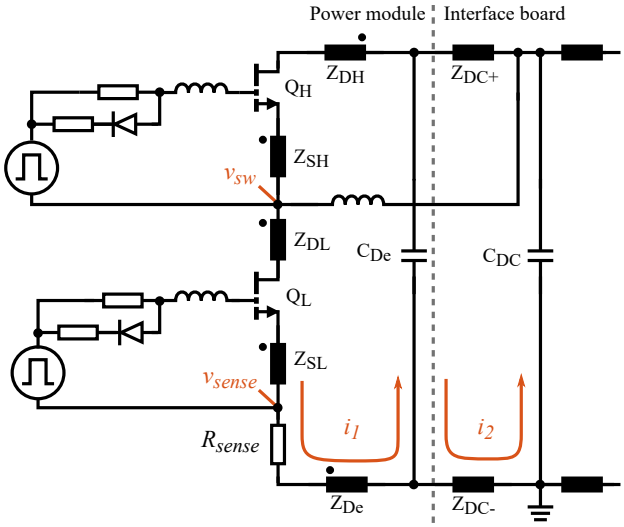

Fig. 9. Simplified schematic of the simulation model.

TABLE II
SELF-INDUCTANCE OF TRACES

Symbol	Value	Symbol	Value
L_{DH}	0.31 nH	L_{De}	0.23 nH
L_{SH}	0.26 nH	$L_{\mathrm{DC+}}$	1.9 nH
L_{DL}	0.35 nH	$L_{\mathrm{DC-}}$	0.3 nH
L_{SL}	0.86 nH		

approaches are implemented and the simulation results are compared. The first approach is to replace each impedance of Fig. 9 with the self-inductance of the trace. The parasitic capacitances are designed to be low for this board, and thus are neglected. The inductances are evaluated using a point-by-point approach, i.e. from the DC-link to the drain of the high device, then from source of high device to drain of low device and so forth [9], [40], [41]. This model is denoted as a Level 1, and self-inductance calculated for each trace is shown in Table II. A reported issue of this is that the summation of the inductances becomes large, because when evaluating each inductance individually there are no mutual inductance effects included in the model [42].

Thus, often an approach is used at which the full loop is evaluated [30], [43], [44]. In this approach each device is modelled as a conductor, i.e. drain and source of a switch are electrically shorted. The effective inductance of a full loop is calculated, and by this approach the mutual inductance effects are included in the solution. However, to use the extracted inductance in a SPICE simulation it must be placed accordingly in the circuit diagram, and this is difficult when inductances are calculated for the full loop. Thus, an approach considered for this paper, is to use both the self-inductance and mutual-inductance [44]–[46]. From ANSYS Q3D Extractor an RLC matrix is exported, meaning that it models the resistance and self-inductance in each trace, mutual-inductance and parasitic capacitances between nodes. This is denoted as a Level 2 model. It is advantageous during development that electromagnetic fields and couplings are already included in

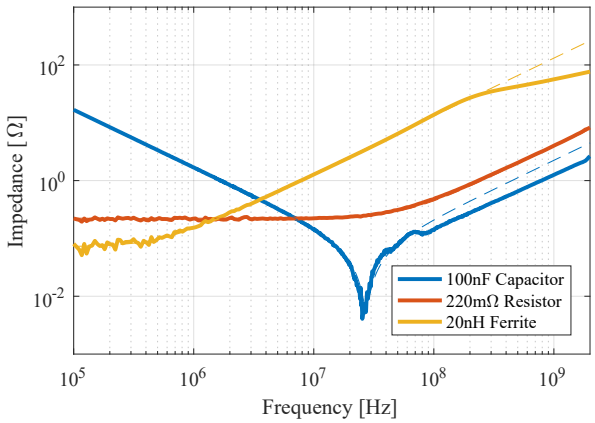

Fig. 10. Impedance as a function of frequency of main components of the half-bridge circuit (including their simulated models in dashed line).

TABLE III
PARASITICS EXTRACTED OF SMD COMPONENTS

Model			
Component	R	L	C
100 nF, 1210 capacitor	6 mΩ	257 pH	95.6 nF
220 mΩ, 0805 resistor	224 mΩ	616 pH	-
20 nH, 0603 ferrite bead	71 mΩ	21 nH	-

the circuit simulation which reveals effects of conducted and near-field electromagnetic interference issues related to the board-structure.

When exporting the RLC matrix, the parameters must be extracted at a certain frequency. Typically, resistance values are extracted for low frequencies, where skin effect is neglected and current is assumed to flow equally distributed in the conductor volume. This is done to correctly model steady state power loss of the board. The inductance values are extracted for high frequencies, at which the current path shifts to reduce the total loop area, and the inductance value becoming lower. Using this value results in the best approximation of the inductance during fast switching transients.

A. Measurement of component parasitics

In addition to extraction of parasitics of the board, the influence of the parasitics in the components is also of interest. As board parasitics are small, the relative influence of the surface mount device (SMD) packages become larger. Especially the measurement of voltage across the shunt resistors where the influence of the parasitic inductance can be significant. As resistors are conducting the full current and the voltage across them is just a few hundred millivolts, it requires a good estimation of how they are influenced by parasitics. Measuring the parasitic inductance and capacitance of SMD resistors, capacitors and ferrite beads down to just a few nH and pF requires a large frequency range to capture the cutoff/resonance frequency of the component. A Keysight E5016B impedance analyzer is used, which is capable of measuring the components up to 3 GHz. The Keysight 16192A test fixture has a measurement capability up to 2 GHz and is

TABLE IV
COMPLEXITY IN SIMULATION MODEL

	Board parasitics	Component parasitics
Level 1	L w/o coupling	Ideal R, L or C
Level 2	RLC incl. coupling	Ideal R, L or C
Level 3	RLC incl. coupling	Measured RLC

used to mount the SMD components. The impedance spectrum of an 220 mΩ 0805 shunt resistor, 100 nF 1210 DC-link capacitor and the 20 nH ferrite bead in the gate driver is shown in Fig. 10, which also includes the frequency response of its estimated RLC model. The model used for fitting the response is an idealized RLC series connection. Table III summarizes the parasitics values extracted from the frequency response. The simulation model which includes both RLC board parasitics and RLC of SMD components is denoted as a Level 3 model.

B. Simulation results

The results are compared for the three different levels of simulation complexity. A summary of what is included in the three simulation models is shown in Table IV. All simulations use the SPICE model of the GS66508T GaN eHEMT device, and are all solved using the recommended solver settings provided by GaNSystems [47]. The SPICE model used includes a drain-source stray inductance of 0.4 nH originating from the packaging of the device and its temperature is set at 25 °C.

A double pulse test is simulated. The DC-link voltage is 200 V and current is ramped up in a 10 μH load inductor for 1 μs, to achieve a load current of 20 A. Transients of turn on and turn off are investigated, as shown in Fig. 11 and 12, respectively.

The voltage rise time is defined as the time from 10 % to 90 % of DC-link voltage, and vice versa for voltage fall time. By this definition, both the fall and rise time is 6 ns, equivalent to 27 V/ns. These switching speeds are the same for all three simulation cases. Following turn-on and turn-off oscillations in both voltage and current are visible, due to the resonance frequency of the power loop, shown as i_1 in Fig. 9. The resonance frequency is given by

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{8}$$

For the Level 1 model, the power loop inductance is calculated as the sum of inductances in the power loop, i_1 in Fig. 9, combined with the 0.4 nH contribution from the packaging of the two GaN devices. The resonance frequency for the Level 1 model is calculated by reading the time period of oscillations in Fig. 11 and 12. The output capacitance of the GaN eHEMT device is estimated for the given test condition by rearranging (8).

$$C = \frac{1}{(2 \cdot \pi \cdot 325\text{MHz})^2 \cdot 2.8\text{nH}} = 85\text{pF} \tag{9}$$

From the simulation result the resonance frequency is slightly higher for the Level 2 and 3 models. However, because they include mutual inductance coupling terms the effective loop inductance is cumbersome to calculate. Instead, the effective loop inductance for Level 2 and 3 models are calculated by reading the resonance frequency from the simulation results and equals 358 MHz and 338 MHz, respectively. By rearranging (8) the effective inductance for the Level 3 model is

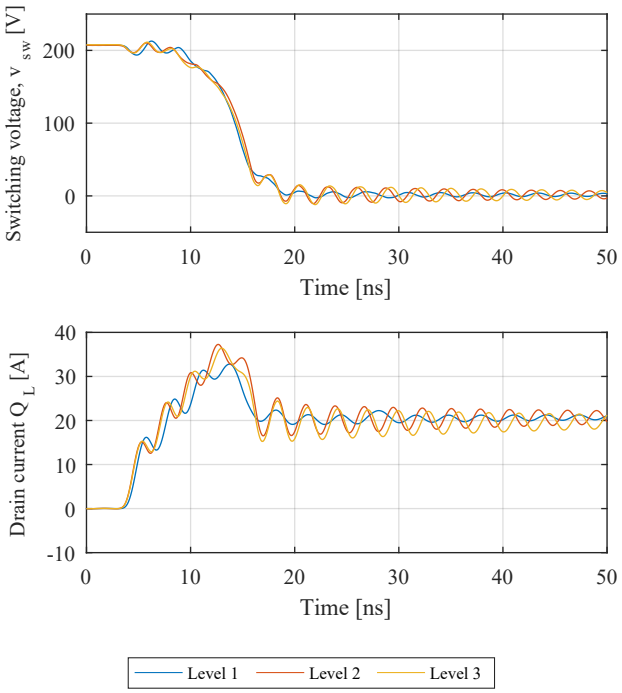

Fig. 11. Simulated waveforms of switching voltage and drain-source current during turn-on for three different levels of simulation complexity.

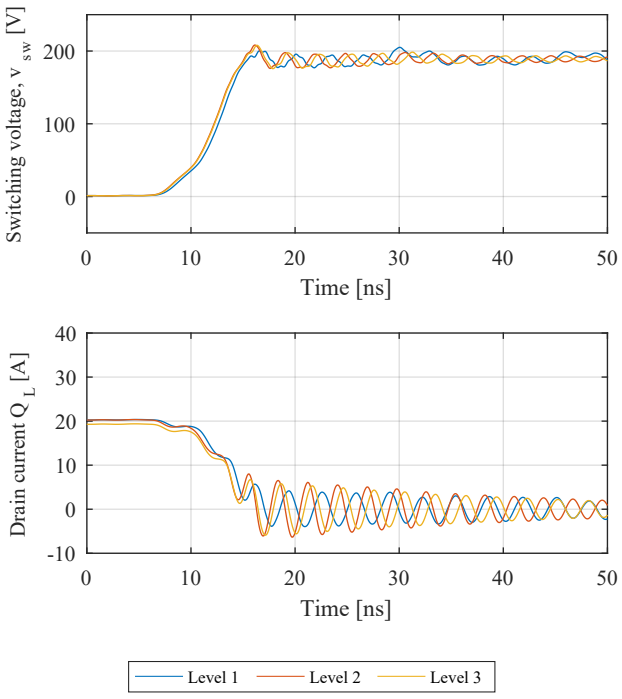

Fig. 12. Simulated waveforms of switching voltage and drain-source current during turn-off for three different levels of simulation complexity.

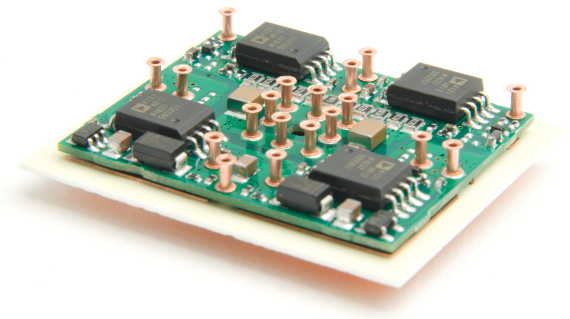

Fig. 13. Photograph of power module after soldering.

calculated as

$$L_{L3} = \frac{1}{(2\pi \cdot 338\text{MHz})^2 \cdot 85\text{pF}} = 2.6\text{nH} \qquad (10)$$

Thus, the effective inductance is 8 % higher for Level 1 which only includes self-inductance, compared with Level 3 case where mutual inductance coupling and component parasitics are included. The slightly higher inductance values of the Level 1 model, means it could be more susceptible to false and oscilattory turn on during simulation, due to increased ringing of the gate-source loop [25], [48]. However, this cannot be concluded because the coupling of the RLC matrix introduce new complexity that have not yet been studied in literature. The three models differ in terms of time required to generate the simulated turn on/off waveforms, which are simulated for a total of 5 μs. The real time required in LTSpice XVII is 5.5s, 7.4s and 11.3s for the Level 1, Level 2 and Level 3 model, respectively. Thus the total simulation time is about 2 times longer for the increased complexity.

V. Experimental results

The power module is built for experimental tests on a $0.63\,\text{mm}$ thick Al_2O_3 DBC and is etched with the designed pattern. All components are soldered to the PCB board in a multi-vacuum vapor phase oven. Following this step, the PCB board including the GaN eHEMT devices are soldered to the DBC, as shown in Fig. 13. At last the pressfit pins are inserted in the sockets and the plastic housing is mounted. For the experimental tests the power module is connected to a test board, as shown in Fig. 14. The test board interfaces the auxiliary voltages and control signals for the gate drivers. It includes the main DC power supply and switching output terminals for each half-bridge. BNC connectors are used to measure the voltage switching outputs and the current shunt signal. The voltage switching waveforms are measured using 500 MHz LeCroy PP018-1 probes on a Lecroy HDO6104A oscilloscope. All cables of probes, auxiliary power supply and main power supply are equipped with common mode choke cores.

A. Switching behaviour

The experimental waveforms are compared with the level 3 simulation model during turn-off and turn-on as shown in Fig. 15. The voltage switching waveforms show very good coherence with the simulation model. The experimental results shows that the GaN eHEMT devices for both voltage fall and rise time switch in $6\,\text{ns}$ for the tested $200\,\text{V}$ / $20\,\text{A}$ condition, equivalent to a voltage transient of $27\,\text{V/ns}$. The resonance frequency of the experimental results is read as $335\,\text{MHz}$. Assuming that the loop capacitance is the same as observed from the simulation model in Section IV, it indicates that the effective power loop inductance is $2.65\,\text{nH}$.

To further verify the simulation model, the operating conditions are modified to $400\,\text{V}$ / $15\,\text{A}$, as shown in Fig. 16. The simulation model is the same, except for a change in the DC bus voltage and gate-timing to achieve the right current value. At $400\,\text{V}$ / $15\,\text{A}$ the voltage fall and rise times are $5\,\text{ns}$ and $8\,\text{ns}$, respectively. This corresponds to voltage transients during turn-on and turn-off of $64\,\text{V/ns}$ and $40\,\text{V/ns}$.

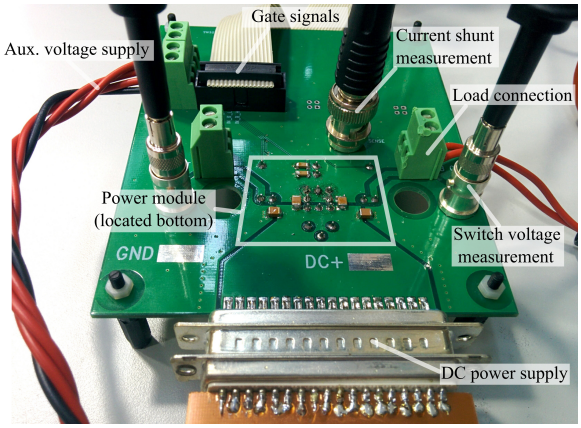

Fig. 14. Test board interfacing auxiliary voltage supply, gate control signals and BNC connector points for measurements of switching voltage and current shunt. The power module is located below the test board.

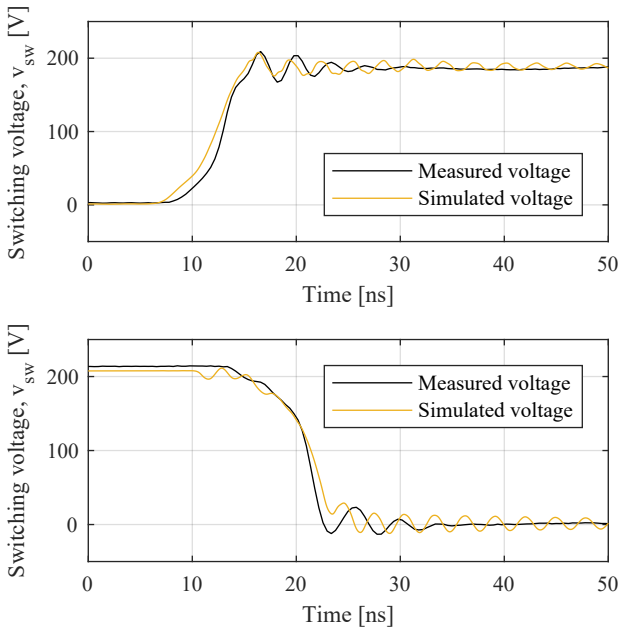

Fig. 15. Comparison of experimental and level 3 simulated waveforms of switch voltage during turn-off and turn-on at 200 V / 20 A.

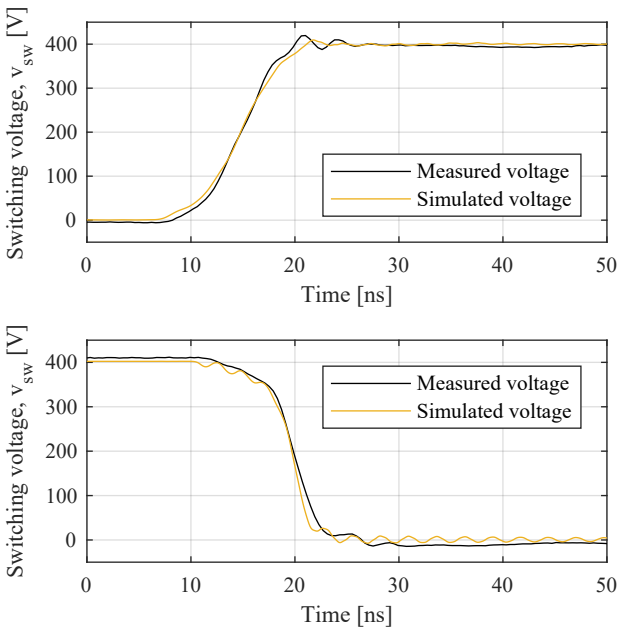

Fig. 16. Comparison of experimental and level 3 simulated waveforms of switch voltage during turn-off and turn-on at 400 V / 15 A.

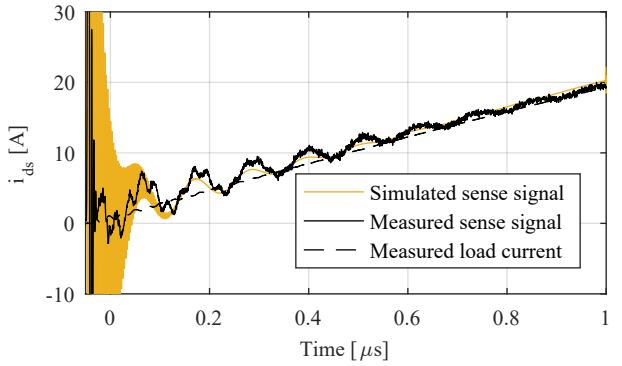

Fig. 17. Measured load current of inductor, measured sense current and level 3 simulated sense current.

In addition to verifying the switching voltage, it is also ensured that the shunt resistor array delivers accurate current measurements for control purposes, preferably without additional measurements and computational expensive compensations. The measured sense voltage is divided by 22 mΩ (now called measured sense signal). As an additional verification the current through the inductor is measured using a Teledyne LeCroy CP030 current probe, as a reference which is not affected by the high frequency ringing. The measured sense current, the measured inductor load current and the simulated sense current are shown in Fig. 17. The results highlight that due to damping in the circuit, the influence of inductive terms shown (7) are decayed after 1 μs, at which an accurate current measurement can be sampled. The initial high frequency oscillations are due to the power loop, indicated as i_1 in Fig. 9. The lower frequency ringing is due to ringing of the decoupling and main DC-link capacitors. As the GaN eHEMTs are switching, power is delivered from the decoupling capacitors, C_{De}, inside the power module and their voltage drop. Current i_2, as denoted in Fig. 9, conducts to charge the decoupling capacitors. When the two voltages are equal, current is still loaded in inductances, and thus charges the decoupling capacitors slightly above their initial 200 V. This causes an oscillating current, which experimentally is measured at a frequency of 8.8 MHz. This oscillation is correctly predicted by the simulation model. In general, the oscillations of the simulated response are less damped than the experimental results. This can be explained by the choice of using the DC resistance values in the exported RLC matrix from ANSYS Q3D Extractor. To solve this a frequency dependent resistance model should be implemented, such that the resistance is higher for increasing frequency due to the skin effect. However, in terms of the switching speed of both turn-on and turn-off voltage as well as its frequency and amplitude of oscillation this has minor impact. In conclusion the use of ANSYS Q3D Extractor provides a very good simulation result of the switching voltage transient.

VI. Conclusion

A hybrid PCB/DBC structure is proposed, designed for fast-switching and high power dissipation. In contrast to other hybrid methods, the proposed structure does not require embedding of dies and molding of PCBs on top of a DBC. The DBC, PCB and semiconductors are available from suppliers and only requires vapor phase soldering to assemble the stack, which decreases the manufacturing complexity.

A finite element simulation is used to assess the thermal characteristics of the power module, and the thermal resistance from junction to heatsink is evaluated as 2.4 K/W. ANSYS Q3D Extractor is used to extract the parasitics of the board, which are implemented in a SPICE solver. Three levels of simulation complexity were investigated. A level 1 simulation model only including self inductance, a level 2 model with a coupled RLC matrix and a level 3 which is also combined with SMD component parasitics, by using an impedance analyzer up to 2 GHz. The level 1 simulation case estimates 8 % higher loop inductance, when compared to the level 3 model. The experimental results verified the simulation model for the main switching voltage waveforms, and shows a turn-on and turn-off speed of both 6 ns during switching at 200 V / 20 A. By analyzing the resonance frequency, it is concluded that the achieved power loop inductance is 2.65 nH including current measurement circuitry. The level 3 simulation model provides the best approximation of the inductance seen from the experimental results, but takes two times longer to simulate when compared to level 1. The power module is tested at 400 V / 15 A, at which voltage fall and rise times of 5 ns and 8 ns are achieved, respectively. This equals a maximum dv/dt of 64 V/ns. The measured switching voltage waveform of the GaN eHEMT integrated power module shows low overshoot and ringing, which proves the proposed module structure and its accompanying board layout. Compared with other integrated power module structures, the proposed hybrid DBC/PCB power module structure performs well in terms of thermal performance, has very low commutation loop inductance and is relatively easy to manufacture.

REFERENCES

[1] D. Cooper, "Power Module Integration: A new approach," *IEEE Power Electronics Magazine*, vol. 3, no. 3, pp. 31–36, sep 2016.

[2] G. Deboy, O. Haeberlen, and M. Treu, "Perspective of Loss Mechanisms for Silicon and Wide Band-Gap Power Devices," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 2, pp. 89–100, 2017.

[3] P. Gammon, "Silicon and the Wide Bandgap Semiconductors, Shaping the Future Power Electronic Device Market," in *2013 14th International Conference on Ultimate Integration on Silicon (ULIS)*. IEEE, Mar 2013, pp. 9–13.

[4] H. Li and S. Munk-Nielsen, "Detail Study of SiC MOSFET Switching Characteristics," in *2014 IEEE 5th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, June 2014, pp. 1–5.

[5] S. Guo, L. Zhang, Y. Lei, X. Li, F. Xue, W. Yu, and A. Q. Huang, "3.38 Mhz Operation of 1.2kV SiC MOSFET with Integrated Ultra-Fast Gate Drive," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*. IEEE, nov 2015, pp. 390–395.

[6] S. Guo, L. Zhang, Y. Lei, X. Li, W. Yu, and A. Q. Huang, "Design and Application of a 1200V Ultra-Fast Integrated Silicon Carbide MOSFET Module," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, Mar 2016, pp. 2063–2070.

[7] P. Roussel and J. Azemar, "Technology, industry and market trends in WBG power module packaging," in *CIPS 2014; 8th International Conference on Integrated Power Electronics Systems*, 2014, pp. 1–3.

[8] W. W. Sheng and R. P. Colino, *Power Electronic Modules Design and Manufacture*. Boca Raton, Florida: CRC Press LLC, 2005.

[9] H. Shaowei, L. Que, L. Jian, and S. S. Ang, "Silicon Carbide Power Electronic Module Packaging," in *2015 16th International Conference on Electronic Packaging Technology (ICEPT)*. IEEE, Aug 2015, pp. 483–486.

[10] K. Takao and S. Kyogoku, "Ultra Low Inductance Power Module for Fast Switching SiC Power Devices," in *2015 IEEE 27th International Symposium on Power Semiconductor Devices IC's (ISPSD)*, May 2015, pp. 313–316.

[11] M. Meisser, D. Hamilton, and P. Mawby, "DCB-based Low-Inductive SiC Modules for High Frequency Operation," in *CIPS 2014; 8th International Conference on Integrated Power Electronics Systems*, Feb 2014, pp. 1–10.

[12] C. Neeb, J. Teichrib, R. W. D. Doncker, L. Boettcher, and A. Ostmann, "A 50 kW IGBT Power Module for Automotive Applications with Extremely Low DC-link Inductance," in *2014 16th European Conference on Power Electronics and Applications*, Aug 2014, pp. 1–10.

[13] M. Schmenger, M. Meisser, D. Hamilton, B. Leyrer, M. Bernd, P. Mawby, and T. Blank, "Highly Integrated Power Modules Based on Copper Thick-Film-on-DCB for High Frequency Operation of SiC Semiconductors - Design and Manufacture," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Sept 2015, pp. 1–8.

[14] R. Randoll, W. Wondrak, and A. Schletz, "Dielectric Strength and Thermal Performance of PCB-Embedded Power Electronics," *Microelectronics Reliability*, vol. 54, no. 9-10, pp. 1872–1876, sep 2014.

[15] D. Kearney, S. Kicin, E. Bianda, A. Krivda, D. Bauman, and A. B. B. Corporate, "PCB Embedded Power Electronics for Low Voltage Applications," in *CIPS 2016 - 9th International Conference on Integrated Power Electronics Systems*, 2016, pp. 3–8.

[16] C. F. Bayer, U. Waltrich, A. Soueidan, R. Schneider, E. Baer, and A. Schletz, "Enhancement of the Partial Discharge Inception Voltage of DBCs by Adjusting the Permittivity of the Encapsulation," in *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*, 2016, pp. 1–5.

[17] H. Hourdequin, L. Laudebat, M.-L. Locatelli, and P. Bidan, "Design of Packaging Structures for High Voltage Power Electronics Devices: Electric field Stress on Insulation," in *2016 IEEE International Conference on Dielectrics (ICD)*, vol. 2. IEEE, jul 2016, pp. 999–1002.

[18] L. Zhang, P. Liu, A. Q. Huang, S. Guo, and R. Yu, "An Improved SiC MOSFET-Gate Driver Integrated Power Module with Ultra Low Stray Inductances," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Oct 2017, pp. 342–345.

[19] M. Meisser, M. Schmenger, M. Bernd, B. Leyrer, H. Demattio, D. Hamilton, P. Mawby, and T. Blank, "Highly Integrated SiC Module with Thick-Film Dielectric Allows for High Frequency Operation," in *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*, March 2016, pp. 1–6.

[20] E. Hoene, A. Ostmann, B. T. La, C. Marczok, A. Musing, and J. W. Kolar, "Ultra-Low-Inductance Power Module for Fast Switching Semiconductors," in *Proceedings of the PCIM Europe Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany,*, May 2013.

[21] O. Kreutzer, B. Eckardt, and M. Maerz, "Optimum Gate Driver Design to Reach SiC-MOSFETs Full Potential - Speeding up to 200 kV/us," in *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Blacksburg, VA, 2015, pp. 41–46.

[22] K. Klein, E. Hoene, R. Reiner, and R. Quay, "Study on packaging and driver integration with gan switches for fast switching," in *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*, March 2016, pp. 1–6.

[23] G. Feix, E. Hoene, O. Zeiter, and K. Pedersen, "Embedded Very Fast Switching Module for SiC Power MOSFETs," in *Proceedings of PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Nuremberg, Germany, 2015, pp. 1–7.

[24] GaN Systems Inc, "Top-side cooled 650 V E-mode GaN transistor." [Online]. Available: http://www.gansystems.com/datasheets/GS66508T DS Rev 171101.pdf

[25] F. Zhao, Y. Li, Q. Tang, and L. Wang, "Analysis of Oscillation in Bridge Structure Based on GaN Devices and Ferrite Bead Suppression Method," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE*, 2017, pp. 391–398.

[26] R. Matsumoto, K. Umetani, and E. Hiraki, "Optimization of the Balance between the Gate-Drain Capacitance and the Common Source Inductance for Preventing the Oscillatory False Triggering of Fast Switching GaN-FETs," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 405–412.

[27] K. Umetani, K. Yagyu, and E. Hiraki, "A Design Guideline of Parasitic Inductance for Preventing Oscillatory False Triggering of Fast Switching GaN-FET," *IEEJ Transactions on Electrical and Electronic Engineering*, vol. 11, pp. S84–S90, 2016.

[28] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Springer US, 2001.

[29] GaN Systems Inc, "GN001 Application Guide Design with GaN Enhancement mode HEMT." [Online]. Available: http://www.gansystems.com/whitepapers.php

[30] E. Gurpinar, F. Iannuzzo, Y. Yang, A. Castellazzi, and F. Blaabjerg, "Design of Low Inductance Switching Power Cell for GaN HEMT Based Inverter," *IEEE Transactions on Industry Applications*, vol. 9994, no. c, pp. 1–1, 2017.

[31] C. New, A. N. Lemmon, and A. Shahabi, "Comparison of Methods for Current Measurement in WBG Systems," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2017, pp. 87–92.

[32] J. C. Hernandez, L. P. Petersen, M. A. E. Andersen, and N. H. Petersen, "Ultrafast Switching Superjunction MOSFETs for Single Phase PFC Applications," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, March 2014, pp. 143–149.

[33] A. Anthon, J. C. Hernandez, Z. Zhang, and M. A. E. Andersen, "Switching Investigations on a SiC MOSFET in a TO-247 Package," in *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, Oct 2014, pp. 1854–1860.

[34] E. Shelton, N. Hari, X. Zhang, T. Zhang, J. Zhang, and P. Palmer, "Design and Measurement Considerations for WBG Switching Circuits," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, no. 1, 2017, pp. 1–10.

[35] Wolfspeed, "CPM2-1200-0040B." [Online]. Available: https://www.wolfspeed.com/power/products/sic-mosfets/cpm2-1200-0040b

[36] C. Qian, A. M. Gheitaghy, J. Fan, H. Tang, B. Sun, H. Ye, and G. Zhang, "Thermal Management on IGBT Power Electronic Devices and Modules," *IEEE Access*, vol. 6, pp. 12 868–12 884, 2018.

[37] I. Mudawar, D. Bharathan, K. Kelly, and S. Narumanchi, "Two-Phase Spray Cooling of Hybrid Vehicle Electronics," *IEEE Transactions on Components and Packaging Technologies*, vol. 32, no. 2, pp. 501–512, June 2009.

[38] R. Skuriat and C. M. Johnson, "Direct Substrate Cooling of Power Electronics," in *5th International Conference on Integrated Power Electronics Systems*, March 2008, pp. 1–5.

[39] ANSYS, Inc., "ANSYS Q3D Extractor." [Online]. Available: http://www.ansys.com/products/electronics/ansys-q3d-extractor

[40] F. Yang, Z. Liang, Z. J. Wang, and F. Wang, "Parasitic Inductance Extraction and Verification for 3D Planar Bond All Module," in *2016*

International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM), vol. 5, no. 3, 2016.

[41] P. D. Reigosa, F. Iannuzzo, S. Munk-Nielsen, and F. Blaabjerg, "New Layout Concepts in MW-scale IGBT modules for Higher Robustness During Normal and Abnormal Operations," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2016, pp. 288–294.

[42] L. Popova, R. Juntunen, T. Musikka, M. Lohtander, P. Silventoinen, O. Pyrhonen, and J. Pyrhonen, "Stray Inductance Estimation with Detailed Model of the IGBT Module," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, Sept 2013, pp. 1–8.

[43] A. B. Jørgensen, N. Christensen, D. N. Dalal, S. D. Sønderskov, S. Bęczkowski, C. Uhrenfeldt, and S. Munk-Nielsen, "Reduction of Parasitic Capacitance in 10 kV SiC MOSFET Power Modules Using 3D FEM," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Sept 2017, pp. P.1–P.8.

[44] Y. Ren, X. Yang, F. Zhang, L. Wang, K. Wang, W. Chen, X. Zeng, and Y. Pei, "Voltage Suppression in Wire-Bond-Based Multichip Phase-Leg SiC MOSFET Module Using Adjacent Decoupling Concept," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8235–8246, Oct 2017.

[45] S. Beczkowski, A. B. Jørgensen, H. Li, C. Uhrenfeldt, X. Dai, and S. Munk-nielsen, "Switching Current Imbalance Mitigation in Power Modules with Parallel Connected SiC MOSFETs," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 2017, pp. 1–8.

[46] Y. Ren, X. Yang, F. Zhang, L. Tan, and X. Zeng, "Analysis of a Low-Inductance Packaging Layout for Full-SiC Power Module Embedding Split Damping," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2016, pp. 2102–2107.

[47] GaN Systems Inc, "GN006 App Note SPICE model for GaN HEMT - usage guidelines and example." [Online]. Available: http://www.gansystems.com/whitepapers.php

[48] K. Wang, X. Yang, L. Wang, and P. Jain, "Instability Analysis and Oscillation Suppression of Enhancement-Mode GaN Devices in Half-Bridge Circuits," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1585–1596, Feb 2018.

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