Switching current imbalance mitigation in power modules with parallel connected SiC MOSFETs

Beczkowski, Szymon; Jørgensen, Asger Bjørn; Li, Helong; Uhrenfeldt, Christian; Dai, Xiaoping; Munk-Nielsen, Stig

Published in:
Proceedings of 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)

DOI (link to publication from Publisher):
10.23919/EPE17ECCEEurope.2017.8099245

Publication date:
2017

Document Version
Accepted author manuscript, peer reviewed version

"Switching current imbalance mitigation in power modules with parallel connected SiC MOSFETs"

by S. Bęczkowski, A. B. Jørgensen, H. Li, C. Uhrenfeldt, X. Dai and S. Munk-Nielsen

This is a post-print of a paper published at 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe). The final published version is available at the IEEE Xplore Digital Library: https://ieeexplore.ieee.org/document/8099245

Citation for published version:
S. Bęczkowski, A. B. Jørgensen, H. Li, C. Uhrenfeldt, X. Dai and S. Munk-Nielsen, "Switching current imbalance mitigation in power modules with parallel connected SiC MOSFETs," *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Warsaw, 2017, pp. P.1-P.8.

Switching current imbalance mitigation in power modules with parallel connected SiC MOSFETs

Szymon Bęczkowski[1], Asger Bjørn Jørgensen[1], Helong Li[2],
Christian Uhrenfeldt[1], Xiaoping Dai[2], Stig Munk-Nielsen[1]

[1] Department of Energy Technology
Aalborg University
Aalborg, Denmark
{sbe,abj,chu,smn}@et.aau.dk

[2] DYNEX Semiconductor
Lincoln, United Kingdom
{helong.li,andy.dai}@dynexsemi.com

Keywords

packaging, power semiconductor device, silicon carbide (SiC), parallel operation

Abstract

Multichip power modules use parallel connected chips to achieve high current rating. Due to a finite flexibility in a DBC layout, some electrical asymmetries will occur in the module. Parallel connected transistors will exhibit uneven static and dynamic current sharing due to these asymmetries. Especially important are the couplings between gate and power loops of individual transistors. Fast changing source currents cause gate voltage imbalances yielding uneven switching currents. Equalizing gate voltages seen by paralleled transistors, done by adjusting source bond wires, is proposed in this paper. Analysis is performed on an industry standard DBC layout using numerically extracted module parasitics. The method of tuning individual source inductances shows clear improvement in dynamic current balancing and prevents excessive current overshoot during transistors turn-on.

Introduction

Due to relatively low current ratings of individual SiC power MOSFET dies, many chips need to be paralleled to obtain the desired module current rating. Power modules used in mid- to high-power applications require nominal currents in the range of hundreds to thousands of amps. Taking into account mechanical limitations, in order to achieve this high current rating, modules are typically built as a parallel connection of multiple substrate subassemblies [1],[2]. Each of the subassemblies may, in term, house several paralleled transistor dies.

Power module design is often a compromise between thermal and electrical performance. A fully symmetric current module would experience perfect current sharing and thermal stress between semiconductors. Because of various constraints, some asymmetries will be present in a package due to e.g. thermal or mechanical constraints, DBC layout limitations and final product price.

Asymmetries in the power module design and variations in electrical parameters of individual chips (e.g. threshold voltage) may lead to static or dynamic current sharing imbalances [3]–[5]. Moreover, electrical couplings between power and gate paths may produce a similar effect [6]. In turn, non-uniform heating or electrical stress may be seen by the transistors causing some of the devices to fail faster. One way to protect against it is to de-rate the power module, which leads to poor utilization of semiconductors.

One such coupling can be seen in the layout shown in figure 1a. Part of the source path of the DBC layout is shared by both gate and power loops. This kind of coupling is sometimes introduced on purpose in order to add a negative feedback path to a gate loop [7]. This feedback slows down the switching, which may be necessary to keep the power module stable and lower the generated EMI.

a) b)

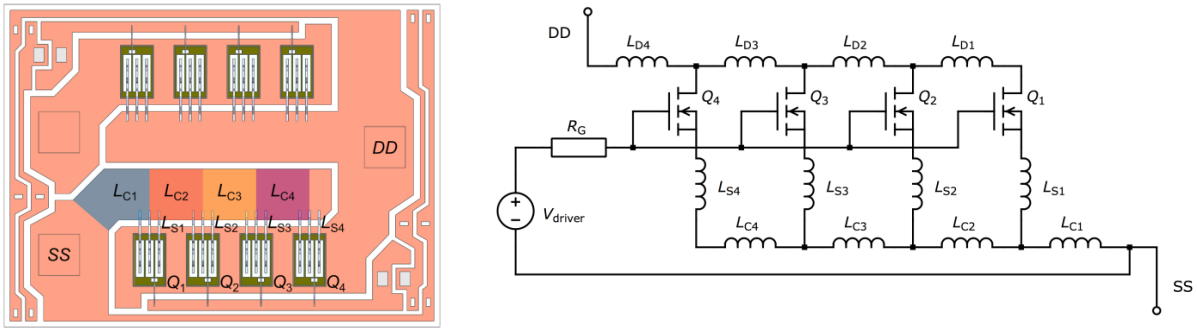

Fig. 1. A multichip half-bridge power module with four parallel connected SiC MOSFETs: a) DBC layout; b) lumped simulation model used for analysis.

A drawback of such a connection is that a complex interaction between the individual source currents and parasitic inductances of the DBC is created [6]. A current coupling effect causes imbalance in gate-source voltages seen by the parallel connected MOSFETs, resulting in big dynamic current differences. This paper proposes a possible solution to the presented problem by purposefully increasing some of the inductances in the layout and mitigating the dynamic current sharing issue.

Transient current imbalance

Analysing the voltage loops of the DBC layout shown in figure 1b, the equation for the gate voltage, seen by the *n*-th transistor, can be written as:

$$v_{\mathrm{GS}n} = v_{\mathrm{driver}} - R_{\mathrm{G}} \cdot i_{\mathrm{G}} - v'_{\mathrm{LS}n} \tag{1}$$

where $v'_{\mathrm{LS}n}$ is the total voltage contribution from voltage drops on parasitic inductances in the circuit. These voltage drops are caused by fast-changing currents flowing through bond-wires and common parts of the DBC marked in the figure 1b as $L_{\mathrm{S}n}$ and $L_{\mathrm{C}n}$ respectively. E.g. for the Q_2 transistor, the v'_{LS2} voltage drop is caused by currents flowing through L_{S2}, L_{C2} and L_{C1}:

$$v'_{\mathrm{LS2}} = L_{\mathrm{S2}} \frac{\mathrm{d}i_{\mathrm{S2}}}{\mathrm{d}t} + L_{\mathrm{C2}} \frac{\mathrm{d}(i_{\mathrm{S4}} + i_{\mathrm{S3}} + i_{\mathrm{S2}})}{\mathrm{d}t} + L_{\mathrm{C1}} \frac{\mathrm{d}(i_{\mathrm{S4}} + i_{\mathrm{S3}} + i_{\mathrm{S2}} + i_{\mathrm{S1}})}{\mathrm{d}t} \tag{2}$$

and is generalized to:

$$v'_{\mathrm{LS}n} = L_{\mathrm{Sn}} \frac{\mathrm{d}i_{\mathrm{Sn}}}{\mathrm{d}t} + \sum_{m=1}^{n} L_{\mathrm{Cm}} \frac{\mathrm{d}}{\mathrm{d}t} \sum_{p=m}^{k} i_{\mathrm{Sp}} \tag{3}$$

for *k* parallel connected chips. Collecting all gate loops' equations in matrix form yields [6]:

$$\begin{bmatrix} v'_{\mathrm{LS1}} \\ v'_{\mathrm{LS2}} \\ v'_{\mathrm{LS3}} \\ v'_{\mathrm{LS4}} \end{bmatrix} = \begin{bmatrix} L_{\mathrm{C1}} + L_{\mathrm{S1}} & L_{\mathrm{C1}} & L_{\mathrm{C1}} & L_{\mathrm{C1}} \\ L_{\mathrm{C1}} & L_{\mathrm{C1}} + L_{\mathrm{C2}} + L_{\mathrm{S2}} & L_{\mathrm{C1}} + L_{\mathrm{C2}} & L_{\mathrm{C1}} + L_{\mathrm{C2}} \\ L_{\mathrm{C1}} & L_{\mathrm{C1}} + L_{\mathrm{C2}} & L_{\mathrm{C1}} + L_{\mathrm{C2}} + L_{\mathrm{C3}} + L_{\mathrm{S3}} & L_{\mathrm{C1}} + L_{\mathrm{C2}} + L_{\mathrm{C3}} \\ L_{\mathrm{C1}} & L_{\mathrm{C1}} + L_{\mathrm{C2}} & L_{\mathrm{C1}} + L_{\mathrm{C2}} + L_{\mathrm{C3}} & L_{\mathrm{C1}} + \ldots + L_{\mathrm{C4}} + L_{\mathrm{S4}} \end{bmatrix} \cdot \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{\mathrm{S1}} \\ i_{\mathrm{S2}} \\ i_{\mathrm{S3}} \\ i_{\mathrm{S4}} \end{bmatrix} \tag{4}$$

Each transistor will see different gate-source voltage during switching, caused by fast changing currents flowing through $L_{\mathrm{C}n}$ inductances, yielding dynamic current imbalance. To achieve equal current sharing during switching, the gate-source voltages seen by all four paralleled chips need to be the same. In order to do that, the $v'_{\mathrm{LS}n}$ voltage drops need to be kept equal during switching. Taking the two constrains into account: equal $v'_{\mathrm{LS}n}$ voltages and equal $i_{\mathrm{S}n}$ currents, in order to balance the equation, the sums of rows in the inductance matrix in equation 4 also need to be equal.

For clarity of analysis, a simplification $L_{\mathrm{C}} = L_{\mathrm{C1}} = L_{\mathrm{C2}} = L_{\mathrm{C3}} = L_{\mathrm{C4}}$ is done, as the corresponding DBC segments are similar (see fig. 1a). Balancing the inductance matrix is performed by adjusting the L_{Sn} inductances. In practice, this means adjusting the inductances of die source bond-wires. The matrix can also be balanced by changing the L_{Cn} inductances but this means adjusting the layout of the DBC. As bond-wires can be controlled much easier they were chosen as the control variables. The bond-wire inductance can be controlled by the wire shape and bond feet location. Moreover, wire bonds can be reworked, thus allowing fast hardware prototype iterations.

Rewriting equation 4, under the condition that all currents are equal, the sums of rows of inductance matrix are expressed as effective source inductances L'_{Sn} seen by the transistors:

$$\begin{bmatrix} v'_{\mathrm{LS1}} \\ v'_{\mathrm{LS2}} \\ v'_{\mathrm{LS3}} \\ v'_{\mathrm{LS4}} \end{bmatrix} = \begin{bmatrix} L'_{\mathrm{S1}} & 0 & 0 & 0 \\ 0 & L'_{\mathrm{S2}} & 0 & 0 \\ 0 & 0 & L'_{\mathrm{S3}} & 0 \\ 0 & 0 & 0 & L'_{\mathrm{S4}} \end{bmatrix} \cdot \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} i_{\mathrm{S1}} \\ i_{\mathrm{S2}} \\ i_{\mathrm{S3}} \\ i_{\mathrm{S4}} \end{bmatrix} \tag{5}$$

where

$$\begin{cases} L'_{\mathrm{S1}} = L_{\mathrm{S1}} + 4L_{\mathrm{C}} \\ L'_{\mathrm{S2}} = L_{\mathrm{S2}} + 7L_{\mathrm{C}} \\ L'_{\mathrm{S3}} = L_{\mathrm{S3}} + 9L_{\mathrm{C}} \\ L'_{\mathrm{S4}} = L_{\mathrm{S4}} + 10L_{\mathrm{C}} \end{cases} \tag{6}$$

Refactoring equation 4 to the form of equation 5 is similar to simplifying a signal flow graph in control engineering. As shown in figure 2, all contributions from L_{Cn} voltage drops are pushed to effective source inductances $L'_{\mathrm{S}n}$. The transistors can then be easily individually analyzed. It is also clearly visible that by equalizing effective source inductance L'_{Sn} values, the gate loops become electrically identical.

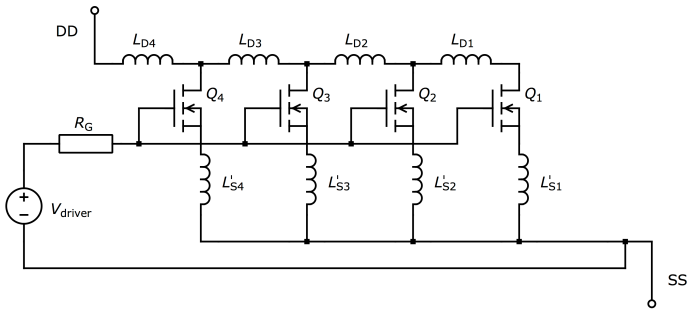

Fig. 2. Lumped model of a DBC layout with L_{Cn} and L_{Sn} inductances from figure 1b merged into effective L'_{Sn} inductances.

Equalization of the effective source bond wire inductance is performed by extending the bond wire loop thus effectively increasing their inductance. Equation 6 predicts, that transistor Q_4 sees the highest effective source inductance therefore any inductance increase should be performed on $Q_1 \ldots Q_3$ transistors. L_{S4} is kept at its simulated nominal value of 0.75nH. L_{S1}, L_{S2} and L_{S3} values are adjusted with respect to L_{S4} inductance. With the set of equations 6, in order to satisfy the symmetry condition $L'_{\mathrm{S1}} = L'_{\mathrm{S2}} = L'_{\mathrm{S3}} = L'_{\mathrm{S4}}$, the source bond-wires need to be adjusted to the following values:

$$\begin{cases} L'_{\mathrm{S1}} = L_{\mathrm{S4}} + 10L_{\mathrm{C}} \\ L'_{\mathrm{S2}} = L_{\mathrm{S4}} + 10L_{\mathrm{C}} \\ L'_{\mathrm{S3}} = L_{\mathrm{S4}} + 10L_{\mathrm{C}} \\ L'_{\mathrm{S4}} = L_{\mathrm{S4}} + 10L_{\mathrm{C}} \end{cases} \text{ and (6) } \Rightarrow \begin{cases} L_{\mathrm{S1}} = L_{\mathrm{S4}} + 6L_{\mathrm{C}} \\ L_{\mathrm{S2}} = L_{\mathrm{S4}} + 3L_{\mathrm{C}} \\ L_{\mathrm{S3}} = L_{\mathrm{S4}} + L_{\mathrm{C}} \end{cases} \tag{7}$$

This means, that by adding some inductance to all but one set of source bond-wires, a balanced DBC layout, where each transistor "sees" the same source inductance, can be achieved. This, however, may negatively affect the switching speeds and, in turn, switching losses of the module.

These equations can be generalized to modules with similar layout with different number of power transistors connected in parallel. The maximum added inductance to Q_1 transistor depends on the number of paralleled chips:

$$L_{S1} = L_{Sn} + \left[\left(\sum_{i=1}^{n} n\right) - n\right] L_C \tag{8}$$

for n chips connected in parallel. The multiplier for L_C inductances is {0, 1, 3, 6, 10, 15} for {1, 2, 3, 4, 5, 6} dies connected in parallel. This limits the usefulness of this method to either a relatively small number of paralleled chips or to DBC layouts with very small L_C inductance value.

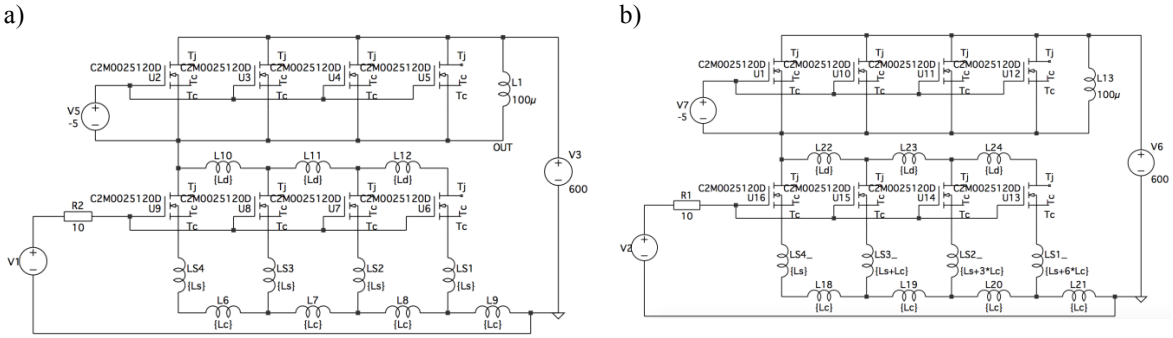

Fig. 3. Simulation models of: a) imbalanced DBC layout; b) DBC balanced with modified L_{Sn} inductances

The method was simulated in LTspice. Four SiC power MOSFETs are connected in parallel to form a half bridge module [8]. In order to compare the applicability of the method two configurations were compared: one with imbalanced DBC layout (fig. 3a) and one with source inductances modified according to equation 7 (fig. 3b).

Results, shown in figure 4, illustrate significantly improved dynamic current sharing in the balanced layout. This is especially visible in case of Q_1 (the transistor that shares the least of the common path), where a substantial overshoot is removed after balancing. Comparing the turn-on and turn-off events for the imbalanced case, one can notice that the transistors that turn-off the fastest also turn-on the slowest. Another visible difference is that the balanced transistors, on average, switch slower. This is attributed to the added inductance in the system and might be compensated by changing the gate resistance.

This simplified analysis proves that the interaction between gate and power paths in a multichip power module is crucial to achieving good dynamic current sharing and that there is a possibility of improving the sharing by a simple bondwire length change. However, more complex interactions, like magnetic coupling between inductances were not modelled. In order to validate the method with a higher degree of certainty a more complex DBC model needs to be used.

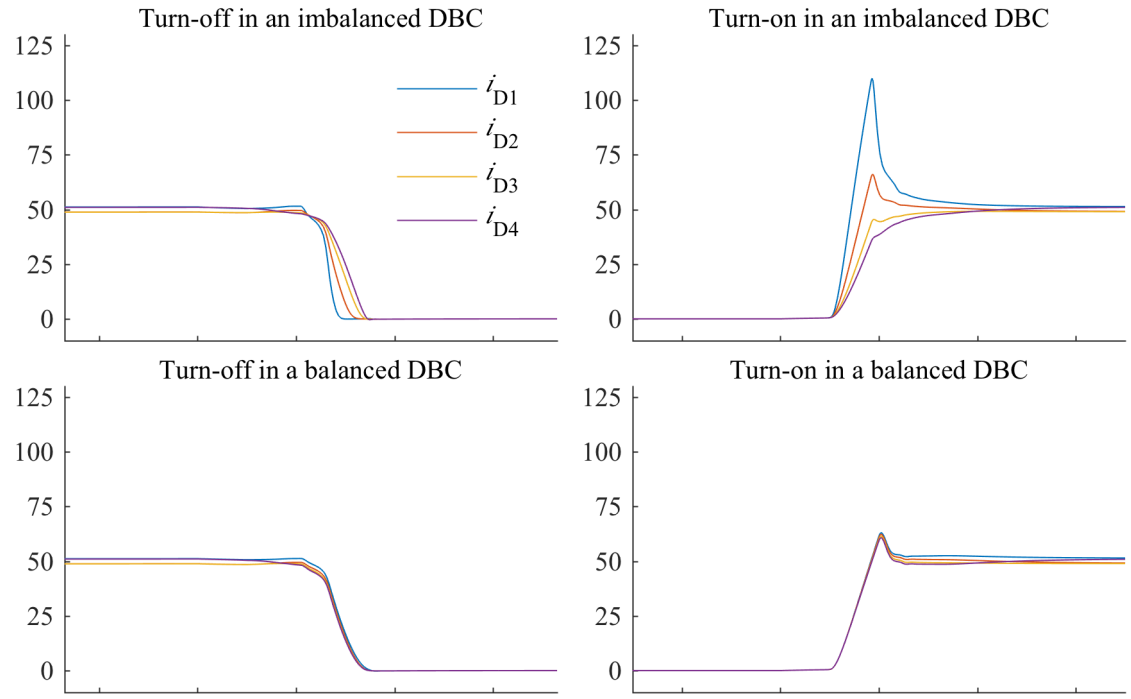

Fig. 4. Switching currents for the two simulated cases of imbalanced and balanced DBC layouts. Time base 200ns/div.

DBC simulations using extracted parasitic model

The simplified models of DBC layouts presented in the previous section do not include many of the couplings present in a real system. In order to verify the method a parasitic extraction was performed on a 3D model of the power module using ANSYS Q3D Extractor software.

With the presented module layout, the L_C inductance is approximately equal to 1.1nH and L_{S4} is equal to 0.75nH. L_{S1} ... L_{S4} values predicted by the equation 7, for this DBC layout should be 7.35, 4.05, 1.85 and 0.75nH. Achieving the higher inductance values for the bondwires is not easy. Increasing the wire loop may compromise the mechanical stability of the wire as well as yield an increase in DC resistance. This, in turn, may impact reliability of the power module.

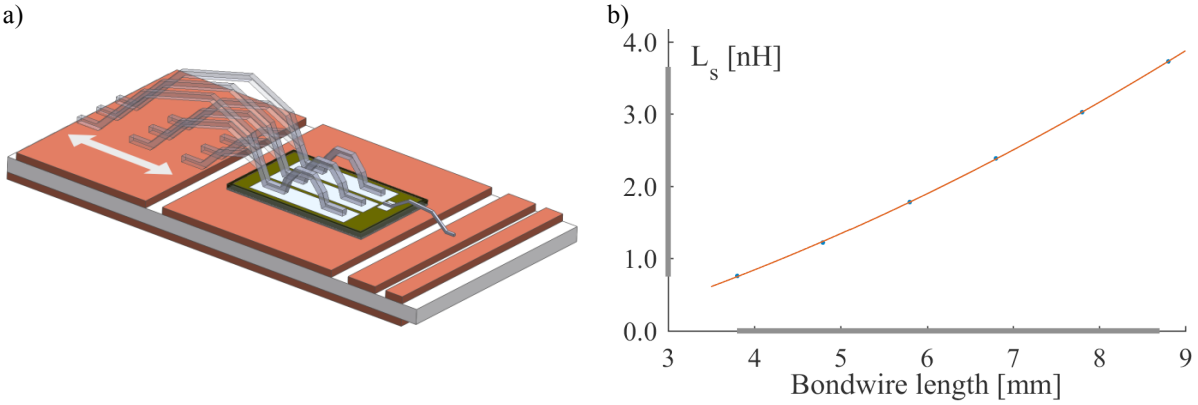

Fig. 5. Adjustable bondwire: a) geometry used in the 3D model; b) source bondwires' inductance as a function on the variable loop length, simulated in Q3D.

A simple adjustable bondwire loop model was created (fig. 5a) and the inductance of the source bond wires triplet was then analysed as a function of the loop length (fig. 5b). Within the DBC layout limitations (bondwire length 3.8–8.7mm), source bondwires' inductance is in the range of 0.75–3.8nH. This means by increasing the bondwire length to its maximum 8.7mm value would only contribute an increase of only $2.64L_C$, far less than the required $6L_C$ for Q_1 (eq. 7). It is clear that this specific DBC layout cannot be fully compensated simply by adjusting the source bond wire lengths. However, a comparison between original DBC layout and a semi-compensated one will be performed to assess the qualitative change in dynamic current sharing between the two cases shown in figure 6.

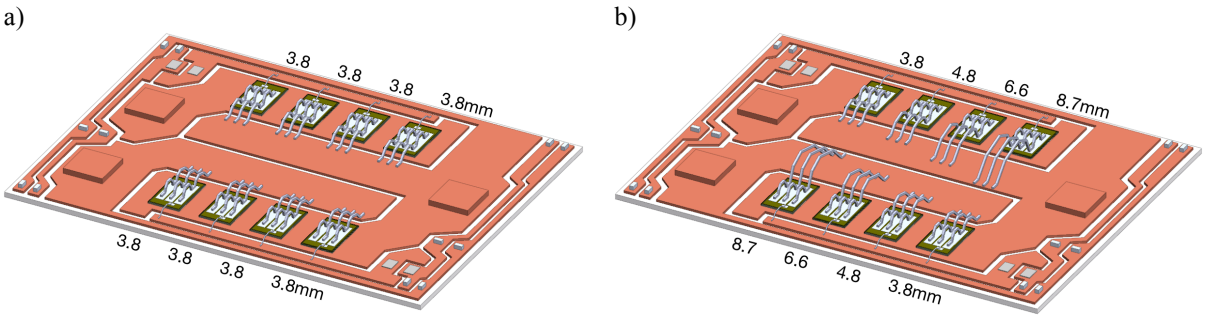

Fig. 6. DBC layouts: a) original; b) with adjusted source bondwires.

Calculated L_{S1} ... L_{S4} values were scaled linearly to fit within the possible values for the bondwires yielding 3.80, 2.28, 1.26 and 0.75nH that correspond to 8.7, 6.6, 4.8 and 3.8mm wire loops. A Q3D simulation was performed to extract the inductance matrix of the adjusted layout. A Spice model was created in the Q3D software and imported to LTspice. A CP2M-1200-0025B transistor model provided by the manufacturer was used in the simulations. Results, shown in figure 7, present a well-balanced turn-off and turn-on events.

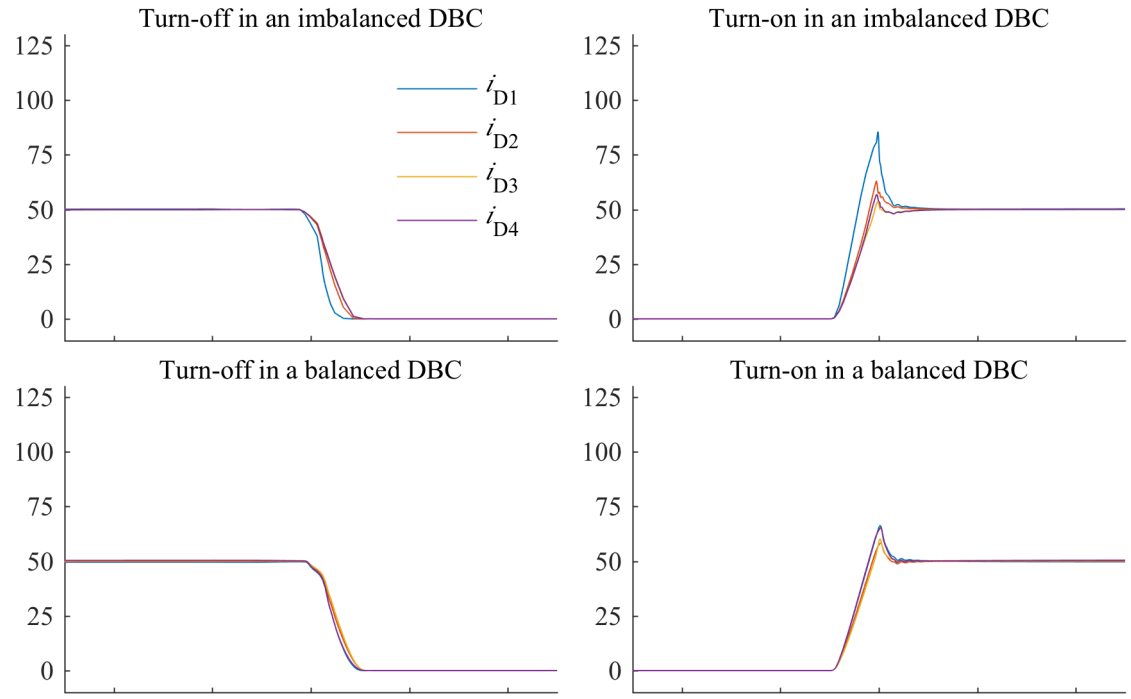

Fig. 7. Switching currents for the two simulated cases of imbalanced and balanced DBC layouts. Parasitics exctracted with Q3D. Time base 200ns/div.

Table 1. Peak current overshoot in imbalanced and balanced DBC layouts.

DBC	Q1	Q2	Q3	Q4
imbalanced	76.8%	26.2%	0.7%	1.2%
balanced	32.4%	16.0%	20.2%	30.4%

Especially noticeable, in the simulation results from figure 7, are the balanced overcurrents. Table 1 presents the achieved overcurrent equalisation in a numerical form. Differences in overcurrents in the imbalanced DBC will cause the turn-on and turn-off switching losses to be unequally distributed between the chips.

Table 2. Switch losses in imbalanced and balanced DBC layouts. All values in mJ.

	DBC	Q1	Q2	Q3	Q4	total
turn-off losses	imbalanced	**0.74**	1.16	1.30	1.28	4.48
	balanced	1.07	1.22	1.29	1.01	4.59 (+2.5%)
turn-on losses	imbalanced	**2.67**	1.84	1.62	1.68	7.81
	balanced	2.19	1.96	1.89	2.20	8.24 (+5.5%)
total losses	imbalanced	**3.41**	3.00	2.92	2.96	12.29
	balanced	3.26	3.18	3.18	3.21	12.83 (+4.4%)

Table 2 shows the simulated turn-on and turn-off losses. There is a slight increase in total switching losses in the case for the balanced DBC (an increase of 4.4% of total losses). As previously noted, this is expected due to increased inductances in the module. The module is balanced by slowing down the fastest switching semiconductors. This can be compensated by lowering the external gate resistors.

Another observation based on the presented data is that, in the imbalanced DBC layout, transistor Q_1 experiences ca. 15% higher total losses than the other transistors and, at the same time, experiences the highest overcurrent during turn-on. This means that this transistor will experience higher operating temperature compared to the other transistors.

Conclusions

The analysis, presented in this paper, focuses on dynamic current sharing between paralleled transistors in an industry standard DBC layout. The layout is typical for power modules with DC power terminals on one side and output terminal of a half-bridge on the other side of a DBC.

The DBC layout greatly affects the switching performance of multichip power modules. Gate and power loops of parallel-connected power transistors may share common inductance in the source terminal. When this happens, one needs to analyze the effective source inductance seen by each of the transistors. If the inductances are not equal, the DBC layout is imbalanced and the dynamic current sharing performance will be poor.

By inserting additional inductance into source connections of individual dies a balanced layout is achieved. Both simplified circuit model and model extracted using Q3D software support the proposed hypothesis. For simplicity, the adjustment procedure presented in this paper used only source bond wire length change. In practice, many other parameters may be modified to achieve similar results. A designer may change the DBC layout, die placement, bond wire geometry (loop shape and individual bond positions).

Turn-on and turn-off losses are found to be different for different paralleled chips in the imbalanced layout. This effect is attributed to different switching speeds of individual dies. By matching the effective source inductances their switching speeds are equalized therefore transistor switching losses are also balanced. Overall power module losses were marginally increased.

References

[1] Schnell, R., Hartmann, S., Truessel, D., Fischer, F., Baschnagel, A., & Rahimo, M. (2015, May). LinPak, a new low inductive phase-leg IGBT module with easy paralleling for high power density converter designs. In *PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of* (pp. 1-8).

[2] Schilling, O., Wölz, M., Borghoff, G., Nübel, T., Bräker, G., & Lübke, C. (2005). Properties of a new PrimePACK™ IGBT module concept for optimized electrical and thermal interconnection to a modern converter environment. In *PCIM Europe* (pp. 7-9).

[3] Sadik, D. P., Colmenares, J., Peftitsis, D., Lim, J. K., Rabkowski, J., & Nee, H. P. (2013, September). Experimental investigations of static and transient current sharing of parallel-connected silicon carbide MOSFETs. In *Power Electronics and Applications (EPE), 2013 15th European Conference on* (pp. 1-10). IEEE.

[4] Li, H., Munk-Nielsen, S., Wang, X., Maheshwari, R., Bęczkowski, S., Uhrenfeldt, C., & Franke, W. T. (2016). Influences of device and circuit mismatches on paralleling silicon carbide MOSFETs. *IEEE Transactions on Power Electronics*, *31*(1), 621-634.

[5] Cui, Y., Chinthavali, M. S., Xu, F., & Tolbert, L. M. (2012, May). Characterization and modeling of silicon carbide power devices and paralleling operation. In *Industrial Electronics (ISIE), 2012 IEEE International Symposium on* (pp. 228-233). IEEE.

[6] Li, H., Bęczkowski, S., Munk-Nielsen, S., Maheshwari, R., & Franke, T. (2015, May). Circuit mismatch and current coupling effect influence on paralleling SiC MOSFETs in multichip power modules. In *PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of* (pp. 1-8).

[7] Li, H., Munk-Nielsen, S., Wang, X., Bęczkowski, S., Jones, S. R., & Dai, X. (2017). Effects of Auxiliary-Source Connections in Multichip Power Module. *IEEE Transactions on Power Electronics*, *32*(10), 7816-7823.

[8] Wolfspeed (Sep. 2016), CPM2-1200-0025B Available: http://www.wolfspeed.com/cpm2-1200-0025b