# Double Deadbeat Plus Repetitive Control Scheme for Microgrid System

Madichetty, S.; Basu, M.; Mishra, S.; Guerrero, J. M.

*Published in:*
IEEE Systems Journal

*DOI (link to publication from Publisher):*
10.1109/JSYST.2018.2875543

*Publication date:*
2019

*Document Version*
Accepted author manuscript, peer reviewed version

# Double Deadbeat Plus Repetitive Control Scheme for Microgrid System

Sreedhar Madichetty, *Member, IEEE*, Malabika Basu, *Member, IEEE*, Sukumar Mishra, *Senior Member, IEEE*, and Josep M. Guerrero, *Fellow, IEEE*

***Abstract*—Parallel connection of converters is a convenient choice when system capacity is to be increased. Parallel-connected voltage source converters, especially neutral point clamped converters, are one of the best choices for its range. However, with the parallel connectivity, the converter possesses a circulating current in its legs, which consequently threatens the safe operation of the system. To alleviate this circulating current problem, in this paper, a double deadbeat (DD) plus repetitive control (RC) scheme is proposed. The RC scheme is employed to mitigate the circulating currents and the DD loop control scheme is employed to achieve a high operating bandwidth for voltage and current characteristics. Furthermore, the DD loop is associated with an adaptive controlling technique, which adjusts internally by itself and provides better performance for nonlinear loads. The proposed DD method forces the equivalent system elements to be placed outside the closed loop, which does not affect the system stability. Initially, the system has been executed with a conventional proportional + integral scheme and then with the proposed DD + RC scheme. The proposed method is verified by implementing a Simulink model in the OPAL-RT platform. Furthermore, the proposed method is built with a prototype, and its results are explored.**

***Index Terms*—Deadbeat control (DB) scheme, microgrids, parallel converters, repetitive control scheme.**

## I. Introduction

PARALLEL power converters are one of the convenient ways to increase the power rating of the systems, where reliability and efficiency can also be increased to a great extent. Pulsewidth modulation (PWM) based converters for drives application, grid-connected inverters, uninterrupted power supply systems, and distributed generation based microgrid system are typical application areas, where the paralleling concept of the converters/inverters can be used effectively [1]–[6]. Neutral point clamped converters (NPCCs) are a preferred topology for medium voltage ranges, which effectively improves the system level output voltage profile with less harmonic content, and hence reduces the filtering requirement and system size. However, due to the parallel connection, circulating currents appear among legs [2]. This deteriorates the system performance and threats the safety operation of converter switches [2]. Several methods have been proposed in the literature to reduce circulating currents among the legs of the converter, which is critiqued in [3] and [4]. Among them, repetitive controller (RC) and deadbeat control (DB) scheme are very promising.

RC can provide a promising solution where periodic disturbances are present in feedback systems. Theoretically, a suitably designed RC can track the periodic reference signal or/and reject exogenous periodic disturbances with zero steady-state error even in the presence of model uncertainties. An advanced closed-loop RC to suppress various harmonics has been proposed in [5], where the sluggish response of a typical RC is overcome by paralleling with a proportional + integral (PI) controller. Furthermore, the stability of the combined controller has been ensured.

The DB scheme is also proven to be an advantageous control scheme for parallel-connected voltage source converters (VSCs). Various DB schemes have been developed in [6] and [7] to eliminate the circulating current problem, where the converters are sharing both common dc bus and paralleled in the ac side as well. This scheme [6] is shown to work in a grid-connection mode with non-standard *LC/LCL* filter and is able to achieve the broader bandwidth for its current characteristics. A reduced order DB scheme has been implemented in [8] for distribution static compensator application, which simplifies the design of the controller for its dynamic states. A double deadbeat (DD) control scheme has been implemented for its voltage and current loops [9]. This may effectively reduce the voltage and current harmonics, but due to its non-decoupling nature, all the control parameters are sensitive to loads, which may affect the system stability. To overcome the drawback, a decoupled DB scheme has been implemented in [10]. This scheme in [11] controls the circulating currents in the legs of the converter by using space vector modulation (SVM) methods. This SVM method adjusts its zero vector to block the circulating currents. However, it [11] did not discuss the effect of parameters on the proposed control scheme. Another SVM scheme in conjunction with the DB scheme has been implemented to mitigate the circulating current in [7]. With the usage of the SVM scheme, the converter switches have to be operated with high speed, which may incur switching losses affecting the system efficiency. Cost of implementation of the control scheme plays a very important role. To reduce the cost of implementation, a cost-effective control scheme based on a DB strategy has been applied and imple-

Manuscript received April 16, 2018; revised August 21, 2018; accepted October 6, 2018. This work was supported by Science and Engineering and Research Board (SERB) under NPDF scheme-SERB/NPDF/ENGG/2017/00568. *(Corresponding author: Sreedhar Madichetty.)*

S. Madichetty and S. Mishra are with the Electrical Engineering Department, Indian Institute of Technology Delhi, New Delhi 110016, India (e-mail: sreedhar.803@gmail.com; sukumarmiitdelhi@gmail.com).

M. Basu is with the School of Electrical and Electronic Engineering, Dublin Institute of Technology, Dublin D08 X622, Ireland (e-mail: mbasu@dit.ie).

J. M. Guerrero is with Aalborg University, Aalborg 9220, Denmark (e-mail: joz@et.aau.dk).

Digital Object Identifier 10.1109/JSYST.2018.2875543

mented to a wind energy system [12]. Furthermore, some more modifications have been done for the DB scheme in terms of its predictive approach for voltage/current waveform [13], [14]. Despite the advantages, the challenges of the DB design problem are 1) limitation due to inherent plant delay and 2) sensitivity to plant uncertainties [15]. This has been effectively addressed by combining the RC with DD control in this paper. Topology wise a five-level NPCC with its parallel scheme is an excellent choice due to its simplicity and practical implementation in paralleled connectivity. A single-phase NPCC with a deadbeat predictive control scheme has been implemented [16]. This discussion is limited to only single-phase applications, because of its railway track application. However, the application of a deadbeat controller to permanent magnet synchronous motors is proven, perhaps the problems of circulating current were not alleviated [17]–[20]. To overcome the above-mentioned drawbacks, a comprehensive controller with a DB scheme in conjunction with a customized repetitive control scheme has been proposed in this paper. The deadbeat current control technique is inherently the fastest control strategy that can be adopted. With DB, in principle, the current loop replicates exactly the current reference with a two-cycle delay. However, the control is based on an internal model of the converter load, and therefore inherently sensitive to model and parameter mismatches. Unfortunately, parameter mismatches are always encountered in practice. In the presence of a model mismatch, significant deviations from the expected closed-loop performance can take place (instabilities or lightly damped oscillations). Application of the RC scheme can negate this impact and, hence, is also utilized to mitigate the circulating currents in the legs of the converter independently.

The main contributions of the paper can be summarized as follows.

1) Implementation of combined DD plus repetitive control scheme to three-phase five-level parallel NPCCs.
2) Designing a circulating current control scheme, which combines the effect of two parallel controllers, namely, a PI controller and a modified odd harmonic higher-order repetitive control (OHHORC).
3) System implementation with various linear/nonlinear loads having disturbance rejection property in its control.
4) Most importantly, the proposed scheme can be easily expanded and modified for larger systems as well.

This paper is broadly categorized into six sections. After the introduction and literature reviews in the first section, Section II deals with the problem statement associated with the parallel-connected scheme. Section III discusses the proposed circulating control scheme. Section IV deals with the proposed deadbeat plus repetitive controller and its results are presented in Section V. Finally, the paper concludes with Section VI.

## II. PODPWM and Circulating Current Scheme

The basic diagram describing the proposed scheme is shown in Fig. 1. It mainly consists of distributed generation systems (DGS), such as diesel energy power generating (DG) systems, solar photovoltaic systems, and fuel cell system that are connected to a common dc bus with a circuit breaker. However,

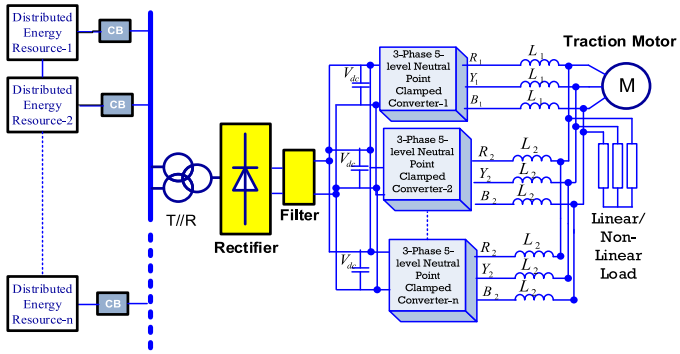



Fig. 1. Proposed system configuration.

the proposed scheme focuses on the parallel connection of an inverter-connected distributed generation bus system. This is then given to the VSCs for dc–ac conversion. In this paper, three-phase five-level NPCCs are connected in parallel to increase the current-carrying capacity to cater large quantity of loads. With the parallel connectivity, circulating current will exist in the system. There are mainly three ways to reduce the circulating currents in the parallel-connected inverters.

1) To use a delta-connected transformer at the end of the converter to interface with the load. But the usage of a bulky transformer increases not only the size but also the cost.
2) By not providing the circulating path for harmonic components will be the second option, so that this scheme may require to operate with extra solid state switches, which again increases the complexity and losses of the system.
3) Each inverter is to operate with isolated dc power supply. Providing isolated supplies for VSCs is a difficult and cost involving task. Hence, a unified controller is required to mitigate the circulating currents.

The basic parallel-connected five-level NPCC is shown in Fig. 2. Each converter consists of 12 switches in total, i.e., $S_1, S_2, \ldots, S_{12}$ for converter 1 and $S_{13}, S_{14}, \ldots, S_{24}$ for converter 2.

This converter is fed with a phase opposition and disposition pulsewidth modulation scheme (PODPWM) [21], which is shown in Fig. 3(a). This scheme is given in [21] for a three-phase three-level converter. However, a five-level converter is operated with four carrier waves in the upper half (0 to 1) and four carrier waves the lower half (0 to –1) with its modulation index "*M*" varying between 0 and 1. Carrier signals are compared with a single sine wave reference. When the carrier signal is greater than the reference signal, high pulse enables the respective switches. The resultant contour plot for a five-level NPCC applied PODPWM scheme is shown in Fig. 3(b) and this is drawn with a natural sampling of $\varphi = \cos^{-1}(\frac{1}{2M})$. The switching scheme for the five-level NPCC is given in Table I. The contour plot describes the voltage as per switch states given in Table I, where $\omega_r, \omega_c$ represent the angular frequency of the reference wave and the frequency of the carrier wave, respectively. The modulation index "*M*" is decided by the current reference, which will be discussed in subsequent sections. When multiple/many converters are connected in parallel to a single

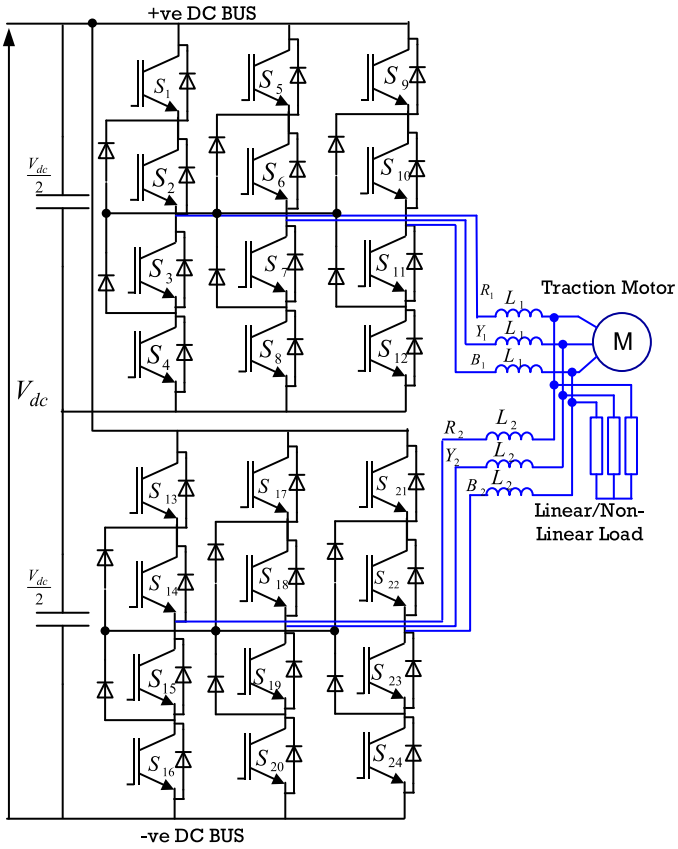



Fig. 2. Three-phase five-level parallel-connected neutral point clamped converter.

dc bus, the circulating currents will flow through the legs of the converter. Fig. 4 shows the simplified circuit in Fig. 1, where $V_1$, $V_2$ are the voltage across inverters 1 and 2, respectively. $L_1$, $L_2$, $R_1$, $R_2$ are the voltage and resistance of respective inverters with its grid voltage as $V_g$

$$V_g = V_1 + I_1 (R_1 + X_{L1}) \tag{1}$$

$$V_g = V_2 + I_2 (R_2 + X_{L2}). \tag{2}$$

### A. Modeling of the PODPWM Scheme

$I_1$, $I_2$ are the current passing through inverters 1 and 2, respectively. Eq(1) = Eq(2). Therefore,

$$V_1 + I_1 (R_1 + X_{L1}) = V_2 + I_2 (R_2 + X_{L2}). \tag{3}$$

The voltage drop across the inductor may be small due to its low resistance compared to the grid voltage. Then, one can obtain the following equation:

$$V_1 + I_1 (J\omega_{L1}) = V_2 + I_2 (J\omega_{L2}). \tag{4a}$$

### B. Mathematical Modeling of the Circulating Current Scheme

The terminal voltage depends upon the scheme of PWM employed. The circulating currents will also depend upon the terminal voltages. The circulating currents in the three phases of the two inverters have the same magnitude, but they are in the opposite direction, as shown in the following equation, and its equivalent circulating direction is shown in Fig. 4:

$$i_{\text{Cir1}} = -i_{\text{Cir2}} = i_{R1} + i_{Y1} + i_{B1} = -i_{R2} - i_{Y2} - i_{B2}. \tag{4b}$$

The terminal voltages and its circulating currents can be written as given in (5) and (6)

$$V_1 = \frac{L_1 (i_{R1} + i_{Y1} + i_{B1}) + V_{R1} + V_{Y1} + V_{B1}}{3} \tag{5}$$

$$V_2 = \frac{L_2 (i_{R2} + i_{Y2} + i_{B2}) + V_{R2} + V_{Y2} + V_{B2}}{3} \tag{6}$$

$$i_{\text{cir1}} = \frac{3 (V_1 - V_2)}{(R_1 + R_2) + (X_{L1} + X_{L2})}. \tag{7}$$

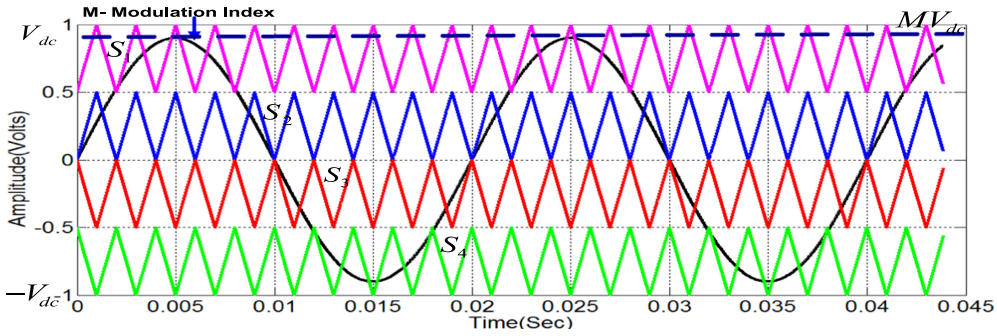
Here, $i_{R1} + i_{Y1} + i_{B1}$ is the current passing through "*R*", "*Y*", "*B*" phases of NPCC 1, respectively, and similar will be true with subscript "2" for NPCC 2.

## III. Proposed Circulating Current Control Scheme

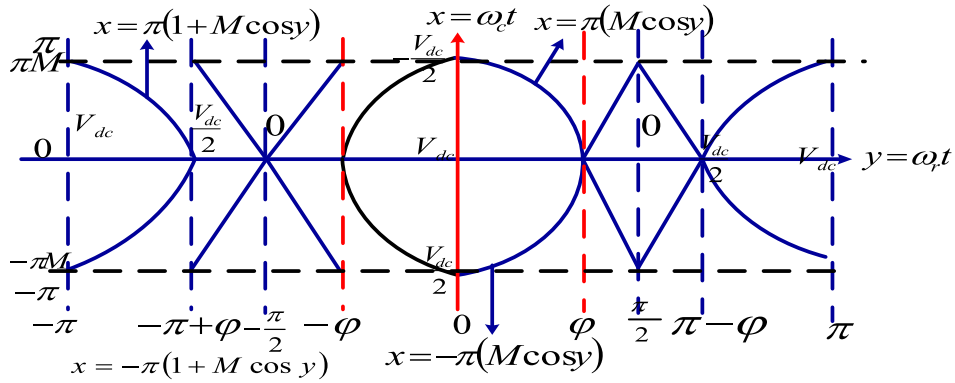
The proposed circulating current control scheme combines the effect of two parallel controllers, namely, a PI controller and a modified OHHORC scheme. The design and purpose of the controller components are explained in details as follows. As majority of the circulating current due to zero sequence components are odd harmonics, the reference signal needs to be carefully constructed for perfect tracking. To enable disturbance rejection property, a model reference signal is included in the closed-loop transfer function of the system. For instance, the zero static error could be achieved in a step reference/disturbance by employing an integrator in the closed-loop system. For a periodic reference signal, it can be achieved by including a conjugate imaginary pole at the frequency $\omega$ of the signal. To eliminate various other order frequencies, the conjugate imaginary poles are bundled in the form of $\frac{1}{S^2+\omega^2}$. This type is known as a proportional resonant control scheme [3]. However, the repetitive control adopts an infinite dimensional internal model $M(s)$ to provide a series of conjugate poles at all harmonic frequencies [21].

To improve the stability, a low-pass filter is added in its closed loop by a positive feedback. This scheme is employed under repetitive frequency. This scheme is shown in Fig. 5(a) that is provided with a null phase low-pass filter $H(z)$ and delay function $\omega(z)$ with feedback sign $\sigma$. The transfer function model of the delay function is given in (9).

However, under varying frequencies, the controller performance can be improved by a weighted sum of several signal periods. This improves the characteristic frequency response to a broad region of harmonic components. Hence, a stabilizing controller $G_x(z)$ has been used in a feed-forward path, to assure the closed-loop stability. Furthermore, to ensure stability at all conditions, a PI control scheme has been paralleled with the above-mentioned repetitive controller scheme and is shown in Fig. 5(b). Furthermore, to improve the robustness of the controller, a stabilizing filter $s(z)$ is implemented in its positive feedback. To make it fine-tuned for critical loads, a weighted current approach has been implemented in the feed-forward path, as shown in Fig. 5(c).




(a)




(b)

Fig. 3. (a) Phase opposition and disposition PWM scheme applied for a three-phase three-level parallel-connected neutral point clamped converter. (b) Contour plot of a five-level PODPWM scheme.

TABLE I
SWITCHING SCHEME FOR THE FIVE-LEVEL NPCC

| Voltage | Switching in lies between $0 < x \leq \pi$ | Switching in lies between $\pi \leq x \leq 2\pi$ |
|---|---|---|
| $V_{dc}$ | $Msin\left(\frac{\pi}{2}-y\right) > 0.5\left(1+\frac{x}{\pi}\right)$ | $Msin\left(\frac{\pi}{2}-y\right) > -0.5\left(1+\frac{x}{\pi}\right)$ |
| $\frac{V_{dc}}{2}$ | $0.5\frac{x}{\pi} < Msin\left(\frac{\pi}{2}-y\right) < 0.5\left(-1+\frac{x}{\pi}\right)$ | $-0.5\frac{x}{\pi} Msin\left(\frac{\pi}{2}-y\right) < 0.5\left(-1-\frac{x}{\pi}\right)$ |
| 0 | $-0.5\frac{x}{\pi} < Msin\left(\frac{\pi}{2}-y\right) < 0.5\left(\frac{x}{\pi}\right)$ | $0.5\frac{x}{\pi} < Msin\left(\frac{\pi}{2}-y\right) < -0.5\left(\frac{x}{\pi}\right)$ |
| $-\frac{V_{dc}}{2}$ | $-0.5-0.5\frac{x}{\pi} < Msin\left(\frac{\pi}{2}-y\right) < -0.5\left(\frac{x}{\pi}\right)$ | $-0.5+0.5\frac{x}{\pi} < Msin\left(\frac{\pi}{2}-y\right) < 0.5\left(\frac{x}{\pi}\right)$ |
| $V_{dc}$ | $Msin\left(\frac{\pi}{2}-y\right) < 0.5\left(-1-\frac{x}{\pi}\right)$ | $Msin\left(\frac{\pi}{2}-y\right) < 0.5\left(-1+\frac{x}{\pi}\right)$ |

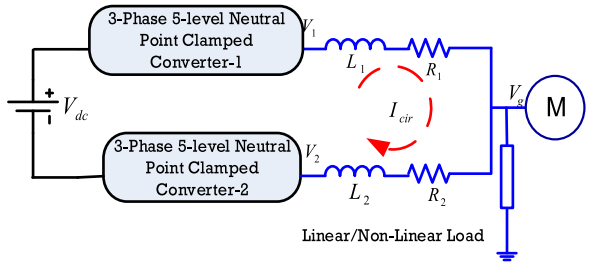



Fig. 4. Simplified circuit diagram of a parallel-connected NPCC connected to a grid.

The closed-loop transfer function model can be written as

$$G_{rc}(z) = \frac{\sum_{i=1}^{K} \omega_i Z^{-iN} H(z) \cdot G_x(z)}{1 - \sum_{i=1}^{K} \omega_i Z^{-iN} H(z) \cdot S(z)} \tag{8}$$

where $N = \frac{T_P}{T_s}$; $T_P$ is the sampling period, $T_s$ is the signal period; and $S(z)$ is the stabilizing filter. To obtain the high gain at all frequencies, the weighted signal $\sum_{i=1}^{K} \omega_i = 1$

$$\omega(z) = \left(1 - \left(1 - Z^{-N}\right)^k\right). \tag{9}$$

And the inverter (plant) transfer function is

$$G_p(z) = \frac{T_s}{(z-1)L_r}. \tag{10}$$

The transfer function model is shown in Fig. 5(d).
The overall proposed scheme is shown in Fig. 5(e).

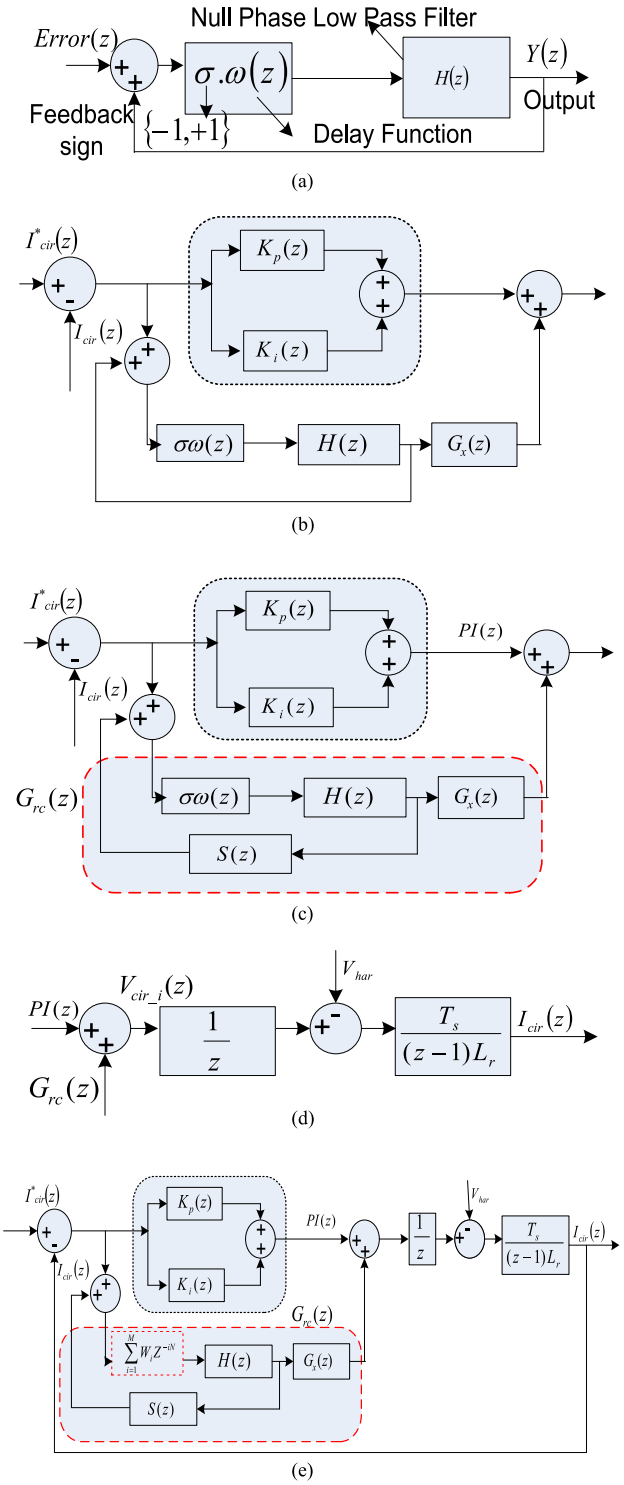



Fig. 5. (a) General repetitive control scheme. (b) General repetitive control scheme with parallel P + I control. (c) Repetitive control scheme with parallel P + I control plus weighed signal approach $s(z)$. (d) Proposed control scheme with the inverter. (e) Proposed HORC scheme with the inverter.

The important aspect of the design is that the proposed system is able to provide infinite gains at all odd harmonic components, i.e., $\omega_k = \frac{2(2k-1)\pi}{N} \quad \forall k = 1, 2, \ldots, \frac{N}{2}$ and $Z = e^{\frac{2(2k-1)\pi}{N} \cdot j}$.

TABLE II
SIMULATION PARAMETERS

| Simulation Parameter | Value |
|---|---|
| DC Voltage $V_{dc}$ | 550 V |
| Carrier Frequency wave $f_{PWM}$ | 1000 Hz |
| Modulation index "M" (initially), adaptive later | 0.9 |
| Random parameter ´ ξ ´ | 0-1 |
| Sampling period $T_P$ | 2e-06 |
| Signal period $T_s$ | 1.9e-06 |
| Proportional gain $K_p$ | 2000 |
| Integral gain $K_I$ | 356 |
| Signal/ Reference wave Frequency wave $f_S$ | 50 Hz |
| Inductor $L$ | 3 mH |
| Capacitor filter C | 3.6 μF |
| Circle radius $K_r$ | $K_r \in (0,2)$ |

### A. Comment on Stability

The closed-loop transfer function of the proposed scheme can be written as

$$\frac{I_{\text{cir}}(z)}{I_{\text{cir}}{}^{*}(z)} = \frac{(\text{PI}(Z) + G_{rc}(z))\left(\frac{1}{Z}\right)\left(\frac{T_s}{(Z-1)L}\right)}{1 + (\text{PI}(Z) + G_{rc}(z))\left(\frac{1}{Z}\right)\left(\frac{T_s}{(Z-1)L}\right)} - \frac{k_p(z) \cdot V_{\text{har}}(z)}{1 + (\text{PI}(Z) + G_{rc}(z))\left(\frac{1}{Z}\right) \cdot k_p(z)}. \quad (11)$$

Hence, the closed-loop poles can be written as

$$Z = \frac{N}{2}\sqrt{|1 - K_r|} \cdot e^{\frac{2(2k-1)\pi}{N}} + \pi \cdot \frac{1 - \text{sgn}(1 - k_r)}{2}. \quad (12)$$

From the above-mentioned equation, one can easily come to a conclusion that all the poles are uniformly distributed on a circle radius $\frac{N}{2}\sqrt{|1 - K_r|}$, where $K_r$ is the circle radius and $K_r \in (0, 2)$. All the controller parameters are listed in Table II.

## IV. Proposed Adaptive Double Deadbeat Control Scheme

The complete schematic of the DD controller is shown in Fig. 6(a). This scheme is used to control the voltage and current of both the converters. For the sake of simplicity, the three-phase voltage/current signals have been transformed into $\alpha\beta$ with *abc*-$\alpha\beta$ transformation as shown in (13). Similar kind of transformation can be implemented for other converters as well. This obtained signal has been given to the deadbeat controller. The proposed DB scheme contains two inputs (voltage and current) from the other converters and these are compared with (voltage/current) of converter 1

$$\begin{bmatrix} i_{\alpha 1} \\ i_{\beta 1} \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{R1} \\ i_{Y1} \\ i_{B1} \end{bmatrix}. \quad (13)$$

The inherent part of the deadbeat controller is marked in red-dotted lines. This is a nonlinear controller consisting of nonlinear differentiator, state observer, and state feedback

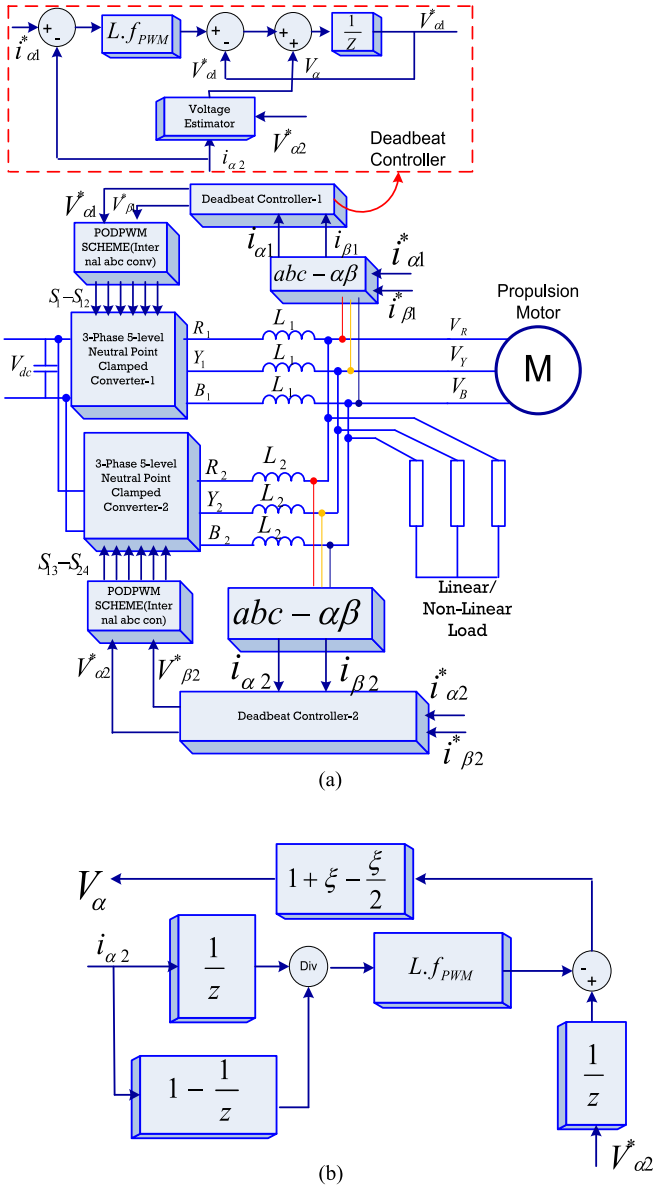



Fig. 6. (a) Proposed double deadbeat controller scheme. (b) Proposed voltage estimator for the deadbeat controller.

mechanisms. The similar kind of cross-coupled controller can be implemented for converter 2 as well, where "$*$" indicates that the command value is generated from the controller. The reference signal, thus, obtained from the deadbeat controller is then given to the PODPWM modulator and it is estimated as

$$V_{\alpha 1}{}^{*} = Lf_{\mathrm{PWM}}\left[(i_{\alpha 1}{}^{*} - i_{\alpha 2})\right] + 2V_{\alpha} - V_{\alpha 1} \tag{14}$$

where $f_{\mathrm{PWM}}$ is the modulator carrier frequency, $L_1 = L_2 = L$ is the inductance of the converter, and $V_{\alpha}$ is the output obtained from the voltage estimator. $i_{\alpha 1}{}^{*}$ is the command value of the current from converter 1, and $i_{\alpha 2}$ is the nominal value of the current from converter 2. To perfectly track and balance the voltage of the converter, a voltage estimator has been designed inherently with the DB scheme, as shown in Fig. 6(b).

The voltage estimator is equipped with a random parameter "$\xi$". This random parameter is seen as adaptive gain considering its range as per the load demand and it lies between 0 and 1. The output obtained from the converter 2 currents, command voltage, and the overall input to the reference wave has been given, respectively, as

$$i_{\alpha 2\ (\mathrm{op})} = L \cdot f_{\mathrm{PWM}} \frac{(1/z)}{(1 - 1/z)} \tag{15}$$

$$V_{\alpha 2(\mathrm{op})}{}^{*} = \frac{1}{z} \tag{16}$$

$$V_{\alpha(\mathrm{op})} = \left[\left(V_{\alpha 2(\mathrm{op})}{}^{*} - i_{\alpha 2\ (\mathrm{op})}\right)\left(1 + \xi - \frac{\xi}{2}\right)\right]. \tag{17}$$

Thus, the voltage and current signals are perfectly tracked as per the load demand. The robustness of the controller has been greatly improved by adding a filter at controller input 2. Furthermore, there is no dependence of the repetitive controller on the DB scheme that makes the system more effective.

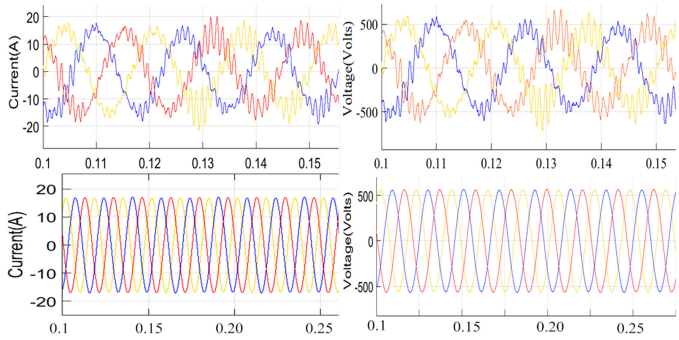



Fig. 7. System executed with and without the double deadbeat plus repetitive controller: From top left to right, current waveform and voltage waveform before application. From bottom left to right, current waveform and voltage waveform after application.

## V. Results and Analysis

The three-phase parallel-connected system has been executed with the proposed controller in the OPAL RT platform and its results are given below. The complete list of simulation parameters is shown in Table II. The simulated waveform without the proposed controller scheme and with the proposed controller scheme is shown in Figs. 7 and 8, respectively.

Initially, the modulation index "*M*" has been chosen as 0.9, and later, *M* is changed as per the load demand/non-linear loads. The carrier frequency of the carrier signals in the PODPWM scheme is 1000 Hz. Under these conditions, voltage waveform and current waveform before and after the application of the proposed scheme are shown in Fig. 7. Here, the voltage lies between +510 and –510 V peak–peak and its load current waveform is between +20 and –20 A peak–peak.

Without the application of the proposed controller, the circulating currents are 4 A peak–peak. The voltage and current waveform total harmonic distortion (THD) has 27.1% THD with the lowest order harmonic, which is 23rd order, and the current waveform has 35.6% THD with the lowest order harmonic, which is 23rd order. Then, the system has been executed with the proposed RC + DD scheme and its results are shown in Fig. 7. System with the proposed controller shows a

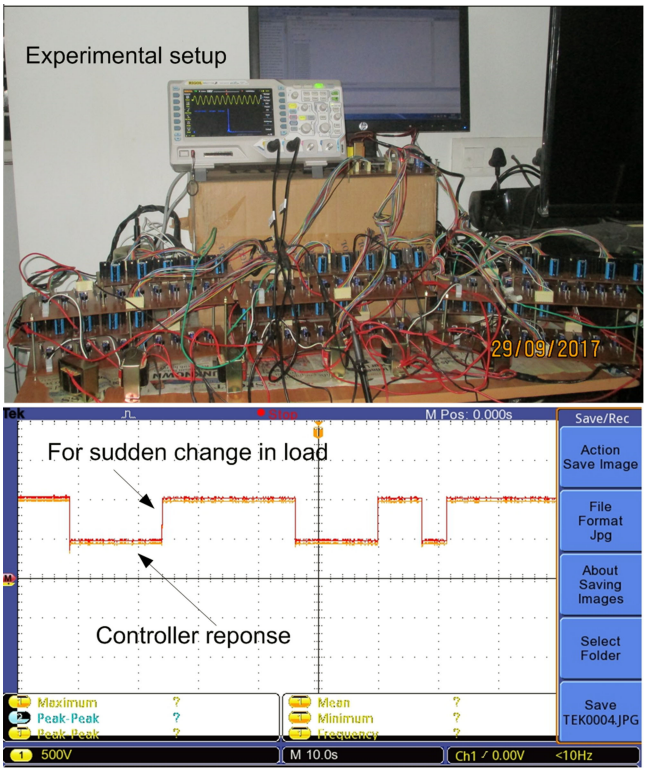



Fig. 8. Experimental setup and controller response.

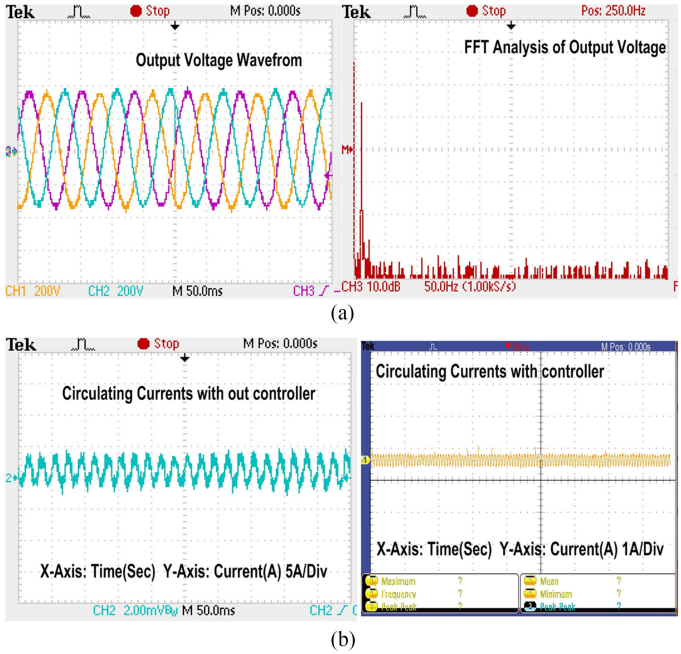



Fig. 9. (a) Output voltage waveform and its FFT analysis. (b) Circulating currents without and with the controller.

substantial improvement in voltage/current waveform quality and fast Fourier transform (FFT) analysis as well. Voltage waveform shows 3.7% THD and current waveform shows 4.2% THD at 60 Hz as its fundamental components.

The circulating currents after the implementation of the controller have been reduced from 4 to 0.2 A. In addition, the controller performance has been verified subjected to the sudden change in loads. The system has been executed on an OPAL-RT real-time simulator and then with the hardware prototype as the setup is shown in Fig. 8. In the experimental analysis, "Texas instruments msp-exp430fr5994" digital signal processor has been used for control logic implementation. Furthermore, "STGW20NC60VD" IGBT is considered for its fast switching, which utilizes the advanced power MESH process resulting in an excellent trade-off between switching performance and low ON-state behavior. The input voltage to the converter is given from a 300 V–50 A dc–dc converter, which mimics the dc microgrid. A dc-link capacitor of 2200 $\mu$F is used to maintain the input voltage. A 50 V 600 $\mu$F capacitor is used a submodule capacitance. All the results were captured on a diligent digital storage oscilloscope. The important point to note is that the common coupling point of the converter does not use any inductor, which favors the reduction in losses. Furthermore, the controller response for a sudden change in load is shown in the bottom in Fig. 8, and it is verified that the controller responds very quickly for sudden changes in load.

The results obtained in the experiment are in excellent agreement with the simulation results. The system output voltage with the controller is shown in Fig. 9(a) with its FFT analysis. This figure shows that the resultant THD obtained with the controller is 3.7%, which is slightly higher than the simulation but they are in a close agreement.

TABLE III
THD COMPARISON

| *Component* | *THD* |
|---|---|
| Voltage-Simulation- Without controller | 27.1% |
| Current- Simulation- Without controller | 35.6% |
| Voltage-Simulation- With controller | 3.6% |
| Current- Simulation- With controller | 4.2% |
| Voltage-Experiment- With controller | 3.7% |
| Current-Experiment- With controller | 4.5% |
| Circulating Currents- Without controller | 4A P-P |
| Circulating Currents- With controller | 0.2A P-P |
| Controller Stability reaching | > 75 msec |

All the lower order harmonics are completely mitigated. In addition, the system circulating currents with the controller and without the controller are shown in Fig. 9(b). Here, the circulating currents are 4 A (peak–peak) and 0.2 A (peak–peak) without and with the controller, respectively. From these, it can be claimed that the proposed controller is able to perform very well for non-linear loads and can offer impressive improvement in mitigating the circulating currents. Summary of the results is given in Table III.

Hence, from this one can come to a conclusion about the controller that it performs well at sudden load conditions as well and it gets stabilized in less than 75 ms.

## VI. CONCLUSION

This paper presented a comprehensive controller with a DB scheme in conjunction with customized repetitive control to mitigate the voltage/current harmonics and circulating currents,

which is a potential challenge in parallel-connected converters. The proposed system is initially implemented on the OPAL-RT real-time simulator further verified with a prototype. The proposed RC scheme has mitigated the circulating currents in the legs of the converter from 4 to 0.2 A and improved the performance at dynamic load conditions. Implementation of the DD loop control scheme results in effective improvement of voltage and current profile and it is verified by calculating its THD. In addition, the proposed controlling scheme is able to operate for various ranges of loads and can be scaled for a larger system as well. These types of schemes will, therefore, find its perfect application in electrical locomotives.

## REFERENCES


[1] X. Zhang, W. Zhang, J. Chen, and D. Xu, "Deadbeat control strategy of circulating currents in parallel connection system of three-phase PWM converter," *IEEE Trans. Energy Convers.*, vol. 29, no. 2, pp. 406–417, Jun. 2014.

[2] S. Madichetty, A. Dasgupta, S. Mishra, C. K. Panigrahi, and G. Basha, "Application of an advanced repetitive controller to mitigate harmonics in MMC with APOD scheme," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6112–6121, Sep. 2016.

[3] B. Li, Z. Xu, S. Shi, D. Xu, and W. Wang, "Comparative study of the active and passive circulating current suppression methods for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 1878–1883, Mar. 2018.

[4] S. Xu, W. Cao, K. Liu, S. Wang, and J. Zhao, "Analysis and control of switching circulating currents in multi-module parallel SPWM converters," *IEEE Access*, vol. 6, pp. 32637–32648, 2018.

[5] M. Sreedhar, A. Dasgupta, and S. Mishra, "New harmonic mitigation scheme for modular multilevel converter–An experimental approach," *IET Power Electron.*, vol. 7, no. 12, pp. 3090–3100, 2014.

[6] J. He, Y. W. Li, D. Xu, X. Liang, B. Liang, and C. Wang, "Deadbeat weighted average current control with corrective feed-forward compensation for microgrid converters with nonstandard LCL filter," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2661–2674, Apr. 2017.

[7] X. Xing, Z. Zhang, C. Zhang, J. He, and A. Chen, "Space vector modulation for circulating current suppression using deadbeat control strategy in parallel three-level neutral-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 64, no. 2, pp. 977–987, Feb. 2017.

[8] H. Xiao, A. Luo, and Z. Shuai, "Double deadbeat-loop control method for distribution static compensator," *IET Power Electron.*, vol. 8, no. 7, pp. 1104–1110, Jul. 2015.

[9] J.-F. Stumper, V. Hagenmeyer, S. Kuehl, and R. Kennel, "Deadbeat control for electrical drives: A robust and performant design based on differential flatness," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4585–4596, Aug. 2015.

[10] P. Wen and T.-W. Lu, "Decoupling control of a twin rotor MIMO system using robust deadbeat control technique," *IET Control Theory Appl.*, vol. 2, no. 11, pp. 999–1007, Nov. 2008.

[11] A. Bouafia, J.-P. Gaubert, and F. Krim, "Predictive direct power control of three-phase pulsewidth modulation (PWM) rectifier using space-vector modulation (SVM)," *IEEE Trans. Power Electron.*, vol. 25, no. 1, pp. 228–236, Jan. 2010.

[12] K. Nishida, T. Ahmed, and M. Nakaoka, "Cost-effective deadbeat current control for wind-energy inverter application with LCL filter," *IEEE Trans. Ind. Appl.*, vol. 50, no. 2, pp. 1185–1197, Mar. 2014.

[13] L. Tong *et al.*, "An SRF-PLL-based sensorless vector control using the predictive deadbeat algorithm for the direct-driven permanent magnet synchronous generator," *IEEE Trans. Power Electron.*, vol. 29, no. 6, pp. 2837–2849, Jun. 2014.

[14] A. Wu and H. Geyer, "The 3-D spring–mass model reveals a time-based deadbeat control for highly robust running and steering in uncertain environments," *IEEE Trans. Robot.*, vol. 29, no. 5, pp. 1114–1124, Oct. 2013.

[15] Y. Abdel-Rady Ibrahim Mohamed and E. F. El-Saadany, "An improved deadbeat current control scheme with a novel adaptive self-tuning load model for a three-phase PWM voltage-source inverter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 747–759, Apr. 2007.

[16] W. Xie *et al.*, "Finite-control-set model predictive torque control with a deadbeat solution for PMSM drives," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5402–5410, Sep. 2015.

[17] X. Zhang, B. Hou, and Y. Mei, "Deadbeat predictive current control of permanent-magnet synchronous motors with stator current and disturbance observer," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3818–3834, May 2017.

[18] M. H. Vafaie, B. M. Dehkordi, P. Moallem, and A. Kiyoumarsi, "Improving the steady-state and transient-state performances of PMSM through an advanced deadbeat direct torque and flux control system," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2964–2975, Apr. 2017.

[19] A. D. Alexandrou, N. Adamopoulos, and A. Kladas, "Development of a constant switching frequency deadbeat predictive control technique for field-oriented synchronous permanent-magnet motor drive," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 5167–5175, Aug. 2016.

[20] J. S. Lee and R. D. Lorenz, "Robustness analysis of deadbeat-direct torque and flux control for IPMSM drives," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2775–2784, May 2016.

[21] M. J. Tsai, H. C. Chen, M. R. Tsai, Y. B. Wang, and P. T. Cheng, "Evaluation of carrier-based modulation techniques with common-mode voltage reduction for neutral point clamped converter," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3268–3275, Apr. 2018.


**Sreedhar Madichetty** (M'16) received the B.Tech. degree from Jawaharlal Nehru Technological Univeristy, Anantapur, India, in 2010, and the M.Tech. and Ph.D. degrees from Kalinga Institute of Industrial Technology University, Bhubaneswar, India, in 2012 and 2015, respectively.

In 2014, he joined the Department of Electrical and Electronics Engineering, Birla Institute of Technology and Science, Pilani, as a Lecturer. He is currently a Post-Doctoral Fellow with the Department of Electrical Engineering, Indian Institute of Technology Delhi, New Delhi, India. He has authored or coauthored more than 20 research articles (including papers in international journals, conferences, and book chapters). His research interests include power electronics, power system studies, and renewable energy.

**Malabika Basu** (S'99–M'03) received the B.E. and M.E. degrees from the Bengal Engineering College, Shibpur, India, in 1995 and 1997, respectively, and the Ph.D. degree from the Indian Institute of Technology Kanpur, Kanpur, India, in 2003, all in electrical engineering.

From 2001 to 2003, she was a Lecturer with Jadavpur University, Kolkata, India. From 2003 to 2006, she was an Arnold F. Graves Postdoctoral Fellow with Dublin Institute of Technology, Dublin, Ireland, where she has been a Lecturer since 2006. She has authored or coauthored more than 90 technical publications in various international journals and conference proceedings. Her current research interests include grid integration of renewable energy sources, power quality conditioners and power quality control and analysis, photovoltaics and wind energy conversion, HVDC systems, smart grid, and microgrids.

**Sukumar Mishra** (M'97–SM'04) received the B.E. degree from the University College of Engineering, Burla, India, in 1990, and the M.E. and Ph.D. degrees from the Regional Engineering College, Rourkela, India, in 1992 and 2000, respectively.

In 1992, he joined the Department of Electrical Engineering, University College of Engineering, as a Lecturer, and subsequently became a Reader in 2001. He is currently a Professor with the Department of Electrical Engineering, Indian Institute of Technology Delhi, New Delhi, India. He is working as a National Thermal Power Corporation Chair Professor and has previously worked as a Power Grid Chair Professor, New Delhi. He is also serving as an independent Director with the Cross Border Power Transmission Company Ltd., Gurugram, India, and an Industry Academic Distinguish Professor. He has authored or coauthored more than 100 research articles (including papers in international journals, conferences, and book chapters). He has handled many research projects and industrial consultancies. His research interests include power systems, power quality studies, and renewable energy.

Dr. Mishra is currently the Vice-Chair of the IEEE Intelligent System SubCommittee of the Power and Energy Society. He was a recipient of the Indian National Science Academy Medal for Young Scientists, the Indian National Academy of Engineering (INAE) Young Engineer Award, and the INAE Silver Jubilee Young Engineer Award. He is also a Fellow of the IET (U.K.), the National Academy of Sciences (India), INAE (India), the Institution of Engineers (India), and the Institution of Electronics and Telecommunication Engineers (India). He currently serves as an Editor for the IEEE TRANSACTIONS ON SMART GRID and an Associate Editor for *IET Generation, Transmission, and Distribution*.

**Josep M. Guerrero** (S'01–M'04–SM'08–F'15) received the B.S. degree in telecommunications engineering, the M.S. degree in electronics engineering, and the Ph.D. degree in power electronics from the Technical University of Catalonia, Barcelona, Spain, in 1997, 2000, and 2003, respectively.

Since 2011, he has been a Full Professor with the Department of Energy Technology, Aalborg University, Aalborg, Denmark, where he is responsible for the Microgrid Research Program. From 2014, he is a Chair Professor with Shandong University, Jinan, China; from 2015, he is a Distinguished Guest Professor with Hunan University, Changsha, China; and from 2016, he is a Visiting Professor Fellow with Aston University, Birmingham, U.K., and a Guest Professor with Nanjing University of Posts and Telecommunications, Nanjing, China. He has authored or coauthored more than 450 journal papers in the fields of microgrids and renewable energy systems, which are cited more than 30 000 times. His research interests are oriented to different microgrid aspects, including power electronics, distributed energy-storage systems, hierarchical and cooperative control, energy management systems, smart metering, and the internet of things for ac–dc microgrid clusters and islanded minigrids; recently specially focused on maritime microgrids for electrical ships, vessels, ferries, and seaports.

Dr. Guerrero is an Associate Editor for a number of IEEE Transactions. He was a recipient of the Best Paper Award of the IEEE TRANSACTIONS ON ENERGY CONVERSION for the period 2014–2015, the Best Paper Prize of the IEEE Power and Energy Society in 2015, and the Best Paper Award of the *Journal of Power Electronics* in 2016. During five consecutive years, from 2014 to 2018, he was awarded by Thomson Reuters as a Highly Cited Researcher. In 2015, he was elevated as an IEEE Fellow for his contributions on "distributed power systems and microgrids."