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A Carrier Synchronization Method for Global Synchronous Pulse Width Modulation Application Using Phase-Locked-Loop

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***Abstract*—When many distributed parallel inverters are integrated into grid without switching sequence coordinated control capability, the high frequency harmonics will accumulate randomly at the Point of Common Coupling (PCC). Global synchronous pulse width modulation (GSPWM) method can significantly attenuate the accumulated switching ripples by intentionally assuming an intelligent optimization algorithm and a communication system. To avoid the dependence on low-latency communication system, this paper proposes a novel phase locked loop based PWM carrier synchronization (PLL-CS) method for GSPWM system, where the switching sequences can be effectively synchronized as expected without using low-latency synchronization signals. By doing so, the operational reliability of the whole GSPWM system can be significantly improved while the additional hardware cost of GSPWM can be dramatically reduced, which can enhance the implementation adaptability of GSPWM method. Experimental results have verified the performance of the proposed PLL-CS GSPWM method.**

***Index Terms*—Carrier synchronization method; global synchronous pulse width modulation; phase locked loop; distributed inverters**

I. Introduction

Nowadays, a large number of distributed generation (DG) units have being integrated into the distribution power grid driven by the environmental issues, economical factors, and social interests [1-3]. Most of the distributed generators are connected to the grid through the grid-tied inverters as shown in Fig. 1. The injected currents from DGs unavoidably contain the high frequency harmonics. A LC or LCL filter could be employed to attenuate the current harmonics of single inverter [4-11]. Alternatively, a multi-leg inverter with the interleaved PWM can achieve the similar performance either [12-15]. The interleaving technology leads to the reduction of filter size and cost. But the traditional multi-leg circuits are supplied by a common DC source and controlled by one controller. Reference [16] employed the distributed approach to interleave the power converter cells with their own controllers. But they were also supplied by a common DC source. Reference [17] and [18] explored the phase shifting method for non-uniform duty ratios and different input sources for each phase. But this method can only be used in DC-DC converter. Therefore, for the scenario, where multiple distributed inverters connect to the same point of common coupling (PCC), the current interleaving techniques cannot be directly employed and the current harmonics would be randomly summed and induce the current and voltage distortions. The individual inverter cannot guarantee its output current to be purely sinusoidal under the tradeoff among switching frequency, cost and efficiency. Besides, the active power filter (APF) can only compensate the low order harmonics limited by its control bandwidth, leaving the high frequency harmonics unchanged [19][20]. Therefore, the state of the art techniques cannot solve the problem of high frequency current harmonics accumulation in the distribution grid with the high-density distributed inverters.

Distributed voltage source inverters (VSIs) have been widely implemented in many applications, such as PV plants and wind plants, to connect the distributed power sources to power grid [1-6]. The accumulated switching current ripples at the point of common coupling (PCC) are randomly distributed from the maximum allowed value to the minimum value in theory because the switching sequences of the distributed inverters cannot be controlled coordinately.

A global synchronous pulse width modulation (GSPWM) method has been proposed to effectively coordinate the switching sequences [7]. Doing so, the current quality at the PCC can be intentionally controlled even when the current quality of the individual inverter severely exceeds the maximum allowed limitation. On this basis, reference [8] proposed that the GSPWM can help to reduce the value of filter parameters or switching frequency while keeping the power quality at PCC unchanged and then the efficiency or the reliability of inverters can be improved. In order to employ GSPWM in PV station, reference [9] proposed a two-layer GSPWM method which can effectively reduce the common mode leakage current meanwhile attenuate the current harmonics injected into the grid. In addition to eliminating current harmonics and leakage current, reference [10] analyzed the sideband harmonics stability problem and proposed that the GSPWM can synchronize the PWM sequences and in consequence avoid the sideband harmonics instability. Therefore, the GSPWM is expected to become one of the

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solutions to solve high order harmonic accumulation problem or high frequency resonance in complex power electronics system and even simplify the inverter design [11].

When implementing the GSPWM method for distributed inverters, one of the key techniques is to synchronize the PWM sequences among distributed inverters [7]. Intuitively, the low-latency communication system can be employed, while the distributed inverters are not controlled by one central controller and located in a large area. Therefore, compared with multilevel converters or interleaved converters, where a central controller and pre-designed low-latency communication system whose time delay is much lower than 1μs [12] can well satisfy the operational requirement, the PWM sequences synchronization among distributed inverters should be specially designed. The traditional GSPWM method synchronizes the PWM sequences by sending several synchronization pulses per second [7], which means GSPWM does not need high-bandwidth communication channels. But the requirement for low-latency is still necessary. Further, reference [13] proposed a carrier self-synchronization method to deal with the short-term communication fault by analyzing the historical received synchronization signals. But it still cannot avoid the dependence on low-latency communication system. Although some communication systems (Wifi, Zigbee, etc.) have been integrated into distributed inverters, most of them cannot meet the requirement of carrier synchronization because of the unacceptable latency (100us to several seconds) caused by the data packaging or long communication distance [14, 15]. Therefore, the carrier synchronization method without depending on the low-latency communication system becomes necessary. Reference [16] proposed a virtual oscillator control based carrier synchronization method without using communication, which however can only be employed in some specific applications, where the inverters must use a common DC link. So far, the method that can synchronize the carrier among distributed inverters without low-latency communication channels has not been proposed, which limits the implementation reliability of GSPWM method.

Phase locked loop (PLL) has been widely studied and most of them focus on how to synchronize the grid voltage phase or harmonic phase to better operate synchronously with the grid, attenuate harmonics whose frequencies are much lower than switching frequency and increase the operational stability [17-20]. But the existing methods mainly focus on how to design the PLL for current/voltage control loop and the method to synchronize the PWM carrier phase using PLL has not yet been proposed.

Aiming to realize GSPWM without employing the low-latency communication system, this paper proposes a phase locked loop based PWM carrier synchronization (PLL-CS) method that can effectively synchronize the switching sequences without using the low-latency communication signals. In Section II, this paper reviews the basic principles of traditional GSPWM and analyzes the shortcomings, especially the dependence on the low-latency communication system. In Section III, the basic principle and main issues of PLL-CS method are explained and the whole structure of PLL-CS method is proposed, where the estimated voltage phase by PLL is multiplied by the rated pulse ratio to correct the phase of the PWM carrier. In Section IV, the sub-system in PLL-CS for generating the expected carrier is well analyzed and designed by fully considering the features of the estimated voltage phase and the implementation issues of PLL-CS in practice. Finally, the experimental prototype with four distributed inverters whose parameters are different is built to verify the performance of the proposed method.

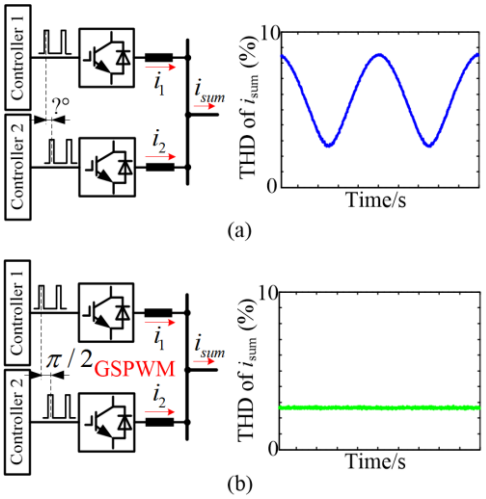

Fig. 1. Phase shift between two inverters and the THD trajectory (a) without GSPWM and (b) with GSPWM.

II. Operational Principle and Communication Requirement of Traditional GSPWM

Before analyzing the dependence on the low-latency communication system, the basic principle of GSPWM will first be presented in this subsection for a brief theoretical introduction. In this paper, the m and N indicate the number and quantity of inverters, where m=1,2,……,N.

When many distributed inverters are connected to the same PCC, their high order current harmonics output will randomly accumulate at PCC because the phase shift angles of PWM sequences among multiple inverters change along with the time progress. To clearly illustrate this phenomenon, a simple example with two identical inverters is assumed [7], whose output harmonic characteristics are generally shown in Fig. 1(a), where the THD of the total current i_{sum} will change along with the time due to the oscillation frequency variation of crystal oscillator inside the micro control unit. The original purpose of GSPWM is to fix the phase shift angles of the triangular carriers around their optimal values, so that the THD of the total current can be minimized as illustrated in Fig. 1(b) [7].

When implementing the GSPWM method in practice, two main issues should be carefully addressed. One is that the inverter parameters, such as switching frequency, output filter, dc-link voltage, and output power, may be different among each other and it is difficult to determine the optimal phase shift angles. Another is that the oscillation frequency of digital controller is not fixed and does not exactly maintain at the rated value during operation, which will lead to the deviation of optimal phase shift angles along with the time progress.

The global synchronous pulse width modulation method was proposed to well solve the above-mentioned two issues in practice, whose basic structure is shown in Fig. 2(a), where the *Calculation part* can calculate the optimal phase shift angles $\varphi_{m,PWMb}$ according to the received parameters and *Synchronization part* can fix the phase shift angels among distributed inverters by sending the low frequency

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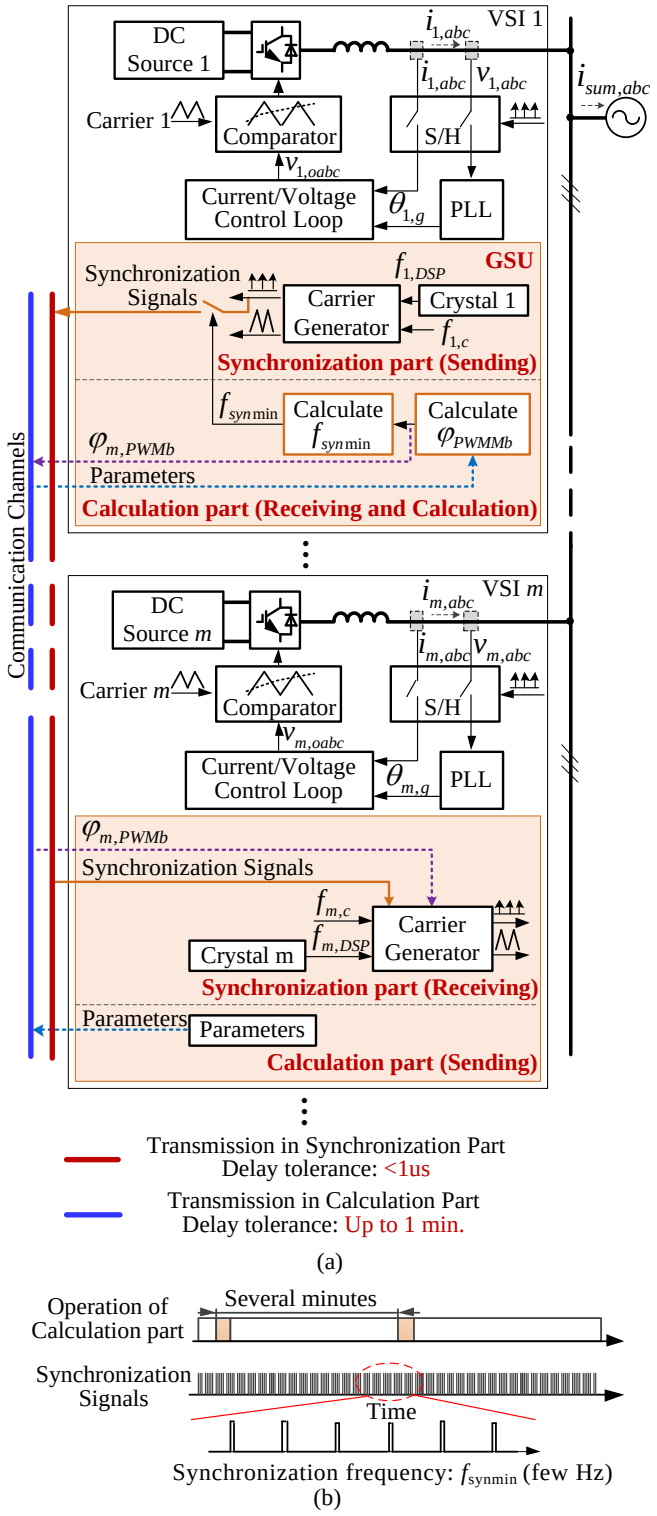

Fig. 2. Illustration of the distributed inverters with the traditional GSPWM method. (a) Block diagram, (b) Operation period of calculation part and synchronization part.

synchronization signals, respectively. Global Synchronization Unit (GSU) can be an individual device or a function embedded into one inverter and will undertake the *Calculation part* as well as the sending function of *Synchronization part*. Other inverters mainly contain the sending function of the *Calculation part* and the receiving function of *Synchronization part*. Other basic functions, including current/voltage control loop, PLL, comparator, sampling hold (S/H) are exactly the same as those in traditional inverters. The procedures of *Calculation part* and *Synchronization part* are summarized here:

Calculation part: Firstly, GSU will collect the operational parameters of distributed inverters including switching frequencies, output filter parameters, dc-link voltages, output power and the operation states of inverters (On/Off). Secondly, GSU calculates the optimal phase shift angles of triangular carriers $\varphi_{m,PWMb}$ using the intelligent calculation method, such as particle swarm optimization (PSO) method, according to the collected parameters. Thirdly, GSU will dispatch the optimal phase shift angles to the distributed inverters. Fourthly, the GSU will calculate the synchronization frequency f_{synmin} according to the switching frequency, parallel connected inverter counts and the maximum deviations of crystal oscillators (generally 30PPM, 1PPM=10^{-6}) to guarantee the THD of total current will not exceed the allowed operation range. The above four procedures do not require the real-time calculation and low-latency communication system because some mandatory parameters for calculation (rated switching frequency and output filter information) are not variable during operation and other mandatory parameters for calculation including dc-link voltage and output power will not change rapidly. After the initial phase shift angle calculation, the GSU needs to update the optimal phase shift angles and the synchronization frequency periodically (e.g. once per several minutes as shown in Fig. 2(b)) to respond to the variation of inverter parameters, especially the output power.

Synchronization part: Upon GSU determines the optimal phase shift angles of triangular carriers and the synchronization frequency, it will send the synchronization signals to the distributed inverters at a very low frequency (e.g. few Hz as shown in Fig. 2(b)) for locating the proper position of triangular carrier initial phase angle and then the corresponding digital controller will modify the phase shift angle of triangular carrier gradually to reach the $\varphi_{m,PWMb}$ [7].

According to the above procedures and structure of traditional GSPWM in Fig. 2(a), both the *Calculation part* and the *Synchronization part* need the communication system. But the requirements for communication system, especially the time delay tolerance and fault tolerance, are totally different for these two parts.

For *Synchronization part*, the dedicated low-latency communication system are necessary because the time delay should be lower than 1μs otherwise the carriers whose frequencies are usually dozens of kHz cannot be well synchronized. In addition, the short-term and the long-term communication faults in *Synchronization part* can invalidate the operation of GSPWM. In contrarily, *Calculation part* does not need the low-latency communication channels because its time delay tolerance can be up to several minutes when calculating and updating the $\varphi_{m,PWMb}$. In practice, the data pack in *Calculation part* can be easily integrated into the existing wireless or wired communication system because of its large time delay tolerant capability.

It is obvious that the main implementation restriction of GSPWM method is the low-latency communication system after carefully comparing the communication requirements of *Synchronization part* and *Calculation part*. Therefore, this paper proposes a new carrier synchronization method for *Synchronization part* without using any dedicated low-latency

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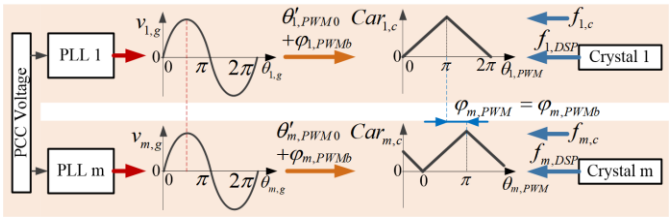

Fig. 3. Illustration of PLL outputs and the carrier generation when using PLL-CS GSPWM.

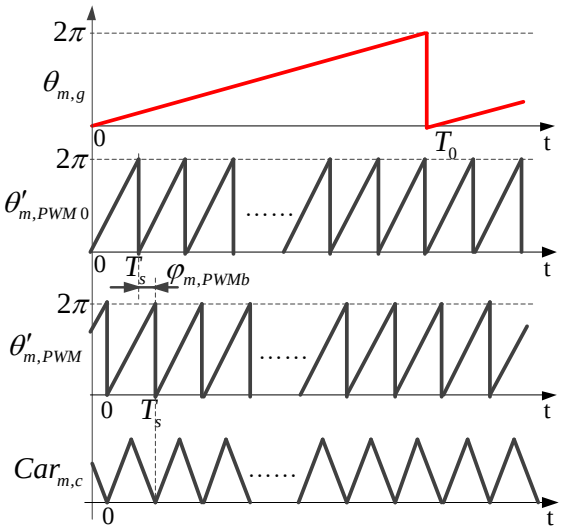

Fig. 4. Illustration of generating carrier phase reference according to $\theta_{m,g}$.

communication system so that the whole GSPWM method can be realized with high operational reliability by only employing the existing wireless or wired communication system inside the commercial distributed inverters.

III. Basic Principles and Whole Structure of PLL-CS

According to the analysis in Section II, the low-latency communication-based PWM carrier synchronization method (C-CS) limits the applicability and reliability of GSPWM. In this section, a PLL-based PWM carrier synchronization method (PLL-CS) is proposed. Different from the C-CS, the PLL-CS can work without the transmitted low-latency synchronization signals, which makes the GSPWM practical and reliable. Additionally, the PLL-CS is a real-time synchronization method and can reduce the fluctuation of total current's THD. The basic principle of PLL-CS is explained below.

In principle, to realize carrier synchronization among distributed inverters, the inverters should obtain a common synchronous information, which should be highly identical for distributed inverters. When the inverters are parallelly connected to the grid, their common information could be the angle of the grid voltage, especially the angle of positive sequence fundamental voltage. Fortunately, the angle of the positive sequence fundamental voltage can be easily obtained by the well-known PLLs. Then, the calculated angle by PLL can multiply the defined pulse ratio, which is a constant number, to help generate the PWM carrier. Doing so, the phase shift angles among the carriers can be fixed and synchronized.

In this section, it is assumed that the PLL can well track the phase angle of grid voltage without any error. The real phase angle and frequency of the fundamental PCC voltage are θ_g and f_g, respectively. The estimated PCC voltage phase angle and frequency by PLL are defined as $\theta_{m,g}$ and $f_{m,g}$, respectively. If the PLL can effectively track the angle of the grid voltage without any error, $\theta_{m,g}$ in distributed inverters will have the same value which is equal to θ_g as shown in Fig. 3, where the PWM carrier is defined as $Car_{m,c}$ and $\theta_{m,PWM}$ indicates the angle of $Car_{m,c}$. The carrier frequency is defined as $f_{m,c}$. The phase difference between $\theta_{m,PWM}$ and $\theta_{1,PWM}$ is indicated as $\varphi_{m,PWM}$. To synchronize the carriers according to the estimated grid voltage angle, $\theta_{m,g}$ will first multiply a constant to generate the basic carrier phase angle $\theta'_{m,PWM0}$ as expressed in (1).

$$\theta'_{m,PWM0}=R_{m,c}\theta_{m,g} \tag{1}$$

Where, $R_{m,c}$ is a defined pulse ratio as:

$$R_{m,c}=\frac{f_{m,c\_r}}{f_{m,g\_r}} \tag{2}$$

Where, f_{m,c_r} and f_{m,g_r} refer to the rated value of $f_{m,c}$ and $f_{m,g}$, respectively. According to (1), $\theta'_{m,PWM0}$ totally depends on $\theta_{m,g}$, which is the same value for distributed inverters because $R_{m,c}$ is a constant value and will not change during operation. Doing so, $\theta'_{m,PWM0}$ can be employed to help synchronize the PWM sequences without any phase shift as shown in Fig. 4.

Then, the optimal phase shift angles $\varphi_{m,PWMb}$ obtained by *Calculation part* in Fig. 2 is added to generate the PWM carrier angle reference $\theta'_{m,PWM}$ given as:

$$\theta'_{m,PWM}=\theta'_{m,PWM0}+\varphi_{m,PWMb} \tag{3}$$

It is obvious that the carrier frequency will directly depend on the estimated PCC voltage frequency as expressed in (4).

$$f_{m,c}=R_{m,c}\cdot f_{m,g} \tag{4}$$

In practice, $R_{m,c}$ could be different for distributed inverters. But the PWM sequences among multiple inverters can still be synchronized once equation (5) is satisfied.

$$\frac{W_{i,c}}{R_{i,c}\cdot f_{i,g}}=\frac{W_{j,c}}{R_{j,c}\cdot f_{j,g}}\Rightarrow\frac{W_{i,c}}{R_{i,c}}=\frac{W_{j,c}}{R_{j,c}} \tag{5}$$

Where, $W_{i,c}$ and $W_{j,c}$ are two independent integers. It is observed that $W_{i,c}$ periods of $Car_{i,c}$ and $W_{j,c}$ period of $Car_{j,c}$ are synchronized. For example, when $R_{i,c}=100, R_{j,c}=200$, 1 period of $Car_{i,c}$ is synchronized with 2 periods of $Car_{j,c}$. Therefore, as long as the GSU can calculate the optimal phase shift angles $\varphi_{m,PWMb}$, the proposed synchronization method for GSPWM can work well.

When implementing the PLL-CS in practice, two main issues should be carefully solved. One is that the output of the PLL cannot track the grid voltage angle without any delay or fluctuation even under steady states. This distortion has little influence on the voltage/current control loop but will effectively influence the PWM synchronization when PLL-CS is employed. Another is that the transient states, such as phase jump or voltage jump, will change the estimated voltage frequency dramatically and further influence the carrier frequency. It is a challenge to limit the switching frequency within the desired range while keeping the PWM synchronization.

In order to solve the above issues, one sub-system including Grid Angle Tracker and Compensation parts is added in PLL-CS as shown in Fig. 5. The output of the PLL is employed as the input of PLL-CS. The Sub-system can track

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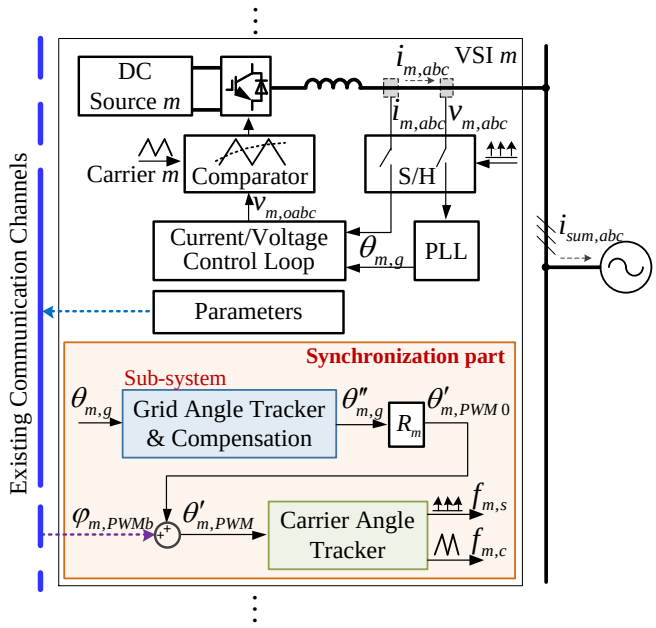

Fig. 5. Block diagram of PLL-CS.

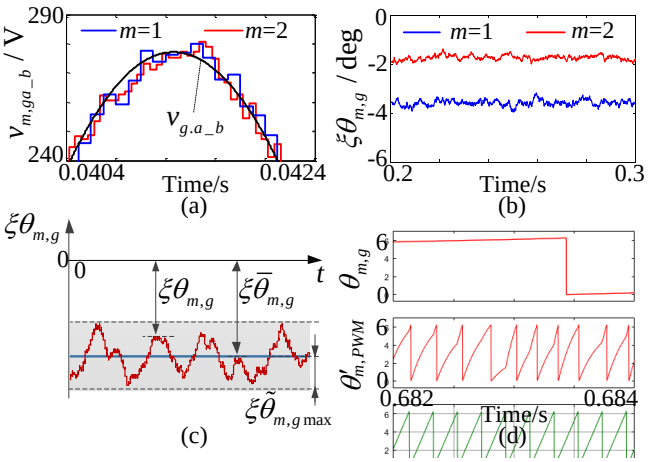

Fig. 6. Simulated PLL results among two distributed inverters in steady states. (a) Grid phase-phase voltage and sampled voltage (f_{1c}=5kHz, f_{2c}=10kHz). (b) $\xi\varphi_{m,g}$ of two inverters. (c) Illustration of offset and fluctuation in $\xi\varphi_{m,g}$.(d) The $\theta'_{m,PWM}$ generated by $\theta_{m,g}$.

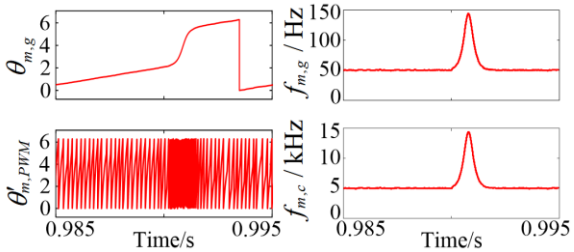

Fig. 7. Illustration of carrier angle and frequency change when phase jump occurs.

the grid voltage angle $\theta_{m,g}$ with small fluctuation and phase delay under steady states to keep the switching frequency in a limited range while keeping the PWM synchronization under transient states.

The *Calculation part* of GSPWM can be embedded into one inverter or several inverters, which is not the focus of this paper and not shown in Fig. 5. The data in *Calculation part*, especially the parameters and $\varphi_{m,PWMb}$ are transmitted by existing communication channels. Only the structure of inverter *m* is shown in Fig. 5, where the structure of PLL-CS among inverters are identical and each inverter can synchronize the carrier individually with its own PLL results. The proposed PLL-CS method does not need the pre-designed low-latency communication system and the additional hardware cost. So, the PLL-CS method makes GSPWM much more practical. It is totally different from the realization principle of the traditional C-CS based GSPWM as shown in Fig. 2.

IV. Realization and Analysis of PLL-CS

A. Realization of PLL-CS

Section III presented the basic principles and whole structures of PLL-CS, whose realization and design principles will be introduced in this subsection. To be noted, there exist many kinds of PLLs with different performance, while the typical synchronous reference frame PLL (SRF-PLL) [17-20] which is a standard PLL in three-phase inverters is employed in this paper for calculating the grid phase angle. The Sub-system in Fig. 5 is firstly designed according to the operational requirement under steady states and then modified by further considering the performance under transient states.

In detail, the real grid phase angle with the possible small disturbance is given by:

$$\theta_g = \theta_{g\_r} + \Delta\theta_g \tag{6}$$

Where, θ_{g_r} indicates the ideal steady state value and $\Delta\theta_g$ refers to the small disturbance in the grid. Fig. 6(a) shows the sampled PCC line voltage waveforms with different $f_{m,s}$ and noise $\tilde{v}_{m,abc}$. $f_{m,s}$ is the sampling frequency which is identical to $f_{m,c}$ in this paper. The grid phase angle calculated by inverter *m* is given as:

$$\begin{aligned} &\theta_{m,g} = \theta_{g\_r} + \Delta\hat{\theta}_{m,g} + \xi\bar{\theta}_{m,g} + \xi\tilde{\theta}_{m,g} \\ &\Delta\hat{\theta}_{m,g}(s) = G_{m,PLL}(s)\Delta\theta_g(s) \end{aligned} \tag{7}$$

Where, $\Delta\hat{\theta}_{m,g}$ represents the output disturbance caused by $\Delta\theta_g$ in PLL small-signal model. $\xi\bar{\theta}_{m,g}$ and $\xi\tilde{\theta}_{m,g}$ indicate the steady state offset mainly caused by Zero-Order-Hold (ZOH) and the fluctuation caused by the noise, respectively. $G_{m,PLL}(s)$ is the small signal transfer function of PLL. Fig. 6(b) shows the waveform of $\xi\theta_{m,g}$, which indicates the phase difference between $\theta_{m,g}$ and θ_g as expressed below.

$$\begin{aligned} \xi\theta_{m,g}(s) &= \theta_{m,g}(s) - \theta_g(s) \\ &= \left(G_{m,PLL}(s) - 1\right)\Delta\theta_g(s) + \xi\bar{\theta}_{m,g}(s) + \xi\tilde{\theta}_{m,g}(s) \end{aligned} \tag{8}$$

Since $\Delta\theta_g(s)$ is identical for all inverters, therefore, the phase difference caused by $\Delta\theta_g(s)$ does not have influence on the carrier synchronization with a well-designed PLL-CS. But $\xi\bar{\theta}_{m,g}$ and $\xi\tilde{\theta}_{m,g\max}$ are totally different among inverters, so they are the main variables that will introduce different phases. As shown in Fig. 6(c), the maximum range of fluctuation is defined as $\xi\tilde{\theta}_{m,g\max}$. In order to synchronize the PWM carrier phase using the PLL results, $\xi\bar{\theta}_{m,g}$ and $\xi\tilde{\theta}_{m,g\max}$ should be attenuated as much as possible because $\xi\bar{\theta}_{m,g}$ can

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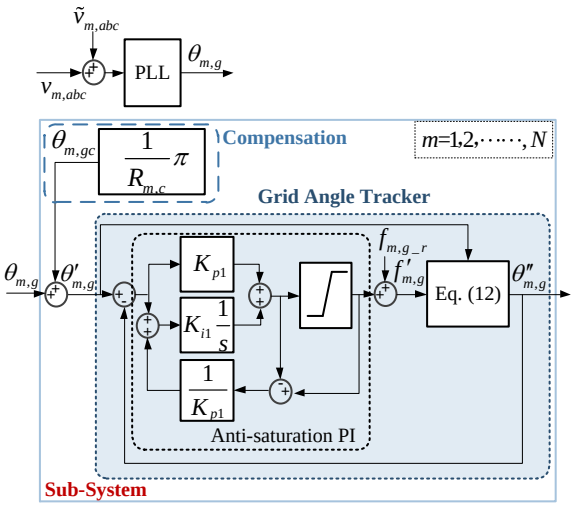

Fig. 8. Detail block diagrams of Sub-system in PLL-CS.

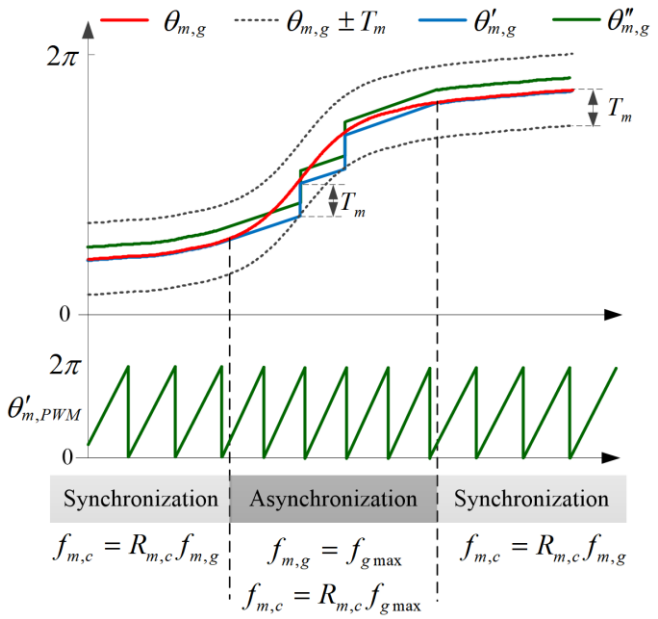

Fig. 9. Illustration of $\theta_{m,g}$, $\theta'_{m,g}$, $\theta''_{m,g}$, $\theta'_{m,PWM}$ during transient state.

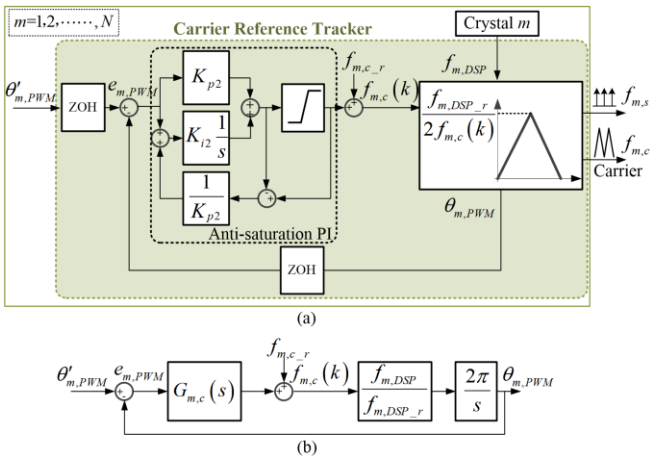

Fig. 10. (a) The structure and (b) block diagram of Carrier Angle Tracker (CAT).

lead to the offset of $\theta'_{m,PWM}$ and $\xi\tilde{\theta}_{m,g\max}$ can cause the distortion of $\theta'_{m,PWM}$ as shown in Fig. 6(d). The offset and distortion in $\theta'_{m,PWM}$ can make $\varphi_{m,PWM}$ unfixed. Therefore, the compensation and low-pass filtering capability of the Sub-system should overcome these problems and reduce $\xi\theta_{m,g}$ in steady state.

During the transient states, a phase jump or frequency jump of the PCC voltage will increase or reduce the estimated $f_{m,g}$ and further directly influence the value of $f_{m,c}$ according to (4). $f_{m,c}$ is proportional to the change rate of $\theta_{m,g}$. This phenomenon is shown in Fig. 7, where the phase angle of the PCC voltage suddenly changes and $f_{m,c}$ will rise to a large value while the range of $f_{m,c}$ should be limited in practice otherwise it will increase the power loss and even destroy the inverter. So, a saturation function should be integrated into the Sub-system in Fig. 5. But the PWM carriers cannot be synchronized once the saturation occurs because the $f_{m,c}$ will be a constant value and the phase shift angles cannot be fixed due to the oscillation frequency deviation of the crystal. So, the Sub-system should quickly resume from the saturation when only the transient state is considered.

To solve the above issues in steady states and transient states, the block diagram of the Sub-system is shown in Fig. 8, which mainly contains a grid angle tracker (GAT) and phase compensation parts. In specific, the phase compensation part is added to compensate $\xi\bar{\theta}_{m,g}$ introduced by ZOH. It has been proved in many papers that ZOH causes $0.5T_{m,s}$ time delay when the sampling frequency is much higher than the signal frequency [21]. So, the phase compensation $\theta_{m,gc}$ is calculated with:

$$\theta_{m,gc}=\frac{1}{R_{m,c}}\pi\approx-\xi\bar{\theta}_{m,g} \tag{9}$$

According to (9), $\xi\bar{\theta}_{m,g}$ can be well compensated even when the rated ratios $R_{m,c}$ are different. After adding $\theta_{m,gc}$, $\theta_{m,g}$ is modified as $\theta'_{m,g}$ in (10):

$$\theta'_{m,g}=\theta_{m,g}+\theta_{m,gc}=\theta_{g\_r}+\Delta\hat{\theta}_{m,g}+\xi\tilde{\theta}_{m,g} \tag{10}$$

The saturation is integrated in the GAT with an upper limit $f'_{m,g\max}$ and lower limit $f'_{m,g\min}$, which are given as:

$$f'_{m,g\max}=f_{g\max}-f_{m,g\_r};\ f'_{m,g\min}=f_{g\min}-f_{m,g\_r} \tag{11}$$

Where, $f_{g\min}$ and $f_{g\max}$ indicate the minimum and maximum frequency of the grid. In order to avoid the saturation of the integral part of the traditional PI controller, anti-saturation in the PI controller is employed.

In addition, equation (12) in Fig. 8 is given as:

$$\begin{cases}\text{if } \theta''_{m,g}(k-1)-\theta'_{m,g}(k-1)\ge T_m\\ :\ \theta''_{m,g}(k)=\theta''_{m,g}(k-1)-T_m\\ \hline \text{if } \theta''_{m,g}(k-1)-\theta'_{m,g}(k-1)\le -T_m\\ :\ \theta''_{m,g}(k)=\theta''_{m,g}(k-1)+T_m\\ \hline \text{else}\\ :\ \theta''_{m,g}(k)=\theta''_{m,g}(k-1)+2\pi f'_{m,g}(k-1)\cdot T_{m,s}(k-1)\end{cases} \tag{12}$$

Where, T_m is a constant value and it should be carefully calculated, otherwise it will impact the Carrier Angle Tracker function in Fig. 5. T_m can be written as:

$$T_m=\mathrm{Q}\cdot 2\pi/R_{m,c} \tag{13}$$

Where, Q is an integer number. It is noted from (12) that $\theta''_{m,g}$ will be corrected by adding T_m or $-T_m$ when $\theta''_{m,g}$ cannot track $\theta'_{m,g}$ within the limited range of T_m because of

the saturation effect. Doing so, $\theta'_{m,PWM}$ will suddenly change with $Q\cdot 2\pi$. Fortunately, it will not influence the continuity of $\theta'_{m,PWM}$ because Q is an integer number. With (12), the PLL-CS can quickly resume from the saturation and change from asynchronization state to synchronization state within one fundamental period.

B. Synchronization Accuracy Analysis under Steady State

Under steady state, (12) performs like an integration function when $\theta''_{m,g}$ can track $\theta'_{m,g}$ within a limited range. The transfer function $G_{m,GAT}(s)$ from $\theta'_{m,g}$ to $\theta''_{m,g}$ is given as:

$$G_{m,GAT}(s)=\frac{K_{p1}s+2\pi K_{i1}}{s^2+K_{p1}s+2\pi K_{i1}} \tag{14}$$

So, $\theta''_{m,g}$ is given as:

$$\begin{aligned}&\theta''_{m,g}(s)=G_{m,GAT}(s)\cdot\theta'_{m,g}(s)\\&=G_{m,GAT}(s)\theta_{g\_r}(s)+G_{m,GAT}(s)G_{m,PLL}(s)\Delta\theta_g(s)\\&+G_{m,GAT}(s)\xi\tilde{\theta}_{m,g}\end{aligned} \tag{15}$$

Although GAT is not a traditional low pass filter (LPF), $G_{m,GAT}(s)$ is a second-order system and presents the low-pass filtering characteristics. So, K_{p1} and K_{i1} are chosen to make $G_{m,GAT}(s)$ over-damped in order to avoid oscillation because the stability problem is not the main issue and $\theta''_{m,g}$ should be as smooth as possible. The purpose of integrating GAT instead of the traditional LPF is to realize the carrier synchronization both in steady states and transient states.

$\theta''_{m,g}$ is further employed to generate the carrier angle reference. So, the synchronization accuracy of the carrier depends on the synchronization accuracy of $\theta''_{m,g}$. The phase shift between two $\theta''_{m,g}$ (m=*i* and m=*j*) is defined as $\Delta\varphi_{ij,g}$ which is given as:

$$\begin{aligned}&\Delta\varphi_{ij,g}=\theta''_{i,g}-\theta''_{j,g}\\&=\left(G_{i,GAT}(s)-G_{j,GAT}(s)\right)\theta_{g\_r}(s)\\&+\left(G_{i,GAT}(s)G_{i,PLL}(s)-G_{j,GAT}(s)G_{j,PLL}(s)\right)\Delta\theta_g(s)\\&+\left(G_{i,GAT}(s)\xi\tilde{\theta}_{i,g}-G_{j,GAT}(s)\xi\tilde{\theta}_{j,g}\right)\end{aligned} \tag{16}$$

$G_{i,GAT}(s)$ and $G_{j,GAT}(s)$ have the same response characteristics at low frequency because of the low-pass filter characteristics. So, θ_{g_r}, which is a constant value under steady state, will not contribute to $\Delta\varphi_{ij,g}$. Then, (16) can be simplified as (17):

$$\begin{aligned}&\Delta\varphi_{ij,g}=\theta''_{i,g}-\theta''_{j,g}\\&=\left(G_{i,GAT}(s)G_{i,PLL}(s)-G_{j,GAT}(s)G_{j,PLL}(s)\right)\Delta\theta_g(s)\\&+\left(G_{i,GAT}(s)\xi\tilde{\theta}_{i,g}-G_{j,GAT}(s)\xi\tilde{\theta}_{j,g}\right)\end{aligned} \tag{17}$$

When $G_{m,GAT}(s)\cdot G_{m,PLL}(s)$ are totally the same, (17) can be further simplified. But in real applications, $G_{m,GAT}(s)\cdot G_{m,PLL}(s)$ in different inverters cannot be totally the same in the full frequency band. One reason is that $G_{m,PLL}(s)$ depends on the structure and parameters of PLL. Another reason is that the control system is discrete in practice, and the transfer function is influenced by the sampling frequency in the z-domain. Fortunately, the small-signal models of the most well-known PLLs are similar for the positive-sequence fundamental signals [16] and the sampling frequency mainly influences the transfer function at high frequency. So, $G_{m,GAT}(s)\cdot G_{m,PLL}(s)$ in different inverter can be treated equal at low frequency by carefully tuning $G_{m,GAT}(s)$. Also, $\Delta\theta_g$ is a low frequency disturbance under steady states when the power system has enough inertia [22]. So, (17) can be further simplified as:

$$\begin{aligned}&\Delta\varphi_{ij,g}=\theta''_{i,g}-\theta''_{j,g}\\&=G_{i,GAT}(s)\xi\tilde{\theta}_{i,g}-G_{j,GAT}(s)\xi\tilde{\theta}_{j,g}=\xi\tilde{\theta}''_{i,g}(s)-\xi\tilde{\theta}''_{j,g}(s)\end{aligned} \tag{18}$$

Where, $\Delta\varphi_{ij,g}$ is mainly caused by the noise and can be reduced with the well-designed $G_{m,GAT}(s)$.

Doing so, the phase shift angle $\varphi_{m,PWM}$ is given as:

$$\varphi_{m,PWM}=R_{m,c}\xi\tilde{\theta}''_{m,g}+\varphi_{m,PWMb} \tag{19}$$

$\varphi_{m,PWM}$ contains the fluctuation and the optimal phase shift angle. So, the range of $\varphi_{m,PWM}$ is given as:

$$\varphi_{m,PWMb}-R_{m,c}\xi\tilde{\theta}''_{m,g\max}\le\varphi_{m,PWM}\le\varphi_{m,PWMb}+R_{m,c}\xi\tilde{\theta}''_{m,g\max} \tag{20}$$

Where, $\xi\tilde{\theta}''_{m,g\max}$ indicates the fluctuation range of $\xi\tilde{\theta}''_{m,g}$. $\xi\tilde{\theta}''_{m,g\max}$ is determined both by the noise and filter capability of the $G_{m,GAT}(s)$. $\xi\tilde{\theta}''_{m,g\max}$ is small, but the fluctuation range in $\varphi_{m,PWM}$ is $R_{m,c}$ times of $\xi\tilde{\theta}''_{m,g\max}$. The fluctuation of $\varphi_{m,PWM}$ will increase the RMS value of the total harmonics. In order to properly design $G_{m,GAT}(s)$ which can determine the value of $\xi\tilde{\theta}''_{m,g\max}$, the worst RMS value of total harmonics can be evaluated by the following equation:

$$\begin{aligned}&\max\quad I_{sumh}=F(\varphi_{PWM})=\sqrt{\sum_{f=0}^{\infty}\left|\sum_{m=1}^{N}\dot{I}_{m,hf}(\varphi_{m,PMW})\right|^2}\\&\textit{Subject to}\quad \boldsymbol{\varphi}_{PWM}=\left[\varphi_{1,PWM},\varphi_{2,PWM},\cdots\cdots,\varphi_{N,PWM}\right]\\&\qquad\varphi_{m,PWMb}-R_{m,c}\xi\tilde{\theta}''_{m,g\max}\le\varphi_{m,PWM}\le\varphi_{m,PWMb}+R_{m,c}\xi\tilde{\theta}''_{m,g\max}\end{aligned} \tag{21}$$

Where, $\dot{I}_{m,hf}$ refers to the phasor of output current harmonics injected from inverter *m* with frequency *f* [7]. The THD of the total current can be calculated as:

$$THD_{sum}=\frac{I_{sumh}}{I_{sum1}} \tag{22}$$

Equation (21) is calculated with intelligent optimization method (e.g. PSO: Particle Swarm Optimization) in order to get the maximum value of I_{sumh}. The maximum THD_{sum} can be calculated with (22). If the maximum THD_{sum} is large and cannot meet the requirement (e.g. <5%), then the bandwidth of all $G_{m,GAT}(s)$ can be reduced with the same factor and repeat the above evaluation until THD_{sum} will meet the requirement.

C. Synchronization Accuracy Analysis under Transient States

When phase jump or frequency jump occurs, the output of the anti-saturation PI controller in Fig. 8 will saturate due to (11) and $f_{m,g}$ can be limited in the range of [$f_{g\min}$, $f_{g\max}$]. As a consequence, $f_{m,c}$ can be limited in the range of [$R_m f_{g\min}$, $R_m f_{g\max}$]. But the PWM carriers cannot be synchronized if saturation occurs because $f_{m,c}$ will have a constant value, which is $R_m f_{g\min}$ or $R_m f_{g\max}$ and the phase shift cannot be fixed because of the oscillation frequency deviation of the crystal the same as the performance without GSPWM introduced in Section II. Equations (12) and (13) can make the GAT to resume from the saturation within a few calculation periods

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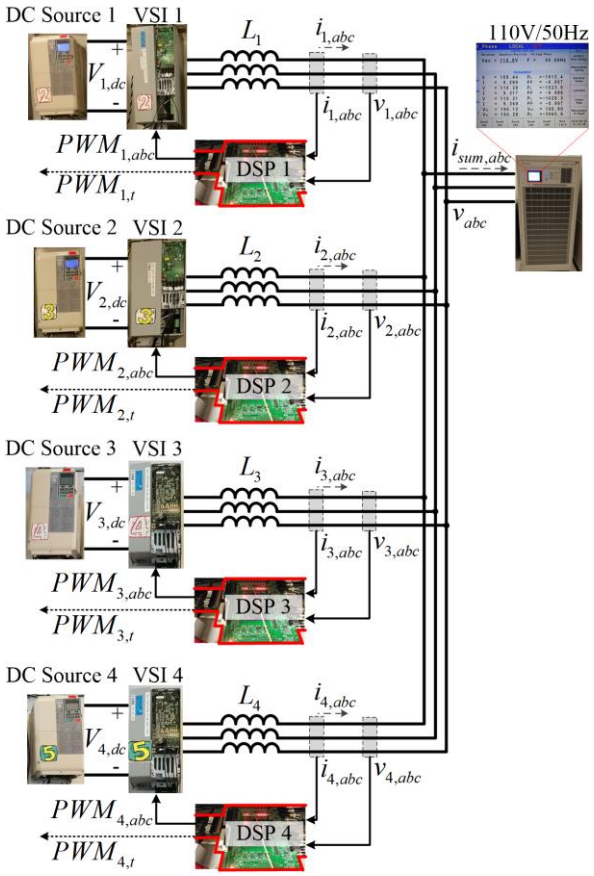

Fig. 11. Configuration of the experimental setup.

TABLE I. PARAMETERS OF EXPERIMENT 1

m	$V_{m,dc}$ /V	L_m /mH	$f_{m,c}$ /kHz	P_m /W	Q_m /W	$\varphi_{m,PWMb}$
1	600	5	5	550	0	0
2	600	5	5	550	0	π/2

while maintain the slope of $\theta''_{m,g}$ in a limited range as shown in Fig. 9. The PLL-CS can then resume from asynchronization when the slope of $\theta_{m,g}$ returns to the limited range. Most of the PLL can well track θ_g within one fundamental period even when the worst frequency jump or phase jump occurs. So, the PLL-CS can resume from asynchronization within one fundamental period. This response time is acceptable, because the main current distortion in the first fundamental period after a large disturbance is mainly induced by the overcurrent and not the switching ripple.

D. Carrier Angle Tracker (CAT)

The function of CAT in Fig. 5 is to control the angle of carrier by dynamically generating the carrier with changeable frequency to track $\theta'_{m,PWM}$. The CAT contains a phase detector, a loop filter and a controlled PWM generator. The structure of CAT is shown in Fig. 10(a).

The phase detector can detect the phase difference between the reference angle $\theta'_{m,PWM}$ of carrier m and the real angle $\theta_{m,PWM}$ of carrier m:

$$e_{m,PWM}=\theta'_{m,PWM}-\theta_{m,PWM} \tag{23}$$

Another anti-saturated PI controller is employed in CAT, whose transfer function is given as:

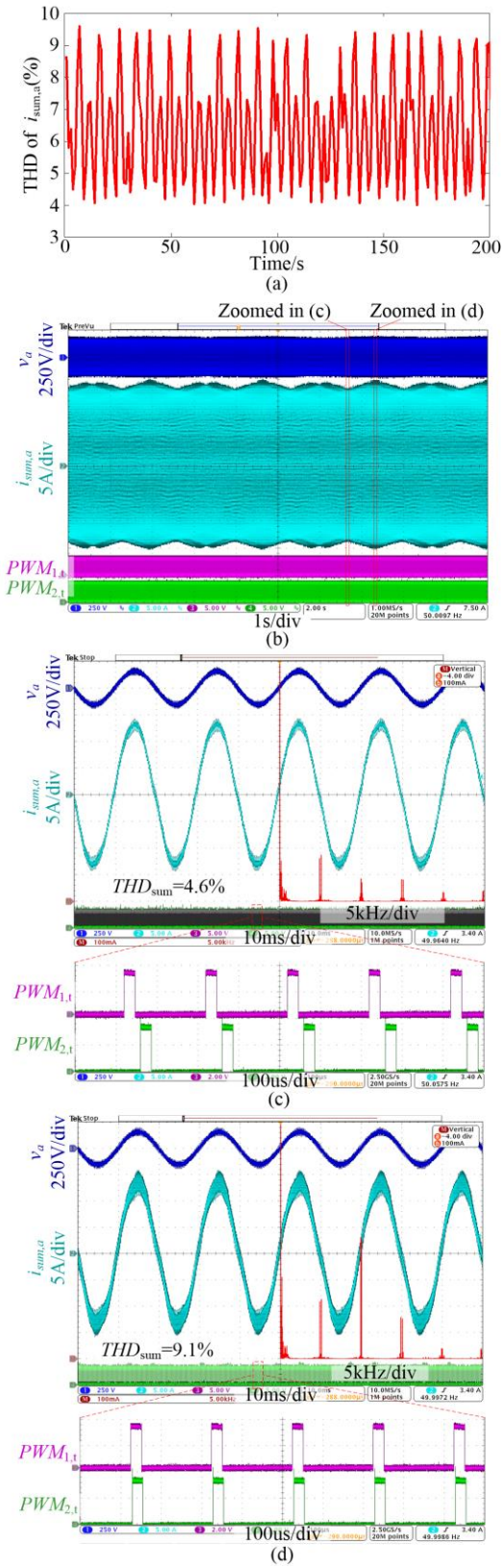

Fig. 12. Experimental results with C-CS based GSPWM: (a) THD trajectory of $i_{sum,a}$; (b) Waveforms from 120s to 140s (c) Zoomed waveforms and FFT spectrum of $i_{sum,a}$ in (b); (d) Zoomed waveforms and FFT spectrum of $i_{sum,a}$ in (b).

$$G_{m,c}(s)=K_{p2}+K_{i2}\frac{1}{s} \tag{24}$$

The output of the PI controller in CAT is $f_{m,c}$ and it can only

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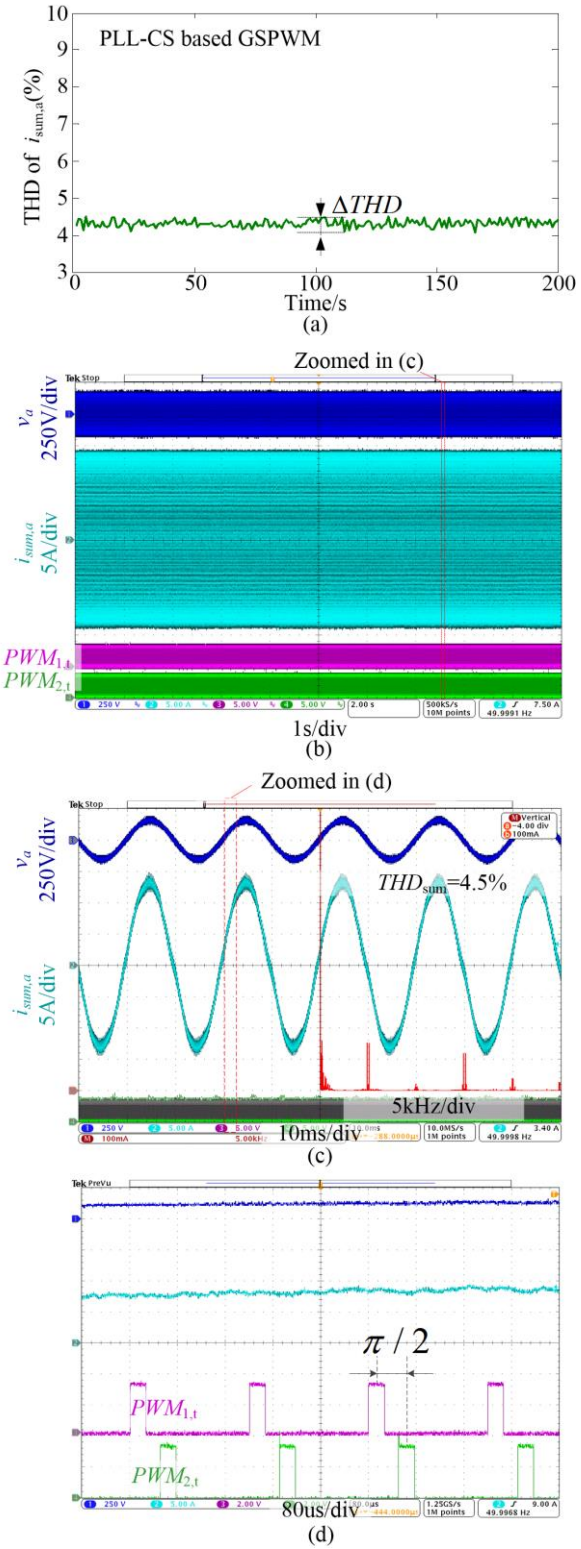

Fig. 13. Experimental results with PLL-CS based GSPWM: (a) THD trajectory of $i_{sum,a}$; (b) Waveforms from 120s to 140s; (c) Zoomed waveforms and FFT spectrum of $i_{sum,a}$ in (b); (d) Zoomed waveforms in (c).

change in a limited range, whose upper and lower limits are:

$$f_{m,c\min} = R_m f_{g,\min}; \quad f_{m,c\max} = R_m f_{g,\max} \tag{25}$$

Then the carrier is generated by setting the peak value of the carrier according to $f_{m,c}(k)$:

$$C_{m,peak}(k) = \frac{f_{m,DSP\_r}}{2 f_{m,c}(k)} \tag{26}$$

Where, f_{m,DSP_r} is the rated resonance frequency of crystal. $\theta_{m,PWM}$ is the integral of $f_{m,c}$. So, in the s-domain, the controlled carrier generator is given as:

$$\theta_{m,PWM} = 2\pi f_{m,c} \frac{1}{s} \tag{27}$$

The block diagram of CAT is shown in Fig. 10(b), where $f_{m,DSP}$ changes within the range of 30 PPM(1PPM=10^{-6}). The CAT is a 2nd-order system and can be easily tuned. The open loop gain of the CAT is influenced by $f_{m,DSP}$ and can only change within small range. The CAT is a closed-loop control system and open loop gain can only influence the stability performance within small range. So, the $\theta_{m,PWM}$ can track $\theta'_{m,PWM}$ without error and the tracking accuracy will not be influenced by the real frequency of oscillator from a long-term perspective.

To be noted, the calculation frequency of PLL-CS is the same as the calculation frequency in traditional inverter control strategy. It will not increase the calculation burden of DSP. So, the controllers do not need to be updated. With the well-designed control parameters in PLL-CS, the sensors that widely used in traditional inverters can still satisfy the requirement of PLL-CS.

V. Experimental Verification

The constructed experimental prototype has four distributed three-phase VSIs with their own independent DC sources, 3-phase two-level power converter, output filters and digital controllers. And the configuration of experimental setup is shown in Fig. 11. The used DSP is TMS320F28335. All inverters are connected to an emulated grid using a programmable AC source, whose RMS value of output voltage is 110V and the rated output frequency is 50Hz. The oscilloscope with 4 channels is used to record the waveforms. In experiment 1, only two inverters with the totally same parameters are employed because the synchronization performance can be easily seen according to the THD of total current. In experiment 2, four inverters with different parameters are employed to verify the applicability in practice. The results in steady state and transient state are recorded and analyzed. $PWM_{m,abc}$ are the three phase PWM sequences that control VSI m. $PWM_{m,t}$ is the PWM sequence with constant duty cycle, which is synchronized with $PWM_{m,abc}$ and only employed to test the carrier synchronization among VSI m.

Experiment 1:

The parameters of inverters in experiment 1 are shown in Table 1. Both the steady state results and transient state results are recorded and analyzed.

A. Steady State Results and Analysis

In experiment 1, the frequency of grid voltage changes slowly within a limited range from 49.8Hz to 50.2Hz.

Firstly, the waveforms without GSPWM method are recorded and analyzed. Fig. 12 shows the experimental results without GSPWM. Fig. 12(a) shows the THD trajectory of $i_{sum,a}$ which fluctuates because of the unfixed PWM phase shift angles. Fig. 12(b) shows the waveforms from 120s to 140s, where the current ripple of $i_{sum,a}$ fluctuates. Two zoomed views

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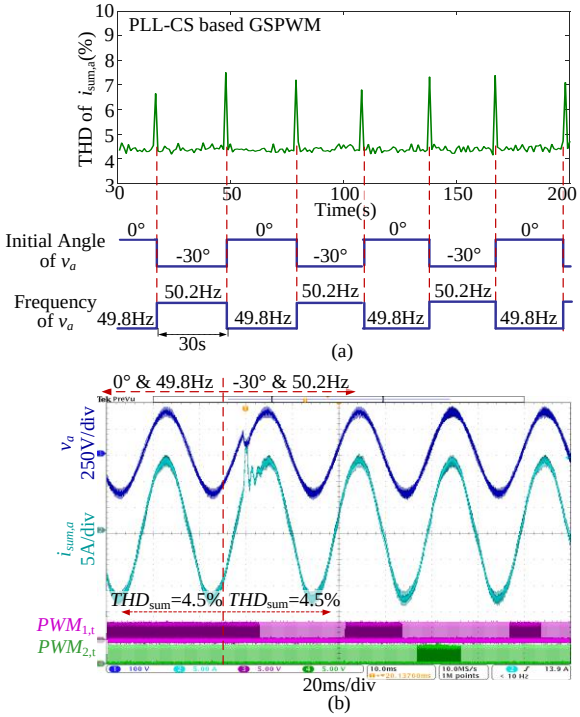

Fig. 14. Experimental results in transient state: (a) *THD* trajectory of $i_{sum,a}$ with PLL-CS based GSPWM; (b) captured waveforms during transient state.

TABLE II. PARAMETERS OF EXPERIMENT 2

m	$V_{m,dc}$ /V	L_m /mH	$f_{m,c}$ /kHz	P_m /W
1	330	2	10	195
2	350	3	10	140
3	296	5	5	156
4	304	4	5	200

at different time are shown in Fig. 12(c) and Fig. 12(d), which indicates that the THD of $i_{sum,a}$ is changing without GSPWM.

Then, the proposed PLL-CS based GSPWM is employed. The PLL-CS does not depend on the low-latency communication signals. So, it is unnecessary to add additional communication channels. The THD of $i_{sum,a}$ can always be lower than 5% as shown in Fig. 13(a), where the fluctuation of the THD is indicated by ΔTHD. Fig. 13(b) shows the waveforms from 120s to 140s, where the current ripple in $i_{sum,a}$ is almost a constant value. Fig. 13(c) shows the zoomed view of Fig. 13(b). And Fig. 13(d) is the zoomed view of Fig. 13(c), which shows that the PWM phase shift angle is a fixed value of $\pi/2$. ΔTHD is mainly determined by the fluctuation in $\theta''_{m,g}$ as analyzed in equations (19)-(22) and it can be reduced by designing well K_{p1} and K_{i1}.

B. Transient State Results and Analysis

In experiment 1, both the frequency and phase of grid voltage will change suddenly to verify the performance of PLL-CS GSPWM under transient state. The frequency of programmable AC source is set to jump between 49.8Hz and 50.2Hz with period of 30s meanwhile the phase is set to jump between 0° and -30° with period of 30s either. To be noted, the PLL-CS GSPWM can still work when 180° phase jump occurs. But the 180° phase jump will lead to large overcurrent and may damage the prototype. So, 30° phase jump is chosen to verify PLL-CS method. Fig. 14(a) shows the THD trajectory of $i_{sum,a}$ and the trajectories of the voltage phase and voltage frequency when PLL-CS is employed. The PLL-CS based GSPWM can keep the THD in a limited range. The rise of THD is mainly caused by the overcurrent at the jump instant. Fig. 14(b) shows the waveforms of one transient instant, where the THD is still a constant value if the overcurrent is ignored. That means the PLL-CS method can still fix the phase shift even when the frequency jump or phase jump occurs.

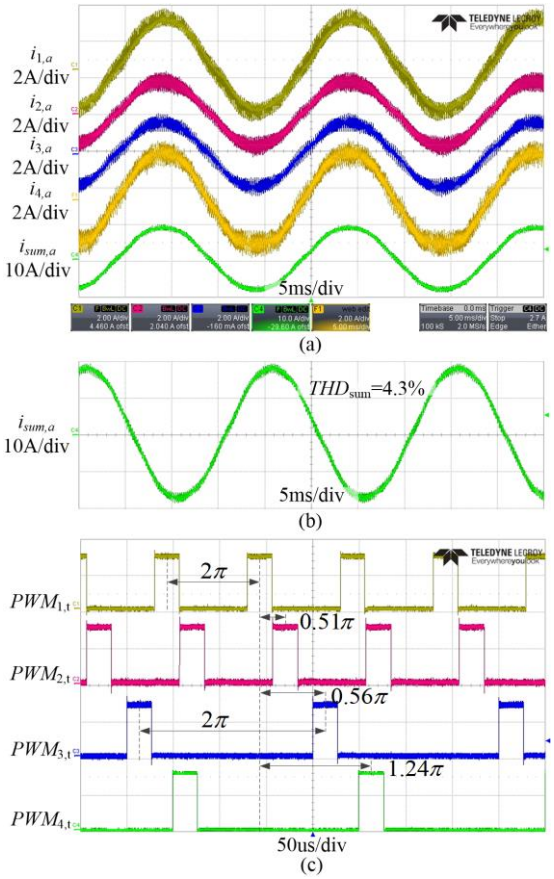

Fig. 15. Experiment waveforms of 4 inverters with PLL-CS in steady state: (a) waveforms of $i_{1,a}$, $i_{2,a}$, $i_{3,a}$, $i_{4,a}$, $i_{sum,a}$; (b) zoomed waveforms of $i_{sum,a}$; (c) waveforms of $PWM_{m,t}$.

Experiment 2:

In experiment 1, the basic performance of PLL-CS has been verified both under steady and transient states. In practice, the parameters of inverters can be different. So, in order to further verify the applicability of PLL-CS, four inverters with different parameters are employed. The parameters are shown in Table II. Being similar to experiment 1, both the steady state results and transient state results are recorded and analyzed.

A. Steady State Results and Analysis

In experiment 2, the frequency of grid voltage will also change slowly with the limited range from 49.8Hz to 50.2Hz. If GSPWM is not employed, the THD of $i_{sum,a}$ can be larger than 7%. By employing PLL-CS based GSPWM, the THD of $i_{sum,a}$ can always be lower than 5% even when the parameters of inverters are different. Fig. 15(a) shows the experimental waveforms of $i_{1,a}$, $i_{2,a}$, $i_{3,a}$, $i_{4,a}$, $i_{sum,a}$, where the zoomed view of $i_{sum,a}$ and THD are shown in Fig. 15(b). Fig. 15(c) shows the phase shift angles of PWM sequences, where the phase shift angles can be fixed at optimal values with limited fluctuation.

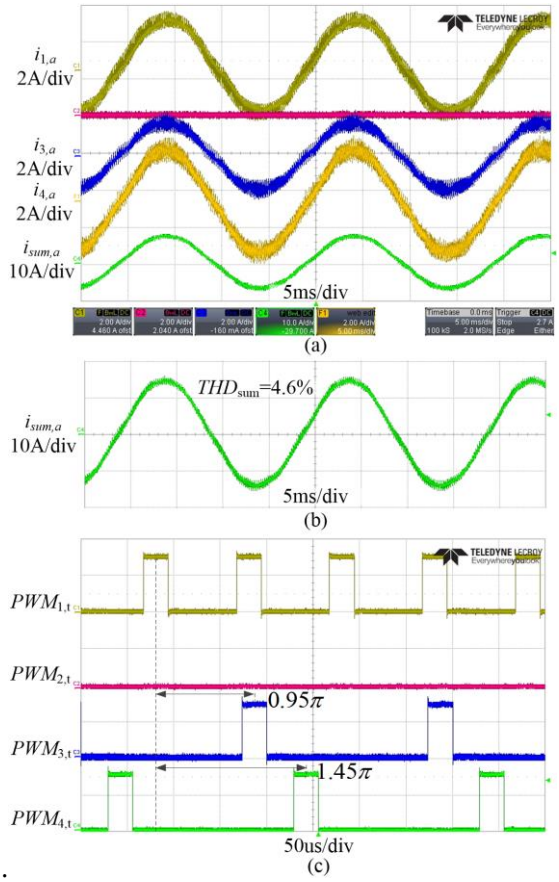

Fig. 16. Experimental waveforms when inverter 2 quits: (a) waveforms of $i_{1,a}$, $i_{3,a}$, $i_{4,a}$, $i_{sum,a}$; (b) zoomed waveforms of $i_{sum,a}$ (c) waveforms of $PWM_{m,t}$.

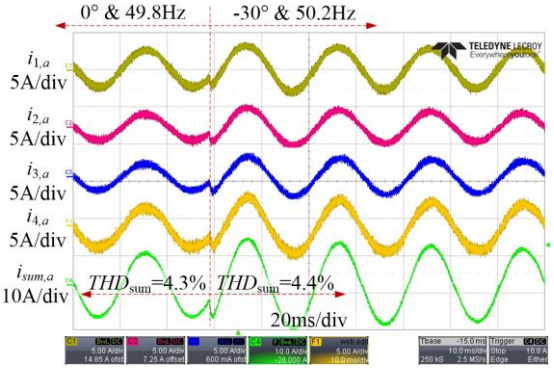

Fig. 17 Experimental waveforms of $i_{1,a}$, $i_{2,a}$, $i_{3,a}$, $i_{4,a}$, $i_{sum,a}$ with PLL-CS in one transient state moment.

In practice, some inverters may quit or restart, where the optimal phase shift angles should be updated. The new optimal phase shift angles are updated by *Calculation Part* through the existing communication channels. In this experiment, inverter 2 quits and the optimal phase shift angles are updated. As shown in Fig. 16, inverter 2 quits and the THD of total current can still keep at the minimum value by updating the optimal phase shift angles from $[0,0.51\pi,0.56\pi,1.24\pi]$ to $[0,\text{---},0.95\pi,1.45\pi]$. That means the GSPWM can well operate with the proposed PLL-CS method.

B. Transient State Results and Analysis

Similarly to the grid in experiment 1, the frequency will jump between 49.8Hz and 50.2Hz meanwhile the phase jumps between 0° and -30° with period of 30s. Fig. 17 shows the waveforms of one transient state moment, where the THD is still a constant value if overcurrent is ignored. That means the PLL-CS method can still fix the phase shift angles during transient state even when the parameters of inverters are different.

VI. Conclusion

This paper proposes a PLL based carrier synchronization method, which can operate without the traditional low-latency synchronization signals, making the GSPWM reliable and applicable. The basic principles of PLL-CS are proposed and their main issues that should be considered are analyzed. Then, a detailed sub-system is added in PLL-CS GSPWM to satisfy the requirements under steady state and transient state operation conditions. The corresponding synchronization accuracy is analyzed. Finally, the experimental results have verified the performance of the proposed PLL-CS method. The PLL-CS carrier synchronization method can be employed even when the parameters of inverters are different.

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