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Analysis of Class-DE PA Using MOSFET Devices With Non-Equally Grading Coefficient

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***Abstract*— The design and analysis of a new operation-mode of the class-DE power amplifier (PA) using two MOSFETs with the non-equal grading coefficient is introduced. The PA uses the optimum shunt capacitance for each MOSFET to achieve zero voltage switching (ZVS) condition and wide range for the load-resistance point of view. As compared with the conventional class-DE PA, this configuration has low value of the series inductance that is reduced the power dissipation. A design procedure with intuitive curves is obtained that are implemented using a different grading coefficient for two MOSFETs. These criteria prepared an effective approach regardless of the fixed shunt capacitance for achieving ZVS condition. The desired operation of the class-DE PA is guaranteed by converging of design parameters and required output power. Moreover, non-similar switches provide reduced switch power dissipations and the number of the driving circuit PA. The simulation and experiment results are approved by implementing the outlined theoretical relationships for a fabricated class-DE PA at 4-MHz switching frequency and obtained 12.1-W output power.**

***Index Terms*— Class-DE power amplifier, switch stress, zero voltage switching (ZVS), zero-derivative switching (ZDS), loaded-quality factor, high efficiency, load-resistance.**

I. Introduction

THE class-DE Power Amplifier (PA) is a developed configuration of a class-D PA topology based on the satisfaction of the class-E nominal conditions, i.e., both zero-voltage switching (ZVS) and zero-derivative switching (ZDS) conditions simultaneously. This operation-mode is obtained using a parallel capacitance to each switch device in the class-D PA configuration [1]–[3]. The active device, i.e., transistor operation-mode with the switching characteristic makes zero-power dissipation and theoretically 100% power conversion efficiency. The class-DE operation-mode is one of an efficient way to satisfy the critical requirements of high-efficiency power amplifiers (PAs) for high-speed wireless communication systems [4]–[6]. The energy consumption in the transmitter is nominated by the function of the PA module. Therefore, the class-DE PA family has been capable to create an effective design environment in high-efficiency and high-frequency power converters. The effect of two parallel capacitances between the drain and the source of the MOSFETs is nominated with the increment of the operating frequency [7]–[10]. The accurate tuning of parallel capacitances is the main critical procedure to satisfy the class-E conditions. The required shunt capacitance is achieved by adding a linear external capacitance with two MOSFETs. On the other hand, the MOSFET drain-source parasitic capacitance is a nonlinear element, which has considerably valued as the operating frequency is increased.

The conventional class-DE operation-mode is designed using two similar MOSFETs with equal grading coefficient m of the MOSFET body junction diode [11]–[14]. In this case, the required shunt capacitance is fixed to satisfy both ZVS and ZDS conditions. The main design study for the class-DE PA is done with the linear parallel capacitance using some assumptions to obtain the circuit components value under the fixed duty ratio 0.25 for same two switches [15]–[17]. These design equations obtained the steady-state response for both switch and output waveforms that are limited with the design specifications such as dc-supply voltage, output power, and load-resistance. However, the adjustments of design parameters and optimization of components value are impossible to obtain desired load resistance with a proper degree of the design freedom [18]–[20]. Although these restrictions can be solved by inserting the linear external parallel capacitance, but this design approach needs to tune with an accurate value of these components using a complicated procedure. In [21] and [22], two types of the class-DE PA configuration with a linear external and nonlinear parasitic capacitance in parallel configuration with two same MOSFETs devices are defined. In this configuration, the required parallel capacitances become considerable as the operating frequency is raised. The parasitic capacitance has a nonlinear function in terms of the grading coefficient m for the MOSFET body

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junction diode. Therefore, several design researches have been studied with same MOSFETs as switching device from an equal grading coefficient m for the MOSFET body junction diode point of view [18]–[23]. This phenomenon becomes a determinative parameter when two MOSFETs are similar by cumulative function for two equal grading coefficients.

The main limitation case for implementing of the classical class-DE PA is subject to restricted load-resistance. The directly effect of the loaded-quality factor to design of the inductor for the series-resonant filter leads to its large value. Consequently, the power dissipation is raised considerably. On the other hand, both the maximum operating frequency and load-resistance related to output power are determined by the required parallel capacitance, which leads to a design forced area for using two MOFETs with a large output capacitance and same grading coefficient m. The charge or discharge time of the dead-time intervals for the class-DE PA is determined by adjusting the required parallel capacitances. This case gives high resistive power-dissipation at high-frequency operation. Although, a one possible solution is the variation of the input signal duty ratio [24]–[26], but same MOSFETs required a high-quality factor that leads to non-sinusoidal output waveform and power dissipations. However, the outstanding advantage of the class-DE PA is the implementation of the parasitic capacitance under ZVS and ZDS conditions. This important specification is considerably disturbed when two MOSFETs are same as increasing the switching operation frequency. The ratio of the voltage across the output inductor to the dc-supply voltage is described in terms of the nonlinear parallel capacitance and grading coefficient m for each MOSET. The discrete MOSFETs products have a fixed grading coefficient m. However, obtaining an efficient class-DE PA operation would need a specific MOSFET with having a required parasitic capacitance and grading coefficient m. The combination of two MOSFETs with a different grading coefficient m as a switching device, prepared a widely design area to tune the required parallel capacitance. Therefore, the theory and design approach for the class-DE PA with a nonlinear parallel capacitance using different MOSFETs effectively governs the PA operation that is unknown yet.

This paper introduced a new operation-mode for the class-DE PA with two non-similar switching devices. The soft-switching performance of the proposed PA with a low value of the inductor for series resonant filter results in lower power dissipation than the conventional one. Moreover, the implementation of the grading coefficient m of two MOSFETs body junction diode as tuning parameter causes the absorption of the parallel capacitance without any change in the circuit topology.

II. Principle Operation of Circuit Configuration

A. Circuit Description

The primary configuration of the class-DE PA with only nonlinear parallel capacitance with switching devices depicted in Fig. 1. To obtain the theoretical operation of the PA, it is assumed that the class-E ZVS and ZDS conditions for switch

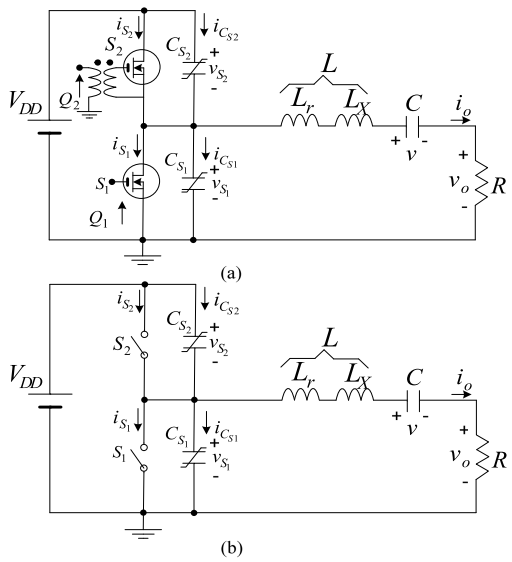

Fig. 1. Class-DE PA arrangement with a nonlinear parallel capacitance. (a) Basic circuit topology. (b) Idealized equivalent circuit.

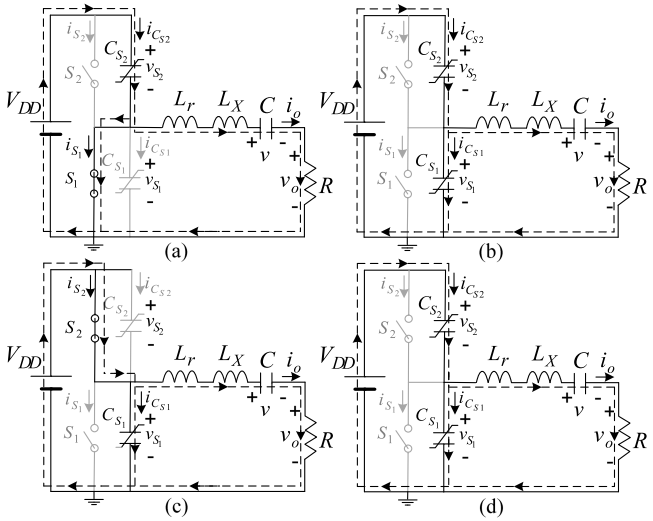

Fig. 2. Class-DE PA operation mode for each interval. (a) $0 \le \theta < \pi/2$. (b) $\pi/2 \le \theta < \pi$. (c) $\pi \le \theta < 3\pi/2$. (d) $3\pi/2 \le \theta < 2\pi$.

S_1 and S_2 at the switching instant are satisfied as

$$v_{s1}(2\pi) = 0, \left.\frac{dv_{s1}(\theta)}{d\theta}\right|_{\theta=2\pi} = 0, \tag{1}$$

$$v_{s2}(\pi) = 0, \left.\frac{dv_{s2}(\theta)}{d\theta}\right|_{\theta=\pi} = 0, \tag{2}$$

where v_{s1} and v_{s2} denote the switch voltage for S_1 and S_2, respectively. Also, the elements of the circuit are dc-supply voltage V_{DD}, a series resonant-filter L-C, and a load-network R. Two non-similar MOSFETs with non-equal grading coefficient m are implemented as the switching elements while only nonlinear parallel parasitic capacitances a C_{s1} and C_{s2}. Note that the duty ratio of the class-DE PA operation is 0.25. All switching and passive components are assumed as zero-parasitic resistances. Therefore, the

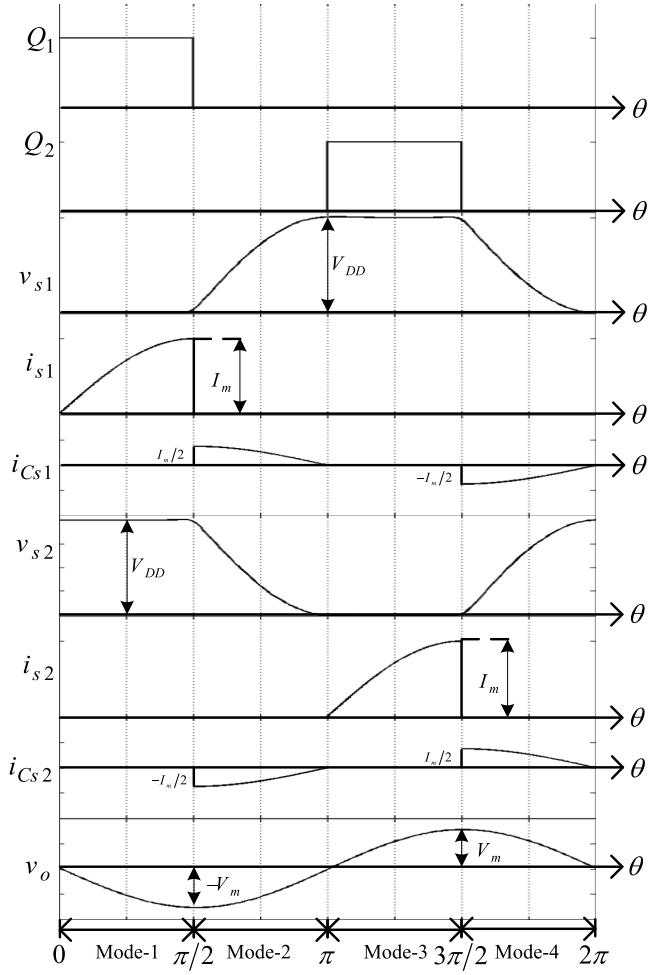

Fig. 3. Operation-mode waveforms of the class-DE PA, Q_1 and Q_2 are the input signals for the control of S_1 and S_2, respectively.

equivalent circuit operation is obtained as depicted in Fig. 1(b). The circuit schematic operation-modes and waveforms of the class-DE PA are depicted in Fig. 2 and 3, respectively.

The class-DE PA operates in four modes, and the equivalent circuit for each operating mode is shown in Fig. 2. The steady-state analysis is performed in the interval $0 \leq \theta < 2\pi$. The general expression between the dc-supply voltage and switching voltage is

$$\frac{v_{s1}(\theta)}{V_{\rm DD}} = 1 - \frac{v_{s2}(\theta)}{V_{\rm DD}}. \tag{3}$$

1) Mode $[0, \pi/2)$: This operation mode is shown in Fig. 2(a). This mode is started from $\theta = 0$ by turning the switch S_1 on and turning the switch S_2 off. The switch voltages in this interval are in fixed values as

$$v_{s1}(\theta) = 0, \text{ and } v_{s2}(\theta) = V_{\rm DD}. \tag{4}$$

Due to the constant value of two switches voltage, the current through the shunt capacitances and S_2 is

$$i_{Cs1}(\theta) = i_{Cs2}(\theta) = i_{S2}(\theta) = 0. \tag{5}$$

Generally, the loaded quality factor for the output resonant filter can be determined as

$$Q = \frac{\omega L}{R}, \tag{6}$$

TABLE I
PARAMETERS OF THE POWER MOSFETS

	m	V_{bi} (V)	C_{j0} (pF)	$r(\Omega)$
2SK2504	0.0682	0.8	217	0.1
IRFZ24N	0.3	0.51	297	0.07
IRF530	0.5	0.8	1151	0. 16

The loaded quality factor in (6) is assumed to be high enough, and the output current is purely sinusoidal that is expressed as

$$i_o(\theta) = I_m \sin(\theta + \varphi) = \frac{V_m}{R} \sin(\theta + \varphi), \tag{7}$$

It can be concluded from (5) and (7) that the switching current in S_1 is given by

$$i_{s1}(\theta) = -I_m \sin(\theta + \varphi). \tag{8}$$

The slope of the switch voltage v_{s1} at dead-time intervals is expressed as

$$\frac{dv_{s1}(\theta)}{d\theta} = -\frac{I_m \sin(\theta + \varphi)}{\omega\,(C_{ds1} + C_{ds2})}. \tag{9}$$

where C_{ds1} and C_{ds2} are expressed as

$$C_{ds1} = \frac{C_{j01}}{\left(1 + \frac{v_{s1}}{V_{bi1}}\right)^{m_1}} = \frac{C_{j01}}{\left(1 + \frac{V_{\rm DD} - v_{s2}}{V_{bi1}}\right)^{m_1}}, \tag{10}$$

and

$$C_{ds2} = \frac{C_{j02}}{\left(1 + \frac{v_{s2}}{V_{bi2}}\right)^{m_2}} = \frac{C_{j02}}{\left(1 + \frac{V_{\rm DD} - v_{s1}}{V_{bi2}}\right)^{m_2}}, \tag{11}$$

respectively. In (10) and (11), V_{bi} is the built-in potential, whose typical value is in the region from 0.5 to 0.9 V for silicon MOSFETs, v_s is the voltage between the drain and source, C_{j0} is the junction capacitance at $v_s = 0$, and m is the grading coefficient of a body junction diode. This analysis is performed with only MOSFET nonlinear drain-source parasitic capacitance as parallel capacitances for two non-similar switches. The output capacitances of three MOSFETs are plotted in Fig. 4 in terms of the switching voltage normalized by the dc-supply voltage. It can be seen from this figure that the value of capacitance depends on the grading coefficient m where the choice of each switch infused this parameter. As it can be realized from (9), the total of C_{ds1} and C_{ds2} individualized the slope of the switch voltage. Three types of power MOSFETs with distinguished different parameters are summarized in Table I [27], [28], to perceive non-similar switching devices in the proposed class-DE PA operation.

The summarized output capacitance with the combination of each type of MOSFET is depicted in Fig. 5. It can be observed that the total required parallel capacitance can be tuned by varying of the grading coefficient m. In the similar two switches case, the total parallel capacitance is decreased as the increment of the grading coefficient. On the other hand, in non-similar case, this value can be adjusted by the combination of each type of MOSFETs without any external circuit tuning. Moreover, the value of this capacitance is considerably increased. This case proved the effectiveness of this approach and the analytical expression relationships.

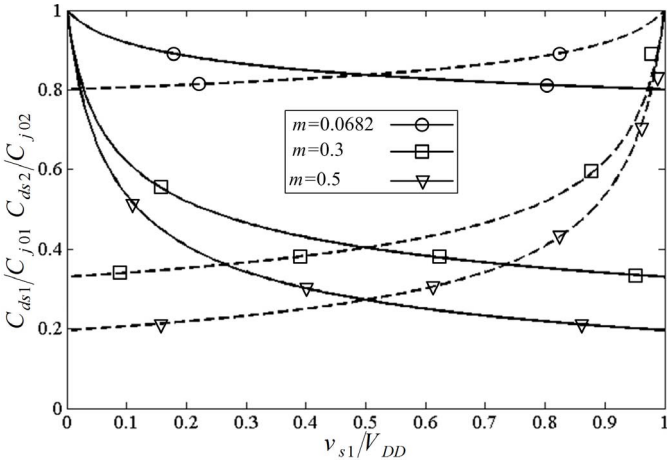

Fig. 4. The normalized drain-source capacitance C_{ds1}/C_{j01} (sold-line) and C_{ds2}/C_{j02} (dash-line) on terms of the normalized switch voltage $\upsilon_{s1}/V_{\rm DD}$ for $V_{\rm DD} = 20$V with $m = 0.0682$, 0.3 and 0.5.

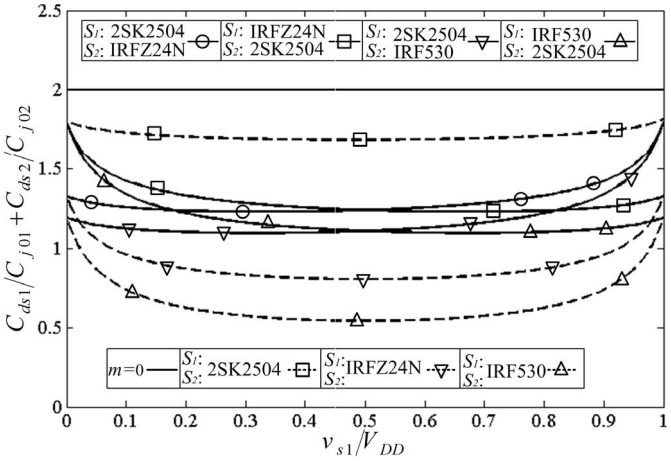

Fig. 5. The total normalized drain-source capacitance $C_{ds1}/C_{j01} + C_{ds2}/C_{j02}$ in terms of the normalized switch voltage $\upsilon_{s1}/V_{\rm DD}$ for $V_{\rm DD} = 20$V for two different switches, similar switches and linear capacitance $m = 0$.

From (4) and the class-E ZDS condition for υ_{S1} in (1), two values for φ is obtained as 0 and π. The amplitude of the output current I_m is consider as positive values, which is given as

$$\varphi = \pi. \tag{12}$$

2) Mode$[\pi/2, \pi)$*:* At this mode, the voltage across the switch S_1 reaches $V_{\rm DD}$ and the switch S_2 becomes zero. Two switches are in the off-state, and currents through switches are determined as

$$i_{s1}(\theta) = i_{s2}(\theta) = 0. \tag{13}$$

From (9), (12) and $\upsilon_{s2}(\theta = \pi/2) = V_{\rm DD}$, the integrally relationship for the current is

$$\omega \int_{V_{\rm DD}}^{\upsilon_{s2}} \left(\frac{C_{j01}}{\left(1+\frac{V_{\rm DD}-\upsilon'_{s2}}{V_{bi1}}\right)^{m_1}} + \frac{C_{j02}}{\left(1+\frac{\upsilon'_{s2}}{V_{bi2}}\right)^{m_2}}\right) d\upsilon'_{s2} = - \int_{\frac{\pi}{2}}^{\theta} I_m \sin(\theta')d\theta'. \tag{14}$$

The solution of (14) is derived as

$$-\frac{V_{bi1}\omega C_{j01}}{1-m_1}\left[\left(1+\frac{V_{\rm DD}-\upsilon_{s2}}{V_{bi1}}\right)^{1-m_1}-1\right] + \frac{V_{bi2}\omega C_{j02}}{1-m_2} \times \left[\left(1+\frac{\upsilon_{s2}}{V_{bi2}}\right)^{1-m_2} - \left(1+\frac{V_{\rm DD}}{V_{bi2}}\right)^{1-m_2}\right] = I_m \cos(\theta) \tag{15}$$

Applying $\upsilon_{s2}(\pi) = 0$ to (15), the amplitude of output current can be calculated as

$$I_m = \frac{V_{bi1}\omega C_{j01}}{1-m_1}\left\{\left[\left(1+\frac{V_{\rm DD}}{V_{bi1}}\right)^{1-m_1}-1\right] - \frac{V_{bi2}}{V_{bi1}}\frac{1-m_1}{1-m_2}\frac{C_{j02}}{C_{j01}}\left[1-\left(1+\frac{V_{\rm DD}}{V_{bi2}}\right)^{1-m_2}\right]\right\}. \tag{16}$$

By substituting (16) into (15), we have

$$\left[\left(1+\frac{\upsilon_{s1}}{V_{\rm DD}}\frac{V_{\rm DD}}{V_{bi1}}\right)^{1-m_1}-1\right] - \frac{V_{bi2}}{V_{bi1}}\frac{1-m_1}{1-m_2} \times \frac{C_{j02}}{C_{j01}} \times \left[\left(1+\frac{V_{\rm DD}}{V_{bi2}}-\frac{\upsilon_{s1}}{V_{\rm DD}}\frac{V_{\rm DD}}{V_{bi2}}\right)^{1-m_2} - \left(1+\frac{V_{\rm DD}}{V_{bi2}}\right)^{1-m_2}\right] + \left\{\left[\left(1+\frac{V_{\rm DD}}{V_{bi1}}\right)^{1-m_1}-1\right] - \frac{V_{bi2}}{V_{bi1}}\frac{1-m_1}{1-m_2} \times \frac{C_{j02}}{C_{j01}} \times \left[1-\left(1+\frac{V_{\rm DD}}{V_{bi2}}\right)^{1-m_2}\right]\right\} \cos(\theta) = 0. \tag{17}$$

3) Mode$[\pi, 3\pi/2)$*:* During this mode, the switch S_2 is in the on-state. The average value of the supply current flowing from the dc-voltage source $V_{\rm DD}$ is the dc-supply current $I_{\rm DD}$ that is analytically obtained from

$$I_D = \frac{1}{2\pi}\int_0^{2\pi}\left\{i_{s2}(\theta') + i_{Cs2}(\theta')\right\}d\theta' = \frac{1}{2\pi}\int_0^{2\pi} i_{s2}(\theta')d\theta' = \frac{1}{2\pi}\int_{\pi}^{3\pi/2} i_{s2}(\theta')d\theta' = \frac{1}{2\pi}\int_{\pi}^{3\pi/2} I_m \sin(\theta')d\theta' = \frac{I_m}{2\pi}. \tag{18}$$

By substituting (15) into (18), the dc-supply current can be written as

$$I_{\rm DD} = \frac{V_{bi1}\omega C_{j01}}{2\pi\,(1-m_1)} \times \left\langle \left(1+\frac{V_{\rm DD}}{V_{bi1}}\right)^{1-m_1} - 1 - \frac{V_{bi2}}{V_{bi1}}\frac{1-m_1}{1-m_2}\frac{C_{j02}}{C_{j01}}\left[1-\left(1+\frac{V_{\rm DD}}{V_{bi2}}\right)^{1-m_2}\right]\right\rangle. \tag{19}$$

4) Mode $[3\pi/2, 2\pi)$*:* This mode begins with the turning S_2 off. By this state, the switch S_1 voltage reached from zero to the dc-supply voltage value. Since the parallel capacitor of the switch S_1 is charged, the accurate tuning of this capacitor is very important for obtaining the maximum operating frequency. The next cycle of class-DE operation is started when the first switch voltage becomes zero.

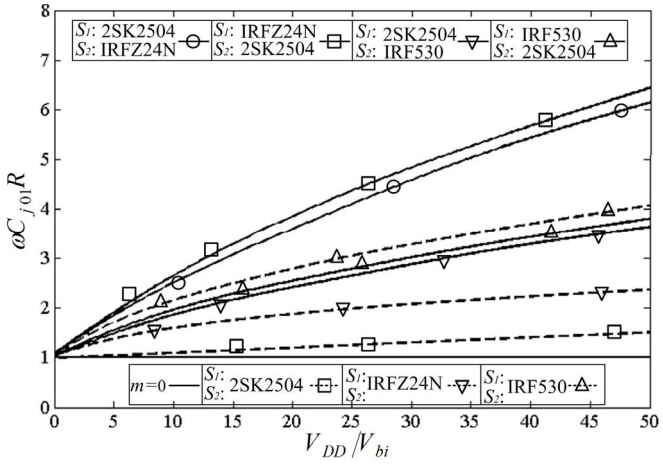

Fig. 6. $\omega C_{j01}R$ in terms of normalized dc-supply voltage $V_{\rm DD}/V_{bi}$.

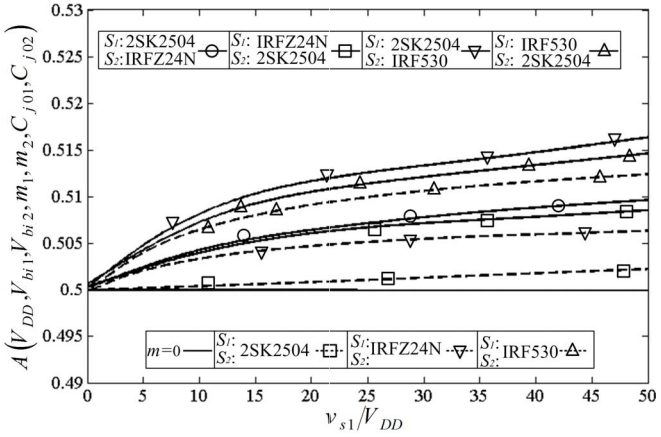

Fig. 7. The normalized across the resonant inductance L with $V_{\rm DD}$ in terms of normalized switch-voltage.

III. Power Conversion Considerations

The output power P_{out} is obtained from (16) as

$$P_{out} = \frac{RI_m^2}{2} = \frac{R}{2}\left(\frac{V_{bi1}\omega C_{j01}}{1-m_1}\right)^2 \times \left\{\left[\left(1+\frac{V_{\rm DD}}{V_{bi1}}\right)^{1-m_1}-1\right] - \frac{V_{bi2}}{V_{bi1}}\frac{1-m_1}{1-m_2}\frac{C_{j02}}{C_{j01}}\left[1-\left(1+\frac{V_{\rm DD}}{V_{bi2}}\right)^{1-m_2}\right]\right\}^2. \quad (20)$$

The dc-supply power P_{in} from (18) and (19) is

$$P_{in} = V_{\rm DD}I_{\rm DD} = \frac{V_{\rm DD}V_{bi1}\omega C_{j01}}{2\pi\,(1-m_1)}\left\{\left[\left(1+\frac{V_{\rm DD}}{V_{bi1}}\right)^{1-m_1}-1\right] - \frac{V_{bi2}}{V_{bi1}}\frac{1-m_1}{1-m_2}\frac{C_{j02}}{C_{j01}}\left[1-\left(1+\frac{V_{\rm DD}}{V_{bi2}}\right)^{1-m_2}\right]\right\}. \quad (21)$$

Based on no parasitic resistance assumption, the power loss in the circuit is zero that it can be performed 100% power conversion efficiency. Therefore, P_{in} input power is equal to P_{out} output power, which is expressed as

$$\omega R C_{j01} = \frac{V_{\rm DD}}{V_{bi1}}\frac{(1-m_1)}{\pi}\times\left\{\left[\left(1+\frac{V_{\rm DD}}{V_{bi1}}\right)^{1-m_1}-1\right] - \frac{V_{bi2}}{V_{bi1}}\frac{1-m_1}{1-m_2}\frac{C_{j02}}{C_{j01}}\times\left[1-\left(1+\frac{V_{\rm DD}}{V_{bi2}}\right)^{1-m_2}\right]\right\}^{-1}. \quad (22)$$

Fig. 6 depicts $\omega C_{j01}R$ in terms of the dc-supply voltage for the combination of difference MOSFETs and the linear parallel capacitance $m = 0$ case. The dc-supply voltage is quite important for power consumption calculation and the switch device selection for the allowable peak switch voltage of the MOSFET point of view. This graph illustrates the value of the load-resistance with non-similar MOSFET is higher than that with similar MOSFET. With regards to the increment of the dc-supply voltage, the value of m is an adjustment variable to control of power dissipations with the desired load-resistance.

The voltage $v_L(\theta)$ across the resonant inductance L is expressed as

$$v_L(\theta) = V_L(-\cos\theta), \quad (23)$$

where V_L is

$$V_L = \omega L I_m. \quad (24)$$

On the other hand, from (12) and (23), the output voltage $v_o(\theta)$ is

$$v_o(\theta) = V_m(-\sin\theta), \quad (25)$$

where V_L is

$$V_m = RI_m. \quad (26)$$

From (24) and (25) we have

$$\frac{V_L}{V_m} = \frac{\omega L}{R}. \quad (27)$$

From the Fourier analysis, the magnitude of V_L normalized with respect to the dc-supply voltage, i.e., $V_{\rm DD}$ is obtained as

$$\frac{V_L}{V_{\rm DD}} = \frac{1}{\pi}\int_0^{2\pi}\frac{v_{s1}}{V_{\rm DD}}(\theta')(-\cos\theta')\,d\theta'. \quad (28)$$

It is seen from (28) that it is obtained in terms of $(1-m_2)/(1-m_1)$, $V_{\rm DD}/V_{bi1}$, $V_{\rm DD}/V_{bi2}$, V_{bi2}/V_{bi1} and C_{j02}/C_{j01}, which is a complex integrally equation. This cannot be solved using the analytically method, which has a numerically solution. Therefore, the analytical expression for $A(V_{\rm DD}, V_{bi1}, V_{bi2}, m_1, m_2, C_{j01}, C_{j02})$ is expressed as

$$A\left(V_{\rm DD}, V_{bi1}, V_{bi2}, m_1, m_2, C_{j01}, C_{j02}\right) = \int_0^{2\pi}\frac{v_{s1}}{V_{\rm DD}}(\theta')(-\cos\theta')\,d\theta' = \frac{\pi V_L}{V_{\rm DD}} \quad (29)$$

Fig. 7 shows the normalized voltage across the series inductor with respect to the dc-supply voltage. It can be seen that this voltage is increased with the combination of difference grading coefficient m of the switch device for both nonlinear parallel capacitance and linear one. The discursive performance proved the wide design range to appear the voltage across the series inductor for reducing of power dissipations that was to be neglected to do factuality in a previously analysis.

From (18) and (19), the relation between the dc-supply voltage and the amplitude of the output voltage is obtained as

$$\frac{V_m}{V_{\rm DD}} = \frac{1}{\pi}. \quad (30)$$

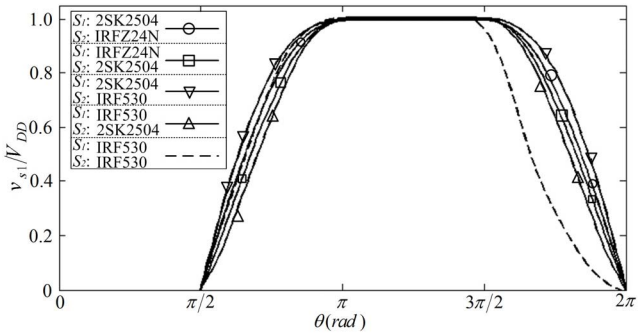

Fig. 8. The normalized switch voltage v_{s1}/V_{DD} for two different MOSFETs with non-equal grading coefficient of a body junction diode.

Therefore, the output power is

$$P_{out} = \frac{V_m I_m}{2} = \frac{V_m^2}{2R} = \frac{V_{\mathrm{DD}}^2}{2\pi^2 R}. \tag{31}$$

By equating two sides of (21) and (30), we have

$$\omega R \frac{V_{\mathrm{DD}} V_{bi1} C_{j01}}{2(1-m_1)} \left\{ \left[\left(1+\frac{V_{\mathrm{DD}}}{V_{bi1}}\right)^{1-m_1} - 1 \right] - \frac{V_{bi2}}{V_{bi1}} \frac{1-m_1}{1-m_2} \frac{C_{j02}}{C_{j01}} \left[1 - \left(1+\frac{V_{\mathrm{DD}}}{V_{bi2}}\right)^{1-m_2} \right] \right\} = \frac{1}{2\pi} \tag{32}$$

From (32), the equivalent linear capacitance of the nonlinear MOSFET drain-source parasitic capacitance is obtained to satisfy the class-E ZVS and ZDS conditions with non-similar MOSFETs, which is expressed as

$$C_{eq} = \frac{V_{\mathrm{DD}} V_{bi1} C_{j01}}{2(1-m_1)} \times \left\{ \left[\left(1+\frac{V_{\mathrm{DD}}}{V_{bi1}}\right)^{1-m_1} - 1 \right] - \frac{V_{bi2}}{V_{bi1}} \frac{1-m_1}{1-m_2} \frac{C_{j02}}{C_{j01}} \left[1 - \left(1+\frac{V_{\mathrm{DD}}}{V_{bi2}}\right)^{1-m_2} \right] \right\} \tag{33}$$

It can be concluded from (33) that the equivalent capacitance is depended on the intrinsically characteristics of each type of MOSFETs. When in the non-similar switches, two switches are soft to actualize ZVS, while in the similar case, this condition is restricted.

As shown in Fig. 8, the switch-voltage waveform with the two different types of MOSFETs is considerably distinguished from the similar two MOSFETs case. It can be concluded that the slope of switch voltage is increased while this difference become more considerable with the increment of the grading coefficient m of two MOSFETs. In similar-switch case, the satisfaction of ZVS condition is deviated due to affect of grading coefficient m. Moreover, non-similar switches provide reduced switch power dissipations and the number of the driving circuit and increasing the stability of PA. These are a major result and reason to perform the analysis in this new topology.

IV. Guideline Relationships For Elements Value

As can be concluded from (22), the maximum operation frequency $f = f_{max}$ is expressed as

$$f_{\max} = \frac{V_{\mathrm{DD}}}{V_{bi1}} \frac{(1-m_1)}{2\pi^2 R C_{j01}} \times \left\{ \left[\left(1+\frac{V_{\mathrm{DD}}}{V_{bi1}}\right)^{1-m_1} - 1 \right] - \frac{V_{bi2}}{V_{bi1}} \frac{1-m_1}{1-m_2} \frac{C_{j02}}{C_{j01}} \left[1 - \left(1+\frac{V_{\mathrm{DD}}}{V_{bi2}}\right)^{1-m_2} \right] \right\}^{-1}. \tag{34}$$

The response of (34) is depicted in Fig. 6. It is shown while the grading coefficient m is equal for two switches the maximum frequency is lower than when are similar. Therefore, this case gives wide design range to operate the class-DE PA with the desired operation frequency as design specification.

The load resistance can be calculated from (31) and (22) as

$$R = \frac{V_{\mathrm{DD}}^2}{2\pi^2 P_{out}} = \frac{V_{\mathrm{DD}}}{V_{bi1}} \frac{(1-m_1)}{2\pi^2 f C_{j01}} \times \left\{ \left[\left(1+\frac{V_{\mathrm{DD}}}{V_{bi1}}\right)^{1-m_1} - 1 \right] - \frac{V_{bi2}}{V_{bi1}} \frac{1-m_1}{1-m_2} \frac{C_{j02}}{C_{j01}} \left[1 - \left(1+\frac{V_{\mathrm{DD}}}{V_{bi2}}\right)^{1-m_2} \right] \right\}^{-1}. \tag{35}$$

The definition of the loaded quality factor Q is used to calculate the total value for the inductor in the series load network as

$$L = \frac{QR}{\omega} = \frac{QR}{2\pi f}. \tag{36}$$

By substituting (30) and (29) into (27), we have

$$L_r = \frac{AR}{2\pi f}. \tag{37}$$

The value of L_x is the subtracted (37) from (36) results that is obtained as

$$L_x = L - L_r = \frac{(Q-A)R}{2\pi f}. \tag{38}$$

As given in Fig. 1, the series load network operates in the resonant mode as

$$f = \frac{1}{2\pi\sqrt{LC}}. \tag{39}$$

Therefore, from (38) and (39), the value of capacitance in the series load network can be written by

$$C = \frac{1}{2\pi f (Q-A) R}. \tag{40}$$

Fig. 9 plots the value of capacitance C_0 in the series load network as a function of the loaded quality factor Q. It is seen from this figure that the required value of C_0 is decreased in two same switches case while higher grading coefficient m are used. On the other hand, the combination of two non-similar MOSFETs with difference m prepared a design range to adjust the value of C_0 for reducing of the out power dissipations. Fig. 10 shows how C_{j0} changes with Q. The variation of C_{j0} with sets of the grading coefficient m in terms of the quality factor Q prepared a design adjustment parameter to be done the tune of class-DE PA for satisfying both Q and m simultaneously. It can be concluded from Figs. 9 and 10 that lowering the grading coefficient m for a given capacitor

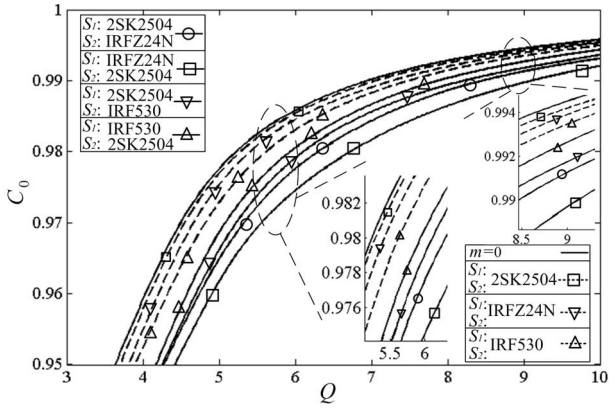

Fig. 9. The ratio of output capacitance C_0 *in* terms of the loaded-quality factor Q.

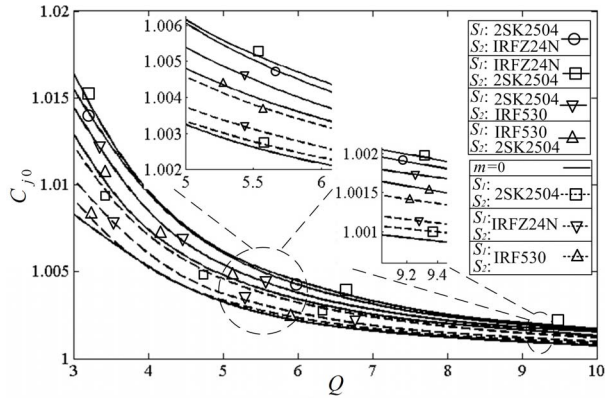

Fig. 10. The ratio of output capacitance C_{j0} in terms of the loaded-quality factor Q.

and minimizes the reduction quality factor and the output capacitance drop, respectively, while maximizing the total ratio of output C_{j0}.

V. Experimental Verification

The justification of theoretical analysis for the proposed class-DE PA with two non-similar MOSFETs as switching elements is designed and implemented with a prototype circuit in operating frequency $f = 4$ MHz, output power $P_o = 11.5$ W, loaded quality factor $Q = 10$, and the dc-supply voltage $V_{\rm DD} = 40$ V. Fig. 11 shows the normalized P_o in terms of $V_{\rm DD}/2\pi^2 f$ for four combinations of non-similar two types of MOSFETs with different grading coefficient m and similar ones that is obtained from (35). It can be seen from these plots that only the combination two grading coefficient as $m = 0.0682$ and 0.5 satisfied the given design parameters such as output power and dc-supply voltage simultaneously. Therefore, IRF530 and 2SK2504 are selected as the switch S_1 and S_2, respectively. From Table I the built-in potential for two MOSFETs is specified as $V_{bi} = 0.8$. Consequently, we had $V_{\rm DD}/V_{bi1} = 50$. From (22), we obtained $\omega C_{j01} R = 3.796$. Hence, the load resistance is 1.76 Ω.

Following the design equations in Section IV, the passive components are obtained as introduced in Table II.

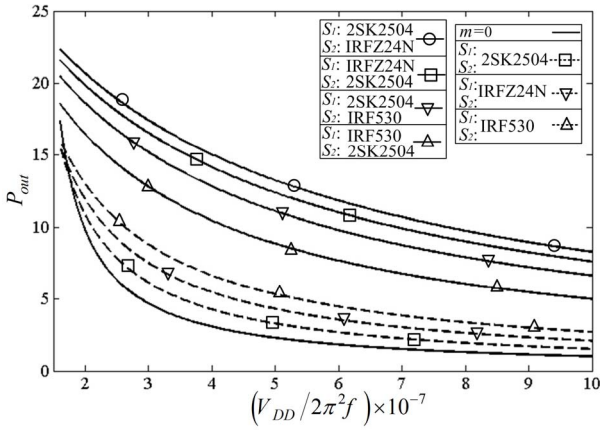

Fig. 11. P_o in terms of $V_{\rm DD}/2\pi^2 f$ for four combinations of MOSFETs and linear parallel capacitance $m = 0$.

TABLE II
Component List And Performance Description For The Circuit Design Example: Theoretical, Pspice, And Measurements

	Theoretical	*Simulated*	*Measured*	*Difference*
R (Ω)	1.76	1.76	1.1	0.37 %
D	0.5	0.5	0.5	0.00 %
V_{DD} (V)	40	40	40	0.00 %
f (MHz)	4.0	4.0	4.0	0.00 %
V_{SM} (V)	40	40	39.8	-0.5 %
I_{DD} (A)	0.287	0.28	0.278	-0.71 %
L_0 (μH)	3.22	3.12	2.95	0.05 %
C_0 (pF)	206	203	194	0.04 %
r_s (Ω)	0.1	0.1	–	–
r_{LC} (Ω)	0.13	0.11	–	–
P_{rLC} (W)	0.1	0.1	–	–
P_o (W)	11.5	11.8	12.1	-0.02 %
THD	0.00 %	4.22 %	4.5 %	–
η	97.8 %	96.2 %	95.1 %	-0.01 %

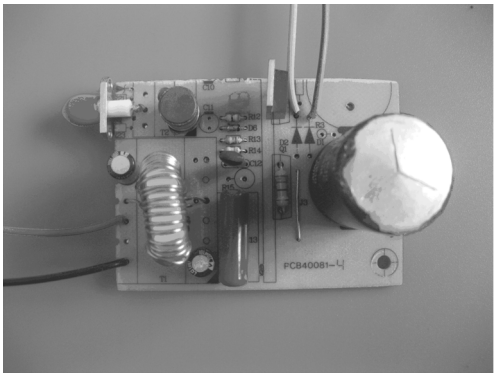

Fig. 12. The photograph of the fabricated proposed class-DE PA with two MOSFETs as IRF530 and 2SK2504.

Fig. 12 shows the photograph of the fabricated class-DE PA. The voltage and current of the implemented class-DE PA are measured by a 34401A Digital Multimeter, which is used for the power losses measurements in all passive components. Figure 13 presents the waveforms obtained from theoretical

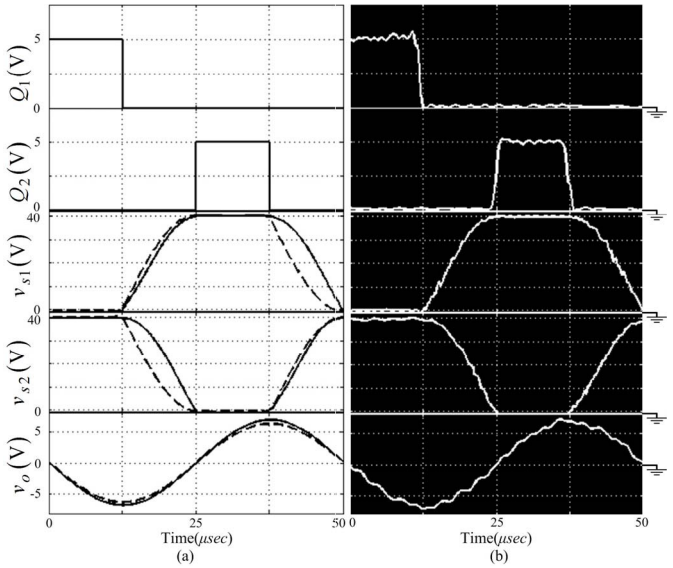

Fig. 13. Input, switching and output waveforms of the implemented class-DE PA. (a) Theoretical (dash-line), Simulation (solid-line). (b) Experimental.

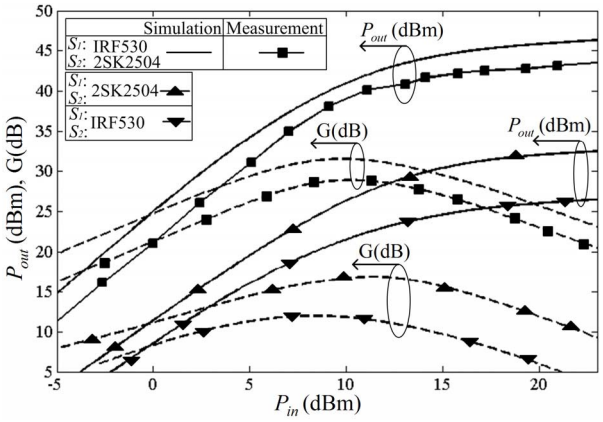

Fig. 14. The simulated and measured results of output power (dBm) and gain (dB) in terms of input power (dBm) for the implemented class-DE PA, and simulation results for two conventional class-DE PAs with two similar switch devices.

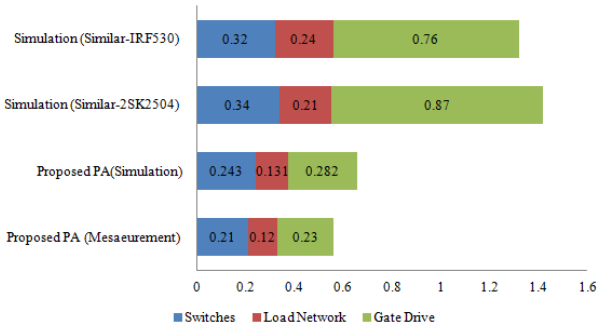

Fig. 15. Power-loss breakdown at output power 12.1 W and dc-supply voltage 40 V.

expressions, PSpice simulations, and circuit experiments for the circuit design example, which indicate the validity of the analytical expressions. The input square waveform is generated by a function generator Stanford Research DS345 with the amplitude of 5 V and 0 V offsets at operating frequency as 4 MHz. The power gain is calculated by

$$G = 10\log_{10}\left(\frac{P_o}{P_{in}}\right), \tag{41}$$

where P_{in} and P_{out} are the input and output power, respectively. Also, the total harmonic distortion (THD) is

$$\mathrm{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} \mathrm{V}_{on}^2}}{\mathrm{V}_{o1}}, \tag{42}$$

where V_{on} is a root-mean-square value of the n^{th} harmonic in the output voltage v_o. Table II gives the measurement summarized results along with the PSpice-simulation and the theoretical predictions for the circuit design example. The steady-state switch voltage across S_1 and S_2 equals to near 40 V that matches with above the initiated design parameters. As it can be observed, two switch devices satisfied ZVS and ZDS conditions simultaneously. The obtained measured output power is 12.1 W while the efficiency of the implemented prototype under different switches is 95.1 %. The vital case in the power dissipation in each switch element occurred due to the overlap between the current through the parallel capacitance and the switch-voltage as predicated in Fig. 3. The non-similar switch makes the switch-voltage up and reduced the power dissipations as observed in Fig. 13. The utilization of peak switch-voltage is used to reduce the conduction loss in the required output power.

Fig. 14 shows the measured output power (dBm) and gain (dB) in terms of the input power (dBm) for the implemented class-DE PA along with simulated output power and gain results for two similar switches device. The proposed class-DE PA with 10 dBm input power exploits 30 dB gain and 12.1 W output power, whereas the conventional class-DE PA with two similar switch devices as IRF530 and 2SK2504 provide 14 dB and 11 dB gain, respectively. Fig. 15 shows the power-loss breakdown simulated and measured results for the proposed class-DE PA along with simulations of the conventional class-DE PA with similar two MOSFETs. It is seen that the largest power loss is occurred in the gate drive, which is decreased by applying two non-similar MOSFETs. Furthermore, the power loss in two switches is 34% lower than that with similar switches such as IRF530. The closely match between the analytically steady-state operation in section III and practically implementation can be observed. In addition, the proposed class-DE PA is considerably suitable for a wide-range of load-network implementations because they can operate in combinations of each non-similar switch with different grading coefficient mode.

VI. Conclusion

The non-similar switch devices in the class-DE PA configuration introduce a novel operation-mode. This mode makes an independent design area for load-network elements from the loaded-quality factor. It is found that the total parallel nonlinear capacitance variation can be retaliated by enforcing

the grading coefficient of a MOSFET body junction diode from the conventional approach. Besides, with the theoretical of the operation mode of the proposed class-DE PA, it is observed that two switches can achieve ZVS and ZVD at a specified load range using adequate the energy stored in the series inductor. Most importantly, the operation-mode of class-DE PA can reach the desired output power along with dc-supply voltage and operating frequency simultaneously without any auxiliary circuit. The verification of analysis and the effectiveness of the proposed class-DE PA is proved with laboratory results of fabricated 12.1W prototype circuit.

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