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A Multilevel Inverter with Minimized Components Featuring Self-balancing and Boosting Capabilities for PV Applications

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***Abstract*—Cascaded H-bridge Multilevel Inverter (CMI) attracts much attention as a versatile converter in photovoltaic (PV) applications. Requiring several isolated dc sources and many switches are the main demerits of the CMI. In PV applications with the CMI, PV modules can be used as the isolated dc sources, which, however, may contribute to inter-module and grid leakage currents due to the module stray capacitors. In this context, a switched-capacitor-based cascaded half-bridge multilevel inverter is proposed in this paper to address the above issues. The proposed topology only requires one dc source, and it achieves the minimum number of switches, spontaneous capacitor charging, voltage boosting, and continuous input current. The inter-module leakage currents can also be eliminated in the proposed topology. The feasibility and effectiveness of the proposed topology are validated through simulations and experimental tests.**

***Index Terms*—Switched capacitor module, Component-count reduction, Multilevel inverter, Photovoltaic applications, Leakage currents.**

I. INTRODUCTION

The integration of distributed generation systems into the modern power grid along with the fast advancement of power electronic devices necessitates employing versatile and expedient converters. Multilevel inverters (MIs) are of importance in modern power systems that can fulfil many requirements. These inverters employ components of low power rating, produce staircase voltages of high quality, and mitigate the electromagnetic interference (EMI) to a large extent [1], [2]. Nevertheless, using extra components makes them bulky, expensive, and complicated with low reliability. As a result, many efforts have been devoted into reducing the component count, while improving the performances [3], [4].

Among the multilevel topologies, the CMI stands out due to its modular structure, possibility of using low voltage rating devices, and flexibility to develop high magnitude voltages. The main drawback of these types of inverters is that many isolated dc sources are required, increasing the system complexity and cost. Thus, several topologies are suggested to reduce the switches and dc sources of the CMI. In terms of the dc-source reduction, the prior-art topologies can be classified into three categories: i) low-frequency transformer-based CMIs (LFT-CMIs) [5]-[7], ii) high-frequency transformer-based CMIs (HFT-CMIs) [8]-[10], and iii) switched-capacitor-based CMIs (SC-CMIs) [11]-[15]. Instead of using separated dc-sources, the LFT-CMIs adopt several low-frequency transformers at the load side. Due to the transformers, these MIs are bulky and expensive; hence, they are justified in the application where the galvanic isolation is required. In the HFT-CMIs, the size of the transformer is deservedly reduced. The high-frequency link and/or transformer in this inverter are used to develop several isolated dc sources. The main advantage of the HFT-CMIs is also the ability to provide a galvanic isolation. On the contrary, the high-frequency link increases the power losses. Compared to transformers, capacitors are cheap and compact, and thus, the SC-CMIs are more compact in size and lower in cost. Nevertheless, the lack of the galvanic isolation and the inrush current of the capacitors are the main shortcomings of the SC-CMIs. The inrush current can increase the failure rate of the capacitors and decrease the reliability of the SC-CMIs. In the topologies in [16] and [17], the inrush current of the capacitors is mitigated through a charging inductor. In this case, the dc source is not used to directly supply the load current. Alternatively, the dc-source charges the capacitors through the charging inductor and then the capacitors provide the load current.

In the CMI with PV applications, the dc-sources are replaced with PV modules; however, this is not an easy task, as the inter-module leakage currents may appear [18]. As shown in Fig. 1, the leakage currents (I_{CM}) in the CMI for PV applications may be generated due to the common-mode voltage and differential-mode voltage variations across the stray capacitor of the PV modules (e.g., C_{pv1}, C_{pv2}, C_{pv3}). The voltage across the stray capacitors and the associated leakage currents for a three-cell CMI are, respectively, obtained by.

$$\begin{cases} V_{DM_i} = S_i V_{pvk} \\ S_i \in \{0,1\} \\ i = 1,2,3,4,5,6 \\ k = 1,2,3 \end{cases} \tag{1}$$

$$I_{CM_k} = C_{pv_k} \frac{dV_{Cpv_k}}{dt} \tag{2}$$

where V_{DMi}, S_i, V_{pvk}, C_{pvk}, I_{CMk} and V_{Cpvk} are differential mode voltage, switching state of the ith switch, voltage of the kth PV cell, stray capacitor of the kth PV cell, leakage current through the kth stray capacitor, and voltage across the kth stray capacitor, respectively.

The inter-module leakage currents bring power losses, and increase output harmonics, leading to safety and electromagnetic interference (EMI) issues.

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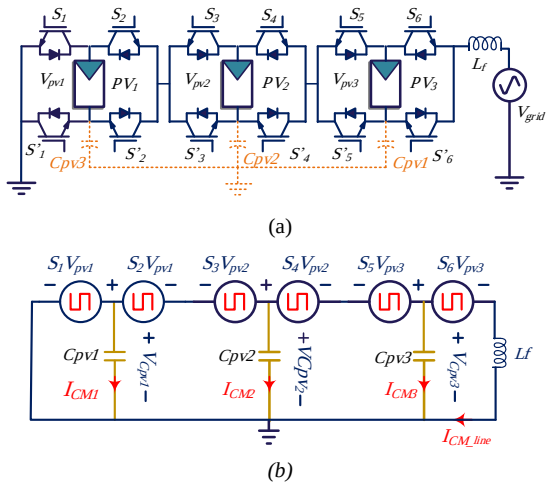

Fig.1. A CMI for PV applications: (a) three-cell CMI and (b) equivalent circuits illustrating the leakage currents and voltage across the stray capacitors.

Attempts have thus been made to tackle the inter-module leakage currents for PV applications with the CMIs. The suggested solutions are primarily based on topology reconfigurations, passive filters, and modulation modifications. The H5 and H6 inverters are two well-known topologies that suppress the leakage currents in grid-tied PV applications [19], [20]. Accordingly, in order to eliminate the inter-module leakage currents in the CMI, the H-bridge cells were replaced with H5 and H6 cells in [21] and [22], respectively. Additionally, dc-side and ac-side filters were designed to limit the leakage currents in [18]. The designed filters can also reduce the EMI due to the inter-module leakage currents. In another attempt, a modified phase disposition pulse width modulation (MPDPWM) is introduced for symmetrical CMIs to eliminate leakage currents [23]. One effective solution to suppress the inter-module leakage current is to use the single-source CMIs [24]. In PV systems with single-source CMIs, the PV modules are connected to a common dc link. This can lower the overall system cost and complexity. Nevertheless, the leakage current issue in grid-tied single-source MIs should be addressed further.

In light of the above, a new single-source SC-MI is proposed in this paper. The proposed topology features a high boosting capability. In order to mitigate the inrush current of the capacitors, an inductor is added in the charging current path of the capacitors, as discussed in Section II. Compared to the conventional CMI, the proposed topology requires half the number of switches, but it uses certain extra diodes to charge the capacitors. It is worth mentioning that the capacitors in this topology are spontaneously charged without any active component. Furthermore, the proposed topology draws a smooth and continuous current from the dc source, but it provides a unidirectional power flow. The proposed topology is analyzed in detail in Section III in terms of voltage stresses and power losses. Considering the mentioned features, the proposed topology can be a promising solution for PV applications, where the continuous input current can facilitate the maximum power point tracking and prolong the life span of the storage unit. Moreover, using only one dc-source can eradicate the inter-module leakage currents and simplify the control approach. The application of the proposed topology in PV systems is then discussed in Section IV. The performance of the proposed CMI has been validated through simulations and experimental tests in Sections V and VI. Finally, concluding remarks are provided in Section VII.

II. Configuration and Operation of the Proposed Topology

The proposed topology is synthesized with several cascaded switched-capacitor-based half-bridge cells and three auxiliary switches. The capacitors in the half-bridge cells are spontaneously charged through diodes termed as charging diodes and a charging inductor. Fig. 2(a) shows the building block of the proposed topology (half-bridge cell) and Fig. 2(b) presents the auxiliary switch configuration. The general configuration of the proposed topology is depicted in Fig. 2(c). For clarity, the dc-source, the charging inductor and the charging diodes are highlighted in red, while the half-bridges and auxiliary switches are in black in Fig. 2(c).

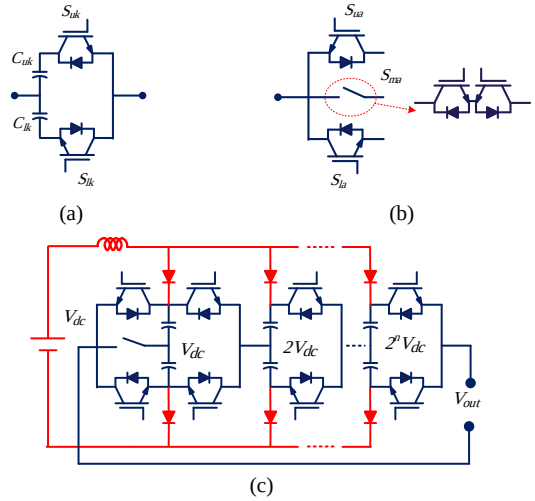

Fig. 2. Proposed multilevel inverter topology: (a) basic module, (b) auxiliary switch configuration, and (c) general configuration

A. Building Block of the Proposed Topology

As it is seen in Fig. 2(a), the half-bridge cells can only develop positive and negative voltage values. In order to produce all the voltage levels, at least one of the cells should be able to develop zero voltages. To do so, the auxiliary switches (Fig. 2(b)) are connected to the first cell and enable it to develop five voltage levels (including zero voltages).

B. Charging Circuit

As depicted in Fig. 2(c), the charging circuit of the proposed topology consists of a charging inductor (L_{ch}) and several charging diodes (two diodes in each cell). The charging inductor is used to limit the inrush current of the capacitors. Additionaly, it acts as a fault current limiter under faulty conditions. Furthermore, in PV applications, this inductor can be used as the input inductor of the boost converter (this will be discussed in Section IV).

C. Operation Principle

The operation principle of the proposed topology is examplified on a three-cell configuration, as shown in Fig. 3.

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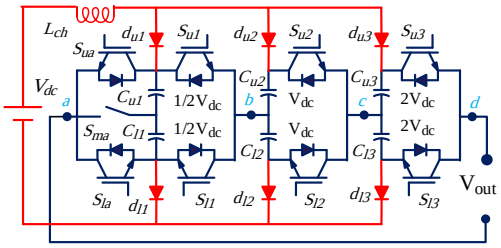
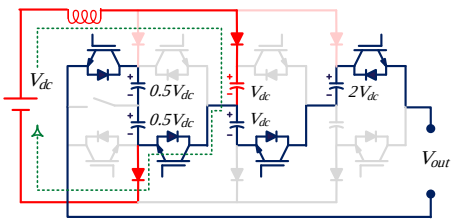


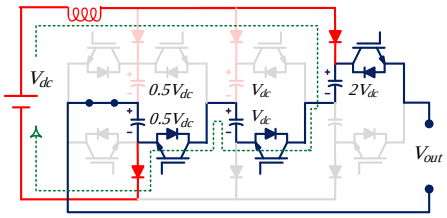
Fig. 3. Seventeen-level (three-cell) configuration of the proposed topology

Since the two capacitors in the first cell (C_{u1} and C_{l1}) are connected in series with the dc source, each of them is charged to half the input dc voltage ($0.5V_{dc}$). The charging path goes through the dc source, L_{ch}, d_{u1}, C_{u1}, C_{l1} and d_{l1}, as indicated by the dash line in Fig. 4(c). As it is seen in Fig. 3, the first cell, which includes the ancillary switches, can develop $0.5V_{dc}$, V_{dc}, 0 , $-V_{dc}$, and $-0.5V_{dc}$ across the points *a* and *b*. The two capacitors in the second cell (C_{u2}, C_{l2}) are both charged to V_{dc}, and thus, this cell will only develop V_{dc} and $-V_{dc}$ across the points *b* and *c*. The capacitors in the third cell are charged to $2V_{dc}$, and hence, this cell can develop $2V_{dc}$ and $-2V_{dc}$ across the points *c* and *d*. Figs. 4(a) to (i) further show the switching patterns to achieve the voltage levels from zero to eight. According to the charging current flowing through the dc source, L_{ch}, d_{u1}, S_{u1}, $C_{l2,}$ and d_{l2}, in Figs. 4(c), (d), (g), (h), and (i), it is understood that, while developing certain voltage levels, C_{l2} is spontaneously charged to V_{dc}. The charging path is shown by the dash line in Fig. 4(h). As it is seen in Figs. 4(a), (b), (e) and (f), C_{u2} is charged when developing the voltage levels in which S_{l1} is turned on (when S_{l1} is turned on, the charging current goes though the dc source, L_{ch}, d_{u2}, C_{u2}, S_{l1}, and d_{l1}, as highlighted by the dash line in Fig. 4(a)). Moreover, C_{u3} and C_{l3} in the third cell will be charged to $2V_{dc}$. As demonstrated in Figs. 4(g), (h) and (i), the charging path for C_{l3} goes though the dc source, L_{ch}, d_{u1}, S_{u1}, C_{u2}, S_{u2}, C_{l3}, and d_{l3} (the dash line in Fig. 4(g)). Similarly, for C_{u3}, the charging current flows though the dc source, L_{ch}, d_{u3}, C_{u3}, S_{l2}, C_{l2}, S_{l1} and d_{l1}, which is depicted by the dash line in Fig. 4(b). Notably, in Fig. 4, the output current and the possible charging paths are colored in black and red, respectively.

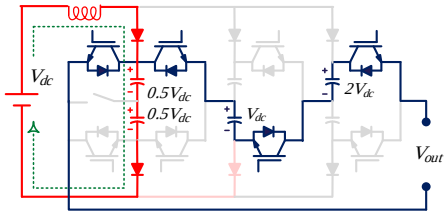
It is worth mentioning that, only positive voltage levels are exhibited in Fig. 4. The negative voltage, however, can be conjured up by referring to Table I, which shows the switching-states for a seventeen-level configuration with three cells. Moreover, in Table I, "on" and "off" states of the switches and diodes are demonstrated by "1" and "0", respectively. In addition, "C", "D", "F" and "N", indicate the charging, discharging, floating, and non-defined states of the capacitors, correspondingly.



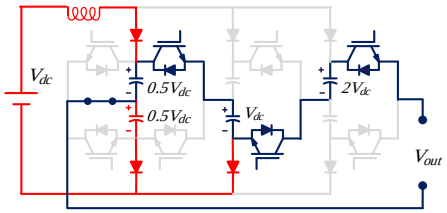
(a)



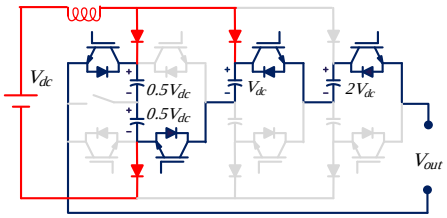
(b)



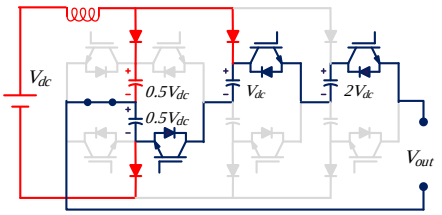
(c)



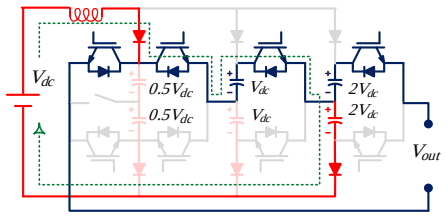
(d)



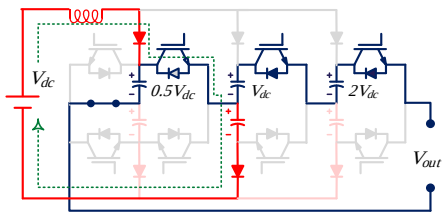
(e)



(f)



(g)



(h)

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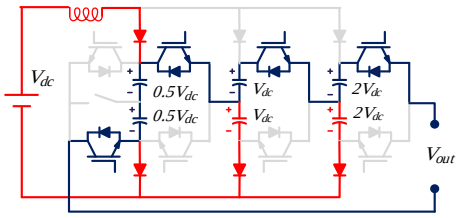

(i)

Fig. 4. Operation modes: (a) to (i) switching patterns to achieve zero to eight voltage levels.

TABLE I.
OPERATION STATES FOR THE INVERTER IN FIG. 3.

Level	Switches states	Charging Diodes	Capacitors states	V_{out}
	$S_{ua},S_{ma},S_{la},S_{u1},$ $S_{u2},S_{u3},S_{l1},S_{l2},S_{l3}$	$d_{u1},d_{u2},d_{u3},$ d_{l1},d_{l2},d_{l3}	$C_{u1},C_{u2},C_{u3},$ C_{l1},C_{l2},C_{l3}	
8	001,111000	100111	C,D,D,C,C,C	$4V_{dc}$
7	010,101010	100111	C,D,D,C,C,C	$7/2V_{dc}$
6	001,011100 100,111000	110100 100111	C,C,D,C,F,F C,D,D,C,C,C	$3V_{dc}$
5	010,011010	110100	C,C,D,C,F,F	$5/2V_{dc}$
4	001,100110 100,011010	100110 110100	C,F,D,C,N,F C,C,D,C,F,F	$2V_{dc}$
3	010,100110	100110	C,F,D,C,C,F	$3/2V_{dc}$
2	001,010110 100,100110	111100 100110	C,C,C,C,N,F C,C,C,N,C,F	V_{dc}
1	010,010110	111100	C,C,C,N,C,F	$1/2V_{dc}$
0	100,010110 001,101001	111100 111100	C,C,C,N,C,F C,C,C,N,C,F	0
-1	010,101001	100111	N,C,F,C,C,C	$-1/2V_{dc}$
-2	001,011001 100,101001	110100 110100	N,C,F,C,C,C C,N,F,C,F,D	$-V_{dc}$
-3	010,011001	110100	C,C,F,C,F,D	$-3/2V_{dc}$
-4	001,100101 100,011001	100110 110100	C,F,F,C,C,D C,C,F,C,F,D	$-2V_{dc}$
-5	010,100101	100110	C,F,F,C,C,D	$-5/2V_{dc}$
-6	001,000111 100,100011	111100 100110	C,C,C,C,D,D C,F,F,C,N,D	$-3V_{dc}$
-7	010,010101	111100	C,C,C,C,D,D	$-7/2V_{dc}$
-8	100,000111	111100	C,C,C,C,D,D	$-4V_{dc}$

III. VOLTAGE STRESS AND POWER LOSS ANALYSIS

A. Voltage Stress of the Components

As described previously, each cell in the proposed topology obtains different voltage values. Eqs. (3) and (4) show the voltage across the capacitors in the n^{th} cell (v_{nm}), and the maximum value of the output voltage (v_{om}) of an m-cell configuration, respectively.

$$v_{nm} = 2^{n-2} v_{dc} \tag{3}$$

$$v_{om} = v_{dc} \sum_{k=1}^{m} 2^{(k-2)} \tag{4}$$

It is seen that each switch in the n^{th} cell experiences the overall voltage across its capacitors. The voltage stress of the charging diodes connected to the first cell is insignificant, and the voltage stress of the diodes in the n^{th} cell is obtained by

$$v_{dss} = 2^{n-3} v_{dc} \tag{5}$$

where v_{dss} is the voltage stress of the diodes.

B. Voltage and Current Ripples

In the proposed topology, the capacitors in the cells have various discharging time. Hence, the capacitors experience different voltage ripples. The voltage ripple of the capacitors in the n^{th} cell can be generalized as

$$\Delta v_{C_n}(\%) = \frac{100}{2^{n-2} C_n V_{dc}} \int_{T_{dn}} i_l(t)\, dt \tag{6}$$

where C_n, T_{dn}, $i_l(t)$ are the capacitance of the capacitors in the n^{th} cell, discharging duration of the capacitors in the n^{th} cell, and the instantaneous load current, respectively.

The input current variation, which is non-linear and depends on the voltage variation of the capacitors, can be estimated by

$$\Delta I_{dc} \approx \frac{\Delta v_{c\max}}{L_{ch}} T_{ch} \tag{7}$$

where Δv_{cmax} and T_{ch} are the maximum voltage variation of the capacitors and charging duration of the capacitors, respectively.

C. Switching Frequency

Referring to Table I, it is seen that in the proposed topology the switches in the last cell operate at the line frequency (f_l), while the switches in the first cell operate at the switching frequency. For an m-cell configuration, the switching frequency of the switches (f_m) in the n^{th} cell is given as

$$f_m = 2^{n-m} f_l \tag{8}$$

D. Power Loss Analysis

Each module of the proposed topology is considered as a half-bridge cell. The power loss of a half-bridge is given by

$$\Delta P_{cell} = v_c f_{sw} (Q_{rr} + Q_{tc}) + v_e |i| + r_e i^2 \tag{9}$$

$$\text{with } \begin{cases} v_e = v_d - f_{sw} (Q_{rr} + Q_{tc}) r_{on} + v_c t_{rr} f_{sw} \\ r_e = (1 - t_{rr} f_{sw}) r_{on} \end{cases}$$

where v_c, f_{sw}, Q_{rr}, Q_{tc}, i, v_d, t_{rr}, and r_{on}, are the voltage across the switches, switching frequency, reverse recovery charge of the switch, reverse recovery charge of the anti-parallel diode, the current passing through the switches, on-state voltage, reverse recovery interval and on-state resistance, accordingly.

The total power loss of the main part (cascaded half-bridge cells) for an n-cell configuration is obtained as

$$\Delta P_{cell}^{t} = \sum_{j=1}^{n} \Delta P_{cell_j} \tag{10}$$

The power loss of a diode is given as

$$\Delta P_d = f_{sw} \left(\int_{T_{ch}} \left(v_{sd}\, i_{ch}(t) + R_{d_n}\, i_{ch}(t)^2 \right) dt + E_{doff} \right) \tag{11}$$

in which T_{ch}, v_{sd}, $i_{ch}(t)$, R_{d_n}, and E_{doff} are the charging period, on-state reverse voltage of the diode, instantaneous current, on-state resistance of the diode, and the wasted energy due to the reverse recovery stage of the diode.

Since, two diodes reside in the charging path at any instant; the power loss from the charging diodes is given as

$$\Delta P_{ch_d} = 2\Delta P_d \tag{12}$$

Power losses of the charging inductor are obtained as

$$\Delta P_{L_{ch}} = R_l i_{dc}^2 \tag{13}$$

with R_l being the resistance of the inductor.

Finally, the total power loss of a single-phase configuration is illustrated by

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$$P_{loss} = \Delta P_{cell}^{t} + \Delta P_{ch_d} + \Delta P_{L_{ch}} \quad (14)$$

Using the characteristics of the commercially available components listed in Table II and assuming an output voltage with the peak value of 320 V and frequency of 50 Hz, the efficiency of a 9-level (2-cell), 17-level (3-cell) and 33-level (4-cell) configurations of the proposed topology are assessed. The results are shown in Fig. 5. As it is evident, due to lower conduction losses, the 9-level configuration offers the highest efficiency (96.3%) among the considered configurations.

TABLE II. COMPONENT CHARACTERISTICS.

Module #	Main Switches	Charging diode
1	TK3R1P04PL	200CNQ040
2	HUF75545P3	VS-249NQ150PbF
3	STP30NF20	VS-249NQ150PbF
4	IXFT50N50P3	STTH20003TV

Parasitic resistances of the capacitors, the charging inductor, and switching frequency are considered 5mΩ, 3 mΩ, and 8 kHz respectively.

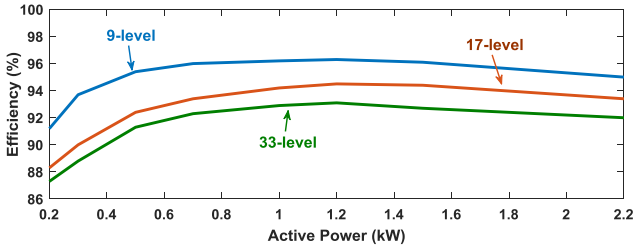

Fig. 5. Efficiency of the proposed topology

E. Cost Analysis

The reduction in components will certainly lead to reduction in size and cost in any converter. Hence, by assuming a 17-level structure (with the input voltage being 50 V, peak output voltage being 320 V and output power being 5 kW), the cost of the proposed topology is briefly compared with that of the conventional HFL-CMI. In this comparison, only the main components are considered. These components and their prices, which are extracted from Mouser and RS On-line stores, are shown in Table III. According to Table III, the proposed topology can reduce the total cost by around 25.38%.

TABLE III. COST OF THE MAIN COMPONENTS

Components	Type	Price ($)	# of component			
Semiconductor switches	IXTH30N50L	9.32	-	HFT-CMI	2	Proposed topology
	IXTR48P20P	8.21	4		2	
	IXFP130N10T2	4.18	4		6	
	IRFP044NPBF	1.62	4		-	
	IXTP80N10T	2.57	4		-	
Gate driver	HCPL-316J	8.71	16		9	
Gate power supply	TMH515s	7.29	16		9	
Capacitors	200 V 3300 µF	13.2	1		2	
	100 V 3300 µF	4.47	1		2	
	50 V 3300 µF	3.02	1		2	
H-bridge diodes	KBPC3502T	3.31	1		-	
	KBPC3501T	3.31	2		-	
Single diode	VS-30.PF0.PBF	3.98	-		2	
	DSA70C200HB	3.27	-		2	
	MBR30H100CT	1.12	-		2	
DSP	TMS320F28335	24.49	1		1	
HF link	HF transformer	6.3	1		-	
The total price of the HFT-CMI= $384.23		The total price of the proposed inverter = $ 286.69				

IV. PROPOSED TOPOLOGY IN PV APPLICATIONS

The converters in PV applications are required to fulfill certain specific requirements. Since the generated power of the PV modules is uncertain and environmental-dependent, the converter should offer a maximum efficiency for a wide power range through a Maximum Power Point Tracking (MPPT) control. The other important issue in PV systems is the leakage current. In order to simplify the MPPT in the proposed topology, an extra switch (S_b) is added, as shown in Fig. 6(a). Under this condition, the cell capacitors in the first cell are used as the capacitor bank, where the boost converters push their switched current into. The charging inductor in this configuration takes three roles: i) filtering the input current harmonics, ii) preventing the inrush current of the capacitor, and iii) facilitating the MPPT process. Furthermore, regarding the use of only one dc-link, the proposed topology can be used as a central inverter, as shown in Fig. 6(b). In such an application, several PV modules can be separately connected to the dc-link through individual dc-dc converters to facilitate the MPPT under partial shading conditions.

The common strategy to track the maximum power in PV systems is to use a dc-dc boost converter. This converter is also used to boost the output voltage of the PV modules. Although it is possible to approach to any arbitrary voltage level through the dc-dc boost converter in theory, the power loss increases in line with the increase of the duty cycle (d) and imposes a limitation on the boosting capability. To tackle the issue, high-step up dc-dc converters are suggested. Considering that the voltage is boosted through the switched-capacitor cells in the proposed topology, the dc-dc stage does not shoulder the boosting burden. The dc-dc section in this topology is essentially used to facilitate the MPPT process. The boost ratio of the voltage in the proposed topology is expressed as

$$v_{out} = \frac{v_{pv}}{1-d} \sum_{k=1}^{n} 2^{k-2} \quad (15)$$

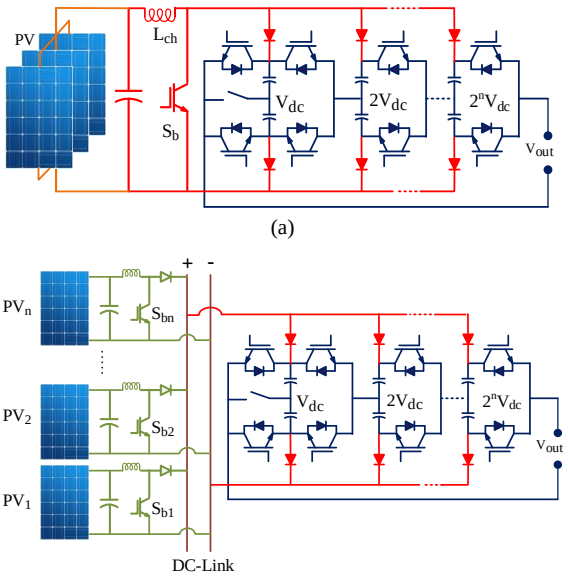

Fig. 6. Proposed topology in PV application: (a) single-converter structure and (b) multi-converter structure.

It is worth mentioning that the proposed topology can only eliminate the inter-module leakage currents. The line

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leakage current, resulting from the common mode voltage (CMV) variation remains. Consequently, this topology is specifically suitable for stand-alone transformerless PV applications. In other words, the proposed topology with grid-tied PV applications necessitates an isolation transformer to block the line leakage current.

Under faulty conditions, the charging inductor delays the fault current and provides enough time for the protection system to operate. The rise time of the fault current is given as

$$t_{rise} = \frac{L_{ch} I_{in}}{v_{dc}} \tag{16}$$

where t_{rise} and I_{in} is the rise time of the fault current and the input current, respectively. Fig. 7 shows the proposed topology which is equipped with a protection system.

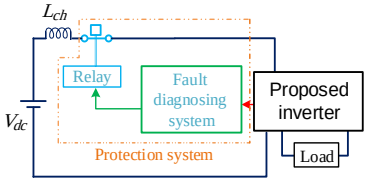


Fig. 7. Proposed topology equipped with a protection system

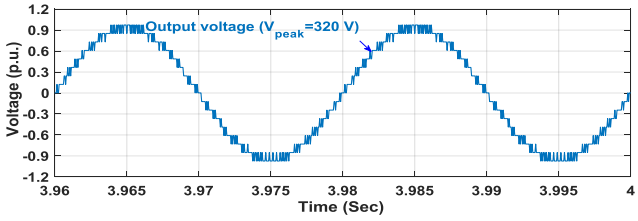
V. Simulation Results

The 17-level configuration shown in Fig. 3 is simulated in Matlab/Simulink. The characteristics of the simulation model are listed in Table IV. Notably, the output voltage and currents are described in per-unit values. The base values for the voltage and current are 320 V and 20 A, respectively.

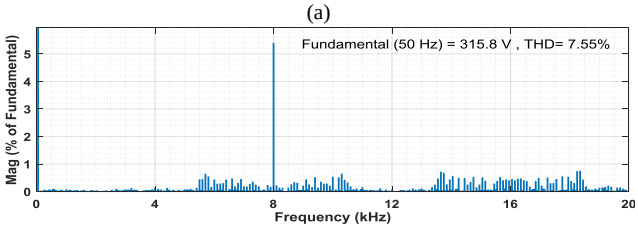
TABLE IV. Characteristics of the Simulated Model

Input voltage	80 V
Output voltage (RMS)	230 V
Output voltage frequency	50 Hz
Charging inductor	0.3 mH
Capacitors	3300 μF
Switching frequency	8 kHz

Fig. 8(a) shows the output and capacitor voltages under no-load condition. Furthermore, the Fast Fourier Transform (FFT) analysis of the developed voltage is depicted in Fig. 8(b). According to the voltage waveform and its FFT analysis, it is evident that the proposed topology can develop the desired voltage with a high quality.



(a)



(b)

Fig. 8. Simulation results of a 17-level configuratopn of the proposed topology under the no-load condition: (a) output voltage under no-load condition, and (b) FFT analysis of the output voltage.

In addition, the output voltage and load current in the presence of a purely resistive load of 2 kW are shown in Fig. 9. As seen in Fig. 9, due to voltage ripple of the capacitors, insignificant ramps appear over the voltage levels.

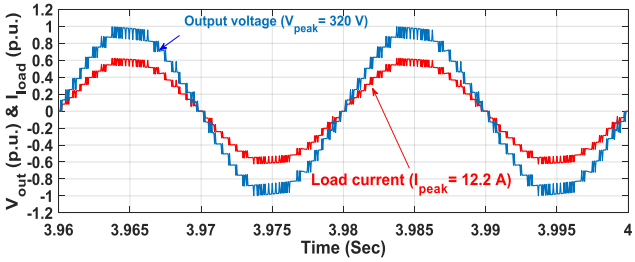
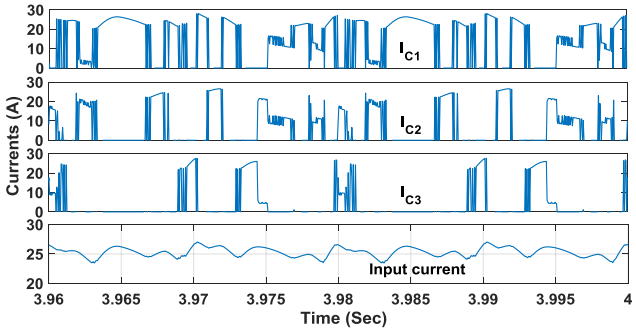
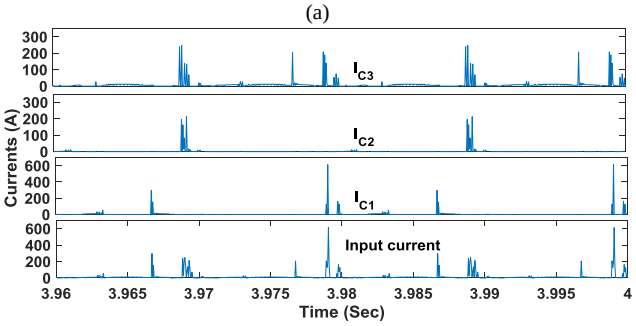


Fig. 9. Output voltage and load current under the purely resistive loading condition.

The input and capacitor charging currents under the mentioned loading condition are shown in Fig. 10(a). As observed, the input current is smooth and continuous. It is accomplished through the charging inductor. To further clarify, considering the mentioned loading condition without the charging inductor, the input and the capacitors charging currents are demonstrated in Fig. 10(b). When comparing Figs. 10(a) and (b), it is seen that the charging inductor has properly smoothed the input current and mitigated the inrush currents.



(a)



(b)

Fig. 10. Simulation results of the input and capacitor currents under a purely resistive loading condition: (a) input current together with the charging current of the capacitor in the presence of the charging inductor, and (b) Input current together with the charging current of the capacitor without using the charging inductor.

In order to show the effect of the voltage ripple of the capacitor on the output voltage, the capacitor voltages along with the output voltage are exhibited in Fig. 11(a). To further clarify, the voltage across the capacitors and the input current are individually shown in Figs. 11(b) and (c), respectively. As it is seen in Fig. 11, the total voltage ripple of the capacitors is 0.07 p.u. (0.07*320 = 22 V), and the input current ripple is 3 A. Fig. 11(a) explicitly shows the

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effect of the capacitors voltage ripple on the output voltage. According to Fig. 11(a), the voltage ripple is high when developing the peak value of the output voltage. The reason is that, when developing the peak value all the capacitors are in the discharging mode, so they have the highest voltage ripples, which are added up to bring the highest voltage ripple of the capacitor voltage. As shown in Fig. 11(b) the capacitors in the first cell experience low voltage ripple because they situate in the charging mode more than the other capacitors. in contrast, the capacitor in the last cell experience the highest voltage ripple as they reside in the charging mode less than the other capacitors.

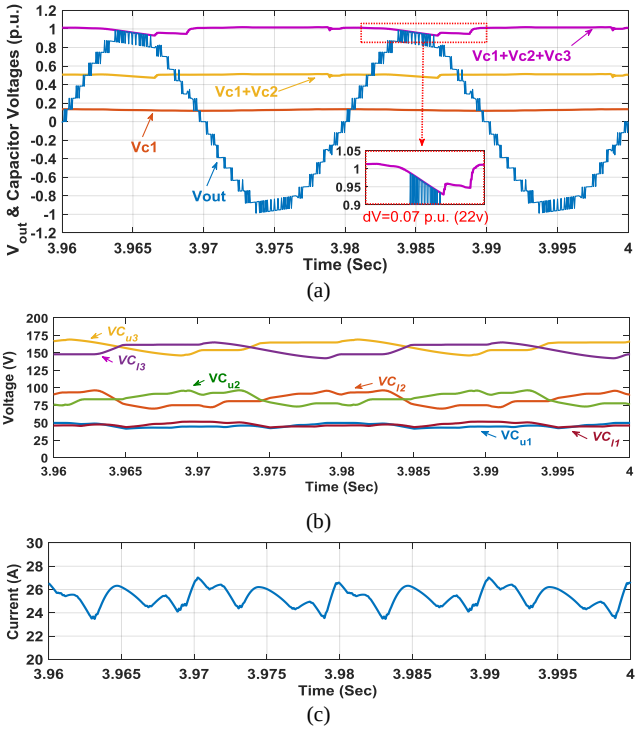

Fig. 11. Simulation results of voltage and current ripples under a purely resistive loading condition: (a) voltage ripple of the capacitors along with the output voltage (b) voltage across the capacitors, and (c) the input current.

The IEEE 1547 standard requires inverters to provide the reactive power upon demand. In order to assess the performance of the proposed topology with reactive power injection, a resistive-inductive load of 1.7 kW+0.85 kVar is assumed. The output voltage and load current under the mentioned loading condition are shown in Fig. 12. As it is observed in Fig. 12, the proposed topology can satisfy the mentioned standard in a good manner.

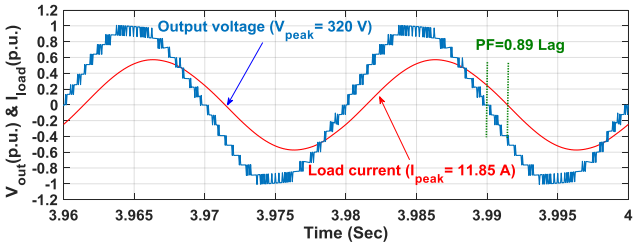

Fig. 12. Output voltage and load current under the resistive-inductive loading condition.

By considering different apparent power (S), power factor (PF) and modulation indexes, the dynamic performance of the proposed inverter is demonstrated in Fig. 13. As shown in Fig. 13, the proposed topology can satisfactorily operate under the considered conditions.

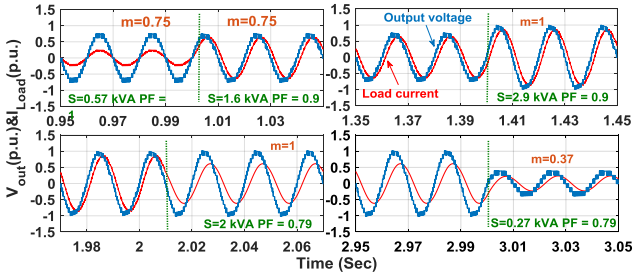

Fig. 13. Dynamic performance of the proposed inverter under different loading conditions and modulation indexes.

VI. Experimental Results

In order to verify the feasibility of the proposed topology, experimental tests are performed on a laboratory-scale prototype. The prototype consists of four cells, so it can develop 33 voltage levels. The characteristics of the prototype are listed in Table V. In addition, the prototype is shown in Fig. 14.

TABLE V.
COMPONENT CHARACTERISTICS.

Components	Type
Switches	IRFP350 PbF
Opto-coupler	TLP250
Microprocessor	DSP-F28335
Capacitors	3300 µF
Switching power supply	iS0515s
Charging inductor	360 µH
Diodes	FFPF20UP40S

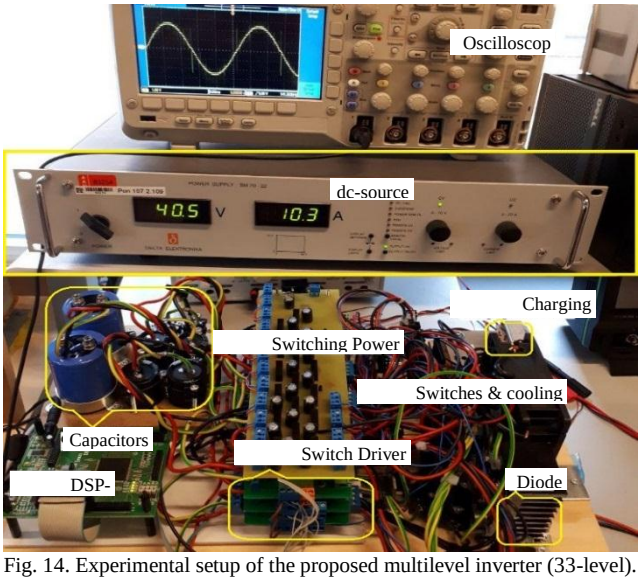

Fig. 14. Experimental setup of the proposed multilevel inverter (33-level).

The peak value and the frequency of the output voltage are 320 V and 50 Hz, respectively. The input voltage and switching frequency are 40 V and 8 kHz, respectively. Fig. 15(a) shows the output voltage under no-load condition. Furthermore, a purely resistive load of 500 W is connected to the output terminals. The output voltage and load current in the presence of the mentioned load are presented in Fig. 15(b).

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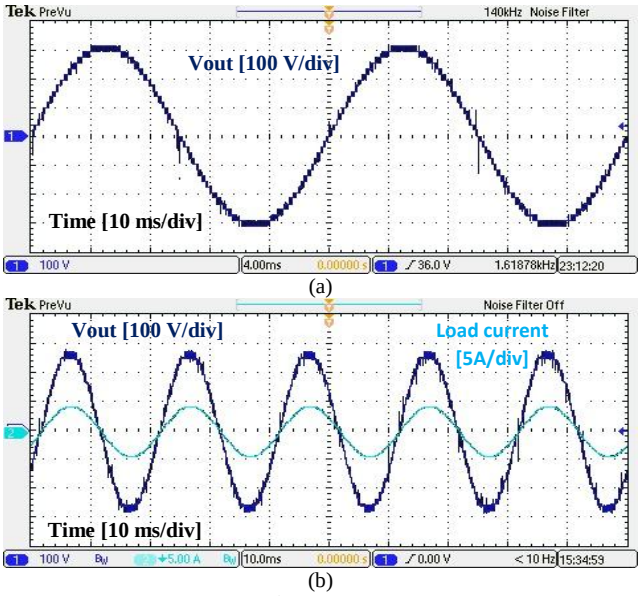

Fig. 15. Experimental results of the proposed inverter under no-load and purely resistive loading conditions. (a) output voltage in no-load condition and (b) output voltage and load current under a purely resistive loading condition.

Moreover, the load current along with the input current is shown in Fig. 16(a). As it is demonstrated in Fig. 16(a), the inverter has drawn a continuous current from the dc source. These results validate the feature of the proposed multilevel inverter achieving a continuous input current. As discussed previously, one of the interesting features of the proposed topology is the ability to limit the inrush current of the capacitors. This performance is demonstrated in Fig. 16(b). As it is observed in Fig. 16(b), the charging currents are limited within a reasonable range. Hence, the capacitors are charged by a safe charging current.

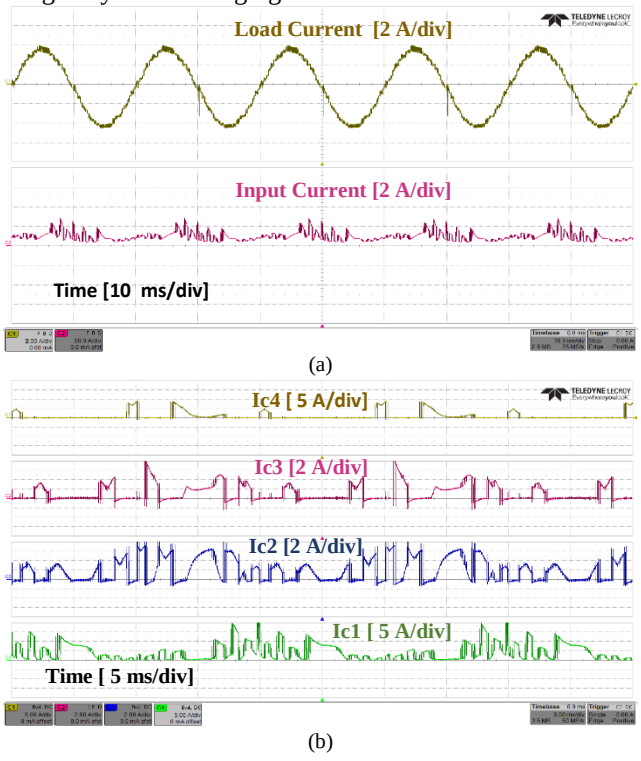

Fig. 16. Experimental results of the input and capacitor charging currents (a) output and input current and (b) charging current of capacitors.

Furthermore, by performing the FFT analysis, the quality of the developed voltage can be analyzed. The FFT result in Fig. 17 describes different harmonic contents of the output voltage. Since the switching frequency is 8 kHz, the harmonics around this frequency are of higher magnitude. Nonetheless, the developed multilevel voltage features a low Total Harmonic Distortion (THD) level.

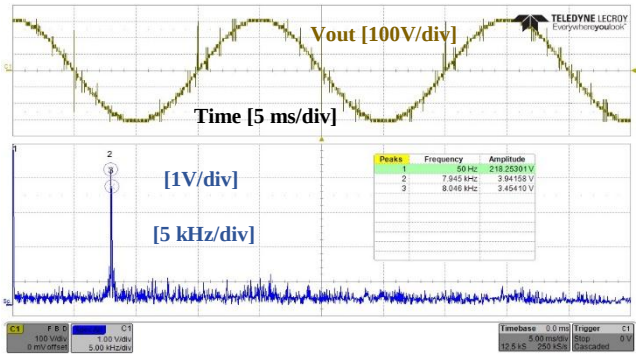

Fig. 17. FFT analysis of the output voltage.

The performance of the proposed topology in the presence of a resistive-inductive load of 510 W + 330 Var is also obtained. The experimental results are presented in Fig. 18. As demonstrated in Fig. 18, the inverter has provided the considered reactive power. In all, the above simulations and experimental tests have confirmed the superior performances of the proposed multilevel inverter topology in terms of lower component-count, self-balancing and continuous input current.

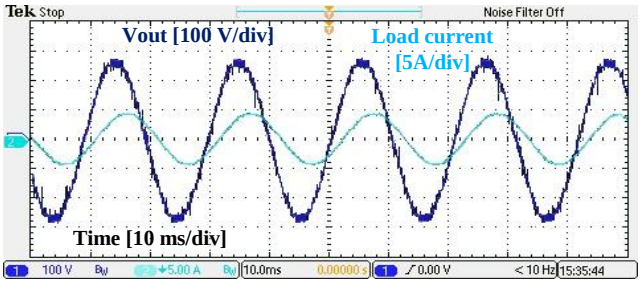

Fig. 18. Output voltage and load current in the resistive-inductive loading condition.

VII. CONCLUSION

In this paper, a new multilevel inverter topology was proposed. The proposed topology uses fewer switches compared to the conventional single source CMI topology. The proposed topology consists of several half-bridge cells. The half-bridges in this topology use two capacitors instead of isolated dc sources. The capacitors are charged through a charging unit. The charging unit is synthesized with a charging inductor, a dc source, and several diodes. The charging inductor can both smooth the input current and avoid the inrush current of the capacitors. In addition, it can limit the fault current. This topology features self-balancing, and boosting abilities, draws a smooth and continuous current from the dc side. Considering the mentioned features and unidirectional power flow possibility, the proposed can be a versatile converter in PV applications. Simulations and

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experimental results have validated the performance of the proposed topology.

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