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A Trans-Inverse Coupled-Inductor Semi SEPIC DC/DC Converter with Full Control Range

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***Abstract*—This letter proposes a single switch magnetically coupled dc/dc converter with high voltage gain. The unique features of the converter are summarized as: 1) voltage gain of the converters is raised by lowering its magnetic turn ratio; 2) wide control range ($0 < D < 1$); 3) continuous current from the source that makes it a suitable candidate for renewable energy applications; 4) there is no dc current saturation in the core due to the presence of capacitor in the primary winding of the inductor. The feasibility of the proposed converter is studied in details supported by circuit analysis and simulation results. Further, the proposed converter is analyzed and compared with other converters with similar features. Finally the superior performance of the circuit is validated experimentally.**

***Index terms*—** dc-dc converter, SEPIC, coupled inductor, regenerative snubber, voltage stress, renewable energy.

I. Introduction

Renewable energy resources such as Photovoltaic (PV), wind and fuel cell are being widely employed in recent years to decrease the negative side effects due to conventional energy resources. However, the renewable energy resources usually cannot be directly connected to the grid because of their intermittent nature. As an example, the low and variable dc-input voltage (20-45 V) generated from the PV modules should be boosted enough to high voltage (e.g., 200-400 V), in order to generate AC utility voltage using DC/AC converter. Similarly, in hybrid EV (HEV) and other electric traction systems, a voltage of 14 or 42 V from batteries, fuel cells and/or super capacitors needs to be raised to 200 or 500 V during various modes of operation [1]. The requirement for dc voltage boosting is even more prominent lately with the emergence of the 400 V micro-grids powered by multiple energy sources, and the introduction of facility-level 400 V DC distribution for data and telecommunication centers. Therefore, high step-up DC/DC converters play a vital role in renewable energy systems [1, 2]. Conventional boost converters have very simple structures, where its theoretical voltage gain reaches infinitely when the duty cycle is near to unity. Meanwhile, due to higher losses at elevated duty cycle, the practical voltage gain cannot exceed 4-5 even with well designed layout [3]. To overcome this issue of limited voltage gain in the conventional boost converter, different solutions have been presented in the literature [4–15]. Switch inductor, switch capacitor; multi-cell and cascaded configurations [4–6] are well investigated to achieve higher voltage gain. However, to achieve a high voltage gain several switched inductor/capacitor cells are typically required, resulting in higher cost, size and complexity [7]. Coupled inductor technique is an interesting method to achieve high voltage gain using less number of components [8, 9]. Usually in most converters with this technique, the voltage gain can be increased by increasing the coupled inductor turn ration, which may lead to higher cost and size [10]. Moreover, usually an additional snubber circuit is required to dissipate the leakage energy of the coupled inductors, which creates the voltage spike across the switch. This leads to more complex circuit with lower overall efficiency [7]. Recently, a series coupled inductor converters based on impedance-source networks have been introduced such as Γ-source [11], Y-source [12], improve Γ-source [13]. In these converters, the voltage gain is increased by lowering the coupled inductor turn ratio, which provides a great advantage in reducing the overall size of the converter for higher voltage gain. However, these converter demands higher voltage rated switch with higher $R_{DS(\mathrm{ON})}$ (equal or higher than the output voltage) resulting in higher power loss. In addition, by lowering the coupled inductor turn ratio, the useful range of duty cycle to achieve practical voltage gain is narrowed down. This results in a very steep voltage gain, which complicate the converter control because of greater sensitivity of the output voltage to the duty cycle [10]. Two trans-inverse converters are presented in [10] and [14] with high voltage gain and much lower voltage stress on the switch, however similar to converters in [11–13] the duty cycle operates in narrow range. A new trans-inverse converter is proposed in [15] where duty cycle can vary between 0 and 1 without very steep voltage gain curve, however its input current has high ripple that makes it inappropriate for PV application, where low input current ripple is preferred. To mitigate the aforementioned problems, a novel trans-inverse converter is presented in this letter with continuous input current with very low ripple magnitude. Its

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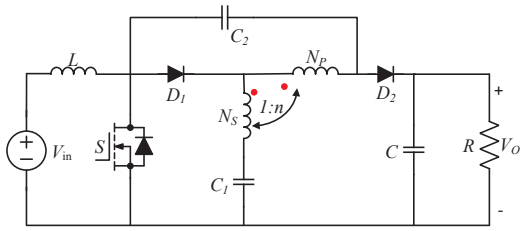

Fig. 1. Schematic of the proposed converter.

duty cycle variation range is between 0 and 1 without very high steep gain curve. In addition, the voltage stress on the switch is much lower than the output voltage. Further it does not require any external snubber circuit, where the leakage energy is recycled by an built-in regenerative snubber circuit and finally the dc-current saturation of the core is prevented due to the presence of the DC current blocking capacitor in series with one of the transformer windings. This letter is organized as follows: in section II, the converter is analyzed in details in continues conduction mode (CCM). The performance of the converter is verified using simulation and experimental results in section III and the findings drawn are finally concluded in Section IV.

II. Proposed Trans-Inverse Converter

A. Description of the converter in CCM

The schematic of the proposed converter is shown in Fig. 1. Similar to the conventional SEPIC converter, it consists of an input inductor (L), one common ground switch (S), an intermediate capacitor (C_2), output diode (D_2) and output capacitor (C). With some modification the intermediate inductor in the SEPIC converter is replaced with an impedance network, which consists of one diode (D_1), one capacitor (C_1) and coupled inductors, where $n = N_P/N_s$ indicates their turn ratio. To simplify the analysis, the following assumptions are made: 1) All components are ideal that means all equivalent series resistance (ESR) in inductors and capacitors are neglected. In addition the forward voltage drop of the diodes, drain-source on resistance $R_{DS(\mathrm{ON})}$ and parasitic capacitances of the switch (S), are negligible. 2) All capacitors are large enough which the voltage across them is constant in one switching cycle. 3) The coefficient of the transformer coupling is one, which means the leakage inductances are zero. However, the leakage inductances effect on the voltage spike across the power switch will be considered in the next subsection. With above assumptions, there are two stages in one switching cycle as shown in Fig. 2. When the power switch turns on as shown in Fig. 2(a), both diodes become reverse bias and turned off. The input inductor charges through the input source and the output load is isolated from the source and is powered by the output capacitor. As it can be seen from Fig. 2(a), we can write:

$$V_{\mathrm{LM}} = \frac{V_{C1} - V_{C2}}{n-1} \tag{1}$$

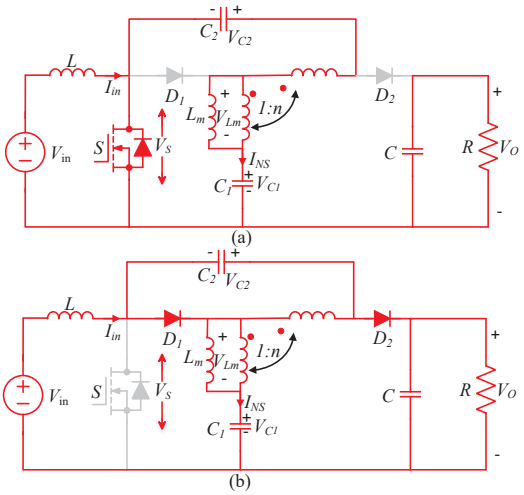

Fig. 2. Equivalent circuits of the proposed converter when the switch turns (a) ON and (b) OFF.

Both diodes are forward biased when the switch is turned OFF as shown in Fig. 2(b). The input inductor releases its energy to the load, where its current decreases and the output capacitor is charged from the input source. In this stage the circuit expressions are given as follows:

$$V_{\mathrm{LM}} = \frac{V_{C1} - V_O}{n-1} \tag{2}$$

Applying volt-second balance principle to input inductor and magnetizing inductor, they can be obtained as:

$$DV_{in} + (1-D)\left(V_{in} - V_{C2} - V_O\right) = 0 \tag{3}$$

$$D\left(\frac{V_{C2} - V_{C1}}{n-1}\right) + (1-D)\left(\frac{V_{C1} - V_O}{n-1}\right) = 0 \tag{4}$$

By some derivations, the voltage gain across C_1, C_2 and output voltage are obtained as:

$$\begin{aligned} V_{C1} &= \left(1 + \tfrac{nD/(n-1)}{1-D}\right) V_{\mathrm{in}} \quad V_{C2} = \left(\tfrac{nD/(n-1)}{1-D}\right) V_{\mathrm{in}} \\ V_O &= G \cdot V_{\mathrm{in}} = \left(\tfrac{1+nD/(n-1)}{1-D}\right) V_{\mathrm{in}} \end{aligned} \tag{5}$$

where G is the voltage gain of the proposed converter. Refer to (5) and Fig. 3 it is clear that the converter gain increases when the turns ratio decreases. However, the duty cycle range can vary in a wide range ($0 < D < 1$), unlike converters presented in [10–13] where the range of duty cycle is narrow.

B. Inbuilt voltage clamp circuit

In practice, the leakage inductance is nonzero and may cause large voltage spikes on the power switch due to resonance with the switch parasitic capacitor. However, in the proposed converter when the power switch is turned OFF, both diodes are turned ON. Refer to Fig. 2(b); the switch voltage is clamped to difference of output voltage and capacitor voltage V_{C2}. Therefore, using capacitorsC_1, C_2, and diode D_1 and D_2 make an inbuilt regenerative snubber circuit that helps to redirect

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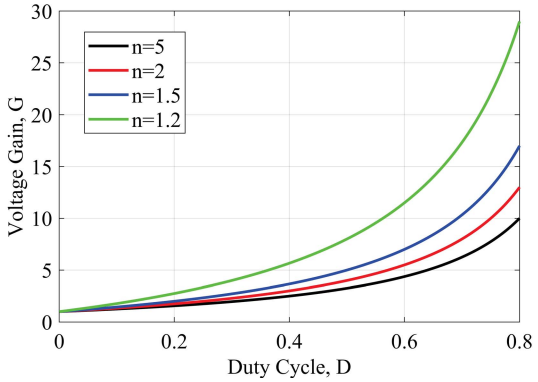

Fig. 3. Voltage gain of the proposed converter in Fig. 1.

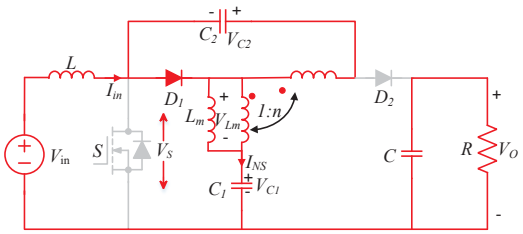

Fig. 4. Equivalent circuits of the proposed converter when the diode D_2 is turned off in stage 2.

the leakage energy safely to the power capacitors. With this arrangement, the requirement of additional lossy snubber circuit is eliminated.

C. Effect of the leakage inductance on the converter performance

The coupled inductor was considered as an ideal to perform the steady-state analysis; however, when the effect of the leakage inductance is considered in analysis, the diode D_2 turned off before the end of the switching cycle. However when its effects is considered, diode D_2 is turned off before the end of the stage 2. Therefore, in addition to Fig. 2(b), there is another equivalent circuit in stage 2, which diode D_2 is turned off as shown in Fig. 4.

With high coupling coefficient in the coupled inductor design ($K \approx 1$), the leakage inductance value is small in comparison with the magnetizing inductance. With this assumption and using voltage-second principle law on input inductor and magnetizing inductance in Fig. 2 and Fig. 4, the voltage across C_1, C_2, and output voltage is the same as (5). Therefore the reverse bias of the diode D_2 in stage 2 does not have considerable effect on the converter performance and its voltage gain. This is verified later in the experimental results section.

D. Comparison with similar topologies

Table I presents a comparison of the proposed converter with several trans-inverse type converter. - source [11] and Y source [12] have the lowest number of components, however

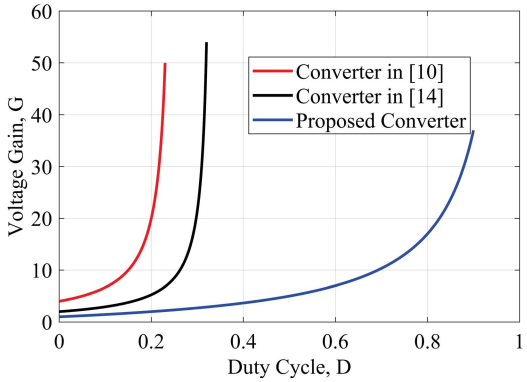

Fig. 5. Voltage gain comparison of the proposed converter and converters in [10, 14] for n=1.5.

their input current is discontinuous with high ripple magnitude that makes them inappropriate in renewable energy systems. Converters in [10] and [13] have continuous input current with low ripple, but the duty cycle variation range is narrow particularly when n is tends to unity which complicates the controller design because of higher sensitivity of the output voltage to duty ratio. In addition, the voltage stress on the switch is high and equal to output voltage in the presented converters in [11–13].

The duty cycle can vary in a wide range in the presented in [15], however the input current ripple in this converter is high, therefore an input filter is mandatory in renewable energy systems that makes its structure more complicated. Compared with [15], the input current ripple in the proposed converter is low and also one diode is saved in the proposed converter compared with [15]. Moreover one DC current block capacitor in series with one coupled inductor can prevent from core saturation in the proposed converter. Compared to converters in [10–13] it has wide range of duty cycle variation for any coupled inductor turn ratio and therefore lower sensitivity to D. In addition, it benefits from low voltage stress on switch in compare with [11–13]. Fig. 5 shows the static voltage gain of the proposed converter and presented converters in [10] and [14] for n=1.5. Converters in [10, 11, 14] have high voltage gain. However, the duty cycle cannot exceed than 1/3 in [10, 11] and 1/4 in [14].

Therefore the duty cycle variation range is narrow and voltage gain varies steeply that makes their control more complicated. In addition, some diodes in [10] and [14] conduct in only a small portion of the switching cycle, which results in a reverse recovery problem. In contrast, the voltage gain variation in the proposed converter is smooth that simplifies its control. From the number of components viewpoint, refer to table I, the converters in [10] and [14] have more number of components compared to the proposed converter.

III. Experimental Results

In order to verify the theoretical analysis a prototype is built as shown in Fig. 6. The circuit parameters of the proposed

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TABLE I
COMPARISON WITH STATE OF THE ART TOPOLOGIES.

Converter	[10]	[11]	[12]	[13]	[14]	[15]	Proposed
Num. of inductors+ couple inductors	1+2	0+2	0+3	1+2	1+2	0+2	1+2
Num. of capacitors	5	2	2	3	5	3	3
Num. of switches	1	1	1	1	1	1	1
Num. of diodes	4	2	2	2	4	3	2
Input current ripple	low	high	high	low	low	high	low
DC current block capacitor	yes	yes	yes	yes	no	no	yes
Switch voltage stress($\frac{v_s}{v_o}$)	$\frac{n-1}{2(n-1)+D}$	1	1	1	$\frac{n-1}{2n-1}$	$\frac{n-1}{2n-1}$	$\frac{n-1}{2n-1}$
Duty cycle variation range	$0<D<\frac{n-1}{n}$	$0<D<\frac{1}{1+\frac{1}{n-1}}$	$0<D<\frac{1}{k}$	$0<D<\frac{1}{2+\frac{1}{n-1}}$	$0<D<\frac{n-1}{2n-1}$	$0<D<1$	$0<D<1$

TABLE II
DESIGN PARAMETERS OF THE PROPOSED CONVERTER.

Parameter/Decription	Value/Part Number
Power rating	150-400 W
Input/Output voltage	48/400 V
Capacitor/input inductance	100 μF/640 μH
Turn ratio	28:20 Core:B66397G0000X197
Leakage/magnetizing inductance	1.27/220 μH
Switching frequency	100 kHz
Duty Cycle	0.62
Switch S	IPP60R099C6XKSA1
Diode D1&D2	IDP30E65D2XKSA1

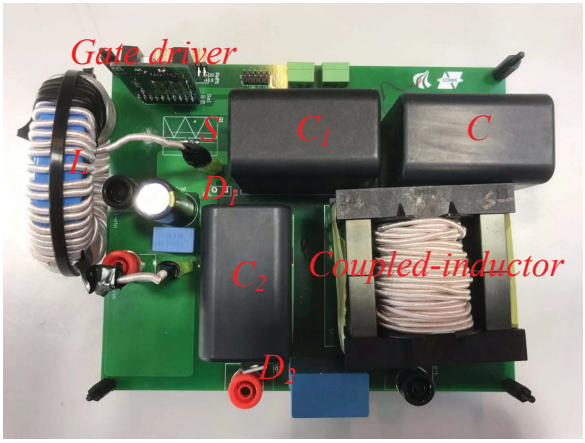

Fig. 6. Picture of the hardware prototype.

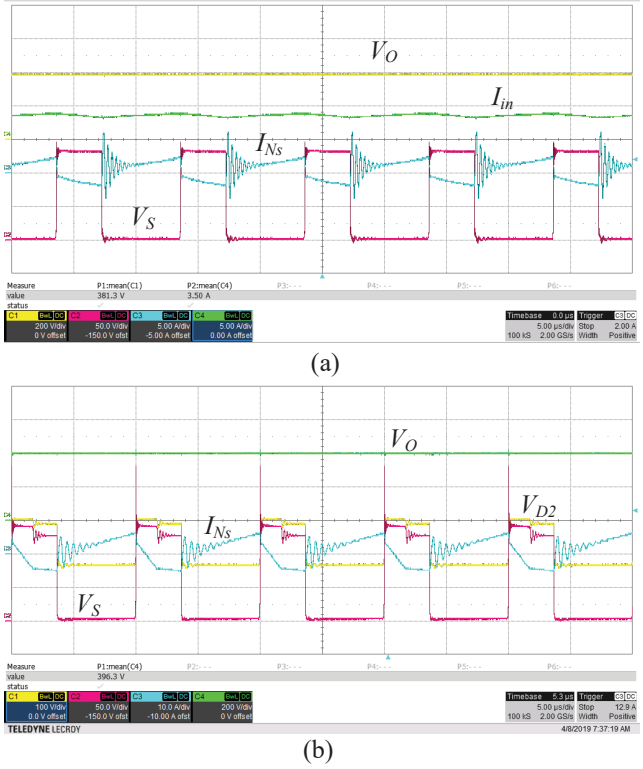

Fig. 7. Experimental results obtained at (a) Po: 168 W (b) Po: 325 W: Output voltage (200 V/div), Input current (5 A/div), Switch voltage (50 V/div) and coupled inductor secondary current (5 A/div) and diode D_2 voltage (100 V/div).

converter are listed in Table II. Fig. 7(a) shows the experimental results under 168 W output power. The output voltage is about 400 V under open loop control. It is clear that the proposed converter is able to boost the 48 V input voltage to higher voltage with acceptable ripple. The input current mean value is 3.5 A. It is obvious that the input current is continuous with low ripple.

The voltage stress on the power switch is about 130 V, that is much lower than the output voltage. It is clear that there is no voltage spike across the power switch that confirms the theoretical analysis. Finally, that figure shows the current that flowing in the transformer secondary winding, it has a periodic signal with no DC current because the capacitor C_1 in series with transformer winding can prevent from core saturation. Experimental results under output power 325 W are shown in Fig. 7(b). Under open loop control the output voltage is about 396.3 V that is much close to its theoretical value. This confirms that the effect of leakage inductance on converter performance and its voltage gain is small. The voltage stress on diode D_2 is about 130 V (Ch2 of Fig. 7(b)), which is much lower than the output voltage. In addition, this diode is turned off before end of the second stage because of the leakage inductance effect as seen in the theoretical analysis in Section II (c). In this case, the voltage stress on switch is lower than the output voltage. The efficiency of the proposed converter is measured at different output power levels from 50 W to 400 W as shown in Fig. 8. The converter efficiency at all output power level is above 92%

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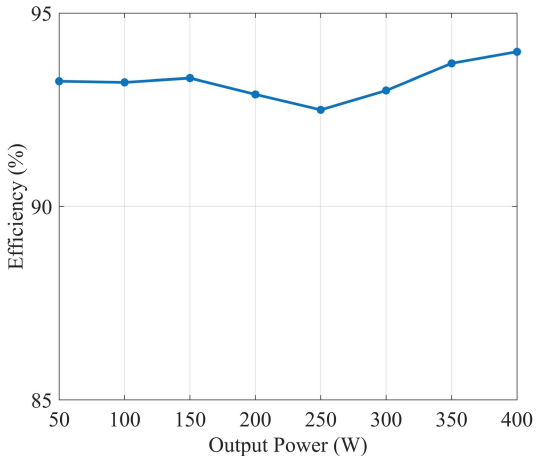

Fig. 8. System efficiency at varying load (Vin=48 V, D=0.62, fs=100 kHz).

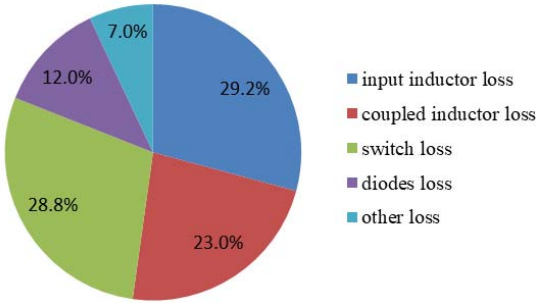

Fig. 9. Power loss distribution.

and its maximum value is 94% at full load (400 W), which confirms high efficiency can be achieved using the proposed converter.

The loss distribution of the proposed converter at Po=325 W is shown in Fig. 9. The major loss is related to magnetic elements (input inductor and coupled inductors). The second power loss comes from the power switch that consists of the switching loss and conduction loss. The power loss on diodes is about 12% of the power loss. Other loss is 7% that mainly consists of the capacitor loss.

IV. Conclusions

A new coupled inductor based Semi SEPIC converter is introduced in this letter. The voltage gain of the converter increases by lowering the coupled inductors turn ratio, which may lead to lower size and cost. Unlike most trans-inverse type converters the duty cycle in the proposed converter can vary in wide range, which simplifies the controller design. In addition, the converter draws a continuous current from the source with low ripple magnitude that makes it suitable for renewable energy applications. In addition, a dc blocking capacitor in series with coupled inductor can prevent from core saturation. These demonstrated performances clearly stands out the proposed topology as a competitive alternative for a practical application where a high voltage gain is demanded, such as for fuel cells and PVs.

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