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Balanced Power Device Currents Based Modulation Strategy for Full-Bridge Three-Level (FBTL) DC/DC Converter

Dong Liu, Member, IEEE, Yanbo Wang, Member, IEEE, Fujin Deng, Member, IEEE, and Zhe Chen, Fellow, IEEE

Abstract - This paper proposes a new modulation strategy with balanced power device currents for the full-bridge three-level (FBTL) DC/DC converter. The proposed modulation strategy has two working patterns, which can not only realize zero-voltage switching (ZVS) but also satisfy the wide input voltage range. More significantly, the two working patterns of the proposed strategy can both balance the currents among the power switches and clamping diodes in comparison with the conventional control strategies causing current imbalances among the power switches and clamping diodes. Consequently, the proposed strategy can balance the thermal stresses among the power switches and clamping diodes, which would thus improve the converter’s reliability. Finally, the experimental results, obtained by a built 1.5 kW experimental prototype, verify almost zero current difference and zero thermal stress difference among the inner power switches, outer power switches, and clamping diodes under the proposed strategy.

Keywords - balanced power device currents, full-bridge three-level (FBTL) DC/DC converter, wide input voltage range, zero-voltage switching (ZVS).

I. INTRODUCTION

The three-level (TL) DC/DC converter is attractive for the high voltage applications, such as three-phase power factor correction systems, renewable energy systems, electric vehicle charging systems, and distributed power systems [1-5], because the voltage stresses on the power switches are only half of the input voltage ($V_{in}/2$) in the TL DC/DC converter [6], [7]. So far, many studies about the TL DC/DC converter have been carried out [8-20]. In [8], a zero-voltage and zero-current switching half-bridge (HB) TL DC/DC converter was proposed, in which the phase-shift control strategy can be applied into the TL DC/DC converter by adding a flying capacitor in the primary side. Based on [8], a TL DC/DC converter with the auxiliary circuit was proposed to reduce the circulating current for the converter’s efficiency improvement [9]. An improved zero-voltage switching (ZVS) DC/DC converter with series-connected transformers was proposed in [10], which can both realize the ZVS within nearly entire load range and balance the output currents. In [11], a novel ZVS TL DC/DC converter was proposed, which features a simple and compact circuit structure by removing two clamped diodes and connecting the mid-points of the input capacitors and switching pairs. Based on [11], four types of new pulse-width modulation PWM TL DC/DC converters with the wide range soft-switching are proposed for industrial applications in [12] and a new ZVS modulation strategy with input capacitors’ current balancing control strategy was proposed in [13] for the TL DC/DC converter. Additionally, a secondary-side phase-shift-controlled ZVS DC/DC converter with the wide voltage gain was proposed in [14] for the high voltage applications, which can effectively reduce the circulating current.

The above studies mainly focus on the HB TL DC/DC converters, but they are not suitable for the high power electronic systems because of the higher current stresses on the power switches in comparison with the full-bridge (FB) DC/DC converters [21-23]. In addition, the modulation strategy of the FB circuit structure is different from that of the HB circuit structure and even more complex due to more power devices in comparison with the HB circuit structure. In [15] and [16], two hybrid ZVS full-bridge three-level (FBTL) DC/DC converters were proposed for high power applications, which are both composed of a TL leg and a two-level leg in the primary side. A zero-voltage and zero-current switching FBTL with reduced circulating current and an improved FBTL DC/DC converter with input capacitors’ voltage balancing control strategy were proposed in [17] and [18] respectively, but they cannot satisfy the wide input voltage range. Two modulation strategies named chopping phase-shift (CPS) strategy and double phase-shift (DPS) strategy were proposed in [19] and [20] respectively for the FBTL DC/DC converter, which can both satisfy the wide input voltage range.

When it comes to the modulation strategies for FBTL DC/DC converters, there are mainly three objectives that previous research aims to achieve, which include the soft switching, wide input voltage range, and reliability of input capacitors (capacitors’ voltages and currents balancing methods). However, there are few studies paying attention on the current balancing among the power devices in the FBTL
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DC/DC converter, which is closely related with the reliability of the converter because the unbalanced currents among the power devices would result in the power loss imbalances and thermal stress imbalances among the power devices [24-26].

In this paper, the current imbalance issue of the power devices under the conventional modulation strategies in the FBTL DC/DC converter is pointed out and analysed in detailed. Then, a new modulation strategy is proposed for the FBTL DC/DC converter to eliminate these current imbalances. In addition, the proposed strategy is composed of two working patterns for satisfying the wide input voltage range. These two working patterns can both realize zero-voltage switching (ZVS) and has the ability of seamless transition. More importantly, the two working patterns can both balance the currents among power switches and clamping diodes. Accordingly, the proposed strategy would balance the power losses and thermal stresses among the power switches and clamping diodes, which is helpful for improving the reliability of the converter. The performances of the FBTL DC/DC converter under the proposed strategy are analysed in detail and verified by the experimental results.

This paper is organized as follows. Section II analyzes the current imbalance issue of the power devices under the conventional strategies. Section III introduces the proposed modulation strategy and analyzes the operation principles of the proposed strategy in detail. Section IV presents the detailed analysis about the characteristics and performances of the proposed strategy. Section V demonstrates the experimental results to verify the proposed strategy. Finally, the main contributions of this paper are summarized in Section VI.

II. CURRENT IMBALANCE ISSUE UNDER CONVENTIONAL STRATEGIES

Fig. 1 shows the circuit structure of the FBTL DC/DC converter.

![Fig. 1. Circuit Structure of FBTL DC/DC converter.](image)

In Fig. 1, in the primary side, \( C_0 \) and \( C_2 \) are two input capacitors which split the input voltage \( V_{in} \) into \( V_1 \) and \( V_2 \); \( S_i, S_s, S_o \) are outer switches and \( D_1, D_4, D_6, D_9 \) are their body or paralleled diodes; \( S_2, S_3, S_5, S_6 \) are inner power switches and \( D_8, D_9, D_{10}, D_{11} \) are their body or paralleled diodes; \( C_1 - C_8 \) are parasitic capacitors of \( S_1 - S_6 \); \( C_{11} \) and \( C_{12} \) are two flying capacitors; \( D_{10} - D_{11} \) are four clamping diodes; \( T_i \) is the isolation transformer; \( L_o \) is the leakage inductor of \( T_i \) plus added inductor in series with \( T_i \). In the secondary side, \( D_{12} - D_{14} \) are four output rectifier diodes; \( L_0 \) and \( C_0 \) are output filter inductor and output filter capacitor, respectively. In addition, \( V_{in} \) is the input voltage; \( V_1 \) and \( V_2 \) are the voltage on the input capacitor \( C_1 \) and \( C_2 \); \( i_{c1} \) and \( i_{c2} \) are the current on the input capacitor \( C_1 \) and \( C_2 \); \( V_{ab} \) is the voltage between the point \( a \) and \( b \); \( l_p \) is the primary current of the transformer \( T_i \); \( i_1 - i_8 \) are currents on the primary power switches \( S_1, D_1 \) - \( S_1, D_9 \); \( i_{290} - i_{212} \) are currents on the clamping diodes \( D_8 - D_{12} \); \( n \) is the turns ratio of the transformer \( T_i \); \( i_{20} \) is the current through the output filter inductor \( L_o \); \( V_0 \) and \( l_o \) are the output voltage and output current respectively.

In order to simplify the following analysis, several assumptions are made as: 1) all the switches and diodes are ideal; 2) two input capacitors \( C_1 \) and \( C_2 \) are large enough to be considered as two voltage sources with the values of the half of input voltage \( (V_{in}/2) \); 3) two flying capacitors \( C_{11} \) and \( C_{12} \) are considered as two voltage sources with the values of \( V_{in}/2 \) but only provide charging and discharging paths for the switches’ parasitic capacitors; 4) the output filter inductor \( L_o \) is large enough to be considered as a constant current source; and 5) the parasitic capacitors of \( S_1 - S_6 \) are the same, which means \( C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = C_7 = C_8 = C_{11} \).

Fig. 2 presents the currents through the power switches \( (i_1 - i_8) \) and currents through the clamping diodes \( (i_{290} - i_{212}) \) under the DPS strategy as an example to explain the current imbalance issue under the conventional modulation strategies, in which \( d_{e1} - d_{e8} \) are driving signals for the power switches \( S_1 - S_6 \); \( T_i \) is one switching period; \( \alpha_1, \alpha_2 \) and \( \theta \) are phase-shift delays. It needs to be mentioned that the currents \( i_1 - i_8 \) and \( i_{290} - i_{212} \) under the CPS strategy are the same as that under the DPS strategy.
From Fig. 2, it can be observed that: 1) for the currents on the outer power switches (i1, i4, i5, i8) as marked by red color, i1, i4 are the same besides 180° phase difference, i5, i8 are the same besides 180° phase difference, and i5, i8 are higher than i1, i4; 2) for the currents on the inner power switches (i2, i3, i6, i7) as marked by blue color, i2, i3 are the same Besides 180° phase difference, i6, i7 are the same besides 180° phase difference, the root mean square (RMS) value of i2, i3, i6, i7 are the same but the average value of i2, i3 are smaller than that of i6, i7; 3) for the currents on the clamping diodes (i9, i10, i11, i12) as marked by orange color, i9, i10 are the same besides 180° phase difference, i11, i12 are zero, so i9, i10 are higher than i11, i12. Therefore, based on the above analysis, it can be concluded that the currents among the outer power switches (i1, i4, i5, i8), inner power switches (i2, i3, i6, i7), and clamping diodes (i9, i10, i11, i12) are unbalanced under the conventional strategies.

Table I presents the calculation equations about the RMS and average values of i1 - i8 and i9 - i12 under the DPS strategy according to Fig. 2.

### III. Proposed Modulation Strategy

In order to eliminate the current imbalances among the power devices under the conventional strategies, a new modulation strategy with balanced power device currents is proposed for FBTL DC/DC converter.

#### Table I. Theoretical Equations About RMS and Average Values of Currents on Primary Power Devices Under DPS Strategy

<table>
<thead>
<tr>
<th>Current</th>
<th>Three-level mode</th>
<th>Two-level mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>i1, i4</td>
<td>RMS value</td>
<td>[ \frac{I}{2} \frac{-4L \cdot I}{n \cdot T} ]</td>
</tr>
<tr>
<td></td>
<td>Average value</td>
<td>[ \frac{I}{2} \frac{-4L \cdot I}{n \cdot T} ]</td>
</tr>
<tr>
<td>i5, i8</td>
<td>RMS value</td>
<td>[ \frac{I}{2} \frac{-4L \cdot I}{n \cdot T} ]</td>
</tr>
<tr>
<td></td>
<td>Average value</td>
<td>[ \frac{I}{2} \frac{-4L \cdot I}{n \cdot T} ]</td>
</tr>
<tr>
<td>i2, i3</td>
<td>RMS value</td>
<td>[ \frac{I}{2} \frac{-4L \cdot I}{n \cdot T} ]</td>
</tr>
<tr>
<td></td>
<td>Average value</td>
<td>[ \frac{I}{2} \frac{-4L \cdot I}{n \cdot T} ]</td>
</tr>
<tr>
<td>i6, i7</td>
<td>RMS value</td>
<td>[ \frac{I}{2} \frac{-4L \cdot I}{n \cdot T} ]</td>
</tr>
<tr>
<td></td>
<td>Average value</td>
<td>[ \frac{I}{2} \frac{-4L \cdot I}{n \cdot T} ]</td>
</tr>
</tbody>
</table>
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Reference [13] had proposed a similar current balancing method, but it is for the HB TL DC/DC converter. Comparing between the HB and FB TL DC/DC converter, the FBTL DC/DC is more suitable for the high power applications and the modulation strategies between HB and FB TL DC/DC converter are quite different. The modulation strategy of the FBTL DC/DC converter is more complex than that of the HB TL DC/DC converter not only because the circuit structure of the FB converter is more complex also because the modulation strategy for the FBTL DC/DC converter normally needs to satisfy the wide input voltage range. In order to satisfy the wide input voltage range, the proposed modulation strategy is composed of two working patterns. More significantly, these two working patterns can both effectively balance the currents among the power devices and the transition between these two working patterns is seamless.

Figs. 3(a) and 3(b) show the operation principles of two working patterns respectively, in which \( d_{15} \) - \( d_{20} \) are driving signals of the power switches \( S_1 \) - \( S_6 \), \( d_1 \) and \( d_2 \) are duty ratios in one switching period \( T \).

![Proposed modulation strategy](image)

Fig. 3. Proposed modulation strategy. (a) Working pattern I. (b) Working pattern II.

1) Working pattern I is used for the low input voltage. In the working pattern I, the output voltage \( V_o \) is adjusted by changing the duty ratio \( d_1 \). The working pattern I operates by swapping the duty ratios for the switching pairs \( (S_1, S_6) \) and \( (S_2, S_5) \) respectively in every switching period to make the currents through the power devices balanced in every two switching periods. Therefore, the working pattern I has two operation modes as marked in Fig. 3(a) that: in the mode I as \([t_1 - t_2]\), the duty ratio of \( d_{15} \) and \( d_{16} \) are both \( d_1 \), the duty ratio of \( d_{13}, d_{12}, d_{16}, d_{17}, d_{18} \) and \( d_{20} \) are all 0.5 if neglecting the dead time. By adjusting the value of \( d_1 \), the time length of the third-level voltages \( (V_{in} \) and \(-V_{in}) \) as marked by red color in Fig. 3(a) can be changed, which would thus change the output voltage \( V_o \). For instance, if reducing \( d_1 \), the time length of the third-level voltages \( (V_{in} \) and \(-V_{in}) \) would decrease, which means that the output voltage \( V_o \) would decrease.

2) Working pattern II is used for the high input voltage when \( d_1 \) reduces to zero. In the working pattern II, the output voltage \( V_o \) is adjusted by changing the duty ratio \( d_2 \). The working pattern II operates by swapping the duty ratios for the switching pairs \( (S_1, S_6), (S_2, S_5), (S_3, S_8) \), and \( (S_4, S_7) \) respectively in every switching period to balance the currents through the power devices in every two switching periods.

Therefore, the working pattern II also has two operation modes as marked in Fig. 3(b) that: in the mode I as \([t_3 - t_4]\), the duty ratio of \( d_{25} \) and \( d_{24} \) are both 0, the duty ratio of \( d_{23} \) and \( d_{22} \) are both \( d_2 \), and the duty ratio of \( d_{20}, d_{21}, d_{23}, d_{25}, \) and \( d_{26} \) are all 0.5 if neglecting the dead time. By adjusting the duty ratio of \( d_2 \), the time length of the second-level voltages \( (V_{in}/2 \) and \(-V_{in}/2) \) as marked by blue color in Fig. 3(b) can be changed, which would thus change the output voltage \( V_o \). For instance, if reducing \( d_2 \), the time length of the second-level voltages \( (V_{in}/2 \) and \(-V_{in}/2) \) would decrease, which means that the output voltage \( V_o \) would decrease.

Fig. 4 presents the equivalent circuits of the working pattern I shown in Fig. 3(a) as an example to analyze the operation principle of the proposed strategy. The analysis of the operation principle in the working pattern II is similar to that in the working pattern I, which is not repeated here.

Stage 1 [before \( t_3 \)]: The power switches \( S_1, S_6, S_4, S_8 \) are all in on-state, so the primary voltage \( V_{ab} \) equals to \(-V_{in}/2 \) and the input power transfers to the load from \( D_2 \) and \( D_3 \). The primary current of the transformer \( i_b \) is \(-i_n/2\).

Stage 2 \([t_3 - t_4]\): At \( t_3 \), the power switches \( S_1, S_6, S_4, S_8 \) are turned off. Then the parasitic capacitors \( C_3, C_4, C_6 \) are charged and \( C_1, C_2 \) are discharged. The primary current \( i_b \) starts to increase and is not enough to provide output current, so the output rectifier diodes \( D_3, D_2, D_5, D_4 \) conduct simultaneously, which clamps both the primary and secondary voltage of the transformer at 0 V.

Stage 3 \([t_4 - t_5]\): At \( t_4 \), the voltages on \( C_3, C_4, C_6 \) increase to \( V_{in}/2 \) and the voltages on \( C_1, C_2, C_7 \) decrease to 0 V, so the primary voltage \( V_{ab} \) reaches to \( V_{in} \). Then the primary current \( i_b \) flows through \( D_1, D_2, D_3, \) and \( D_4 \), which clamps the voltage on \( S_1, S_2, S_3, \) and \( S_5 \) at 0 V. Therefore, \( S_1, S_2, S_3, \) and \( S_4 \) can be turned on with zero-voltage. During this time period, the primary current \( i_b \) increases linearly because the voltage on \( L_p \) is the input voltage \( V_{in} \).

Stage 4 \([t_5 - t_6]\): At \( t_5 \), the primary current \( i_b \) increases to 0 A, which means the current direction of \( i_b \) would change. During
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this time period, the primary current $i_p$ still increases linearly because the voltage on $L_o$ maintains $V_o$.

Stage 5 [$t_6$ - $t_7$]: At $t_6$, the primary current $i_p$ increases to the positive reflected output current whose value is $I_o/n$. Then the output rectifier diodes $D_2$ and $D_3$ are turned off, and the input power would transfer to load from $D_1$ and $D_4$.

Stage 6 [$t_7$ - $t_8$]: At $t_7$, the power switch $S_1$ is turned off. Then the parasitic capacitor $C_1$ is charged and $C_4$ is discharged.

Stage 7 [$t_8$ - $t_9$]: At $t_8$, the voltage on $C_1$ increases to $V_{o/2}$ and the voltage on $C_4$ decreases to 0 V. Then, the clamping diode $D_9$ conducts and the primary current $i_p$ flows through $D_9$, $S_2$, $S_3$, and $S_4$. During this time period, the primary voltage $V_o$ is $V_{o/2}$.

At $t_9$, the power switches $S_2$, $S_3$, and $S_4$ are turned off. The second half cycle [$t_9$ - $t_{10}$] of the mode I starts, whose analysis is similar to the first half cycle [$t_5$ - $t_9$]. The analysis of the mode II is similar to that of the mode I, which is not repeated here.

In the working pattern II shown in Fig. 3(b), [$t_5$ - $t_7$], [$t_{10}$ - $t_{14}$] and [$t_{17}$ - $t_{21}$], [$t_{24}$ - $t_{28}$] are the time intervals of the duty cycle loss in the mode I and II respectively, and these four time intervals are the same. If neglecting the quite short time intervals [$t_5$ - $t_4$], [$t_{10}$ - $t_4$], [$t_{17}$ - $t_{13}$], and [$t_{24}$ - $t_{23}$], they can be calculated by (3).

$$t_i - t_f = t_i - t_o + t_1 - t_7 = t_o - t_n = \frac{3L_v I}{nV_o}$$ (3)

Based on (3), the duty cycle loss in every switching period $T_s$ under the working pattern II namely $d_{loss, II}$ can be obtained by (4).

$$d_{loss, II} = \frac{t_i - t_f}{T_s} = \frac{t_i - t_o}{T_s} - \frac{t_1 - t_7}{T_s} = \frac{t_o - t_n}{T_s} = \frac{3L_v I}{nV_o T_s}$$ (4)

Table II presents the comparison results about the duty cycle loss under the conventional strategies and proposed strategy. From Table II, it can be observed that: 1) the duty cycle loss of the working pattern I under the proposed strategy is smaller than that of the three-level mode under the conventional strategies; 2) The duty cycle loss of the working pattern II under the proposed strategy is the same as that of the two-level mode under the CPS strategy.

B. Output Characteristics

If neglecting the effect of the dead time, the average output voltage in the working pattern I namely $V_{o, I}$ and working pattern II namely $V_{o, II}$ can be calculated by (5) and (6), respectively.

$$V_{o, I} = \frac{2}{T_s} \left( \int_{t_0}^{t_{t_I}} \frac{V_v}{n} + \int_{t_{t_I}}^{t_{t_o}} \frac{V_v}{2n} \right) = \frac{V_v}{n} \cdot (0.5 + d - 2d_{loss, I}) = \frac{V_v}{n} \cdot (0.5 + d - \frac{4L_v I}{nV_o T_s})$$ (5)

$$V_{o, II} = \frac{2}{T_s} \left( \int_{t_0}^{t_{t_{II}}} \frac{V_v}{2n} \right) - \frac{V_v}{n} \cdot (d - d_{loss, II}) = \frac{V_v}{n} \cdot (d - 3L_v I \cdot T_s)$$ (6)

C. ZVS Achievement Conditions

1) Working Pattern I

In the mode I, the zero-voltage switch-on of the power switches $S_5$ and $S_6$ is mainly determined by the reflected current from the output filter inductor. Normally, the output filter inductance is quiet large enough to make the power switches $S_5$ and $S_6$ achieve zero-voltage switch-on even at the light load. For instance, in order to ensure the zero-voltage switch-on of the power switch $S_5$ in Fig. 3(a), the energy $E_1$ is needed to discharge the capacitor $C_4$ from $V_{o/2}$ to 0 V and charge the capacitor $C_1$ from 0 V to $V_{o/2}$, whose expression can be given by (7).

$$E_1 = \frac{1}{2}L_v I^2$$ (7)
TABLE II. COMPARISON RESULTS ABOUT DUTY CYCLE LOSS

<table>
<thead>
<tr>
<th>Item</th>
<th>CPS Strategy</th>
<th>DPS Strategy</th>
<th>Proposed Strategy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Duty Cycle Loss</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Three-level mode/Working pattern I</td>
<td>$4 \frac{L}{n} \cdot \frac{V_o}{T} \cdot 2 \theta$</td>
<td>$4 \frac{L}{n} \cdot \frac{V_o}{T} \cdot 2 \theta$</td>
<td>$4 \frac{L}{n} \cdot \frac{V_o}{T} \cdot 2 \theta$</td>
</tr>
<tr>
<td>Two-level mode/Working pattern II</td>
<td>$6 \frac{L}{n} \cdot \frac{V_o}{T}$</td>
<td>$8 \frac{L}{n} \cdot \frac{V_o}{T} \cdot 2 \alpha$</td>
<td>$6 \frac{L}{n} \cdot \frac{V_o}{T}$</td>
</tr>
</tbody>
</table>

Note: $\theta$ is the phase shift time between the driving signals of $S_i$ and $(S_j, S_k)$ or the driving signals $S_i$ and $(S_6, S_8)$ in the CPS and DPS strategy. $\alpha$ is a constant overlap time between the driving signals of $S_i$ and $(S_j, S_k)$ or the driving signals $S_i$ and $(S_6, S_8)$ in the DPS strategy.

In the mode I, the energy stored in the inductor $L_o$ is used to realize the zero-voltage switch-on for the power switches $S_1$, $S_2$, $S_3$, $S_5$, $S_6$, and $S_8$. For instance, in order to achieve the zero-voltage switch-on for the power switches $S_3$, $S_5$, and $S_6$ in Fig. 3(a), the capacitors $C_3$, $C_5$, and $C_6$ need to be discharged from $V_o/2$ to $0$ V and the capacitors $C_2$, $C_4$, and $C_8$ need to be charged from $0$ V to $V_o/2$. Accordingly, the following equation (8) should be satisfied to achieve the zero-voltage switch-on of $S_1$, $S_3$, and $S_6$.

$$E_o \geq \frac{1}{2} C_o \left(\frac{V_o}{2}\right)^2 + \frac{1}{2} C_1 \left(\frac{V_o}{2}\right)^2 + \frac{1}{4} C_2 \cdot V_o^2$$

(7)

In the mode II, the reflected current from the output filter inductor is used to realize the zero-voltage switch-on for the power switches $S_1$ and $S_5$; and the energy stored in the inductor $L_o$ is used to realize the zero-voltage switch-on for the switches $S_3$, $S_6$, and $S_8$. The requirements for the power switches to achieve zero-voltage switch-on in the mode II are same as that in the operation mode I, which is not repeated here.

Therefore, based on (8), the load range of ZVS achievement in the working pattern I namely $I_{L,ZVS,I}$ can be obtained by (9).

$$I_{L,ZVS} \geq n \cdot V_o \cdot \sqrt[3]{\frac{3C_2}{2L_o}}$$

(9)

2) Working Pattern II

In the mode I, the zero-voltage switch-on of power switches $S_3$, $S_5$, and $S_6$ is mainly determined by the reflected current from the output filter inductor, Normally, the output filter inductance is quiet large enough to make the power switches $S_3$, $S_5$, and $S_6$ achieve zero-voltage-switch-on even at the light load. For instance, in order to achieve the zero-voltage switch-on of the power switch $S_3$ in Fig. 3(b), the energy $E_2$ is needed to discharge the capacitor $C_3$ from $V_o/2$ to $0$ V and charge the capacitor $C_2$ from $0$ V to $V_o/2$, whose expression can be given by (10).

$$E_2 \geq \frac{1}{2} C_3 \left(\frac{V_o}{2}\right)^2 + \frac{1}{2} C_2 \left(\frac{V_o}{2}\right)^2 + \frac{1}{4} C_1 \cdot V_o^2$$

(10)

In the mode II, the energy stored in the inductor $L_o$ is used to achieve the zero-voltage switch-on for the power switches $S_3$, $S_5$, and $S_6$. Therefore, based on (11), the load range of ZVS achievement in the working pattern I namely $I_{L,ZVS,II}$ can be obtained by (12).

$$I_{L,ZVS,II} \geq n \cdot V_o \cdot \sqrt[3]{\frac{3C_2}{2L_o}}$$

(12)

Table III presents the comparison results about the ZVS range under the conventional strategies and proposed strategy. From Table III, it can be observed that: 1) the ZVS range of the working pattern II under the proposed strategy is the same as that of the three-level mode under the conventional strategies; 2) the ZVS range of the working pattern I under the proposed strategy is little smaller than that of the three-level mode under the conventional strategies because the conventional strategies could realize the ZVS of one more power switch by increasing the duty cycle loss.

D. Currents on Power Devices

Fig. 5 shows the currents flowing through the primary power devices under the proposed strategy. From Fig. 5, it can be observed that: 1) under the working pattern I, the currents on the outer power switches $i_1$, $i_4$, $i_5$, $i_8$, on the inner power switches $i_2$, $i_3$, $i_6$, $i_7$, and on the clamping diodes $i_{D21}$, $i_{D20}$, $i_{D11}$, $i_{D12}$ are the same besides phase difference, respectively; 2) under the working pattern II, the RMS and average values of $i_2$, $i_3$, $i_6$, $i_7$ are also the same respectively, and $i_{D20}$, $i_{D21}$, $i_{D11}$, $i_{D12}$ are the same besides phase difference. Based on the above analysis, it can be concluded that the two working patterns of the proposed strategy can both balance the currents among the power switches and clamping diodes.

Table IV presents the calculation equations about the RMS and average values of $i_1 - i_8$ and $i_{D20} - i_{D12}$ under the proposed strategy according to Fig. 5.
TABLE III. COMPARISON RESULTS ABOUT ZVS ACHIEVEMENT CONDITIONS

<table>
<thead>
<tr>
<th>Item</th>
<th>CPS Strategy</th>
<th>DPS Strategy</th>
<th>Proposed Strategy</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZVS Range</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Three-level mode/</td>
<td>( n \cdot V_c \cdot \frac{C}{L} )</td>
<td>( n \cdot V_c \cdot \frac{C}{L} )</td>
<td>( n \cdot V_c \cdot \frac{C}{2 \cdot L} )</td>
</tr>
<tr>
<td>Working pattern I</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Two-level mode/</td>
<td>( n \cdot V_c \cdot \frac{C}{L} )</td>
<td>( n \cdot V_c \cdot \frac{C}{L} )</td>
<td>( n \cdot V_c \cdot \frac{C}{L} )</td>
</tr>
<tr>
<td>Working pattern II</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

According to the equations in Tables I, IV and circuit parameters in Appendix, the theoretical comparison results about the currents on the primary power devices are presented in Figs. 6 - 8, in which \( i_{Srms_{three\_DPS}} \) - \( i_{Srms_{three\_DPS}} \) and \( i_{Irms_{two\_DPS}} \) - \( i_{Irms_{two\_DPS}} \) are the RMS value, average value of the currents on the power switches \( (S_i, D_i) \) - \( (S_n, D_n) \) under the three-level and two-level mode of the DPS strategy respectively; \( i_{D9\_rms\_three\_DPS} \) - \( i_{D12\_rms\_three\_DPS} \), \( i_{D9\_avg\_three\_DPS} \) - \( i_{D12\_avg\_three\_DPS} \), \( i_{D9\_rms\_two\_DPS} \) - \( i_{D12\_rms\_two\_DPS} \), \( i_{D9\_avg\_two\_DPS} \) - \( i_{D12\_avg\_two\_DPS} \) are the RMS value, average value of the currents on the clamping diodes \( D_0 - D_{12} \) under the three-level and two-level mode of the DPS strategy respectively; \( i_{S9\_rms} \) - \( i_{S12\_rms} \), \( i_{S9\_avg} \) - \( i_{S12\_avg} \) and \( i_{I9\_rms} \) - \( i_{I12\_rms} \), \( i_{I9\_avg} \) - \( i_{I12\_avg} \) are the RMS value, average value of the currents on the power switches \( (S_i, D_i) \) - \( (S_n, D_n) \) under the working pattern I and II of the proposed strategy respectively; \( i_{D9\_rms_{three\_DPS}} \) - \( i_{D12\_rms_{three\_DPS}} \), \( i_{D9\_avg_{three\_DPS}} \) - \( i_{D12\_avg_{three\_DPS}} \), \( i_{D9\_rms_{two\_DPS}} \) - \( i_{D12\_rms_{two\_DPS}} \), \( i_{D9\_avg_{two\_DPS}} \) - \( i_{D12\_avg_{two\_DPS}} \) are the RMS value, average value of the currents on the clamping diodes \( D_0 - D_{12} \) under the working pattern I and II of the proposed strategy respectively.

From Figs. 6 - 8, it can be observed that: 1) for the currents on the outer power switches \( (i_1, i_4, i_5, i_8) \) in Fig. 6, the RMS and average value of \( i_s, i_b \) are larger than that of \( i_1, i_4 \) under the conventional strategy; but the RMS and average value of them become the same under the proposed strategy; 2) for the currents on the inner power switches \( (i_2, i_3, i_6, i_7) \) in Fig. 7, the RMS value of them are the same but the average value of \( i_b, i_l \) are larger than that of \( i_2, i_3 \) under the conventional strategy; the RMS and average value of them become the same under the proposed strategy; 3) for the currents on the clamping diodes \( (i_{D9}, i_{D10}, i_{D11}, i_{D12}) \) in Fig. 8, the RMS and average value of \( i_{D9}, i_{D10} \) are larger than that of \( i_{D9_{avg}}, i_{D12} \) under the conventional strategy; but the RMS and average value of them become the same under the proposed strategy; 4) the differences among the currents on outer power switches, inner power switches, and clamping diodes under the conventional strategy would become larger with the increasing of the output power.
### Table IV. Theoretical Equations about RMS and Average Values of Currents on Primary Power Devices Under Proposed Strategy

<table>
<thead>
<tr>
<th>Working pattern I</th>
<th>Working pattern II</th>
</tr>
</thead>
<tbody>
<tr>
<td>$i_1, i_3, i_2, i_4$</td>
<td>$i_1, i_3, i_2, i_4$</td>
</tr>
<tr>
<td><strong>RMS value</strong></td>
<td><strong>RMS value</strong></td>
</tr>
<tr>
<td>$\frac{1}{4} \cdot (1+2 \cdot \text{d}) \cdot 4 \cdot L \cdot i_1' \cdot \sqrt{\frac{4}{n'} \cdot 3 \cdot V_{in} \cdot n \cdot T}$</td>
<td>$\frac{1}{2} \cdot (1- \text{d}) \cdot 6 \cdot L \cdot i_1' \cdot \sqrt{\frac{2}{n'} \cdot V_{in} \cdot n \cdot T}$</td>
</tr>
<tr>
<td><strong>Average value</strong></td>
<td><strong>Average value</strong></td>
</tr>
<tr>
<td>$\frac{1}{4} \cdot (1+2 \cdot \text{d}) \cdot 2 \cdot L \cdot i_1' \cdot \sqrt{\frac{4}{n'} \cdot V_{in} \cdot n \cdot T}$</td>
<td>$\frac{1}{2} \cdot (1- \text{d}) \cdot 3 \cdot L \cdot i_1' \cdot \sqrt{\frac{2}{n'} \cdot V_{in} \cdot n \cdot T}$</td>
</tr>
</tbody>
</table>

| $i_{in}, i_{on}, i_{on}, i_{on}$ | $i_{in}, i_{on}, i_{on}, i_{on}$ |
| **RMS value** | **RMS value** |
| $\frac{1}{n} \cdot \frac{1-2 \cdot \text{d}}{4}$ | $\frac{1}{n} \cdot \frac{1-2 \cdot \text{d}}{2}$ |
| **Average value** | **Average value** |
| $\frac{1}{n} \cdot \frac{1-2 \cdot \text{d}}{4}$ | $\frac{1}{n} \cdot \frac{1-2 \cdot \text{d}}{2}$ |

---

**E. Implementation of Proposed Strategy**

For the working pattern I, the duty cycle $d_1$ calculated by the control loop would be changed in every two switching periods to adjust the output voltage $V_o$ in the practical application. As shown in Fig. 3(a), in the first switching period, the calculated $d_1$ is set for the driving signals of the power switches $S_1$, $S_2$ and the duty cycle 0.5 minus the dead time divided by $T_s$ is set for the driving signals of the power switches $S_6$, $S_3$, $S_4$, $S_5$, and $S_5$ in the second switching period, the calculated $d_1$ is for the driving signals of the power switches $S_1$, $S_6$ and the duty cycle 0.5 minus the dead time divided by $T_s$ is set for the driving signals of the power switches $S_3$, $S_4$, $S_5$, $S_6$, and $S_5$. With the increasing of the input voltage, $d_1$ would decrease to maintain the output voltage at the constant value. When $d_1$ reduces to the zero, then the working pattern II starts to be utilized and $d_1$ is kept at zero, so the transition between the two working patterns is seamless. For the working pattern II, the duty cycle $d_2$ calculated by the control loop would be changed in every two switching periods to adjust the output voltage $V_o$ in the practical application. As shown in Fig. 3(b), in the first...
switching period, the calculated $d_2$ is set for the driving signals of the power switches $S_2$, $S_3$ and the duty cycle 0.5 minus the dead time divided by $T_i$ is set for the driving signals of the power switches $S_4$, $S_6$, $S_7$, and $S_8$; in the second switching period, the calculated $d_2$ is set for the driving signals of the power switches $S_6$, $S_7$ and the duty cycle 0.5 minus the dead time divided by $T_i$ is set for the driving signals of the power switches $S_6$, $S_8$, $S_8$, and $S_8$.

Under the steady operations, the duty cycle $d_1$ and $d_2$ calculated by the control algorithms are adjusted in every two switching periods to control the output voltage and balance the currents on the primary power devices. Under the dynamic changes, the duty cycle $d_1$ and $d_2$ calculated by the control algorithms can be adjusted in every switching period to control the converter, which would thus make dynamic responses as the conventional modulation strategies, because both working pattern I and II have the feature that the mode I and II (shown in Fig. 3) can be utilized alone separately to control the output voltage and have the same output characteristics.

Fig. 9 presents the diagram about the implementation of the proposed modulation strategy, in which the conventional proportional-integral PI control algorithm is utilized to calculate duty cycles $d_1$ and $d_2$. As shown in Fig. 9, the working pattern I is used for the low input voltage by adjusting the duty cycle $d_1$ from maximum value $d_{1,\text{max}}$ to 0; when $d_1$ decreases to 0 due to the increasing of the input voltage, the working pattern II would be used for the higher input voltage by adjusting the duty cycle $d_2$.

Fig. 9. Diagram about implementation of proposed control strategy.

V. EXPERIMENTAL VERIFICATION

In order to verify the proposed modulation strategy, a 1.5 kW experimental prototype is established, whose circuit parameters are presented in Appendix. Figs. 10(a) and 10(b) present the experimental set-up and hardware of FBTL DC/DC converter.

Figs. 11(a) and 10(b) present the experimental results including the primary voltage $V_{ab}$, output voltage $V_o$, primary current $i_p$, and current through the output filter inductor $i_{oL}$ under the working pattern I and II.

Fig. 11. Experimental results including $V_{ab}$, $V_o$, $i_p$, and $i_{oL}$ ($V_o = 50$ V, $P_o = 1.5$ kW). (a) Working pattern I of proposed strategy ($V_o = 350$ V). (b) Working pattern II of proposed strategy ($V_o = 550$ V).

Fig. 12 presents experimental results including the voltages and currents on the input capacitors ($V_1$, $V_2$, $i_{c1}$, and $i_{c2}$) when the output voltage $V_o$ is 50 V and output power $P_o$ is 1.5 kW. From Fig. 12, it can be observed that: under the proposed modulation strategy, 1) the voltages on the input capacitors ($V_1$, $V_2$) are balanced; 2) the currents on the input capacitors ($i_{c1}$, $i_{c2}$) are also balanced, and RMS of $i_{c1}$, $i_{c2}$ under the working pattern I ($V_o = 350$ V) and II ($V_o = 550$ V) are about 5.1 A and 4.5 A respectively.

Fig. 12. Experimental results including $V_1$, $V_2$, $i_{c1}$, and $i_{c2}$ ($V_o = 50$ V, $P_o = 1.5$ kW). (a) Working pattern I of proposed strategy ($V_o = 350$ V). (b) Working pattern II of proposed strategy ($V_o = 550$ V).

Figs. 13(a) - 13(c) show the ZVS achievement performances of the power switches $S_1$, $S_5$, and $S_6$ under the working pattern I, in which it can be observed that $S_1$, $S_5$, and $S_6$ realize zero-voltage switching-on. Figs. 14(a) - 14(b) present the ZVS achievement performances of the power switches $S_2$ and $S_7$ under the working pattern II, in which it can be observed that $S_2$ and $S_7$ realize zero-voltage switching-on. The ZVS achievement performances of other power switches are similar to the results in Figs. 13 - 14, which are not repeated here.
Fig. 13. ZVS achievement performances under working pattern I ($V_o = 350 V$, $V_i = 50 V, P_o = 1.5 kW$). (a) $S_1$, (b) $S_2$, (c) $S_6$. 
Note: In Fig. 13, $V_{DS_{S1}}, V_{DS_{S2}}, V_{DS_{S6}}$ are the drain-source voltage of $S_1, S_2, S_6$, $V_{GS_{S1}}, V_{GS_{S2}}, V_{GS_{S6}}$ are the gate-source voltage of $S_1, S_2, S_6$.

Fig. 14. ZVS achievement performances under working pattern II ($V_o = 550 V$, $V_i = 50 V, P_o = 1.5 kW$). (a) $S_5$, (b) $S_7$. 
Note: In Fig. 14, $V_{DS_{S5}}, V_{DS_{S7}}$ are the gate-source voltage of $S_5, S_7$, $V_{GS_{S5}}, V_{GS_{S7}}$ are the drain-source voltage of $S_5, S_7$.

Figs. 15 - 17 present the experimental results about the clamping diode currents $i_{DS_4}, i_{DS_8}, i_{DS_{10}}, i_{DS_{12}}$ outer switch currents $i_1, i_4, i_5, i_8$, and inner switch currents $i_2, i_3, i_6, i_7$, respectively, under the DPS strategy and proposed strategy.

Fig. 15. Experimental results of clamping diode currents $i_{DS_4}, i_{DS_8}, i_{DS_{10}}, i_{DS_{12}}$ ($V_o = 50 V, P_o = 1.5 kW$). (a) Three-level mode of DPS strategy ($V_o = 350 V$), (b) Working pattern I of proposed strategy ($V_o = 350 V$), (c) Two-level mode of DPS strategy ($V_o = 550 V$), (d) Working pattern II of proposed strategy ($V_o = 550 V$).

Fig. 16. Experimental results of outer switch currents $i_1, i_4, i_5, i_8$ and $i_7$ ($V_o = 50 V, P_o = 1.5 kW$). (a) Three-level mode of DPS strategy ($V_o = 350 V$), (b) Working pattern I of proposed strategy ($V_o = 350 V$), (c) Two-level mode of DPS strategy ($V_o = 550 V$), (d) Working pattern II of proposed strategy ($V_o = 550 V$).

Fig. 17. Experimental results of inner switch currents $i_2, i_3, i_6, i_7$ ($V_o = 50 V, P_o = 1.5 kW$). (a) Three-level mode of DPS strategy ($V_o = 350 V$), (b) Working pattern I of proposed strategy ($V_o = 350 V$), (c) Two-level mode of DPS strategy ($V_o = 550 V$), (d) Working pattern II of proposed strategy ($V_o = 550 V$).

From Figs. 15 - 17, it can be observed that: 1) the clamping diode currents $i_{DS_4}, i_{DS_8}, i_{DS_{10}}, i_{DS_{12}}$, outer switch currents $i_1, i_4, i_5, i_8$, and inner switch currents $i_2, i_3, i_6, i_7$ are unbalanced under the DPS strategy; but 2) by utilizing the proposed strategy, the clamping diode currents $i_{DS_4}, i_{DS_8}, i_{DS_{10}}, i_{DS_{12}}$, the outer switch currents $i_1, i_4, i_5, i_8$, and inner switch currents $i_2, i_3, i_6, i_7$ can be balanced; 3) the experimental results shown in Figs. 15 - 17 are consistent with the theoretical analysis in Section II and IV-D.

Fig. 18 shows the experimental results about transition performance between the two working patterns, which includes the input voltage ($V_i$), voltages on the two input capacitors ($V_1, V_2$), and ac component of the output voltage $\tilde{V}_o$. In Fig. 18, the input voltage steps up from 300 V to 550 V and is finally set back to 300 V when the output voltage $V_o$ is 50 V and output power $P_o$ is 1.5 kW. From Fig. 18, it can be observed that there is no abnormal voltage spike on the two input capacitors during the transitions between the two working patterns.

Fig. 18. Experimental results about transition performance between two working patterns when $V_i = 50 V$ and $P_o = 1.5 kW$. 

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Normally, the conduction power loss and thermal stress on the power device is closely related to the current flowing through it. Figs. 19 and 20 present the comparison results about the loss breakdown and thermal stresses of the primary power devices between the conventional strategy and proposed strategy, respectively.

From Fig. 19, it can be observed that: 1) under the DPS strategy, the conduction losses among the inner power switches are balanced because the RMS values of the currents through the inner power switches are almost the same and MOSFET is used for the primary power switches in the built prototype, but the conduction losses among the outer power switches and clamping diodes are unbalanced; 2) after utilizing the proposed strategy, the conduction losses among the outer power switches, inner power switches, and clamping diodes become balanced. It needs to be mentioned that: if IGBT is used for the power switches, the conduction losses among the inner power switches would become unbalanced under the conventional strategy because the average values of the currents through the inner power switches are different. These power loss imbalances under the conventional strategy would result in the thermal stress imbalance among the primary power devices as shown in Fig. 20. Under the DPS strategy, the thermal stress of \( D_5, D_{10} \) are higher than that of \( D_{11}, D_{12} \) and the thermal stress of \( (S_1, D_1), (S_6, D_4) \) are lower than that of other power switches as shown in Figs. 20(a) and 20(c), which means that the thermal stresses among the power switches and clamping diodes are unbalanced. After utilizing the proposed strategy, the thermal stresses among the clamping diodes \( D_9 - D_{12} \), outer power switches \( (S_1, D_1), (S_6, D_4), (S_5, D_3), (S_6, D_4) \), and inner power switches \( (S_5, D_3), (S_6, D_4), (S_7, D_7) \) become balanced as shown in Figs. 20(b) and 20(d).

![Fig. 19. Loss breakdown of primary power devices \( (V_o = 50 \text{ V} \text{ and } P_o = 1.5 \text{ kW}) \). (a) Working pattern I \( (V_o = 350 \text{ V}) \). (b) Working Pattern II \( (V_o = 550 \text{ V}) \).](image)

Fig. 20. Experimental results about thermal stresses on primary power devices by FLIR thermal camera. \( (V_o = 50 \text{ V}, P_o = 1.5 \text{ kW}, \text{Ambient temperature} = 25^\circ \text{C}) \). (a) Three-level mode of DPS strategy \( (V_o = 350 \text{ V}) \). (b) Working pattern I of proposed strategy \( (V_o = 350 \text{ V}) \). (c) Two-level mode of DPS strategy \( (V_o = 550 \text{ V}) \). (d) Working pattern II of proposed strategy \( (V_o = 550 \text{ V}) \).

Fig. 21 shows the experimental comparison results about efficiencies between the conventional strategy and proposed strategy. From Fig. 21, it can be observed that: 1) the efficiencies under the working pattern I of the proposed strategy are almost the same as that under the three-level mode of the DPS strategy; 2) the efficiencies under the working pattern II of the proposed strategy are slightly lower than that under the three-level mode of the DPS strategy. Fig. 22 presents the loss breakdown of main components in the FBTL DC/DC converter under the conventional DPS strategy and proposed strategy when \( P_o \) is 1.5 kW. From Fig. 22, it can be observed that: 1) the conduction losses of the primary power switches under the DPS strategy and proposed strategy are almost the same; 2) the DPS and proposed strategy both realize ZVS, and the switching-off losses are almost the same, so the switching losses of the primary power switches would be almost the same; 3) the power losses of the transformer under the two strategies would be almost the same because the primary voltage and primary voltage on the transformer are almost the same; 4) the secondary components’ power losses would be almost the same because the secondary voltage and current are almost the same.

It needs to be mentioned that: with the decreasing of the output power, the conduction losses of the primary power devices under the working pattern I of proposed strategy and three-level mode of DPS strategy are almost the same, but the conduction losses of the primary power devices under the working pattern II of proposed strategy become higher than that under the two-level mode of DPS strategy, which results in that the converter’s efficiencies under the working pattern II become lower than that under the two-level mode with the decreasing of the output power as shown in Fig. 21. The reason causing lower efficiencies is that MOSFET is used for the power switches in the established prototype. When using MOSFET, the primary current \( i_t \) flows through the two body diodes of the power switches instead of the power switches themselves during the free-wheeling time periods \( (t_1 < t_5), (t_6 < t_{10}), (t_{10} < t_1), \) and \( (t_{17} < t_{17}) \) in Fig. 5(b) under the working pattern II of proposed strategy. With the decreasing of the output power, the free-wheeling time periods would become longer, which would thus increase the conduction losses in comparison with the DPS strategy because the conduction loss of power switch is lower than that of its body diode when the same current flows through them \([27]\). However, when IGBT
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is used for the power switches to satisfy the higher voltage and power applications, the primary current $i_p$ would both flow through the two power switches and two body diodes during the free-wheeling time periods under the two-level mode and working pattern II.

![Fig. 21. Experimental comparison results about efficiencies.](image)

![Fig. 22. Comparison results about loss breakdown when Total loss. Output rectifier diodes' loss. 6. Output filter inductor’s loss. 8. PCB loss. 10. switching loss. 3. Transformer’s core loss. 4. Transformer’s copper loss. 5. Note: 1. Primary power devices' conduction loss. 2. Primary power switches’ switching loss. 3. Transformer’s core loss. 4. Transformer’s copper loss. 5. Output rectifier diodes’ loss. 6. Output filter inductor’s loss. 8. PCB loss. 10. Total loss. Fig. 22. Comparison results about loss breakdown when $P_o = 50 V$, and $P_o = 1.5 kW$. (a) $V_{in} = 350 V$. (b) $V_{in} = 550 V$.](image)

The derivation of the current expressions in Table IV are presented as below based on Fig. 5.

1) Under working pattern I:

$$
i_{s_{in}} = i_{s_{out}} = i_{s_{in}} = i_{s_{out}} = \sqrt{\frac{\int^{T} V_L \frac{d}{n} \cdot dt + \frac{L}{n} \frac{d}{n} \cdot dt + \frac{L}{n} \frac{d}{n} \cdot dt}{2 \cdot T}}$$

$$
i_{s_{in}} = i_{s_{out}} = i_{s_{in}} = i_{s_{out}} = \frac{L \cdot (1 + 2 \cdot d)}{V \cdot n \cdot T}$$

$$
i_{s_{in}} = i_{s_{out}} = i_{s_{in}} = i_{s_{out}} = \frac{2 \cdot L \cdot I \cdot I}{V \cdot n \cdot T}$$

$$
i_{s_{in}} = i_{s_{out}} = i_{s_{in}} = i_{s_{out}} = \frac{2 \cdot L \cdot I \cdot I}{V \cdot n \cdot T}$$

$$
i_{s_{in}} = i_{s_{out}} = i_{s_{in}} = i_{s_{out}} = \frac{2 \cdot L \cdot I \cdot I}{V \cdot n \cdot T}$$

![Image](image)

VI. CONCLUSION

This paper points out that there exists the current imbalance issue of primary power devices under the conventional strategies in the FBTL DC/DC converter based on the detailed analysis. Then, in order to eliminate these current imbalances, a new modulation strategy is proposed for the FBTL DC/DC converter. In addition, the proposed strategy is composed of two working patterns, which can not only realize zero-voltage switching (ZVS) but also satisfy the wide input voltage range. The transition between these two working patterns is seamless.

More significantly, these two working patterns of the proposed strategy can both effectively balance the currents among power switches and clamping diodes, which would thus improve the reliability of the FBTL DC/DC converter by balancing the thermal stresses among the power switches and clamping diodes. Finally, a 1.5 kW experimental prototype is established, and the experimental results verify that the current difference and thermal stress difference among the inner power switches, outer power switches, and clamping diodes are almost zero under the proposed strategy.

APPENDIX

See Table V.

<table>
<thead>
<tr>
<th>Component</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Switches $S_1 - S_4$</td>
<td>SPW47N60C3</td>
</tr>
<tr>
<td>Power Diodes $D_1 - D_6$</td>
<td>DSE130-10AR</td>
</tr>
<tr>
<td>Rectifier Diodes $D_1 - D_4$</td>
<td>MBR40250TG</td>
</tr>
<tr>
<td>Turns Ratio of Transformer $T_i$ ($n_1 : n_2$)</td>
<td>25 : 8</td>
</tr>
<tr>
<td>Added inductor plus Leakage Inductor $L_i$ ($\Omega$H)</td>
<td>47.7</td>
</tr>
<tr>
<td>Input Capacitors $C_1$ and $C_2$ ($\mu$F)</td>
<td>470</td>
</tr>
<tr>
<td>Flying Capacitors $C_1$ and $C_2$ ($\mu$F)</td>
<td>47</td>
</tr>
<tr>
<td>Output Filter Capacitor $C_3$ ($\mu$F)</td>
<td>140</td>
</tr>
<tr>
<td>Output Filter Inductor $L_1$ ($\Omega$H)</td>
<td>10AR</td>
</tr>
<tr>
<td>Switching Frequency (kHz)</td>
<td>50</td>
</tr>
</tbody>
</table>

![Table V. Parameters of Experimental Prototype](image)
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\[
i_{\text{in, \text{avg}}}=i_{\text{in, \text{avg}}}=i_{\text{in, \text{avg}}}=i_{\text{in, \text{avg}}}=rac{\int_{0}^{T} i_{\text{in}}(t) \, dt}{T}
\]

\[
i_{\text{in, \text{avg}}}=i_{\text{in, \text{avg}}}=i_{\text{in, \text{avg}}}=i_{\text{in, \text{avg}}}=rac{\int_{0}^{T} i_{\text{in}}(t) \, dt}{T}
\]

2. Under working pattern II:

\[
i_{\text{in, \text{avg}}}i_{\text{in, \text{avg}}}i_{\text{in, \text{avg}}}i_{\text{in, \text{avg}}}=rac{\int_{0}^{T} i_{\text{in}}(t) \, dt}{T}
\]

\[
i_{\text{in, \text{avg}}}i_{\text{in, \text{avg}}}i_{\text{in, \text{avg}}}i_{\text{in, \text{avg}}}=rac{\int_{0}^{T} i_{\text{in}}(t) \, dt}{T}
\]

\[
i_{\text{in, \text{avg}}}i_{\text{in, \text{avg}}}i_{\text{in, \text{avg}}}i_{\text{in, \text{avg}}}=rac{\int_{0}^{T} i_{\text{in}}(t) \, dt}{T}
\]

REFERENCES


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