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A Novel Submodule Voltage Balancing Scheme for Modular Multilevel Cascade Converter–Double-Star Chopper-Cells (MMCC-DSCC) Based STATCOM

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ABSTRACT A novel capacitor voltage balancing scheme for modular multilevel cascade converter—double-star chopper-cells (MMCC-DSCC)-based STATCOM is proposed in this paper. Compared with the conventional software voltage balancing methods, the proposed scheme has three main advantages. First, only six voltage sensors are needed, and other voltage sensors have been removed. Then, the control framework can be simple without sort and select process, or some balancing control loops. Additional delay process caused by the sampling and control signals transmission is also mitigated. Finally, the faster capacitor balancing speed can be obtained. In addition, compared with some other hardware voltage balancing schemes, there are superior characteristics in terms of the reduced number of switches and only the popular power modules in the additional units are applied. For these additional modules, the parameters design guide of the proposed scheme has been discussed. Verified results from the 13-level simulated system and 9-level experimental platform for the MMCC-DSCC based STATCOM show the effectiveness of the proposed scheme. By the proposed scheme, both DC capacitor voltage balancing control and reactive power compensation are simultaneously realized for the MMCC-DSCC-based STATCOM even in balanced and unbalanced load.

INDEX TERMS Diode-clamped circuit, double-star chopper-cell (DSCC), modular multilevel cascade converter (MMCC), voltage balancing, STATCOM.

I. INTRODUCTION

With the development of medium and high voltage converters, it raises a series of harsh requirements for the high-power converters. Modular Multilevel Cascaded Converter (MMCC) has many advantages such as modularity, scalability, high fault-tolerant ability, and so on [1], [2]. Consequently, MMCC has been considered as one of the most attractive topologies for HVDC [3]–[5], high-voltage voltage source converter (VSC) [6], [7], active power

filter (APF) [8], [9], STATCOM [10], energy storage system [11], [12], and so on.

As one of the most important applications for reactive power compensation, Modular Multilevel Cascade Converter—Double-Star Chopper-Cells (MMCC-DSCC) based STATCOM is gaining much more attention to generate the dynamic reactive power, improve power factor and power quality of grid [13], [14]. For the STATCOM, a lot of studies have been conducted on various improvements about the operation performance [15]–[17].

For MMCC-DSCC based STATCOM, the capacitor voltage balancing control for the floating submodules (SMs)

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in each arm remains to be a challenging issue, which is a common problem in the multilevel converters [18]. The mainstream of the balancing method can be divided into three categories, an additional injection of modulation wave for each SM, voltage sorting and select methods, and hardware balancing schemes.

For the first category, reference [19]–[22] inject an additional component to the modulation wave of each module according to the voltage derivation of capacitors from the voltage reference. Reference [23] reveals the quantitative relation between the capacitor voltage of SM and other operating parameters. Based on this, the additional injection is calculated and injected to balance the capacitor voltages according to the equation derived in this paper. Another voltage balancing method switching at grid frequency is proposed [24]. By assigning the low-frequency pulses with different pulse widths, the charges of the capacitor are controlled for keeping the capacitor voltage balancing in MMCC-DSCC. Furthermore, reference [25] manages to decouple the SM capacitor voltages balancing process from the DC bus voltage balancing. The SM voltage is controlled with a better result than traditional balancing control methods. However, these methods introduce the feedforward of capacitor voltages in the modulation, which lowers the voltage utilization of modulation wave [26].

For the second category, reference [27] propose the hierarchical control method. All SMs in one arm are grouped, and the sorting algorithm of the voltage balancing in each group is implemented in a decentralized control unit, and the balancing between different groups is realized by an additional injection component. To lower the computation burden of conventional model predictive control (MPC) method reference [28] and [29] propose an improved MPC based sorting and balancing approach which reserves the system performance, especially in high voltage systems. On the basis of these two papers, a priority sorting approach based on simplified MPC is proposed for MMCC in reference [30]. Reference [31] proposes an improved balancing approach based on space vector pulse width modulation (SVPWM). This method simplifies the complexity of balancing control by avoiding the sorting algorithm of all the voltages in one arm. The comparison between different modulators is further performed [32]. It also discusses the priority of each modulator. However, the relationship between sorting frequency and switching is not discussed in detail. Therefore, an adaptive method is proposed to achieve a trade-off between the switching losses and the balancing effect through closed-loop control of the alternating number of the SMs [33]. Reference [34] further proposes an improved balancing method based on the estimation of the current direction, which reduces the current sensors. Despite the flexibility and widely application of software balancing methods, the number of voltage sensors, the extra calculation burden and the signal delay caused by sampling and transmission is still the disadvantage of the software balancing methods.

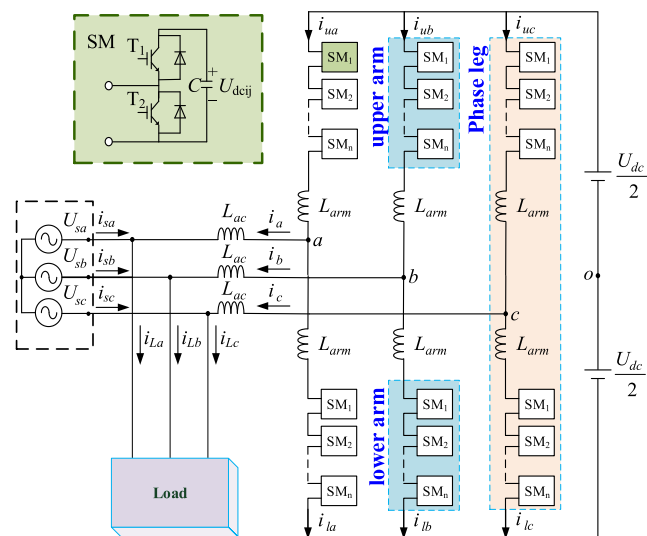


FIGURE 1. The topology of MMCC-DSCC.

In order to decrease the number of voltage sensors and reduce the influence of control delay, hardware balancing methods are gaining popularity [35]–[39]. A simple and low-loss capacitor static voltage balancing method based on self-power supplies is adopted in [35]. Considering the influence of self-power supplies on capacitor voltages, this method can keep the capacitor static voltage balanced by controlling the input characteristic of the self-power supplies. However, this method increases system cost with an additional controller on self-power supplies. In [36], a diode-clamped MMCC topology is proposed, the balancing control between the first and the last module in each arm is realized through an additional transformer. The control of the additional transformer requires a certain resource for this control system, and this will enlarge the volume of the whole device. Based on this paper, reference [37] proposes a parallel-connected improved diode-clamped topology where each arm is composed of two parallel clusters. The rated current of the topology also increases at the same time. However, the structure is much more complex where more switches are needed. In [38], a voltage balancing topology with fault ride-through ability is proposed. Although this topology can operate under DC fault and only need only 3 voltage sensors, the structure is a little complicated. Besides, the power exchange between the upper and the lower arm through hardware may lead to bigger power loss in the additional circuits. Another novel local balancing topology, especially for hybrid SM of half-bridge and full-bridge, is proposed in [39]. For the two adjacent modules, the voltage balancing can be realized within them. It is noted that this presented topology has increased power capacity and the fault ride-through ability. However, only half of the voltage sensors are reduced, and more switches are needed.

In order to achieve SM capacitor voltage balancing control, a novel MMCC-DSCC topology is proposed. It can significantly reduce the number of SM voltage sensors and

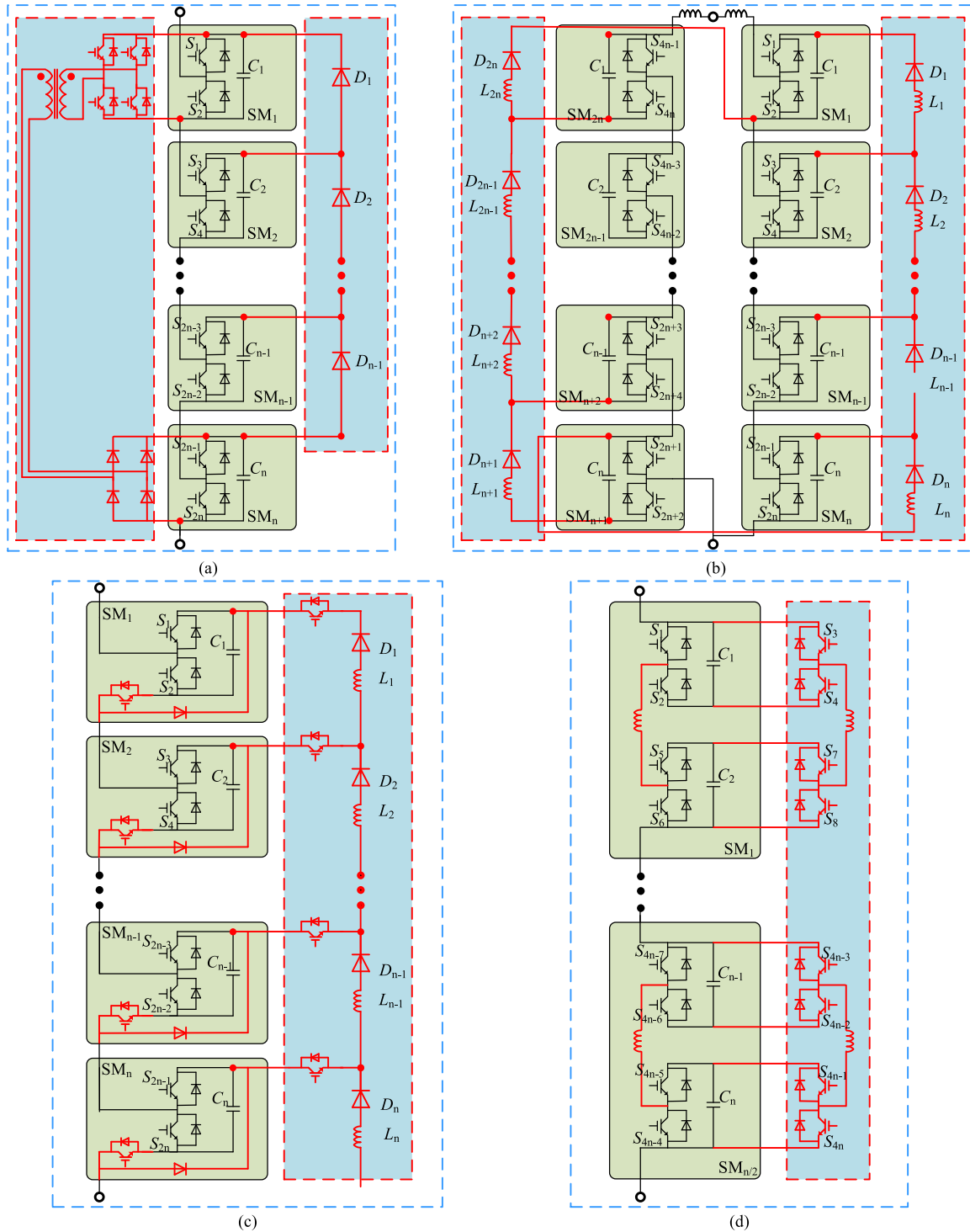


FIGURE 2. Conventional MMCC-DSCC topologies for SM voltage balancing in each arm. (a) The presented diode-clamped topology [36], (b) Parallel-connected diode-clamped topology [37]. (c) Balancing topology with fault ride-through ability [38]. (d) Local voltage balancing topology with increased power capacity [39].

mitigate additional delay process caused by the sampling and control signals transmission. The rest of the paper is organized as follows. In Section II, the proposed topology and its working principle are described, and some comparisons with conventional schemes are presented. Section III introduces

its modeling and control method. The parameters selection guide of the proposed scheme and cost analysis are discussed in Section IV. Simulations and experimental results verify the effectiveness proposed topology in Section V and Section VI. The conclusion is presented in Section VII.

II. DESCRIPTION OF THE PROPOSED MMCC-DSCC

In this section, firstly, some conventional topologies for voltage balancing are presented. Then, the proposed scheme and working principle are described. Finally, detailed comparison results are presented.

The topology of MMCC-DSCC is shown in Fig. 1. It is composed of three identical phase legs, each of which includes the upper arm and the lower arm. The inductor L_{arm} is series-connected in each arm, each of which contains n modules. The output terminal of each phase leg is connected to the grid through a filter inductor L_{ac} . U_{sa} , U_{sb} , and U_{sc} are three-phase grid voltages. i_{La} , i_{Lb} , and i_{Lc} are the three-phase currents of the load, i_a , i_b , and i_c are output currents of MMCC and i_{sa} , i_{sb} , and i_{sc} are currents of the grid. i_{uj} and i_{lj} ($j = a, b, c$) are the output currents of the upper and the lower arm.

A. CONVENTIONAL TOPOLOGIES

Four main conventional MMC topologies for SM voltage balancing in each arm are shown as Fig. 2 [36]–[39].

Fig. 2 (a) shows the presented diode-clamped topology [36], where some additional transformers must be added to achieve SM voltage balancing. Then, Fig. 2 (b) describes the parallel-connected diode-clamped topology where each arm is composed of two parallel clusters [37]. In addition, a novel topology with SM voltage self-balancing and DC fault ride-through ability is described in Fig. 2 (c) [38], where the full bridge SMs are removed from the original topology. Finally, a local voltage balancing topology with bigger power capacity is presented in Fig. 2 (d) [39].

B. THE PROPOSED MMCC-DSCC TOPOLOGY

The proposed MMCC-DSCC topology is shown in Fig. 3. It consists of MMCC-DSCC and $n - 1$ additional series units. Each unit includes two parallel branches. Branch 1 is a series-connected diode and inductor, and Branch 2 is the reversed series-connected diode, inductor, and switch (IGBT and reversed parallel diode). For these switches of n units, no additional switching signals are needed where each switch ($S'_{2,i-1}$) can be controlled by the corresponding IGBT ($S_{2,i}$) PWM signals.

The basic working principle is described in detail as follows. It is assumed that all the switches in the proposed topology in Fig. 3 are ideal devices. There are two situations (**Situation 1** and **Situation 2**) are introduced, and the corresponding equivalent circuit are respectively described as Fig. 4 (a) and Fig. 4 (b).

Situation 1: When the capacitor voltages of the two adjacent capacitors satisfy the constraint $U_{dc,i+1} > U_{dc,i}$, Fig. 4 (a) can be simplified as Fig. 4 (c).

Situation 2: When the capacitor voltages of the two adjacent capacitors satisfy the constraint $U_{dc,i+1} < U_{dc,i}$, the equivalent circuit in Fig. 4 (b) can be simplified as Fig. 4 (d). The switching signal of $S'_{2,i-1}$, and detailed working principle are discussed later in this Subsection.

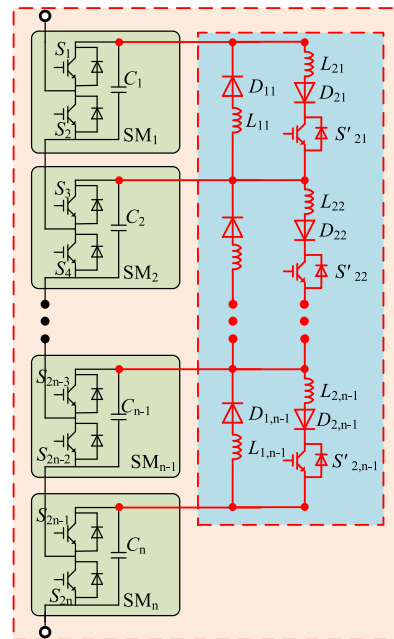


FIGURE 3. The proposed MMCC-DSCC topology.

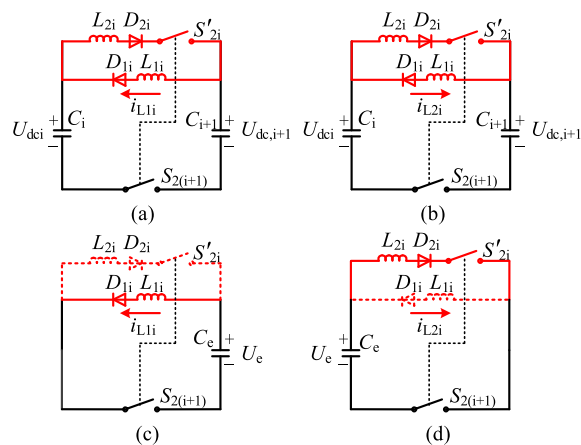


FIGURE 4. The equivalent circuit between two adjacent modules. (a) The equivalent circuit of situation 1. (b) The equivalent circuit of situation 2. (c) Simplified circuit of (a). (d) Simplified circuit of (b).

Based on KVL law, the equivalent voltage in Fig. 4 can be expressed as

$$U_e = \begin{cases} U_{dc,i+1} - U_{dc,i}, & U_{dc,i+1} > U_{dc,i} \\ U_{dc,i} - U_{dc,i+1}, & U_{dc,i+1} < U_{dc,i} \end{cases}$$

$$C_e = \frac{C_i}{2} \quad (1)$$

where U_e and C_e represent the equivalent voltage and capacitor, respectively.

In addition, the basic function of total units for every two branches can be introduced as

Branch 1 of all units:

$$U_{dc1} \geq U_{dc2} \geq U_{dc3} \geq \dots \geq U_{dcn} \quad (2)$$

TABLE 1. Switching status and balancing operation.

IGBT	SM capacitor voltage balancing				
	C_1 and C_2	C_2 and C_3	...	C_{n-2} and C_{n-1}	C_{n-1} and C_n
S_1	-(on/off)	-	-	-	-
S_2	-	-	-	-	-
S_3	-	-	-	-	-
S_4	on	-	-	-	-
⋮	-	-	...	-	-
S_{2n-3}	-	-	-	-	-
S_{2n-2}	-	-	-	on	-
S_{2n-1}	-	-	-	-	-
S_{2n}	-	-	-	-	on

Branch 2 of all units:

$$U_{dc1} \leq U_{dc2} \leq U_{dc3} \leq \dots \leq U_{dcn} \quad (3)$$

Therefore, voltage balancing control of SM capacitors can be achieved where the relationship between switching status and balancing operation can be listed in Table 1.

With the proposed topology, $S'_{2,i}$ can be controlled by the corresponding IGBT ($S_{2(i+1)}$) PWM signals. In situation 2, when $S_{2(i+1)}$ is turned on, the negative sides of the two adjacent capacitors are connected. Then, $S'_{2,i}$ should be turned on simultaneously to connect the positive sides of the two adjacent capacitors at the same time. When both $S_{2(i+1)}$ and $S'_{2,i}$ are on, the capacitor can exchange the power freely, and capacitor voltage balancing is thus realized.

It is also noted that with the proposed SM balancing method, only 6 voltage sensors (one in each arm) are needed to detect and regulate the arm voltage balancing for the following reason.

TABLE 2. Comparison results in each arm of different topologies.

Topology	Conventional MMCC-DSCC	Fig. 2 (a), [36]	Fig. 2 (b), [37]	Fig. 2(c), [38]	Fig. 2(d), [39]	Fig. 3, proposed
SM capacitors	n	n	2*n	n	n	n
IGBT	2*n	2*n+4	4*n	4*n	4*n	3*n-1
Clamping diodes	0	n+3	2*n	2*n	0	2*n-2
Clamping inductors	0	0	2*n	n	n	2*n-2
Voltages sensors	n	1	1	1	n/2	1
Additional resources	Software balancing	One transformer	One inductor	Control on the first SM	Balancing control of SMs	None
Advantage	Fewer power components	SM voltage Self-balanced	Increased rated current	Arm balancing, Fault ride-through	Increased energy, Fault ride-through	Listed below

In order to precisely control the output currents, the arm voltage has to be regulated. As the SM capacitor voltages in the same arm have been already balanced with the proposed balancing method, only one SM capacitor voltage in each arm are needed to monitor the arm voltage.

C. COMPARISONS BETWEEN DIFFERENT TOPOLOGY

For the MMCC-DSCC, comparison results in each arm of different topologies are listed in Table 2. Based on these analysis results, compared with the conventional software balancing or some improved balancing control methods, the proposed topology has some advantages:

- 1) It significantly reduces the number of SM capacitor voltage sensors.
- 2) Control framework can be simple without sort and select process, or some balancing control loops. Additional delay process caused by the sampling and control signals transmission is also mitigated.
- 3) The faster capacitor balancing speed can be obtained [36], [37].

In addition, compared with the presented hardware balancing schemes, some main advantages of the proposed scheme can be found as follow.

- 1) Based on some additional popular diodes insertion, the IGBT number ($n < 5$) can be reduced, and a transformer can be removed [36].
- 2) The number of power modules including IGBT, diodes, clamping inductors can be greatly reduced, and no additional arm inductor integration [37].
- 3) The number of IGBT, diodes are reduced, and no additional resource is needed to regulate the voltage of the first module [38].
- 4) The number of IGBT and voltage sensors are significantly reduced. Besides, instead of local voltage

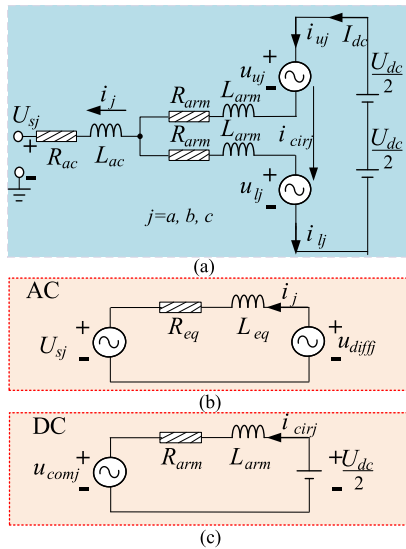


FIGURE 5. The equivalent circuit of MMCC-DSCC. (a). Overall equivalent circuit. (b). The equivalent circuit of the AC path. (c). The equivalent circuit of the DC path.

balancing [39], no sorting algorithm is needed for SM balancing.

III. MODELING AND CONTROL STRATEGY OF MMCC-DSCC BASED STATCOM

This section includes two parts. Firstly, the modeling of MMCC-DSCC is presented. Then, a simple control method is applied.

A. MODELING OF MMCC-DSCC

The equivalent circuit of MMCC-DSCC in Fig. 1 is shown in Fig. 5(a), where the equivalent circuit of the AC and DC paths are respectively as Fig. 5(b) and Fig. 5(c).

The AC part can be characterized as (4), where R_{eq} and L_{eq} are expressed as (5). In equation (5), R_{arm} and L_{arm} are arm resistor and arm inductor, R_{ac} and L_{ac} are AC output resistor and arm inductor.

$$\begin{cases} u_{diffj} = \frac{u_{lj} - u_{uj}}{2} \\ i_j = \frac{i_{uj} - i_{lj}}{2} \\ R_{eq}i_j + L_{eq}\frac{di_j}{dt} = u_{diffj} - U_{sj} \end{cases} \quad (4)$$

$$\begin{cases} R_{eq} = R_{ac} + R_{arm}/2 \\ L_{eq} = L_{ac} + L_{arm}/2 \end{cases} \quad (5)$$

Then, the DC part can be characterized as

$$\begin{cases} u_{comj} = \frac{u_{lj} + u_{uj}}{2} \\ R_{arm}i_{cirj} + L_{arm}\frac{di_{cirj}}{dt} = \frac{U_{dc}}{2} - u_{comj} \end{cases} \quad (6)$$

B. CURRENT CONTROL

Fig. 6 illustrates the overall control diagram of MMCC-DSCC based STATCOM. The control diagram can be divided into three parts. The first part controls the active

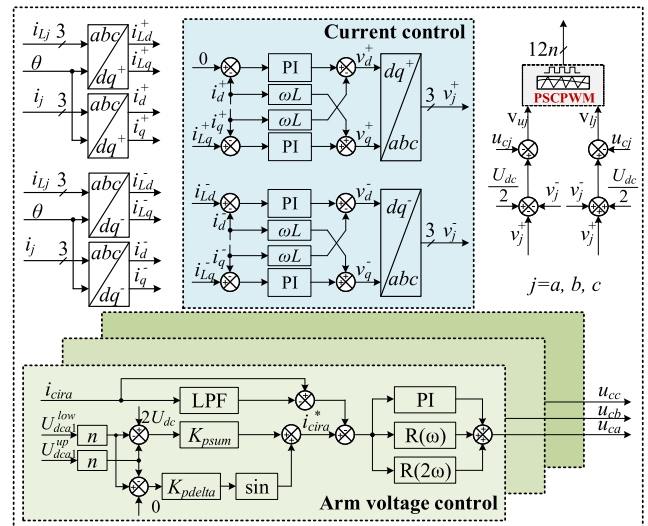


FIGURE 6. Overall control diagram of MMCC-DSCC based STATCOM.

and reactive power in positive and negative sequence dq frames, which can be applied in unbalanced power condition. The second part is adopted to control the sum voltage of each arm. The third part generates the voltage references of each arm and the drive signals of each switch.

The positive and negative sequence current can be transformed into a DC component through an individual transformation in positive and negative sequence dq frame. As a result, the DC component can be accurately tracked by simple PI controllers. The derivation process is exhibited as follows.

The positive sequence and negative sequence is expressed as

$$I_p = \begin{bmatrix} \sin(\omega t + \varphi_p) \\ \sin(\omega t - \frac{2\pi}{3} + \varphi_p) \\ \sin(\omega t + \frac{2\pi}{3} + \varphi_p) \end{bmatrix}, \quad I_n = \begin{bmatrix} \sin(\omega t + \varphi_n) \\ \sin(\omega t + \frac{2\pi}{3} + \varphi_n) \\ \sin(\omega t - \frac{2\pi}{3} + \varphi_n) \end{bmatrix} \quad (7)$$

The transfer matrix of the positive and negative sequence dq frame can be expressed as

$$C_{dq/abc} = \begin{bmatrix} \sin \omega t & \sin(\omega t - \frac{2}{3}\pi) & \sin(\omega t + \frac{2}{3}\pi) \\ \cos \omega t & \cos(\omega t - \frac{2}{3}\pi) & \cos(\omega t + \frac{2}{3}\pi) \end{bmatrix} \quad (8)$$

$$C_{dq/abc}^* = \begin{bmatrix} \sin(-\omega t) & \sin(-\omega t - \frac{2}{3}\pi) & \sin(-\omega t + \frac{2}{3}\pi) \\ \cos(-\omega t) & \cos(-\omega t - \frac{2}{3}\pi) & \cos(-\omega t + \frac{2}{3}\pi) \end{bmatrix} \quad (9)$$

With the transformation of $C_{dq/abc}$, it can be concluded from (10) that the positive sequence current is transferred into the DC component and the negative sequence current is transferred into the second order component.

$$I_{dq}^p = \frac{3}{2}I_p \begin{bmatrix} \cos \varphi_p \\ \sin \varphi_p \end{bmatrix}, \quad I_{dq}^n = \frac{3}{2}I_n \begin{bmatrix} -\cos(2\omega t + \varphi_n) \\ \sin(2\omega t + \varphi_n) \end{bmatrix} \quad (10)$$

With the transformation of $C_{dq/abc}^*$, it can be concluded from (11) that the negative sequence current is transferred into the DC component and the positive sequence current is transferred into the second order component.

$$I_{dq}^{p*} = \frac{3}{2} I_p \begin{bmatrix} \cos(2\omega t + \varphi_p) \\ \sin(2\omega t + \varphi_p) \end{bmatrix}, \quad I_{dq}^{n*} = \frac{3}{2} I_n \begin{bmatrix} -\cos \varphi_n \\ \sin \varphi_n \end{bmatrix} \quad (11)$$

The similar design principle of PI controllers can be found in the reference [40], and it is not be discussed in this paper.

C. ARM VOLTAGE CONTROL

The second part is adopted to regulate the sum voltage of SMs in each arm. The SM voltages within each arm have already been balanced through the proposed topology. It can be easily seen that the arm voltage can be reflected from the measurement of a single SM voltage in (12). Thus, this capacitor voltage balancing process significantly reduces the number of voltage sensors.

$$\sum U_{dcij}^{up} = n \cdot U_{dcil}^{up}, \quad \sum U_{dcij}^{low} = n \cdot U_{dcil}^{low} \quad (12)$$

where U_{dcil}^{up} and U_{dcil}^{low} ($i = a, b, c$) are the capacitor voltages of the first SM in the upper and the lower arm respectively. It's noted that only one SM voltage sensor in each arm is needed. In this paper, the first SM in each arm is applied.

The arm voltage is regulated by control of circulating current. The circulating current reference to regulate the arm voltage includes two components. The first component is to control the sum voltage of two arms in the same phase and the second component is used to control the voltage difference between the upper and the lower arm. According to [39], the reference values of circulating currents can be expressed as

$$i_c^* = K_{psum}(2U_{dc} - \text{LPF}\{U_\Sigma\}) - K_{pdelta}(0 - \text{LPF}\{U_\Delta\}) \sin \omega t$$

$$U_\Sigma = \sum U_{dcij}^{up} + \sum U_{dcij}^{low}, \quad U_\Delta = \sum U_{dcij}^{up} - \sum U_{dcij}^{low} \quad (13)$$

In order to control the circulating currents, the PIR controller is adopted. The PI controller is used to control the DC component of the circulating currents. In addition, the other two resonant (R) controllers are adopted to respectively achieve the fundamental current control and suppress the second order components of circulating currents. For the control parameters design guide of this PIR controller can also be found in reference [41].

D. MODULATION

In this paper, the popular phase shifted carrier (PSC) PWM is used [40], and the final voltage reference of each arm can be expressed as

$$\begin{bmatrix} V_{uj} \\ V_{lj} \end{bmatrix} = \begin{bmatrix} \frac{U_{dc}}{2} - v_j + u_{cj} \\ \frac{U_{dc}}{2} + v_j + u_{cj} \end{bmatrix} \quad (14)$$

where V_{uj} and V_{lj} ($j = a, b, c$) are the voltage reference of the upper and the lower arm.

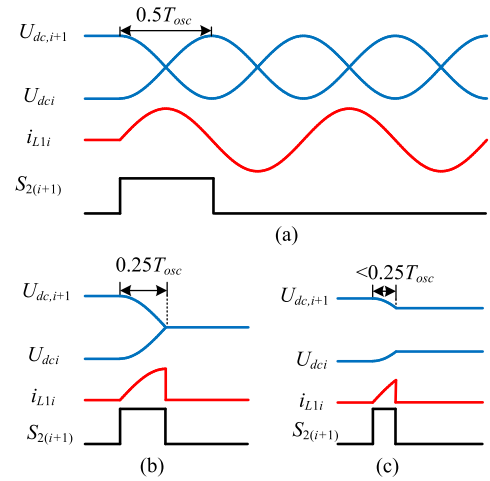


FIGURE 7. The relationship of voltage and current in the diode-clamped circuit. (a) Conduction period of clamping circuit $\Delta T = 0.5T_{osc}$. (b) Conduction period of clamping circuit $\Delta T = 0.25T_{osc}$. (c) Conduction period of clamping circuit $\Delta T < 0.25T_{osc}$.

IV. DISCUSSION

In this section, the parameters design guide for the proposed scheme is discussed first, including clamping inductor, diodes, and IGBT switches. Then, the cost of the proposed balancing scheme is analyzed.

A. PARAMETER SELECTION OF THE CLAMPING INDUCTOR

As the balancing analysis principle of **situation 1** and **situation 2** is identical, **situation 1** is used as an example to describe the parameter selection process. According to Fig. 4 (a), when the switch $S_{2,(i+1)}$ is on, based on KVL law, the following equations can be calculated as

$$\begin{cases} L_e C_e \frac{d^2 U_e}{dt} + U_e = 0 \\ L_e = L_{li} = L_{2i} \end{cases} \quad (15)$$

Thus, it's clearly shown that it is a second-order system and the solution of the linear differential equation can be expressed as

$$\begin{cases} U_e = \frac{U_0}{2}(e^{\gamma t} + e^{-\gamma t}) \\ i_{Lli} = C_e \frac{dU_e}{dt} = \frac{C_e U_0 \gamma}{2}(e^{\gamma t} - e^{-\gamma t}) \end{cases} \quad (16)$$

where U_0 is the initial voltage of U_e , i_{Lli} is the clamping current of the diode-clamped circuit, and γ is system eigenvalue.

$$\gamma = j\omega_0 = j \frac{1}{\sqrt{L_e C_e}} \quad (17)$$

The solution can be further expressed as

$$\begin{cases} U_e = U_0 \cos(\omega_0 t) \\ i_{Lli} = \sqrt{\frac{C_e}{L_e}} U_0 \sin(\omega_0 t) \end{cases} \quad (18)$$

$$T_{osc} = 2\pi \sqrt{L_e C_e} \quad (19)$$

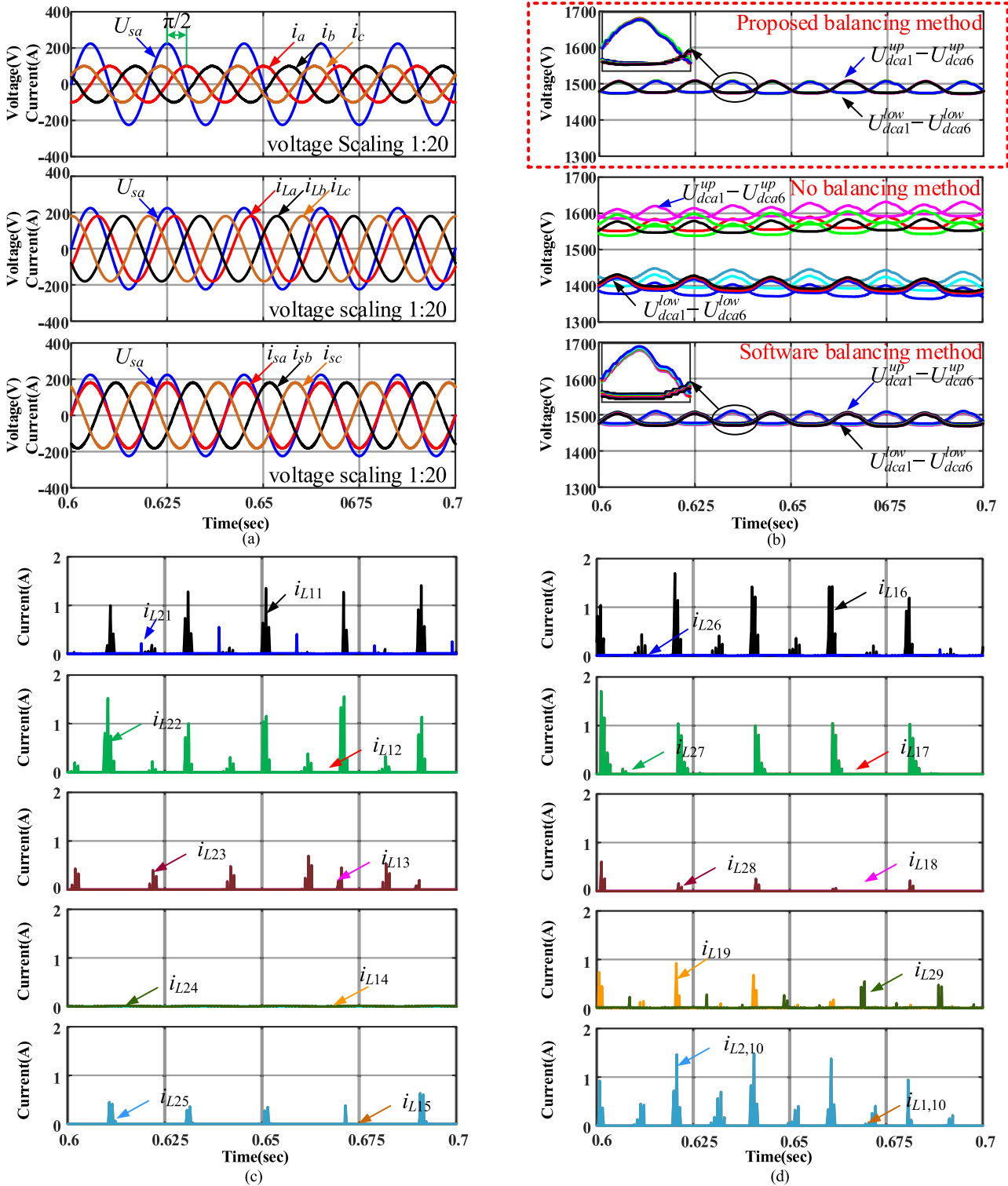


FIGURE 8. Simulation results of MMCC-DSCC based STATCOM under balanced load. (a) System current waveforms. (b) Comparison of SM voltages with different balancing methods. (c) Clamping currents in the upper arm. (d) Clamping currents in the lower arm.

It is clearly seen that the waveform of U_e fluctuates as the sine wave and the period of fluctuation T_{osc} is closely related to the value of clamping inductor L_e .

L_e has a close relationship with system performance. That is to say, if L_e gets larger, the T_{osc} will be larger, and the SM voltage balancing effect will be worse. However, if L_e gets smaller, T_{osc} will be smaller, and the possibility of oscillation

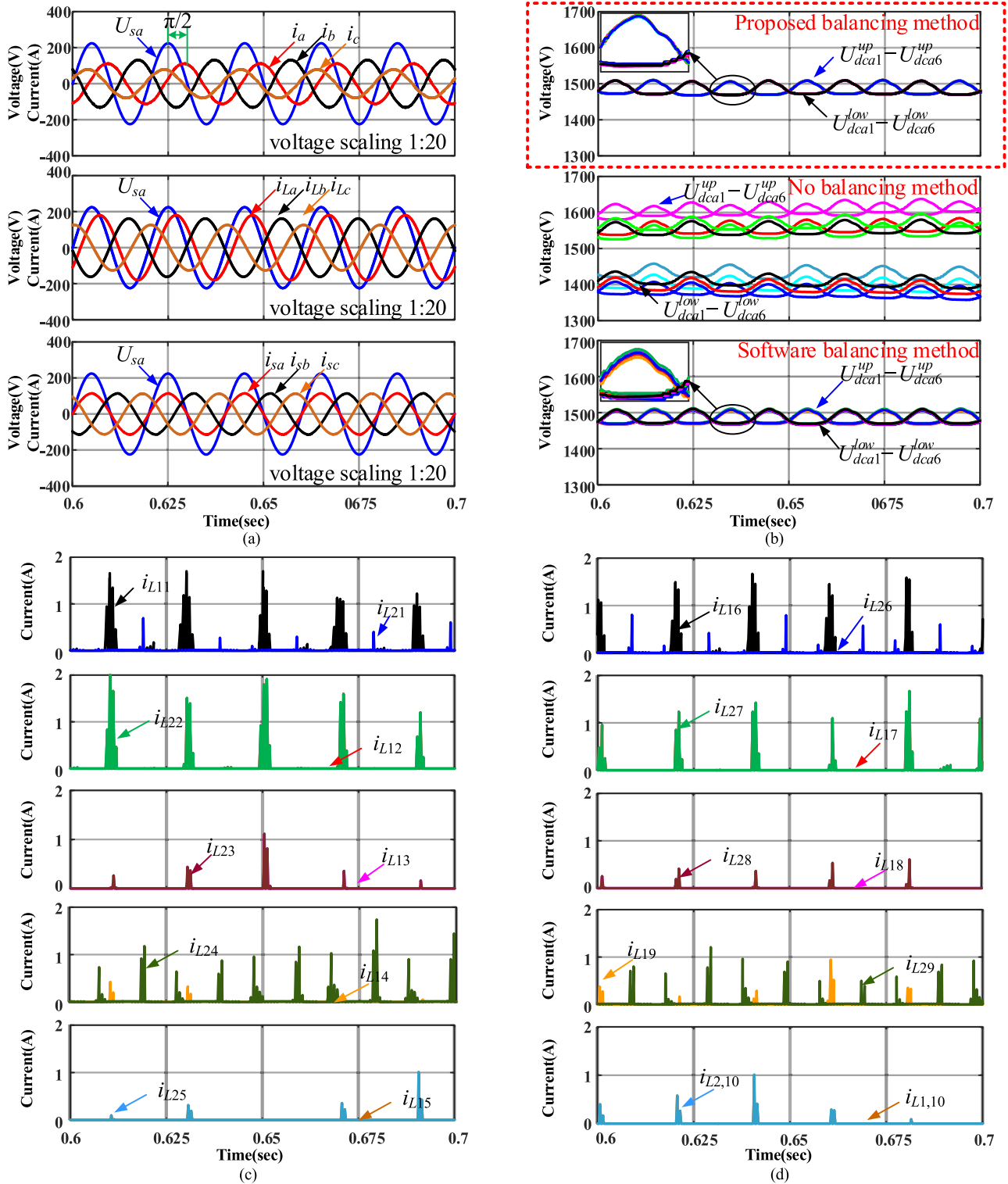


FIGURE 9. Simulation results of MMCC-DSCC based STATCOM under balanced load. (a) System current waveforms. (b) Comparison of SM voltages with different balancing methods. (c) Clamping currents in the upper arm. (d) Clamping currents in the lower arm.

and extra power loss may be higher. Thus, it is very necessary to give the constraint for the inductor selection.

Assuming $U_{dc,i+1} > U_{dc,i}$, the relationship of the voltage U_e and the clamping current i_{L1i} is shown as Fig. 7 according

to (18). Thus, ΔT , the active period of the switch $S_{2(i+1)}$, is supposed to be smaller than $0.25T_{osc}$. However, it is unrealistic to keep each ΔT smaller than $0.25T_{osc}$ in the real application. In a word, an average of ΔT can be described

as

$$\Delta \bar{T} = \lambda m T_{sw} < 0.25 T_{osc} \quad (20)$$

where m is the modulation index, λ is the average coefficient ($0 < \lambda < 1$), and T_{sw} is the reciprocal of the switching frequency.

Therefore, based on the last two equations, the constraint can be presented as

$$L_e > \frac{4\lambda^2 m^2}{\pi^2 f_{sw}^2 C_e} \quad (21)$$

B. PARAMETER SELECTION OF CLAMPING DIODE AND SWITCH

As the manufacture errors, PSC modulation, and other disturbances in the real SM circuits, power unbalance among SMs in each arm occurs.

Each SM power and power difference among SMs in each arm can be respectively defined as

$$P_{SM} = \frac{1}{2} C \left(\frac{U_{dc}}{n} \right)^2 \quad (22)$$

$$P_{dif} = (\sigma + \gamma + \delta) P_{SM} \quad (23)$$

where σ , γ , and δ are power difference proportion values caused by the manufacture errors, PSC modulation, and other disturbances respectively.

The system can be in a balanced condition when exchange power between two adjacent SMs is equal to about half of the power difference P_{dif} . Based on the energy conservation law, it can be described as

$$0.5 P_{dif} = \frac{U_{dc}}{n} i_{DCC_ave} \quad (24)$$

where i_{DCC_ave} is the average clamping current through the Branch 1.

In order to withstand this clamping current, the forward current of clamping diodes is

$$i_{DF} = \alpha i_{DCC_ave} \quad (25)$$

where α is large than 1 for enough current margin of diodes.

Besides, the maximum reverse voltage on diodes is the voltage difference between two adjacent SM and can be expressed as

$$v_{RDF} = \varepsilon \frac{U_{dc}}{n} \quad (26)$$

where ε is usually less than 10%.

Based on these analysis results, the diode can be selected.

In addition, IGBT switch selection is discussed as follows.

For the switch, the maximum conduction current is the same as (25).

$$i_{SF} = i_{DF} = \alpha i_{DCC_ave} \quad (27)$$

The maximum value of the reserved voltage for the switch is described as

$$v_{RSF} = \frac{U_{dc}}{n} \quad (28)$$

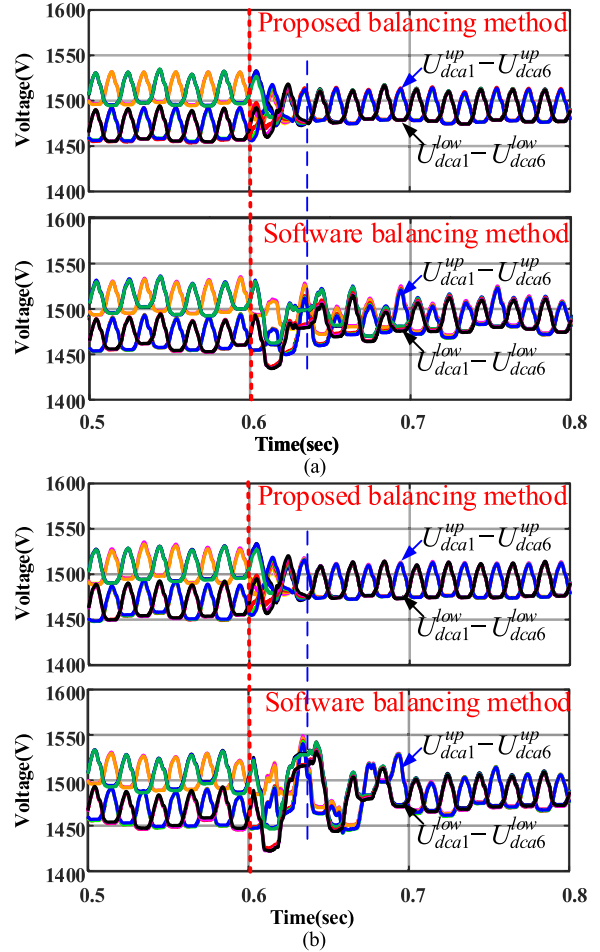


FIGURE 10. Comparisons results of the proposed balancing method and conventional software balancing method. (a) Comparisons under balanced load in Scenario 1. (b) Comparisons under unbalanced load in Scenario 2.

Based on the above analysis results, the diode and switch can be selected considering some real constraints.

C. COST ANALYSIS OF THE PROPOSED BALANCING TOPOLOGY

Compared with traditional software balancing method, the reduced resources and additional resources are listed below.

1) REDUCED RESOURCES

$6n-6$ reduced voltage sensors, $6n-6$ reduced optical senders, $6n-6$ reduced optical receivers, $6n-6$ reduced optical fiber cables, and lowered controller requirement.

2) ADDITIONAL RESOURCES

$6n-6$ IGBTs, $6n-6$ drivers, $12n-12$ diodes and $12n-12$ inductors. The additional cost of the proposed method can be calculated through the following equation.

$$\Sigma_{cost} = (6n - 6)(\Sigma_{IGBT} + \Sigma_{peri}) + (12n - 12)(\Sigma_{dio} + \Sigma_{ind}) - (6n - 6)(\Sigma_{sens} + \Sigma_{send} + \Sigma_{rece} + \Sigma_{cab}) \quad (29)$$

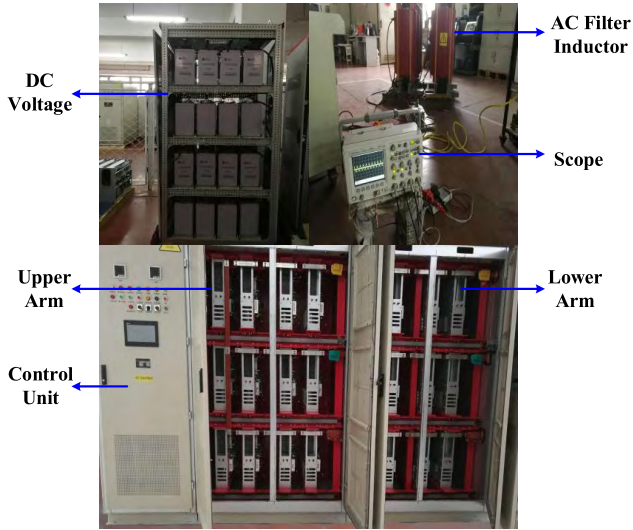


FIGURE 11. Laboratory prototype.

where Σ_{cost} is the total additional cost. Σ_{IGBT} and Σ_{peri} are the cost of IGBT and its peripheral cost (including drivers and other auxiliary costs). Σ_{dio} and Σ_{ind} are the cost of diodes and inductors. Σ_{sens} , Σ_{send} , Σ_{rece} , and Σ_{cab} are the cost of the voltage sensors, optical senders, optical receivers, and optical fiber cables respectively.

According to reference [42], the cost of IGBT can be expressed as

$$\Sigma_{IGBT} = \sigma_{chip}A_{chip} + \Sigma_{pack} \quad (30)$$

where σ_{cost} is the specific price per chip area and A_{chip} is the chip area. Σ_{pack} is the package price.

The peripheral cost can be roughly expressed as

$$\Sigma_{peri} = 0.1 \Sigma_{IGBT} \quad (31)$$

Substituting (30) and (31) into (29), the total additional cost can further be expressed as

$$\Sigma_{cost} = (6n - 6)(1.1(\sigma_{chip}A_{chip} + \Sigma_{pack}) + 2\Sigma_{dio} + 2\Sigma_{ind} - \Sigma_{sens} - \Sigma_{send} - \Sigma_{rece} - \Sigma_{cab}) \quad (32)$$

V. SIMULATION RESULTS

To verify the effectiveness of the proposed MMCC-DSCC scheme, the same topology in Fig. 3 in MATLAB/Simulink is used. The simulation parameters are shown in Table 3.

Three simulation scenarios are shown in Table 4, where **Scenario 1** describes the balanced load condition, **Scenario 2** describes the unbalanced load condition, and **Scenario 3** compares the balancing effect between software balancing method and the proposed balancing method under balanced and unbalanced load.

Scenario 1 Fig. 8 shows the simulation results for the proposed MMCC-DSCC based STATCOM under balanced load. The output currents of MMCC-DSCC, the load currents and three-phase grid currents after reactive power compensation

TABLE 3. Parameters of the simulation system.

Type	Circuit parameters	Values
Three-phase grids	Line voltage	5.5 kV
	frequency	50 Hz
	AC filter inductor	6 mH
MMCC-DSCC	DC voltage	9 kV
	DC capacitor,	4.7 mF
	Switching frequency	1.25 kHz
	Arm inductor	3 mH
	Clamping inductor	100 μ H
	SM number per arm	6
Type	Control parameters	Values
Current control	K_{p1} ,	50
	K_{i1}	500
Arm voltage control	K_{psum} ,	0.004
	$K_{pdeltas}$	0.005
	K_p ,	0.5
	K_i ,	2.5
	$K_{R\omega_s}$	5
	$K_{R2\omega_s}$	10

TABLE 4. Simulation scenarios.

Scenarios	Inductive load	Description		
1	Balanced	Load A, Load B and Load C 340 kW 220 kvar		
2	Unbalanced	Load A 340 kW 340 kvar	Load B 270 kW 250 kvar	Load C 180 kW 160 kvar
3	Balanced (Sc.1) Unbalanced (Sc.2)	Comparison: Software method and proposed method		

are shown in Fig. 8 (a). It's clearly seen that good control performance can be achieved where three-phase grid currents are balanced and the power factor is nearly 1. Then, as shown in Fig. 8 (b), the proposed topology has realized similar SM voltage balancing control of individual capacitors, compared with the software balancing method. However, SM capacitor voltage remains unbalanced without balancing control. In addition, internal currents of Branch1 and Branch2 are very small in the upper five, and the lower five units are respectively depicted in Fig. 8 (c) and Fig. 8 (d), indicating that they are much smaller than AC output currents of this MMCC.

Scenario 2 Fig. 9 depicts the simulation results for the proposed MMCC-DSCC based STATCOM under unbalanced load. The output currents of MMCC-DSCC, the load currents, and three-phase grid currents after reactive power compensation are shown in Fig. 9 (a). It's easily seen that similar simulation results as balanced load in **Scenario1**, where balanced grid currents are maintained, and effective reactive power is compensated. Then, as shown in Fig. 9 (b), similar simulation performance in **Scenario1** under balanced load with SM voltage balancing control can be adopted under unbalanced load. But SM voltages are unbalanced without balancing control. In addition, internal currents of Branch1 and Branch2 are very small in the upper five, and the lower five units are respectively depicted in Fig. 9 (c) and Fig. 9 (d), showing that they are much smaller than AC output currents of this MMCC-DSCC.

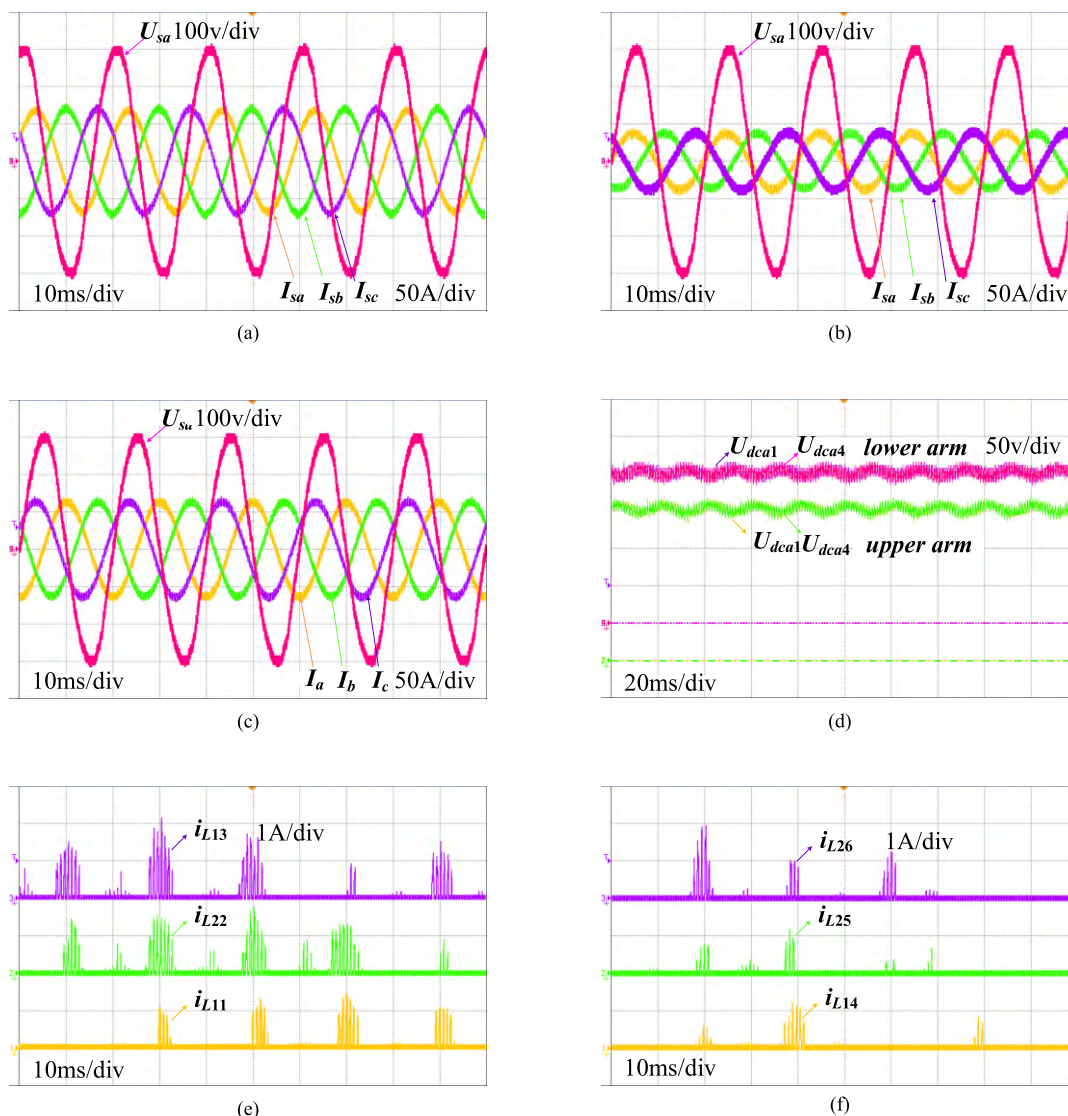


FIGURE 12. Experiment results of MMCC-DSCC based STATCOM under balanced load. (a) Grid voltage and currents before compensation. (b) Grid voltage and currents after compensation. (c) Grid voltage and output currents. (d) Capacitor voltages in phase A. (e) Currents of clamping circuits in the upper arm of phase A. (f) Currents of clamping circuits in the lower arm of phase A.

Based on these simulation results of **Scenario 1** and **Scenario 2**, the proposed scheme for MMCC-DSCC based STATCOM is always effective in balanced and unbalanced load.

Scenario 3 Fig. 10 exhibits the comparison results of the proposed voltage balancing method and the software balancing method [40]. The simulation results include two cases: balanced load and unbalanced load. It should be noted that in order to vividly demonstrate the advantages of the proposed method, an artificial initial deviation of SM voltages is set before 0.6s.

For balanced load, the SM voltages are shown in Fig. 10 (a), where both the proposed balancing method and the software balancing method are activated at 0.6s. As is shown in the figure, the proposed method has the faster balancing speed than the software balancing method during the dynamic

process indicating the proposed balancing method can lower the effect brought by sampling and control delay. For unbalanced load, the dynamic SM voltages are shown in Fig. 10 (b), where both the two balancing methods are activated at 0.6 s. It clearly shows that the proposed balancing method has a faster balancing speed than the software balancing method, indicating that the proposed balancing method can reduce the effect of sampling and control delay.

VI. EXPERIMENTAL RESULTS

A laboratory prototype based on nine-level MMCC-DSCC based STATCOM has been implemented in the laboratory as shown in Fig. 11. The experiment parameters are given in Table 5. The two experiment scenarios are given in Table 6. The proposed control are implemented with TMS320F28335 and 10M02SCE144C8G. The Agilent scope

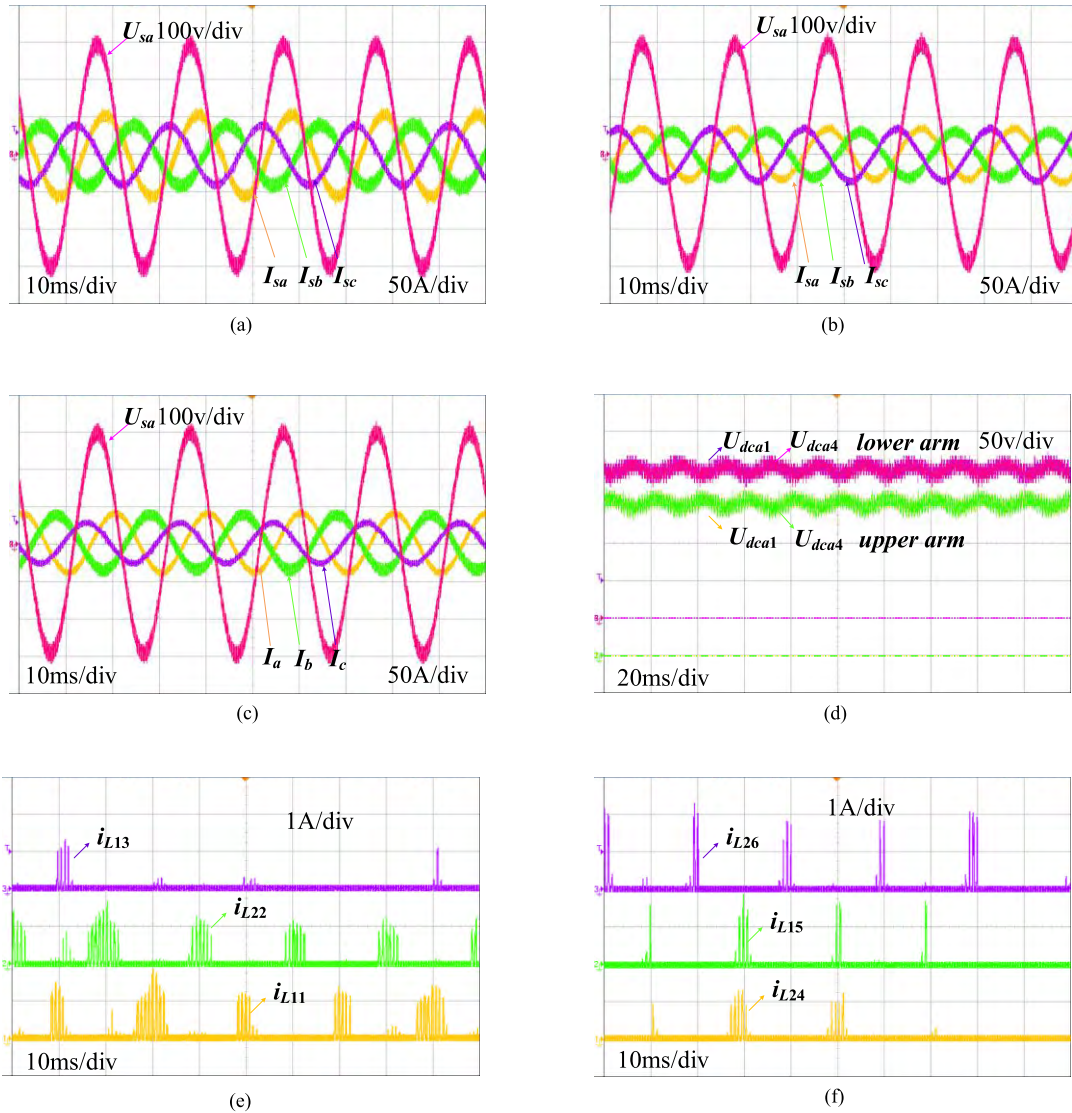


FIGURE 13. Experiment results of MMCC-DSCC based STATCOM under unbalanced load. (a) Grid voltage and currents before compensation. (b) Grid voltage and currents after compensation. (c) Grid voltage and output currents. (d) Capacitor voltages in phase A. (e) Currents of clamping circuits in the upper arm of phase A. (f) Currents of clamping circuits in the lower arm of phase A.

TABLE 5. Parameters of the experiments.

Type	Circuit parameters	Values
Three-phase grids	Line voltage	380 V
	frequency	50 Hz
	AC filter inductor	5 mH
MMCC-DSCC	DC voltage	800 V
	DC capacitor,	3 mF
	Arm inductor	100 μ H
	Clamping inductor	1 mH
	SM number per arm	4

DSO5014A is used to display and record the experimental waveforms.

Scenario 1 The experiment results of the proposed MMCC-DSCC under balanced load are shown in Fig. 12.

TABLE 6. Experiment scenarios.

Scenarios	Inductive load	Load A	Load B	Load C
1	Balanced		7 kW	
	Inductive		9.5 kvar	
2	Unbalanced	7 kW	7 kW	7 kW
	Inductive	8 kvar	5 kvar	4 kvar

The grid voltage and three-phase currents before and after compensation are shown in Fig. 12 (a) and (b), respectively. The output currents of MMCC-DSCC is shown in Fig. 12 (c). It can be clearly seen that the proposed MMCC-DSCC can effectively compensate the reactive power. The capacitor voltages and currents in Branch 1 or Branch 2 in the upper 3 units and the lower 3 units are shown in Fig. 12 (d), (e) and (f) individually. With the limitation of scope signals, only one

clamping current between two adjacent SMs is displayed. As shown in Fig. 12 (d), the individual capacitor voltage of each SM is well balanced. The results in Fig. 12 (e) and Fig. 12 (f) indicates that the internal currents are much smaller than output currents.

Scenario 2 The experiment results of MMCC-DSCC under unbalanced load are shown in Fig. 13. The grid voltage and three-phase currents before and after compensation are shown in Fig. 13 (a) and (b), respectively. The output currents of MMCC-DSCC is shown in Fig. 13 (c). It can be easily showed that reactive power compensation can be achieved by the proposed MMCC-DSCC. The capacitor voltages and currents in Branch 1 or Branch 2 in the upper 3 units and the lower 3 units are shown in Fig. 13 (d), (e) and (f) individually, showing SM capacitor voltages has been well balanced and internal currents are much smaller than the output currents of MMCC-DSCC.

According to the above experimental results of **Scenario 1** and **Scenario 2**, the proposed scheme for MMCC-DSCC based STATCOM is always effective in balanced and unbalanced load.

VII. CONCLUSION

For MMCC-DSCC based STATCOM, a new voltage balancing control scheme for all the SM capacitors is proposed. Compared with conventional software balancing control methods, the number of capacitor voltage sensors by the proposed scheme has been greatly reduced, especially in the higher voltage or more SMs in each arm. Both Simulation waveforms and experimental results verify the effectiveness of this control scheme even under two operation conditions of three-phase balanced and unbalanced load. For the inserted additional units, the design guide of these corresponding components has been described. By the proposed scheme, both DC capacitor voltage balancing control and reactive power compensation are simultaneously realized for MMCC-DSCC based STATCOM even in power unbalanced condition.

More effective combination of the improved controller and this proposed hardware topology will be further developed in the future work.

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