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Fault Diagnosis and Monitoring of Modular Multilevel Converter with Fast Response of Voltage Sensors

Jianzhong Zhang, *Senior Member, IEEE*, Xing Hu, Shuai Xu, Yaqian Zhang
and Zhe Chen, *Fellow, IEEE*

Abstract—Modular multilevel converter (MMC) has been one of the most popular candidates in high voltage applications. However, the reliability is a critical issue due to a large number of power switching devices and capacitors applied in the MMC. To improve the reliability of the MMC, a fast and reliable diagnosis strategy for the open-circuit fault is proposed in this paper, where submodule voltage sensors are relocated to the upper switching device. Furthermore, a voltage observer based on the submodule voltage sensor is established to monitor the capacitor and realize the power control of the MMC under normal operation. A Boolean logic operation based fault indicator is put forward based on the relationship of the operation state and binaried output of voltage sensors, which could detect and locate the open-circuit faults of the MMC very fast. The ratio of the increment of the observed and measured capacitor voltage during the period of positive arm current is applied to monitor the capacitor. The effectiveness of the proposed fault diagnosis strategy and the capacitor monitoring strategy is verified by the experiment results.

Index Terms—Capacitor monitoring, capacitor voltage observation, fault diagnosis, modular multilevel converter, voltage sensor.

I. INTRODUCTION

DUE to the features of high redundancy, superior AC performance and scalability to meet any voltage level, modular multilevel converter (MMC) has been regarded as one of the most promising multilevel converters in high voltage applications [1]-[3]. In general, there might be hundreds of cascaded identical submodules to meet the requirement of voltage, such as the case in high voltage direct current (HVDC) transmission system [4]-[7]. Then the amount of power switching device in the MMC is very high. Since the power

switching devices have a much higher malfunction rate than other components in power converters [8], the reliability of the MMC might be low and the application of fault diagnosis is necessary to improve the system reliability.

There are mainly two types of faults, namely open-circuit and short-circuit that may occur on the power switching devices. However, the short-circuit fault could be easily transformed into open-circuit fault by using fast fuses in series. Then only the open-circuit fault is focused on and studied in this paper.

Once an open-circuit fault happens in a certain submodule, not only the output performance of the MMC would be deteriorated due to the undesired output voltage of faulty submodule, but also the capacitor in faulty submodule would be over-charged if the faulty submodule is not detected and isolated in time. Then the voltage of the capacitor would be increased to a dangerous extent. It might cause subsequent faults and at last break down the whole MMC system.

Several fault diagnosis strategies have been proposed for the MMC in recent years. A sliding mode observer (SMO) based fault detection method is proposed in [9], where the values of arm current and capacitor voltage are observed. The differences between the observed values and the measured values are used to locate the faulty power switching devices. However, this strategy might be failed in the case with multiple faults happened in different submodules. In [10], an improved SMO is proposed to realize the fault diagnosis of the MMC with high robustness, and the consuming time to locate the faulty device is less than 50 ms. In [11], the Kalman filter is applied to the fault detection and voltage deviations of the capacitor in different submodules are used to locate the faulty submodule. However, the faulty power switching device cannot be located by this method, and it would be impracticable when sorting-process is used for the capacitor voltage balancing control in the MMC. A state observer based fault diagnosis is proposed in [12], where similar limitations as [11] exist. Extended state observer (ESO) and adaptive observer are also implemented to the fault diagnosis of the MMC [13]-[15]. Two submodule fault detection methods, namely clustering algorithm (CA) based method, and calculated capacitance (CC) based method are proposed in [16]. In [17], the difference of the estimated voltage between two different algorithms is calculated and used to locate the faults of the submodule. However, the computation burden is high and some of the observer parameters are difficult to design in [16-17]. Most of the observer based fault diagnosis strategies rely on the

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parameters of the MMC system, such as the parameter value of the capacitors and arm inductors. However, these components normally have large manufacturing tolerances and produce parameter deviations due to aging, which might result in wrong judgment and location of the fault for the MMC.

To realize the fault detection, a supplementary hardware circuit is employed in [18] or extra voltage sensor is added in each arm in [19]. However, the cost will be considerably increased. In [20], the voltage sensor is used to measure the submodule terminal voltage instead of the capacitor voltage. The faulty power switching devices could be located based on the measured terminal voltage, arm current and the peaks of triangular carriers. A fast fault diagnosis based on the measurement of submodule output voltage is put forward in [21]. However, the extra hardware circuit in each submodule is required and the cost might be increased greatly. In this paper, a new method with fast and reliable fault diagnosis is proposed, which does not rely on the parameters of the MMC system. The voltage sensors, which are normally employed in every submodule and parallel connected with the capacitor, are relocated to the upper switching devices. A fault indicator for diagnosing and locating the faulty power switching devices is proposed based on the output of the voltage sensors and the operation state of the submodules. Due to the proposed configuration of the voltage sensor in the submodule, a simple and effective capacitor monitoring strategy could also be developed, which is based on the ratio of the increment of observed and measured capacitor voltage during the period of positive arm current.

The rest of the paper is organized as follows. Section II presents a topology description and operating principle of the MMC. The current paths under normal condition and open-circuit fault are discussed in Section III. The proposed fault diagnosis strategy is presented in Section IV. Section V shows the monitoring strategy for the capacitance in MMC. Section VI gives the experiment results. Finally, the conclusions of this paper are drawn in Section VII.

II. MODELLING

A. Topology

Fig. 1 shows the topology of a three-phase MMC, which contains the upper arm and lower arm in one phase. Each arm is constructed by N series-connected identical submodules, respectively. In each phase, two buffer inductors L_s connect the upper arm and the lower arm. The output of the MMC is led out from the midpoint of two buffer inductors.

The circuit of a half-bridge submodule is shown in Fig. 2, where one capacitor and two power switching devices are adopted. The operation state of two power switching devices should be opposite to avoid short circuit of the capacitor. Fig. 2(b) shows the simplified circuit under the upper power switching device turned on ($S=1$), which means the submodule is on the inserted state and the output voltage of the submodule is same as the capacitor voltage. In this case, the variation tendency of the capacitor voltage depends on the direction of the arm current. That is, if the arm current is positive, the capacitor voltage would be increasing, and if the arm current is

negative, the capacitor voltage would be decreasing. Fig. 2(c) shows the simplified circuit under the upper power switching device turned off ($S=0$), which means the submodule is on the bypassed state. The output voltage of the submodule equals zero. In this case, the capacitor voltage would keep constant no matter what the directions of the arm current are.

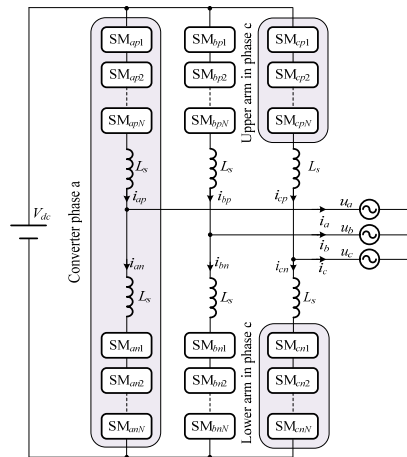


Fig. 1. The topology of the three-phase MMC.

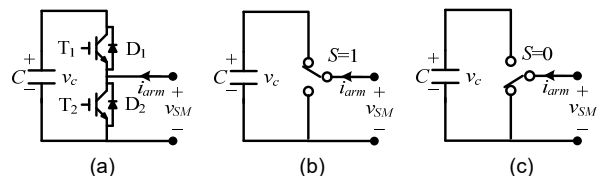


Fig. 2. Circuits of the submodule. (a) Half-bridge circuit, (b) simplified circuit under $S=1$, (c) simplified circuit under $S=0$.

B. Operation Principle

The simplified equivalent circuit of the MMC is shown in Fig. 3, where the voltages of the upper arm and lower arm are shown as adjustable voltage sources due to the submodule state in certain arms [22]. Neglecting inductor resistance R , the voltage equation of the MMC is

$$\begin{cases} u_x = \frac{1}{2}(v_{xn} - v_{xp}) - \frac{1}{2}L_s \frac{di_x}{dt} \\ 2L_s \frac{di_{xz}}{dt} = V_{dc} - (v_{xp} + v_{xn}) \end{cases} \quad (x = a, b, c) \quad (1)$$

where u_x and i_x are the grid voltage and output current of the MMC, respectively. L_s is the arm buffer inductance, i_{xz} is the circulating current, V_{dc} is the DC link voltage, v_{xp} and v_{xn} are the voltage of upper and lower arms, respectively. It can be seen from (1) that the AC output of the MMC is determined by the voltage difference between the upper and lower arms.

The voltage of the upper or lower arm is the sum of the output voltage of the submodules in each arm, which could be expressed as

$$\begin{cases} v_{xp} = \sum_{i=1}^N S_{xpi} v_{cxi} \\ v_{xn} = \sum_{i=1}^N S_{xni} v_{cxi} \end{cases} \quad (x = a, b, c) \quad (2)$$

where N is the number of submodules in one arm, S_{xpi} and S_{xni}

are operation states of i^{th} submodule in upper and lower arms, respectively. v_{cspi} and v_{cxni} are the capacitor voltages of i^{th} submodule in upper and lower arms, respectively.

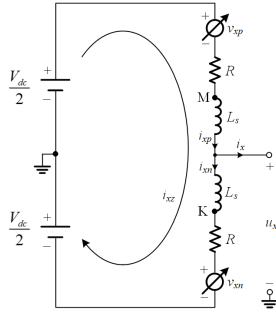


Fig. 3. The equivalent circuit of the MMC.

The expected voltage of upper and lower arms could be calculated as

$$\begin{cases} v_{xp}^* = \frac{V_{dc}}{2} - u_x^* \\ v_{xn}^* = \frac{V_{dc}}{2} + u_x^* \end{cases} \quad (x = a, b, c) \quad (3)$$

where u_x^* is the expected output voltage of MMC given by outer-loop controller, v_{xp}^* and v_{xn}^* are the expected voltage of the upper and lower arms, respectively.

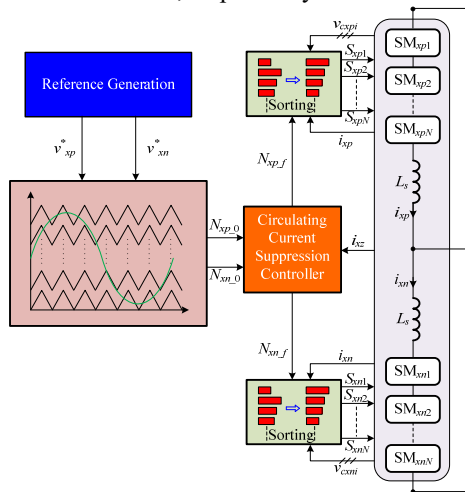


Fig. 4. Diagram of the operation principle of MMC.

The diagram of the operation principle of the MMC is shown in Fig. 4, where phase disposition pulse width modulation (PD-PWM) is adopted. According to the PD-PWM algorithm, the expected voltages v_{xp}^* and v_{xn}^* , as shown in (3), are compared with the carrier waveforms to determine the numbers of inserted submodule in upper and lower arms, which are expressed as $N_{xp,0}$ and $N_{xn,0}$, respectively. If the value of a carrier is smaller than that of the expected voltage, one of the submodules should be inserted. That is, the total number of these particular carriers with a smaller value than that of the expected voltage would be collected and saved as the primary number of the inserted submodules, namely $N_{xp,0}$ and $N_{xn,0}$. The final numbers of inserted submodules are defined as $N_{xp,f}$ and $N_{xn,f}$ for the upper and lower arms, respectively, and $N_{xp,f}$ and $N_{xn,f}$ are the output of the circulating current suppression control algorithm, as shown in Fig. 4. In order to implement the voltage balancing control for the capacitors of different

submodules in the same arm, sorting process is needed to give the operation states ($S_{xm1}, S_{xm2}, \dots, S_{xmN}$) of the submodules in each arm, where the final number of the inserted submodules, the direction of arm current and the capacitor voltages are the input variables. It should be noted that the submodule with lower capacitor voltage is preferentially selected to insert into the arm (inserted state) as the arm current is positive and vice versa.

III. OPEN-CIRCUIT FAULT OF POWER SWITCHING DEVICES

The reliability of the MMC system might be reduced due to large numbers of power switching device adopted in the MMC system. Once a failure happens to the power switching devices, the faulty device should be detected and located timely to avoid further failures on the MMC system.

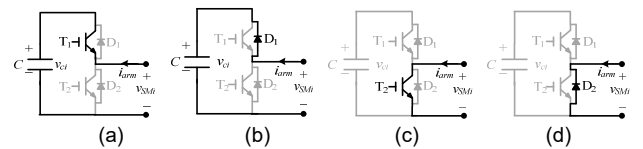


Fig. 5. Arm current paths. (a) Path 1: $S=1$ and $i_{arm}<0$, (b) path 2: $S=1$ and $i_{arm}>0$, (c) path 3: $S=0$ and $i_{arm}>0$, (d) path 4: $S=0$ and $i_{arm}<0$.

Fig. 5 shows the current paths at the normal state of the submodule, where total four current paths and two output voltage levels exist. Fig. 5(a) shows that, as $S=1$ and $i_{arm}<0$, the arm current discharges the capacitor through T_1 . In Fig. 5(b), as $S=1$ and $i_{arm}>0$, the arm current charges the capacitor through D_1 . Fig. 5(c) shows that, as $S=0$ and $i_{arm}>0$, the arm current goes through T_2 and has no effects on the capacitor voltage. It is shown in Fig. 5(d) that the arm current goes through D_2 and has no effects on the capacitor voltage as $S=0$ and $i_{arm}<0$.

In the case that open-circuit fault happens on the power switching devices, the current paths may be influenced and different from the normal. The arm current paths under T_1 and T_2 open-circuit faults are shown in Table I, where the arm current paths and relative status under normal state are also given for comparisons with each other. In Table I, it is obvious that only current path 1 and path 3 of the normal state are affected by T_1 and T_2 failures, respectively. That is, if the active current path is path 1 and T_1 open-circuit fault occurs simultaneously, the current path will be changed from path 1 to path 4, as shown in Table I with highlighting shadow. In another case, if the active current path is path 3 and T_2 open-circuit fault occurs, the current path will be changed to path 2. Due to the changing of the current path under fault conditions, the voltage of the power switching devices would be different from the normal state. Therefore, the fault diagnosis based on the voltage of the power switching devices will be very fast and reliable if this voltage could be measured and collected directly.

TABLE I
ARM CURRENT PATHS UNDER T_1 AND T_2 FAULTS

Normal state		Open-circuit fault	
Status	Current path	T_1	T_2
$S=1 \& i_{arm}<0$	Path 1	Path 4	Path 1
$S=1 \& i_{arm}>0$	Path 2	Path 2	Path 2
$S=0 \& i_{arm}>0$	Path 3	Path 3	Path 2
$S=0 \& i_{arm}<0$	Path 4	Path 4	Path 4

IV. PROPOSED FAULT DIAGNOSIS STRATEGY

A. Voltage Sensor Configurations

In the traditional MMC system, due to the requirement of capacitor voltage balancing, the voltage sensor is needed in each submodule which is directly parallel connected with the capacitor to obtain the capacitor voltage, as shown in Fig. 6(a). Fig. 6(b) shows that an additional voltage sensor is applied to measure the voltage of the upper power switching device, which may increase the response speed of fault diagnosis for the power switching devices. However, this will greatly increase the number of sensors where two voltage sensors are needed in one submodule.

To reduce the cost and improve the reliability of the MMC, the voltage sensor connected with the capacitor could be removed. Then, the proposed submodule with only one voltage sensor could be shown as Fig. 6(c). In [20-21] a fast fault diagnosis method is also proposed by connecting one voltage sensor with the lower power switching device in each submodule. However, the capacitor voltage would not be monitored when the submodule is on bypassed state, where the capacitor voltage is normally supposed keeping constant. At some specific conditions, the bypassed state would last for a relatively long time and then self-discharging of the capacitor will lead to large voltage deviations [23-24]. As an alternative selection, this paper sets the voltage sensor to connect with the upper switching device in each submodule. Due to the proposed position of the voltage sensor, not only a fast and reliable fault diagnosis, but also a simple and effective method to conduct capacitor monitoring could be realized, which will be discussed in Section V.

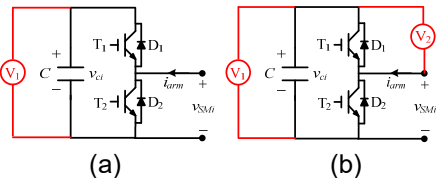


Fig. 6. Voltage sensors in one submodule. (a) The traditional case, (b) case with an additional voltage sensor, (c) proposed case.

B. Capacitor Voltage Monitoring

As mentioned in the above sub-section, keeping the capacitor voltages balancing is a critical issue for the operation of the MMC. In order to keep the capacitor voltage balancing, the capacitor voltage should be acquired by the control system at both the bypassed state and inserted state. If the voltage sensor in submodule is configured as Fig. 6(c), the capacitor voltage could be measured directly by the voltage sensor on the bypassed state. However, on the inserted state, the voltage sensor would be short-circuited by the upper power switching device. Then the capacitor voltage should be estimated by the observer in this case.

It should be noted that current sensors are necessary for the arms of MMC for the circulating current suppression control and capacitor voltage balancing control. Fig. 7 shows the equivalent circuits for the capacitor voltage monitoring on a different state, where only one current sensor is needed for each arm of the MMC due to the series connection of the submodules

in the same arm. On the bypassed state, the input current does not pass through the capacitor. The capacitor voltage can be directly measured by the voltage sensor, as shown in Fig. 7(a). Fig. 7(b) shows the submodule on inserted state with a short-circuited voltage sensor. As the submodule turns to inserted state, the current sensor is directly connected with the capacitor and the capacitor state may be monitored by this current sensor.

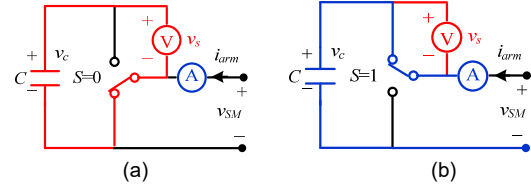


Fig. 7. Equivalent circuits for capacitor voltage monitoring on (a) bypassed state, (b) inserted state.

The voltage observation equation of the capacitor on the inserted state could be expressed as

$$v_c = v_{c0} + \frac{1}{C} \int_{t_0}^t i_{arm} dt \quad (t = t_0 + kT_{cc} \leq t_1) \quad (4)$$

where v_c is the observed capacitor voltage, T_{cc} is the control cycle of the system, k is number of the control cycles during the inserted state, v_{c0} is the last measured capacitor voltage, C is the nominal capacitance of the submodule capacitor, i_{arm} is the arm current, t_0 and t_1 are the start and end time of the inserted state, respectively. The initial voltage of the integral equation v_{c0} is the measured capacitor voltage at last time before this submodule is inserted.

$$v_{c0} = v_s \quad (5)$$

where v_s is the output of the voltage sensor on the bypassed state of the submodule. It can be seen from (4) that the deviations of capacitance C and current measurement would cause observation errors on capacitor voltage and affect the capacitor voltage balancing. However, the observation errors will be periodically eliminated on the bypassed state by the voltage sensor to renew the initial voltage for the capacitor voltage observation during the next inserted state. Then the observation errors are quite small and would be neglected in this paper since they could not be accumulated. It should be noted that in practical numerical system the control variables are discrete. The duration time of the inserted state is related to the control cycle and the integration in (4) starts at time t_0 with S stepping from 0 to 1, and finishes at time t_1 with S stepping from 1 to 0. The duration time of each inserted state could be obtained by a time accumulator at the arriving of time t_1 .

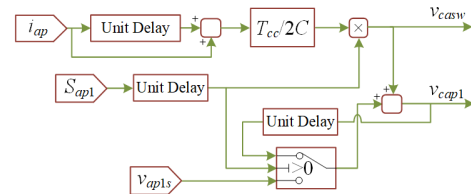


Fig. 8. Diagrams of the capacitor voltage monitoring.

On basis of the (4) and (5), Fig. 8 shows the diagrams of the capacitor voltage monitoring, where the first submodule in the upper arm of Phase A is taken as an example. T_{cc} is the control

cycle of the system, S_{ap1} is the operation state of this submodule, v_{ap1s} is the output voltage of the voltage sensor, v_{cap1} is the monitored capacitor voltage.

C. Fault Indicator

As analyzed in Section III, the current paths will be influenced by the open-circuit fault of the power switching devices, then the output of the voltage sensor could be used to implement the fast fault diagnosis of the MMC. The outputs of the voltage sensor under both the normal and fault states are listed in Tab. II. If the MMC is under normal state, the output of the voltage sensor would be zero on the inserted state and equal the capacitor voltage v_c on the bypassed state. Once a T_1 fault occurs with the status of $S=1$ and $i_{arm}<0$, the current path would shift to path 4, and the output of the voltage sensor would equal the capacitor voltage v_c , instead of zero. Once a T_2 fault occurs with the status of $S=0$ and $i_{arm}>0$, the current path would shift to path 2, and the output of the voltage sensor would be zero, instead of capacitor voltage v_c .

TABLE II
OUTPUTS OF VOLTAGE SENSOR UNDER DIFFERENT STATES

Status	Output of voltage sensor		
	Normal	T_1 fault	T_2 fault
$S=1 \& i_{arm}<0$	0 (0)*	v_c (1)	0 (0)
$S=1 \& i_{arm}>0$	0 (0)	0 (0)	0 (0)
$S=0 \& i_{arm}>0$	v_c (1)	v_c (1)	0 (0)
$S=0 \& i_{arm}<0$	v_c (1)	v_c (1)	v_c (1)

*In brackets shows the binary output of the voltage sensor.

Based on the Boolean logic operation, a fault indicator is introduced for the proposed fault diagnosis strategy. Firstly, the output of the voltage sensor is binarized instead of the measured value. The binarized output of the voltage sensor could be expressed as

$$\begin{cases} v_{sn} = 0 & (\frac{v_s}{v_0} < 0.5) \\ v_{sn} = 1 & (\frac{v_s}{v_0} \geq 0.5) \end{cases} \quad (6)$$

where v_{sn} is the binary output of the voltage sensor, v_0 is the reference voltage of the capacitor for capacitor voltage balancing control. The binary output is given in brackets shown as Tab. II.

Then the indicator of specific states of the submodule may be defined according to Tab. II and (6). Considering the operation state of the submodule S is also a binary value, the Boolean logic operation of S and v_{sn} can be treated to construct state indicators for this submodule. Based on the results of the Tab. II, an indicator of a normal state could be defined as

$$X_1 = S \oplus v_{sn} \quad (7)$$

where X_1 is the indicator of the normal state, " \oplus " is the Boolean logic operation for "exclusive or". $X_1=1$ indicates that the MMC is operating under the normal state, and $X_1=0$ indicates that the MMC is operating under fault state. Since there are two power switching devices in each submodule, the fault location should be further analyzed.

It is shown from Tab. I and Tab. II that only under the status of $S=1$ and $i_{arm}<0$, T_1 fault could be detected. Then an indicator

of T_1 fault could be defined as

$$X_2 = S \bullet v_{sn} \quad (8)$$

where X_2 is the indicator of T_1 fault, " \bullet " is a Boolean logic operation for "and". $X_2=1$ indicates that there is a T_1 fault in a certain submodule, and $X_2=0$ indicates that there is no T_1 fault.

Similar with T_1 fault, the T_2 fault could be detected only under the status of $S=0$ and $i_{arm}>0$. An indicator of T_2 fault could be defined as

$$X_3 = \bar{S} \bullet \bar{v}_{sn} \quad (9)$$

where X_3 is the indicator of T_2 fault, " $\bar{}$ " is the Boolean logic operation for "not". $X_3=1$ indicates that there is a T_2 fault in a certain submodule, and $X_3=0$ indicates that there is no T_2 fault.

Finally, a fault indicator X could be defined as

$$X = (X_1, X_2, X_3) \quad (10)$$

where $X_1, X_2,$ and X_3 are the indicator of a normal state, T_1 fault, and T_2 fault, respectively.

The process of fault diagnosis is shown in Fig. 9, where T_{cc} is the control cycle. The operation state of submodule S and the output of the voltage sensor v_s are collected to calculate the fault indicator X . There is no fault in the MMC system as the indicator X equals (1, 0, 0). If X does not equal (1, 0, 0) and the duration time reaches $T_{cc}/3$, it indicates that a fault has occurred. Then, X is compared with (0, 1, 0) and (0, 0, 1) in turns and the duration of the judgment will be $T_{cc}/3$ to avoid misjudgment. Here (0, 1, 0) and (0, 0, 1) are corresponding to T_1 fault and T_2 fault, respectively.

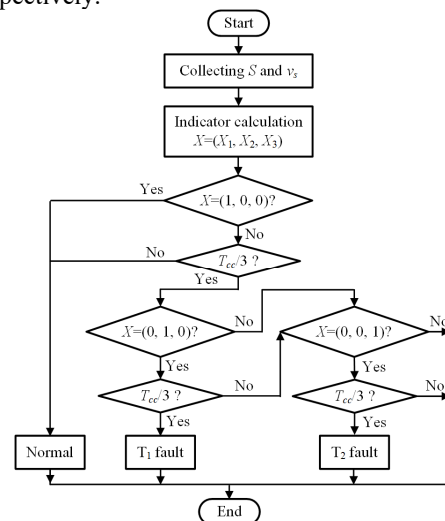


Fig. 9. Fault diagnosis process.

The fault indicator in the proposed fault diagnosis strategy is only related to the output of the voltage sensor and operation state of the submodule. Therefore, the fault diagnosis process is independent and can be implemented simultaneously in each submodule. In addition, if T_1 and T_2 faults occur in a submodule at the same time, only T_1 fault or T_2 fault could be detected in one control cycle, because the arm current cannot flow through T_1 and T_2 simultaneously. That is, as the arm current is negative, T_1 open-circuit fault in the inserted submodule could be detected. And as the arm current is positive, T_2 open-circuit fault in bypassed submodule could be detected. So the multiple faults in one submodule can be still detected. The fault location would be varied periodically between T_1 and T_2 , which is

determined by actual directions of the arm current.

V. CAPACITANCE MONITORING

There are a large number of capacitors in the MMC and the capacitance monitoring is an effective way to improve the reliability of the MMC system. In this paper, a quite easy strategy for capacitance monitoring is proposed due to the special configuration of the voltage sensor in the submodules. In this paper, the rate between the observed and measured voltage increment during the positive arm current is adopted as the indicator for capacitance monitoring.

Fig. 10 shows the shift of operation states in a submodule, where D_1 is the duration time of the inserted state when the arm current keeps positive. As mentioned before, the capacitor voltage may be directly measured at the state $S=0$, and observation of the capacitor voltage should be adopted at the state $S=1$. Supposing the measured voltage of the submodule capacitor in the previous cycle and the current cycle is v_1 and v_2 , respectively. The increment of measured capacitor voltage during period D_1 can be expressed as

$$\Delta v_{1m} = v_2 - v_1 = \frac{1}{C_a} \int i_{arm} dt \quad (11)$$

where Δv_{1m} is the increment of measured capacitor voltage during one switching cycle, C_a is the actual capacitance of the submodule capacitor. To realize capacitance monitoring, the increment of capacitor voltage is also calculated during the period D_1 on the inserted state ($S=1$) to obtain observed increment of capacitor voltage. It has

$$\Delta v_1 = \frac{1}{C} \int i_{arm} dt \quad (12)$$

where Δv_1 is the increment of observed capacitor voltage during one switching cycle. C is the nominal capacitance of the submodule capacitor. Then, the ratio of the increment between observed capacitor voltage and measured capacitor voltage can be obtained as follows

$$\frac{\Delta v_1}{\Delta v_{1m}} = \frac{\Delta v_1}{v_2 - v_1} = \frac{C_a}{C} \quad (13)$$

In this paper, only the period with positive arm current is used to monitor the capacitance, and there might be many switching cycles since the frequency of arm current is quite lower than the switching frequency of the submodule. So the calculations of (12) and (13) could be applied in multiple switching cycles. Supposing the period of the positive arm current in one submodule has k inserted states, it has

$$\left\{ \begin{array}{l} \frac{\Delta v_1}{\Delta v_{1m}} = \frac{\Delta v_1}{v_2 - v_1} = \frac{C_a}{C} \\ \frac{\Delta v_2}{\Delta v_{2m}} = \frac{\Delta v_2}{v_3 - v_2} = \frac{C_a}{C} \\ \vdots \\ \frac{\Delta v_k}{\Delta v_{km}} = \frac{\Delta v_k}{v_{k+1} - v_k} = \frac{C_a}{C} \end{array} \right. \quad (14)$$

(14) could be rewritten as

$$\frac{\Delta v_1 + \dots + \Delta v_i + \dots + \Delta v_k}{v_{k+1} - v_1} = \frac{C_a}{C} \quad (15)$$

where v_{k+1} is the measured capacitor voltage in last time

instance during the period of positive arm current. Since the capacitor is kept on charging operation during the period of the positive arm current, the measured voltages v_{k+1} and v_1 are the maximum and minimum voltage of the capacitor, respectively. It should be noted that Δv_i ($i=1, \dots, k$) have been calculated in (4) to observe the capacitor voltage for the normal operation of the MMC, which means the proposed capacitor monitoring strategy does not increase the calculation burden.

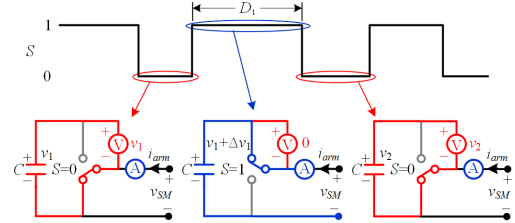


Fig. 10. The shift of operation states in a submodule ($i_{arm} > 0$).

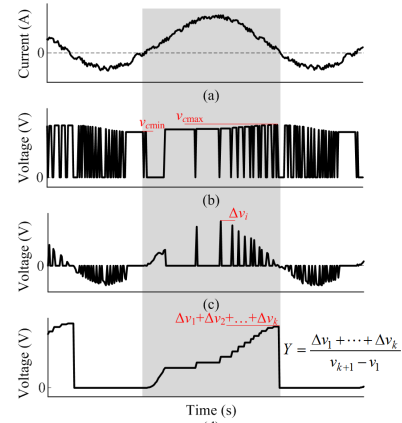


Fig. 11. The processing of the proposed capacitance monitoring strategy. (a) Arm current, (b) output of the voltage sensor, (c) increments of observed capacitor voltage, (d) sum of the increment of capacitor voltage ($i_{arm} > 0$).

The proposed capacitance monitoring strategy can be shown in Fig. 11. During the period of positive arm current, the capacitance monitoring is carried out, where the output of voltage sensor is varied between zero and measured capacitor voltage due to the voltage sensor periodically short-circuited by the upper power switching device. As shown in Fig. 11(b), the minimum and maximum measured capacitor voltage, v_{cmin} , and v_{cmax} , should be collected on the bypassed state of the submodule and recorded as v_{k+1} and v_1 , respectively. However, the voltage sensor is not directly connected with the capacitor and the output might be zero at the inserted state. Therefore, as an alternative, the maximum and minimum value of the measured capacitor voltage is obtained from the monitored voltage of the capacitor. It might cause a minor error, where the maximum error will be less than the integration increment of equation (12) in one switching cycle. Then the increment of the measured capacitor voltage during the period of positive arm current could be substituted. The increment of the observed capacitor voltage during each period D_1 is calculated according to (12), as shown in Fig. 11(c). Finally, the sum of increment of the observed capacitor voltage during the period of positive arm current can be used to construct an indicator for the capacitor monitoring as

$$Y = \frac{Y_1}{Y_2} = \frac{\Delta v_1 + \Delta v_2 + \dots + \Delta v_k}{v_{k+1} - v_1} \quad (16)$$

where Y is the monitoring indicator of the capacitance. Y_1 is the sum of the observed increment of capacitor voltage. Y_2 is the measured increment of capacitor voltage. The proposed indicator shows the ratio of actual capacitance to the nominal capacitance which would be a value less than 1 considering aging of the capacitors. For example, if Y equals 0.8, it means that only 80% of the nominal capacitance remains in this capacitor.

According to (12), Fig. 12 shows the diagram for the sum of observed increment of capacitor voltage during the inserted state under positive arm current. v_{casw} is the capacitor voltage increment during the inserted state, which has been calculated in Fig. 8.

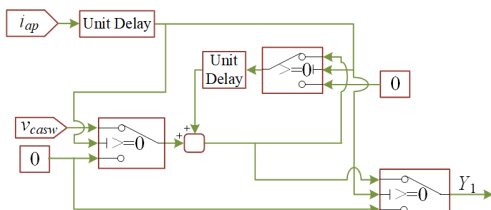


Fig. 12. Diagram for the sum of the observed increment of the capacitor voltage during the inserted state under positive arm current.

VI. EXPERIMENT VALIDATIONS

To verify the effectiveness of the proposed fault diagnosis strategy and capacitor monitoring method, a laboratory scaled single-phase MMC platform with four submodules in each arm is established because of the symmetrical structure of three-phase MMC, as shown in Fig. 13. The parameters of the experimental platform are listed in Tab. III. Same circulating current suppression control strategy as [25] is adopted in the MMC system.

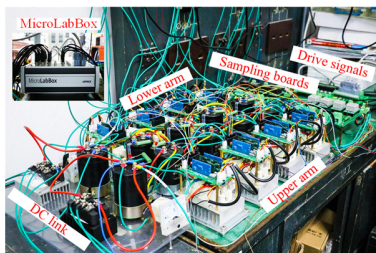


Fig. 13. The experimental platform of single phase MMC.

TABLE III
PARAMETERS OF EXPERIMENTAL PLATFORM

Symbol	Parameter	Values
V_{dc}	DC link voltage	200 V
v_{c0}	Rated capacitor voltage	50 V
m	Modulation index	0.85
C	Capacitance	2200 μ F
L_s	Arm inductance	4.3 mH
N	Number of submodules per arm	4
R	Load resistance	8 Ω
L	Load inductance	4.3 mH
f	Fundamental frequency	50 Hz
f_c	Carrier frequency	2 kHz

Fig. 11 shows that the voltage sensor should measure a step change waveform. However, the requirement for the bandwidth

of the voltage sensor is not high, since at the bypassed state the output of voltage sensor is used to renew the initial voltage v_{c0} in (4), and at the inserted state the output of voltage sensor is only just an indicator of the fault. Then a voltage sensor with 40 μ s response time is adopted in this experimental platform where the control cycle is 100 μ s.

A. Normal State Operation

Fig. 14 shows the experiment results under normal state. It can be seen from Fig. 14(a) that the AC output voltage is symmetrical with nine voltage levels. AC output current with good sinusoidal characteristics is shown in Fig. 14(b). The current waveforms of the upper and lower arms are shown in Fig. 14(c). The circulating current is under control and about 2 A, as shown in Fig. 14(d). Fig. 14(e) shows that all the capacitor voltages are balanced to be their reference voltage, 50 V.

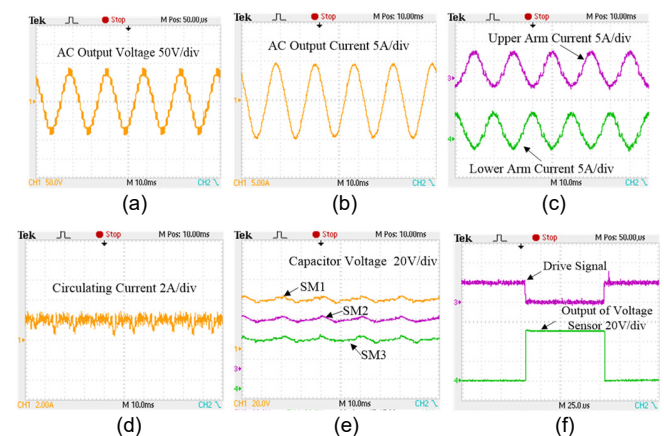


Fig. 14. Experiment results under normal state. (a) AC output voltage (10 ms/div), (b) AC output current (10 ms/div), (c) arm current (10 ms/div), (d) circulating current (10 ms/div), (e) capacitor voltage in upper arm (10 ms/div), (f) operation state and voltage sensor (25 μ s/div).

Fig. 14(f) shows the operation state and the output of the voltage sensor. As the submodule is on the inserted state where the drive signal is high, the output of the voltage sensor would be zero. As the submodule is on the bypassed state, the output of the voltage sensor is about 50 V.

According to the experiment results under a normal state, the MMC system with the proposed capacitor voltage observer could operate well.

The capacitance monitoring is carried out under the normal state. A healthy capacitor with nominal capacitance 2200 μ F is measured by LCR instrument in the laboratory and it shows that its actual capacitance is 2035.6 μ F, which is 92.53% of the nominal capacitance. Another capacitor is measured in the same laboratory, and its actual capacitance of the capacitor is 1032.6 μ F, 46.94% of the nominal capacitance 2200 μ F in this experiment. The capacitor with larger capacitance is set in SM1, and the capacitor with smaller capacitance is set in SM2. The experiment results of the capacitor monitoring for SM1 and SM2 are shown in Fig. 15. Fig. 15(a) shows the maximum value of measured capacitor voltage is 53.2 V, and its minimum value is 47.2 V. Then the increment of measured capacitor voltage could be obtained as 6 V. Fig. 15(a) also gives the increment of observed capacitor voltage as 5.68 V. Therefore, the indicator of capacitor monitoring for SM1 could be calculated as $Y=5.68/6=94.67\%$, which means the capacitance

of this capacitor in SM1 is 94.67% of the nominal value. It shows that the error between the observed and actual capacitance is only 2.14% of the nominal capacitance.

Fig. 15(b) shows the experiment results of capacitor monitoring for SM2. The indicator of capacitor monitoring for SM2 is 45%, and the error between the observed and actual capacitance is 1.94% of the nominal capacitance. It can be concluded from Fig. 15 that the presented capacitance monitoring strategy is effective.

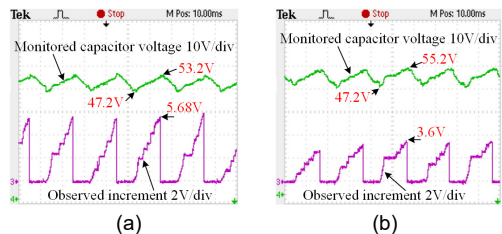


Fig. 15. Experiment results of capacitance monitoring in (a) SM1 (10 ms/div), (b) SM2 (10 ms/div).

B. Fault Diagnosis- T_1 Fault

Fig. 16 shows experiment results under T_1 fault in submodule SM1. In Fig. 16(a), the lowest voltage level is missing after T_1 fault happens in submodule SM1 and the AC output of the MMC only has eight voltage levels. The circulating current is shown in Fig. 16(b), where the reference value is no longer good followed once a T_1 fault occurs.

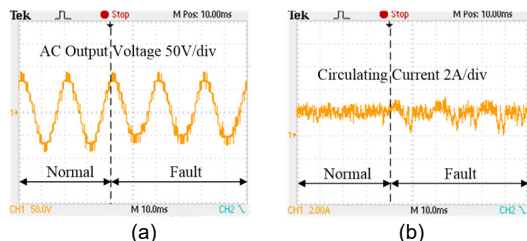


Fig. 16. Waveforms of voltage and current under T_1 fault. (a) AC output voltage (10 ms/div), (b) circulating current (10 ms/div).

Fig. 17 shows the waveforms of the operation state and the binarized output of the voltage sensor in the submodules. Under normal state, the operation state and the binarized output of the voltage sensor are opposites each other and then all the fault indicator X equals (1, 0, 0). However, as the T_1 fault occurs in SM1, the operation state and the output of the voltage sensor are both in a high level on the inserted state of SM1, as shown in Fig. 17(a). Then the fault indicator X of SM1 equals (0, 1, 0), and it indicates that SM1 is a faulty submodule and the faulty power switching device is T_1 . In Fig. 17(b)-(h), the operation state and the binarized output of the voltage sensor are always opposite under both the normal and fault states, which means the fault indicators X for SM2-8 equal (1, 0, 0). Therefore, SM2-8 are normal submodules, and the power switching device under T_1 fault is located within 300 μ s.

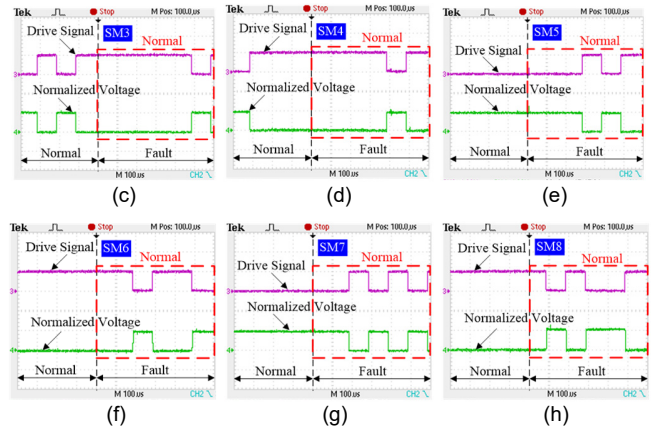
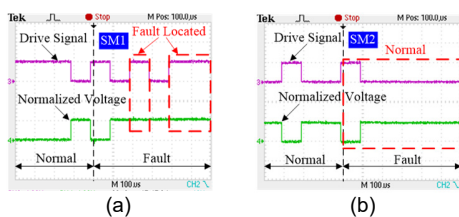


Fig. 17. Operation state and binarized output of voltage sensor under T_1 fault. (a) SM1 (100 μ s/div), (b) SM2 (100 μ s/div), (c) SM3 (100 μ s/div), (d) SM4 (100 μ s/div), (e) SM5 (100 μ s/div), (f) SM6 (100 μ s/div), (g) SM7 (100 μ s/div), (h) SM8 (100 μ s/div).

C. Fault Diagnosis- T_2 Fault

Fig. 18 shows the results under T_2 fault. In Fig. 18(a), AC output voltage with eight voltage levels is shown, where the highest level is missing after a T_2 fault. Fig. 18(b) shows the waveform of the circulating current, which shows the reference value could not be realized once the fault occurs.

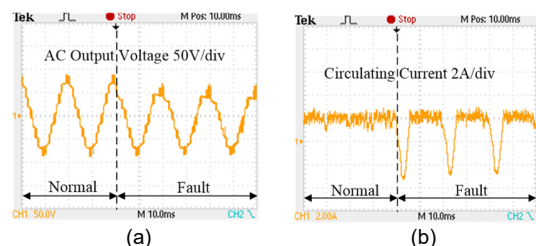
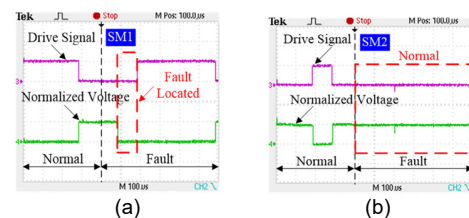


Fig. 18. Waveforms of voltage and current under T_2 fault. (a) AC output voltage (10 ms/div), (b) circulating current (10 ms/div).

Fig. 19 shows the waveforms of the operation states and the binarized output of voltage sensor in each submodule. In Fig. 19(a), the operation state and the binarized output of the voltage sensor in SM1 are always opposites under the normal state, and then X equals (1, 0, 0). However, as the T_2 fault occurs in SM1, operation state and binarized output of voltage sensor are both in the low level at the bypassed state of SM1, as shown in Fig. 19(a). Then X equals (0, 0, 1) and that indicates SM1 is a faulty submodule and the faulty power switching device is T_2 . It can be seen from Fig. 19(b)-(h) that the operation state and the binarized output of voltage sensor in SM2-8 are always opposite under both the normal and fault states. Therefore, SM2-8 are the normal submodules, and the power switching device under T_2 fault is located within 200 μ s.



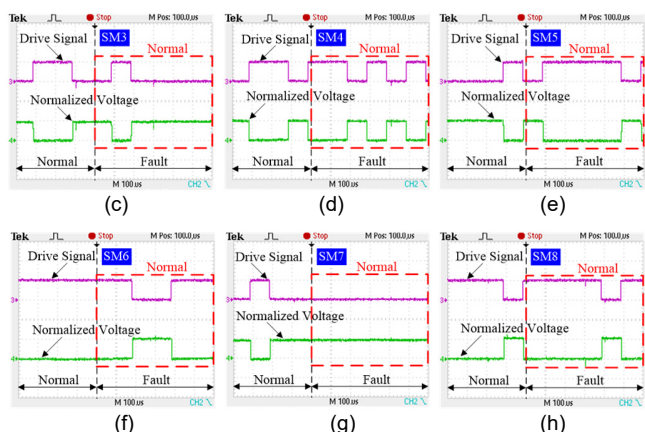


Fig. 19. Operation state and binarized output of voltage sensor under T_2 fault. (a) SM1 (100 μ s/div), (b) SM2 (100 μ s/div), (c) SM3 (100 μ s/div), (d) SM4 (100 μ s/div), (e) SM5 (100 μ s/div), (f) SM6 (100 μ s/div), (g) SM7 (100 μ s/div), (h) SM8 (100 μ s/div).

VII. CONCLUSIONS

In this paper, a fault diagnosis strategy is proposed to improve the reliability of the MMC system. To achieve a fast and reliable fault diagnosis, the voltage sensor in each submodule is relocated from the capacitor to the upper switching device. A fault indicator for the fault diagnosis is given based on the relationship of the operation state and binarized output of voltage sensors. Due to the proposed configuration of the voltage sensor in the submodule, voltage observation of the capacitor is put forward to realize capacitor monitoring and power control of the MMC under normal operation. The ratio of the increment of observed and measured capacitor voltage during the period of positive arm current is applied to monitor the capacitor and quite a high accuracy can be achieved. The experimental results verify the effectiveness of the proposed capacitor monitoring and fault diagnosis strategy.

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