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Abstract

This paper investigates two compact thermal model representations for multi-chip power modules, namely the thermal impedance matrix model and the thermal admittance matrix model. The latter can shape a multi-port thermal network without controlled temperature sources, and can be readily implemented in circuit simulators from the electrical engineer point of view. The mutual transformation between the two models and their relationship to parameters in the multi-port network are revealed. In addition, practical tips regarding the temperature recording and the curve-fitting in the process of the thermal model parameter extraction is discussed. The multi-port thermal model is verified by simulations and experimental results. It confirms that accurate temperature estimation can be achieved compared with the thermal model without the thermal coupling effect.

Preferred track (please, tick one or number 1 to 3 tracks in order of preference: 1 = most suiting, 3 = least suiting)

[ ] A - Quality and Reliability Assessment Techniques and Methods for Devices and Systems
[ ] B1 - Si Technologies & Nanoelectronics: Hot Carriers, High K, Gate Materials
[ ] B2 - Si Technologies & Nanoelectronics: Low K, Cu Interconnects
[ ] B3 - Si Technologies & Nanoelectronics: ESD, Latch-up
[ ] C - Progress in Failure Analysis: Defect Detection and Analysis
[ ] D - Reliability of Microwave and Compound Semiconductors Devices
[1] E1 - Power Devices Reliability: Silicon and Passive
[ ] E2 - Power Devices Reliability: Wide Bandgap Devices
[ ] F - Packaging and Assembly Reliability
[ ] G - MEMS, Sensors and Organic Electronics Reliability
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1. Introduction

In order to overcome the size constrain and to increase the power density, power electronics is moving towards a more compact multi-chip package [1], which inevitably leads to more serious thermal and corresponding reliability concerns [2]. Thus, thermal behaviour has to be carefully evaluated through thermal modelling. The thermal modelling of discrete device has been extensively studied [3]. However, for power modules with multi-chips, the thermal coupling effect has to be taken into account [4-5]. This issue can be addressed by compact thermal model (CTM) [6], which can be represented by two means. One is the thermal admittance matrix [7] as a general form of star-shaped models, and its fully mathematical criteria is reported in [8]. Another approach is the thermal impedance matrix [9]. One of their differences is that the thermal admittance matrix can shape a "topology" for that thermal system with a multi-port thermal network shown in Fig. 1, and all power losses behave just like the current flowing from one driving point to another. While for the thermal impedance matrix as shown in Fig. 2, controlled temperature sources have to be used. Thus, thermal network shaped by thermal admittance matrix is easier to implement in circuit simulators from electrical engineer point of view. On the other hand, the thermal model defined by thermal impedance matrix is more suitable for large-scale analytical calculation, such as the temperature estimation for long term mission profile. However, until now, no literature explains how to get the thermal parameters in the thermal network shown in Fig. 1. Thus, it will be one of the focus of this paper.

In addition, as mentioned in [10], the thermal impedance matrix can be fully defined by a $N\times N$ matrix while the dimension is N+1 for the thermal admittance matrix with N being the number of temperature nodes. This one additional dimension is mainly caused by the ambient temperature. As a matter of fact, if a linear thermal system dominated

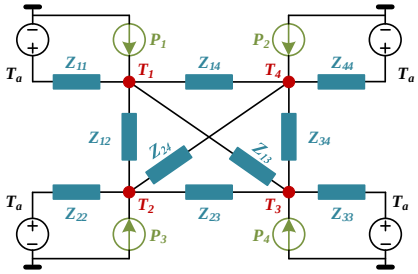

Fig. 1. Multi-port thermal coupling network derived from the thermal admittance matrix with 4 driving nodes.

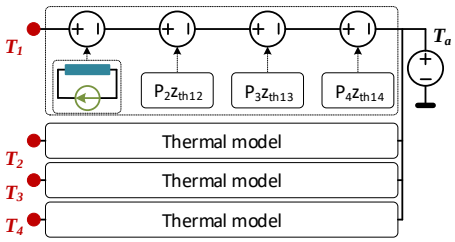

Fig. 2. Multi-port thermal coupling network derived from thermal impedance matrix with 4 driving nodes.

by thermal conduction is assumed, the ambient temperature will be just a potential reference, and has no impact on the thermal description of the thermal system. In this case, the thermal system can be fully defined by any N order impedance or admittance matrix through the temperature rise from ambient instead of the actual temperature. Thus, the focus of this paper is: how the two thermal matrices can be transformed between each other, and how to interpret them into the multi-port network shown in Fig. 1.

2. Two thermal model representations

Taking a thermal system with 4 nodes for example, all nodes can be fully coupled and be characterized through a 4×4 thermal impedance matrix expressed as $\Delta\boldsymbol{T}=\boldsymbol{\Psi P}$ in (1). The impedance matrix shapes a multi-port thermal network as shown in Fig. 2. It can be seen that, as a matter of fact, each temperature node has its own thermal model with the

coupling point of the ambient. Moreover, controlled temperature sources are needed in this model.

$$\begin{bmatrix}\Delta T_1\\ \Delta T_2\\ \Delta T_3\\ \Delta T_4\end{bmatrix}=\begin{bmatrix}\psi_{11} & \psi_{12} & \psi_{13} & \psi_{14}\\ \psi_{21} & \psi_{22} & \psi_{23} & \psi_{24}\\ \psi_{31} & \psi_{32} & \psi_{33} & \psi_{34}\\ \psi_{41} & \psi_{42} & \psi_{43} & \psi_{44}\end{bmatrix}\begin{bmatrix}P_1\\ P_2\\ P_3\\ P_4\end{bmatrix} \quad (1)$$

where ψ_{ii} is the thermal impedance between node i and the ambient T_a; P_i is power applied on node i; ψ_{ij} is the thermal impedance between node i and node j representing the thermal coupling effect between them; ΔT_i is the temperature difference between node i and the ambient.

It should also be noted that the thermal impedances ψ_{ij} do not correspond to the parameters Z_{ij} in the multi-port thermal network defined by thermal admittance matrix. Specifically, the power dissipation P_1 totally goes through ψ_{11} to generate the temperature rise of node T_1 in the thermal impedance matrix. However, in the multi-port thermal network shown in Fig. 1, the power is transferred through all available paths in a 3D manner. Thus, the parameter ψ_{ij} is a combined effect of all elements in the multi-port thermal network, and vice versa. To explore the relationship between the two matrixes, matrix transformation has to be conducted. For simplification, thermal conductance Y_{ij} is used instead of the thermal impedance Z_{ij}, which is simply the reciprocal of Y_{ij}.

Taking node T_1 in Fig. 1 for example, the heat flow balance equation is

$$\begin{pmatrix}(T_1-T_2)Y_{12}+(T_1-T_3)Y_{13}\\ +(T_1-T_4)Y_{14}+(T_1-T_a)Y_{11}\end{pmatrix}=P_1 \quad (2)$$

where Y_{ij} is the thermal conductance between node i and j, and $Y_{ij} = Y_{ji}$. Rearrange (2) to make sure that all temperatures are referred to the same reference T_a,

$$\begin{pmatrix}(Y_{11}+Y_{12}+Y_{13}+Y_{14})\Delta T_1\\ -Y_{12}\Delta T_2-Y_{13}\Delta T_3-Y_{14}\Delta T_4\end{pmatrix}=P_1 \quad (3)$$

Taking heat balance equations of all 4 nodes into account, and the matrix below can be obtained

$$\begin{bmatrix}P_1\\ P_2\\ P_3\\ P_4\end{bmatrix}=\begin{bmatrix}K_{11} & K_{12} & K_{13} & K_{14}\\ K_{21} & K_{22} & K_{23} & K_{24}\\ K_{31} & K_{32} & K_{33} & K_{34}\\ K_{41} & K_{42} & K_{43} & K_{44}\end{bmatrix}\begin{bmatrix}\Delta T_1\\ \Delta T_2\\ \Delta T_3\\ \Delta T_4\end{bmatrix} \quad (4)$$

where $K_{ii}=\sum_{j=1}^{4}Y_{ij}$, K_{ij} = -Y_{ij} $(i\neq j)$. The matrix equation can be further simplified as $\boldsymbol{P}=\boldsymbol{K}\Delta\boldsymbol{T}$, in which $\boldsymbol{K}$ is the thermal admittance matrix, and the relationship $\boldsymbol{\Psi}=\boldsymbol{K}^{-1}$ can be easily derived. It can be extended to thermal systems with N nodes by only changing the range of subscripts i and j to N.

Based on the analysis above, the relationship between the parameters $\boldsymbol{\Psi}$ and $\boldsymbol{Z}$ of the two multi-port thermal networks can be expressed in the following,

$$\begin{cases}K=\Psi^{-1}\\ Y_{ii}=\sum_{j=1}^{j=N}K_{ij},\ Y_{ij}=-K_{ij}(i\neq j)\\ Z_{ij}=\dfrac{1}{Y_{ij}}\end{cases} \quad (5)$$

Note that none of the parameters ψ_{ij}, K_{ij} , and Z_{ij} have physic meaning. All of them are a general thermal description between nodes. In addition, thermal parameters Z_{ij} may contain negative values if Foster RC model is used to fit the thermal transient, which could lead to convergence issues [11].

Moreover, to distinguish the two multi-port thermal coupling networks and their potential applications, their features are summarized as below:

1) The multi-port thermal network defined by thermal admittance matrix can be easily implemented without controlled temperature source, and the power can be transferred in a more "realistic" manner like current. Thus, it is a better option for engineers who prefer thermal model realization with thermal resistor and capacitor only.

2) The multi-port thermal network derived from the thermal impedance matrix can shape independent thermal model for each temperature node, and no coupling exists among nodes. Thus, it is suitable for fast temperature estimation with large-scale data processing, such as the junction temperature estimation for long-term mission profile.

3. Thermal impedance matrix extraction

The thermal impedance matrix are usually obtained from either simulation or experiment. The approach is to apply a step power on each chip of interest until the thermal steady-state is achieved. The on-state voltage drop and the current going through the device under test (DUT) are tested for power loss calculation before switching off the power supply. Then the temperature cooling curves of all chips are recorded simultaneously. In this paper, a four- chip half-bridge IGBT module F4 50R12KS4 from Infineon is used as the DUT. Note

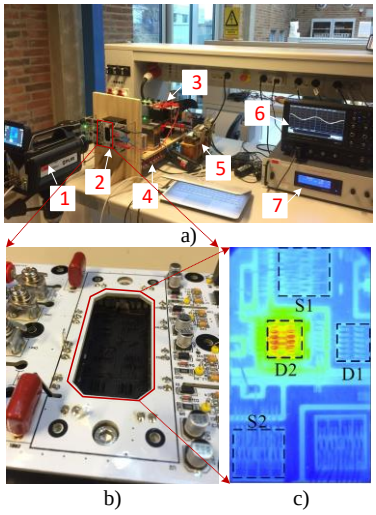

Fig. 2. a) Photo of the test bench (1: Thermal camera, 2: DUT, 3: device for current control, 4: controller, 5: inductor, 6: oscilloscope, 7: power supply.), b) Photo of submodule, and c) Temperature distribution of chips.

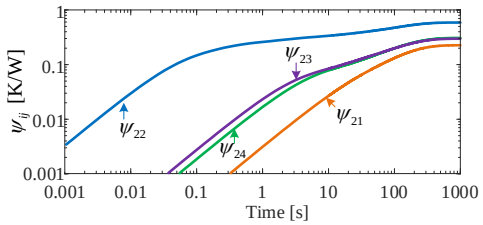

Fig. 3. Thermal impedances ψ_{ij} related to device S_2.

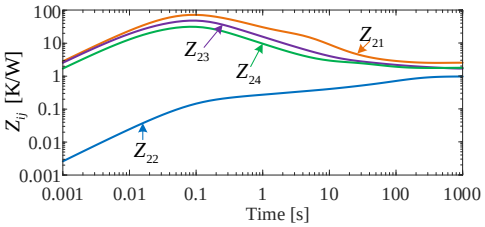

Fig. 4. Thermal impedances Z_{ij} related to device S_2.

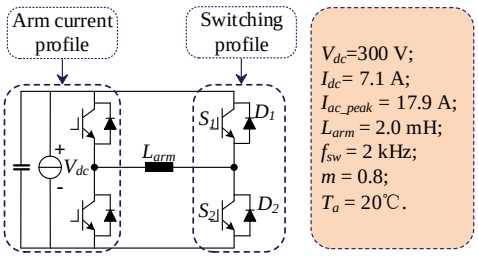

Fig. 5. Circuit topology and system parameters of the setup.

that to facilitate the temperature measurement by thermal camera as shown in Fig. 2, the IGBT has to be black painted. Based on the tested power loss and temperature responses, the self and mutual thermal impedances can be calculated by the temperature rise over the constant power dissipation. They can be further fitted into a series of Foster RC network and finally get the thermal impedance matrix $\boldsymbol{\Psi}$. Based on $\boldsymbol{\Psi}$ and the thermal model transformation method in section 2, the thermal admittance matrix $\boldsymbol{K}$ can be obtained. Fig. 3 and Fig. 4 show part of the thermal parameters of ψ_{ij} and Z_{ij}. As can be seen, different from the thermal impedance matrix with all values of its Foster model being positive, certain negative values can be expected for the Foster model of the thermal admittance matrix parameters. In addition, the thermal impedance matrix (t =1000 s) is illustrated in (6), in which the symmetrical characteristics (ψ_{ij} =ψ_{ji}) can be observed with a negligible difference caused by the measurement and the nonlinearity in the system.

$$\Psi_{t=1000\text{s}} = \begin{bmatrix} 0.5880 & 0.2244 & 0.3058 & 0.2961 \\ 0.2228 & 0.5353 & 0.2466 & 0.2452 \\ 0.2974 & 0.2512 & 0.6172 & 0.2933 \\ 0.2954 & 0.2466 & 0.3092 & 0.5995 \end{bmatrix} \quad (6)$$

Moreover, several practical tips are listed for the parameter extraction through experiments:

1) Cooling curve is preferred since a constant power dissipation is difficult to achieve due to the temperature-dependent output characteristic of power devices in the heating process.

2) It is sufficient to select a 4th or 5th order Foster model for main diagonal elements and 2nd or 3rd Foster model for non-diagonal elements, which depend on the characteristic of baseplate and heatsink with a relatively large time-constant [12].

4. Simulation and experiment validation

A series of simulations and experiments are conducted based on the multi-chip IGBT module mentioned in section 3. Its power loss characteristics are measured by power device analyzer under different temperature conditions. The tested on-state voltage and switching loss under different current are used in simulation thermal models.

To evaluate the accuracy of the two thermal model representations, the multi-chip IGBT module is set to operate under the same current and blocking voltage condition in both simulations and experiments. A sinusoidal current profile with a dc offset is applied to the device under test (DUT) to

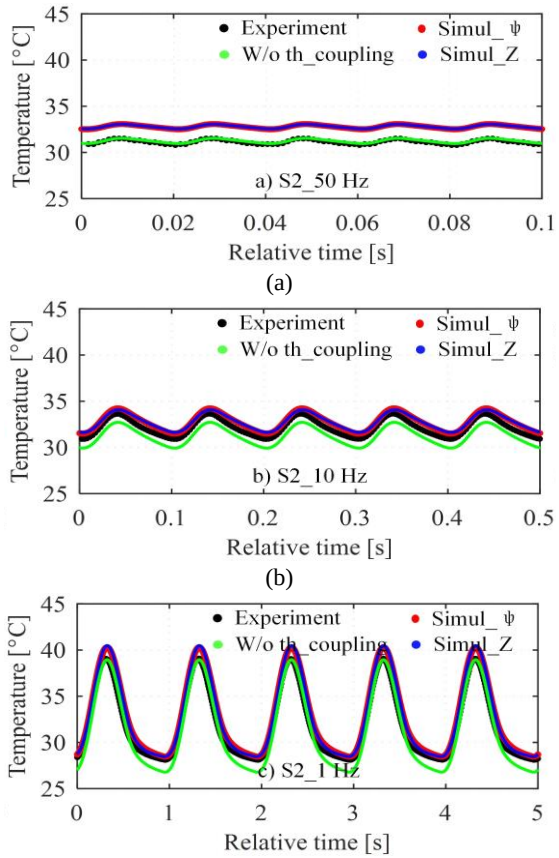

Fig. 6. Simulated and experimental steady-state junction temperature of device S_2 under different current profiles. a) 50 Hz, b) 10 Hz, and c) 1 Hz. (Black: experiment, red: simulation with Ψ matrix, blue: simulation with Z matrix, and green: simulation without thermal coupling.)

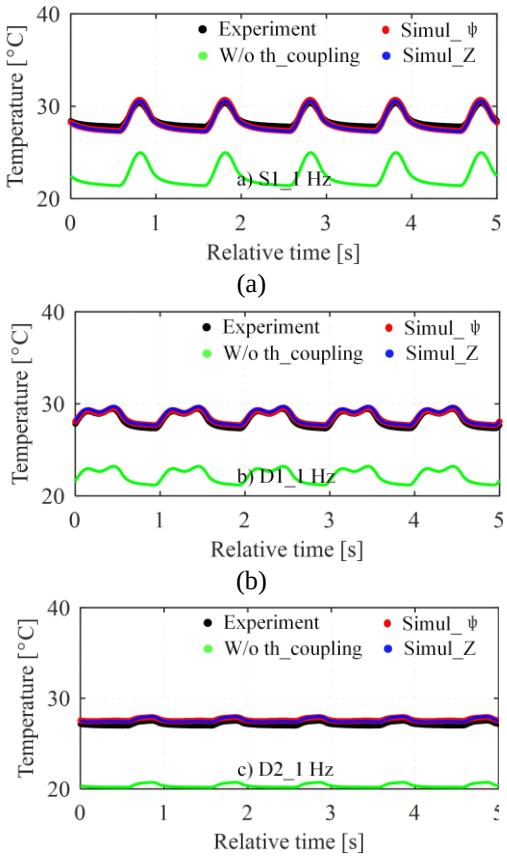

Fig. 7. Simulated and experimental steady-state junction temperature of the other three devices under 1 Hz current profile. a) S1, b) D1, and c) D2. (Black: experiment, red: simulation with Ψ matrix, blue: simulation with Z matrix, and green: simulation without thermal coupling.)

generate an unbalanced power dissipation among the four chips (4.3 W dissipated in S_1, 19.9 W for S_2, 3.5 W for D_1, and 0.6 W for D_2), which leads to more severe thermal coupling issue [13]. Fig. 5 shows the circuit topology of test bench made up of two half-bridges and one inductor. One half-bridge converter serves as the DUT, it is controlled by switching profile obtained from simulations. Another half-bridge converter functions to regulate the current going through the DUT. The main operating parameters are listed in Fig. 5. In this paper, three current profiles with different frequencies, namely 50 Hz, 10 Hz and 1 Hz, are utilized. Temperatures of the four devices under different current conditions are recorded and compared with the corresponding simulation results. Note that all temperatures are tested under the steady state with the ambient temperature being 20 ℃.

Fig. 6 shows the simulated and experimental steady state junction temperature of the most stressed device S2 under current profiles with different frequencies. It can be seen that junction temperature waveforms obtained from the two thermal matrixes coincide with each other, but shows a higher temperature than the experimental results. This confirms the equivalence of the two thermal model representations. In additional, the thermal model without considering the thermal coupling effect underestimates the temperature as indicated by the green line, and the estimation error becomes larger with the decrease of the current frequency. However, the error is about 1 ℃ and is small enough.

Fig. 7 shows the simulated and experimental steady-state junction temperature of other three

device (S_1, D_1 and D_2) under the same current profile with the frequency being 1 Hz. It can be clearly observed that the junction temperatures obtained by simulations based on the thermal impedance matrix $\boldsymbol{\Psi}$ are in well agreement with that from the thermal model represented by $\boldsymbol{Z}$ and experiments in terms of both average temperature and temperature variation. It further validates the equivalence of the two representations in linear thermal system applications. However, if the thermal coupling is neglected, the junction temperature of the three devices are all greatly under estimated with the error being up to 7°C. The reason is that in addition to the thermal coupling, the power dissipated in each node also has a great impact on the junction temperature. It means that S_2 dissipating the most power has the greatest thermal impact on the other devices, and the thermal impact of the other devices with less power loss on S_2 are negligible.

5. Conclusion

Two thermal model representations for multi-chip power modules and their mutual transformations are investigated in this paper. Based on this, two multi-port thermal networks are defined. The one shaped by the thermal admittance matrix can be easily implemented without controlled temperature source, and it could be a better option for engineers who prefer the thermal model realization with thermal resistor and capacitor only in circuit simulators. The multi-port thermal network defined by the thermal impedance matrix is characterized as independent thermal model for each node without coupling inside, it is suitable for temperature estimation with large-scale data processing. Simulation results obtained from the two multi-port networks and the experimental results validate the effectiveness and equivalence of the two methods.

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