A ZVZCS DC/DC Converter with Capacitive Output and Input-series Output-parallel (ISOP) Structure

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A ZVZCS DC/DC Converter with Capacitive Output and Input-series Ouput-parallel (ISOP) Structure

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***Abstract*—This paper proposes a zero-voltage and zero-current switching (ZVZCS) DC/DC converter characterized by 1) capacitive output and 2) input-series output-parallel (ISOP) structure for the high input voltage and high power applications. The proposed converter can reduce the circulating current and duty cycle loss in comparison with the conventional converter with the inductive output. More significantly, the proposed converter can also effectively reduce the ripple current on the secondary clamping capacitor. Therefore, the proposed converter can improve the reliability of the secondary clamping capacitor. The characteristics and performances of the proposed converter are analyzed in detail. Finally, the simulation results verify the proposed converter.**

Keywords—Capacitive output, input-series output-parallel (ISOP), ZVZCS DC/DC converter.

I. INTRODUCTION

The DC-DC converter is one of most important kinds of power electronics converters to adjust the voltage levels for DC applications [1-6]. Conventional DC/DC converters with the inductive output had been widely used due to simple realization of soft switching, compact circuit structure [7-9]. However, this converter has three major drawbacks: 1) narrow zero-voltage switching (ZVS) range for the lagging switches, which increases the power devices' switching losses at the light load; 2) high circulating current during the free-wheeling time periods, especially for the large phase-shift angle, which increases the power devices' conduction losses; and 3) high duty cycle loss, especially for the high primary current and low input voltage, which reduce the effective duty cycle.

The zero-voltage and zero-current switching (ZVZCS) DC/DC converter is one of most attractive candidates to solve these problems. In the ZVZCS DC/DC converter, the leading and lagging switches can realize the ZVS and ZCS, respectively. In addition, the power devices of the output rectifier can also realize zero-current switching (ZCS). Many studies about the ZVZCS DC/DC converter have been done [10-19]. The ZVZCS DC/DC converters can be mainly classified into two types named primary reset [10-14], and secondary reset [15-19]. Table I shows the comparison results between the primary reset and secondary reset ZVZCS DC/DC converters. Base on the analysis results in Table I, the secondary reset ZVZCS DC/DC converter with only secondary clamping capacitor has the more compact circuit structure and is thus more suitable for the high power density applications. However, the high ripple current on the secondary clamping capacitor is one of most important limitations which leads it not being widely applied.

In this paper, a ZVZCS DC/DC converter is proposed for the high input voltage and high power applications. The proposed converter is characterized by 1) capacitive output and 2) input-series output-parallel (ISOP) structure. In comparison with the conventional converter with the inductive output, the proposed converter can reduce the circulating current and duty cycle loss. More importantly, the proposed converter can also effectively reduce the ripple current flowing through the secondary clamping capacitor, which could thus improve the reliability of the secondary clamping capacitor. The characteristics and performances of the proposed converter are analyzed in detail. Finally, the simulation results are presented to verify the proposed converter.

This paper is organized as follows. Section II introduces the circuit structure of the proposed converter and analyzes the operation principle of the proposed converter in detail. Section III analyzes the characteristics and performances of the proposed converter. Section IV presents the simulation results to verify the effectiveness and feasibility of the proposed converter. Finally, the main contributions of this paper are summarized in Section V.

II. PROPOSED CONVERTER

A. Circuit Structure

Fig. 1 shows the circuit structure of the proposed converter. In Fig. 1, C_1 and C_2 are two input capacitors, which split the input voltage V_{in} into two voltages V_1 and V_2; $S_1 - S_8$ are primary power switches; T_{r1} and T_{r2} are two isolated transformers; L_{r1} is the leakage inductance of T_{r1} plus the added transformers; L_{r1} is the leakage inductance of T_{r1} plus the added inductance in series with T_{r1}; L_{r2} is the leakage inductance of T_{r2} plus the added inductance in series with T_{r2};L_{m1} and L_{m2} are magnetizing inductance of T_{r1} and T_{r2} respectively; $D_{r1} - D_{r8}$ are four output rectifier diodes; C_o is the secondary clamping capacitor.

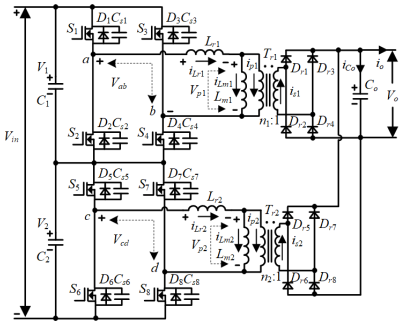


Fig. 1. Circuit structure of proposed converter.

TABLE I. COMPARISON RESULTS BETWEEN PRIMARY AND SECONDARY RESET ZVZCS DC/DC CONVERTER

	Method	Merits	Limitations
Primary reset ZVZCS	Adding extra power devices (diodes or power switches) and capacitor [8-10]	Applicable of inductive output (low ripple current on the output filter capacitor)	High cost Complex circuit structure
	Adding multi-port transformer [11], [12]		Complex circuit structure
Secondary reset ZVZCS	Adding power devices and secondary clamping capacitor [13], [14]	Simple implementation Simple circuit structure	Hard switching of the secondary reset devices
	Only adding secondary clamping capacitor [15-17]		High ripple current on the secondary clamping capacitor High capacitance of secondary clamping capacitor

In Fig. 1, V_{ab} and V_{cd} are two primary voltages; i_{Lr1} and i_{Lr2} are the primary current on L_{r1} and L_{r2} respectively; i_{Lm1} and i_{Lm2} are the current on L_{m1} and L_{m2} respectively; i_{p1} and i_{p2} are the primary current of T_{r1} and T_{r2}; i_{Co} is the ripple current on C_o; V_o and i_o are output voltage and output current.

B. Operation Principle

Before analyzing the operation principle of the proposed converter, some assumptions as below are made to simply the analysis.

- The input capacitors C_1 and C_2 are large enough to be regarded as the voltage sources and $C_1 = C_2 = C_{in}$, $V_1 = V_2 = V_{in}/2$.
- The parameters of two transformers $Tr1$ and $Tr2$ are identical, having same turns ratios $n_1 = n_2 = n$ and same inductances $Lr1 = Lr2 = Lr$, $Lm1 = Lm2 = Lm$.
- The secondary clamping capacitor C_o is large enough to be regarded as a voltage source, which means output voltage V_o and output current i_o are constant.

Fig. 2 shows the operation principle of the proposed converter.

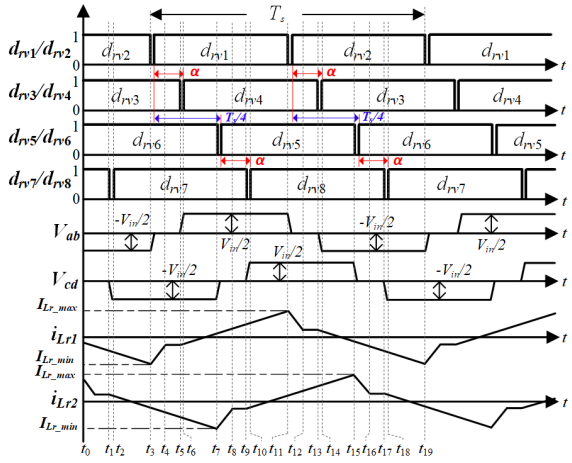
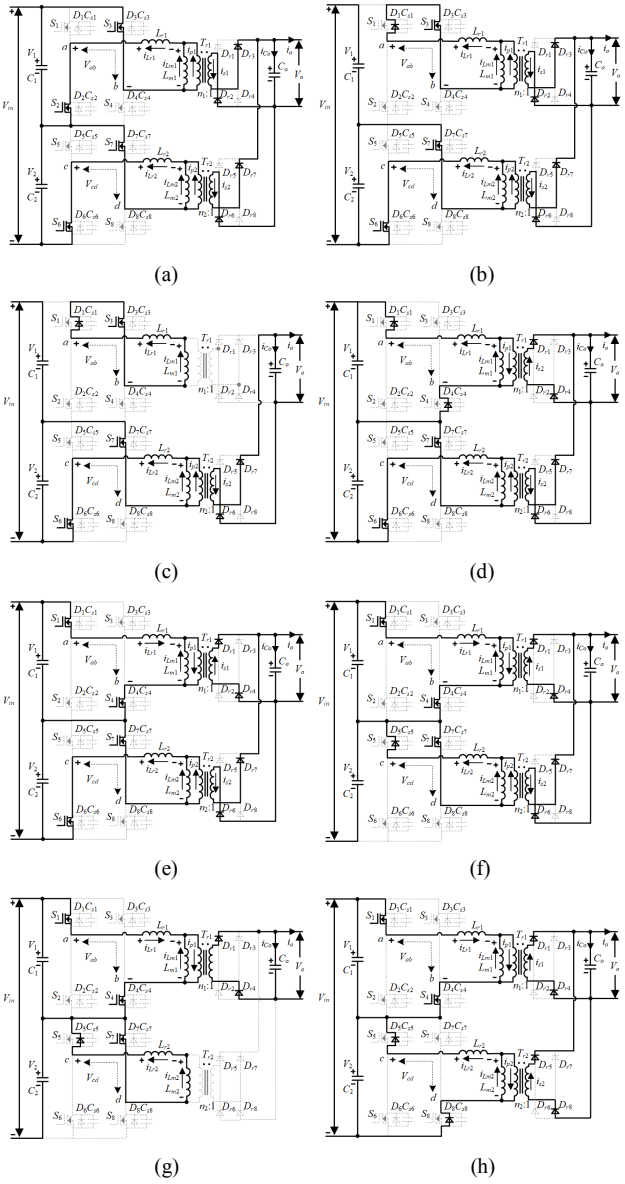


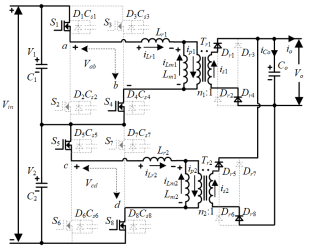
Fig. 2. Operation Principle of proposed converter.

In Fig. 2, $d_{rv1} - d_{rv8}$ are driving signals for primary power switches $S_1 - S_8$; T_s is one switching period; (S_1, S_2), (S_3, S_4), (S_5, S_6), and (S_7, S_8) are complementary switch pairs; α is the phase shift time of switch pairs (S_1, S_4), (S_2, S_3), (S_5, S_8), and (S_6, S_7); the phase shift time of switch pairs (S_1, S_5), (S_2, S_6), (S_3, S_7), and (S_4, S_8) are $T_s/4$. I_{Lr_max} and I_{Lr_min} are the maximum and minimum value of the currents i_{Lr1}, i_{Lr2}.

Fig. 3 shows the equivalent operation circuits during the half switching period.

Stage 0 [before t_3] The switches S_2, S_3, S_6, and S_7 are all in on-state. The primary currents i_{Lr1} and i_{Lr2} both decreases linearly. The secondary currents i_{s1} and i_{s2} flow through D_{r2}, D_{r3} and D_{r6}, D_{r7} respectively to the secondary clamping capacitor and load.





(i)

Fig. 3. Equivalent operation circuits. (a) [before t_3]. (b) [$t_3 - t_4$]. (c) [$t_4 - t_5$]. (d) [$t_5 - t_6$]. (e) [$t_6 - t_7$]. (f) [$t_7 - t_8$]. (g) [$t_8 - t_9$]. (h) [$t_9 - t_{10}$]. (i). [$t_{10} - t_{11}$].

Stage 1 [$t_3 - t_4$] At t_3, the switch S_2 is turned off, then the primary current i_{Lr1} starts to increase linearly because the voltage on L_{r1} is $n*V_o$. During this time period, the switch S_1 can be turned on with zero voltage. The secondary current i_{s1} still flows through D_{r2} and D_{r3} to the output. In addition, the switches S_6 and S_7 remains in on state, so the primary current i_{Lr2} continues to decrease linearly because the voltage on L_{r2} is $-(V_{in}/2-n*V_o)$. The secondary current i_{s2} flows through D_{r6} and D_{r7} to the output. The expressions of i_{Lr1} and i_{Lr2} can be obtained by (1) and (2). The expressions of i_{Lm1} and i_{Lm2} can be obtained by (3) and (4).

$$i_{Lr1} = i_{Lr1}(t_3) + \frac{n \cdot V_o}{L_r} \cdot (t - t_3) \tag{1}$$

$$i_{Lr2} = i_{Lr2}(t_3) - \frac{V_{in}/2 - n \cdot V_o}{L_r} \cdot (t - t_3) \tag{2}$$

$$i_{Lm1} = i_{Lm1}(t_3) - \frac{n \cdot V_o}{L_m} \cdot (t - t_3) \tag{3}$$

$$i_{Lm2} = i_{Lm2}(t_3) - \frac{n \cdot V_o}{L_m} \cdot (t - t_3) \tag{4}$$

Stage 2 [$t_4 - t_5$] At t_4, the primary current i_{Lr1} increases to the value of the current on the magnetizing inductance i_{Lm1}. Then, D_{r2} and D_{r3} turn off with zero current and the primary voltage V_{p1} become zero, so i_{Lr1} and i_{Lm1} become the same and kept at a constant value obtained by (5) during this time period. In addition, the primary current i_{Lr2} decreases linearly during this time period.

$$\begin{aligned} & i_{Lr1\_t4} = i_{Lm1\_t4} \\ & i_{Lr1}(t_3) + \frac{n \cdot V_o}{L_r} \cdot (t_4 - t_3) = i_{Lm1}(t_3) - \frac{n \cdot V_o}{L_m} \cdot (t_4 - t_3) \end{aligned} \tag{5}$$

Stage 3 [$t_5 - t_6$] At t_5, the switch S_3 is turned off with almost zero current because the magnetizing inductance L_{m1} is relatively huge and the current on the magnetizing inductance i_{Lm1} is very small. Then, i_{Lr1}, i_{Lm1} both begin to increase linearly and D_{r1}, D_{r4} conducts. Therefore, the secondary current i_{s1} flows through D_{r1} and D_{r4}. During this time period, the primary current i_{Lr2} decreases linearly.

$$i_{Lr1} = i_{Lr1}(t_5) + \frac{V_{in}/2 - n \cdot V_o}{L_r} \cdot (t - t_5) \tag{6}$$

Stage 4 [$t_6 - t_7$] At t_6, the switch S_4 is turned on. During this time period, the primary current i_{Lr1} increases linearly and i_{Lr2} decreases linearly. At t_7, the primary current i_{Lr2} reaches to its minimum value I_{Lr1_min}.

Stage 5 [$t_7 - t_8$] At t_7, the switch S_6 is turned off, then the primary current i_{Lr2} starts to increase linearly because the voltage on L_{r2} is $n*V_o$. During this time period, the switch S_5 can be turned on with zero voltage. The secondary current i_{s2} flows through D_{r6} and D_{r7} to the secondary clamping capacitor C_o and load. In addition, the switches S_1 and S_4 are both in on state and the primary current i_{Lr1} increases linearly because the voltage on L_{r2} is $V_{in}/2+n*V_o$. The secondary current i_{s1} flows through D_{r1} and D_{r4} to the secondary clamping capacitor C_o and load.

$$i_{Lr2} = i_{Lr1}(t_7) + \frac{n \cdot V_o}{L_r} \cdot (t - t_7) \tag{7}$$

Stage 6 [$t_8 - t_9$] At t_8, the primary current i_{Lr2} increases to the value of current on the magnetizing inductance i_{Lm2}. Then, D_{r6} and D_{r7} turn off and the primary voltage V_{p2} become zero, so the i_{Lr2} and i_{Lm2} become the same and kept at a constant value obtained by (8) during this time period. In addition, the primary current i_{Lr1} increases linearly during this time period.

$$\begin{aligned} & i_{Lr2\_t8} = i_{Lm2\_t8} \\ & i_{Lr2}(t_7) + \frac{n \cdot V_o}{L_r} \cdot (t_8 - t_7) = i_{Lm2}(t_7) - \frac{n \cdot V_o}{L_m} \cdot (t_8 - t_7) \end{aligned} \tag{8}$$

Stage 7 [$t_9 - t_{10}$] At t_9, the switch S_7 is turned off with almost zero current because the magnetizing inductance L_{m2} is relatively huge and current on the magnetizing inductance i_{Lm2} is very small. Then, i_{Lr2} and i_{Lm2} both begin to increase linearly and D_{r5}, D_{r8} conduct. Therefore, the secondary current i_{s2} flows through D_{r5} and D_{r8}. During this time period, the primary current i_{Lr1} still increases linearly.

Stage 8 [$t_{10} - t_{11}$] At t_{11}, the switch S_1 is turned on. During this time period, the primary currents i_{Lr1} and i_{Lr2} both increases linearly. At t_{11}, the primary current i_{Lr1} reaches to its maximum value.

At t_{11}, the next half switching period [$t_3 - t_{11}$] starts, the analysis of [$t_3 - t_{11}$] is similar to that of the first half switching period [$t_{11} - t_{19}$], which thus does not repeat here.

III. Characteristics and Performances

A. Ouput Characteristic

Three time periods in Fig. 2 are defined by (9), (10), and (11), respectively.

$$\Delta t_1 = t_4 - t_3 \tag{9}$$

$$\Delta t_2 = t_5 - t_4 \tag{10}$$

$$\Delta t_3 = t_{11} - t_5 \tag{11}$$

The following seven equations (12) – (19) can be obtained, in which f_s is the switching frequency of the primary power switches.

$$I_{Lr\_\min} + I_{Lr\_\max} = 0 \tag{12}$$

$$I_{Lr\_\min} + \frac{n \cdot V_o}{L_r} \cdot \Delta t_1 + \frac{V_{in}/2 - n \cdot V_o}{L_r} \cdot \Delta t_3 = I_{Lr\_\max} \tag{13}$$

$$I_{Lm\_\min} + I_{Lm\_\max} = 0 \tag{14}$$

$$I_{Lm\_\min} + \frac{n \cdot V_o}{L_m} \cdot (\Delta t_1 + \Delta t_3) = I_{Lm\_\max} \tag{15}$$

$$I_{Lr\_\min}+\frac{n\cdot V_o}{L_r}\cdot\Delta t_1=I_{Lm\_\min} \tag{16}$$

$$\Delta t_1+\Delta t_2+\Delta t_3=\frac{1}{2\cdot f_s} \tag{17}$$

$$\Delta t_1+\Delta t_2=\alpha \tag{18}$$

Therefore, based on (12) – (19), the output voltage V_o can be obtained by (20).

$$V_o=\frac{L_m\cdot V_{in}^2\cdot\left(2\cdot\alpha\cdot f_s-1\right)^2}{2\cdot n\cdot V_{in}\cdot\left(L_m+L_r\right)\cdot\left(2\cdot\alpha\cdot f_s-1\right)^2+8\cdot i_o\cdot f_s\cdot L_r\cdot\left(L_m+L_r\right)} \tag{20}$$

B. Soft Switching Perforamnces

For the leading switches S_1, S_2, S_5, and S_6, ZVS can be realized.

In the practical applications, the magnetizing inductance of the transformer is normally much larger than that of the leakage inductance plus added inductance, which means that the turn-off current of lagging switches would be very small. Therefore, the lagging switches S_3, S_4, S_7, and S_8 can realize the ZCS.

C. Ripple currents on Secondary Clamping Capacitor

In Fig. 1, the ripple current on the secondary clamping capacitor i_{co} can be expressed by (21) according to the Kirchhoff's Current Law (KCL).

$$i_{Co}=\left|i_{s1}\right|+\left|i_{s1}\right|-i_o \tag{21}$$

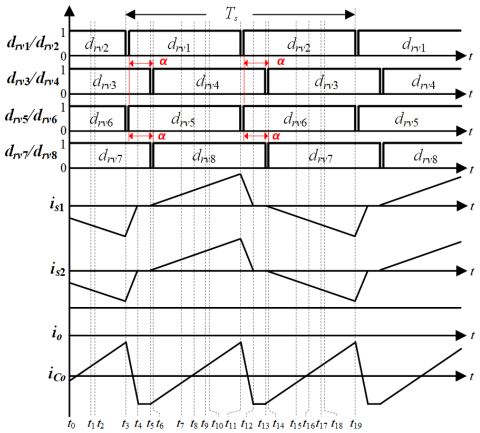
Figs. 4(a) and 4(b) shows the secondary currents (i_{s1}, i_{s2}), ripple current on the secondary clamping capacitor i_{co}, and output current i_o without and with the interleaving strategy respectively. From Fig. 4, it can be observed the ripple current on the secondary clamping capacitor can be highly reduced by using the ISOP circuit structure with the interleaving strategy in comparison with that without interleaving strategy.

According to Fig. 4, $|i_{s1}|$, $|i_{s2}|$, and i_o can be obtained by (22), (23), and (24), respectively.

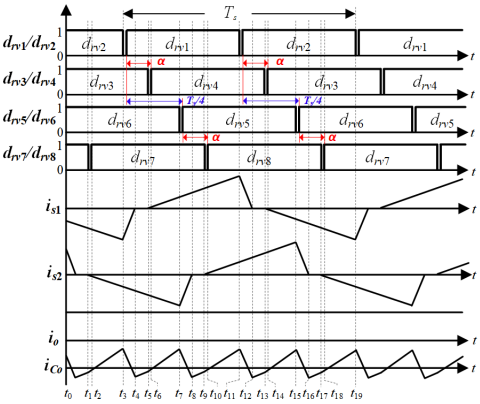
$$\left|i_{s2}(t)\right|=\left|i_{s1}(t-\frac{T_s}{4})\right| \tag{23}$$

$$i_o(t)=P_o/V_o^2 \tag{24}$$

According to (22) – (24), the root mean square (RMS) value of i_{Co_rms} can be obtained by (25) in Appendix.



(a)



(b)

Fig. 4. Operation waveforms of i_{s1}, i_{s2}, i_{co}, and i_o. (a) w/o interleaving strategy. (b) w/ interleaving strategy.

$$\frac{\int_0^{\Delta t3}\left(\frac{V_{in}/2-n\cdot V_o}{L_r}\cdot t-\frac{n\cdot V_o}{L_m}\cdot t\right)\mathrm{d}t+\int_0^{\Delta t1}\left[I_{Lr\_\max}-\frac{n\cdot V_o}{L_{r1}}\cdot t-\left(I_{Lm\_\min}+\frac{n\cdot V_o}{L_m}\cdot\Delta t_3+\frac{n\cdot V_o}{L_m}\cdot t\right)\right]\mathrm{d}t}{1/\left(2\cdot f_s\right)}=\frac{I_o}{2\cdot n} \tag{19}$$

$$\left|i_{s1}(t)\right|=\begin{cases}n\cdot\left[I_{Lm1\_\min}-I_{Lr1\_\min}+\frac{n\cdot V_o}{L_{m1}}\cdot(t_4-t_3)-\left(\frac{n\cdot V_o}{L_{m1}}+\frac{n\cdot V_o}{L_{r1}}\right)\cdot\left(t-t_3\right)\right] & [t_3,t_4]\\ 0 & [t_4,t_5]\\ n\cdot\left[\left(\frac{V_{in}-n\cdot V_o}{L_{r1}}-\frac{n\cdot V_o}{L_{m1}}\right)\cdot\left(t-t_5\right)\right] & [t_5,t_{11}]\end{cases} \tag{22}$$

$$\left|i_{s1}(t+k\cdot\frac{T_s}{2})\right|=\left|i_{s1}(t)\right|\quad[t_3,t_{11}]\qquad k=\pm1,\pm2,\pm3\ldots$$

IV. SIMULATION VERIFICATION

In order to verify the proposed converter, a simulation model is established in PLECS. After changing the capacitive output to the inductive output in the proposed converter, the proposed converter with the inductive output is similar to the conventional converter with the inductive output. Therefore, the proposed converter with the inductive output is also established in PLECS for comparison. Table II shows the circuit parameters of the established two simulation models.

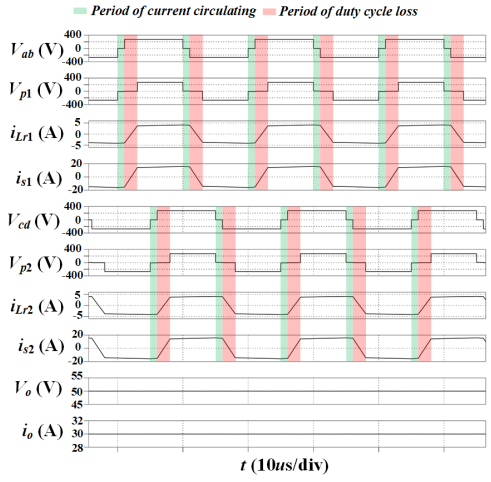
TABLE II. CIRCUIT PARAMETERS OF SIMULATION MODELS

Description	Parameter	
	Inductive output	Capacitive output
Input voltage (V)	550	
Output voltage (V)	50	
Output power (W)	1500	
Input capacitors C_1 and C_2 (uF)	470	
Switching frequency f_s (kHz)	50	
Magnetizing inductance L_m	infinity	
Turns ratios of T_{r1} and T_{r2}	3.8 : 1	5.2 : 1
Leakage inductance L_r (uH) plus added inductance if needed	70	20
Secondary clamping inductors (uH)	100	/
Secondary clamping capacitor C_o (uF)	/	100

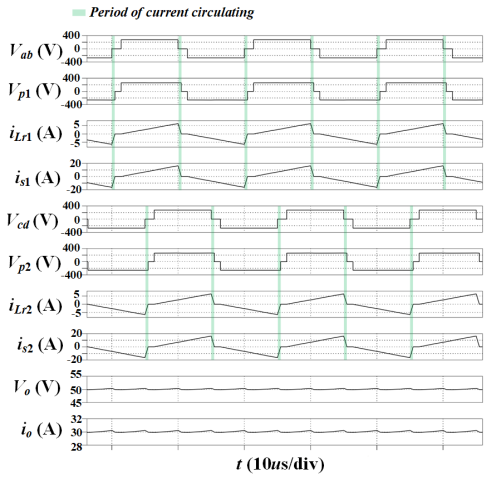
Note: Under the inductive output, the value of leakage inductance plus added inductance is selected according to the requirement of realizing ZVS of lagging switches above 16% of the output power and used parasitic parameter of power switch for calculation is from the datasheet of SPW47N60C3.

Fig. 5 shows the simulation results about V_{ab}, V_{cd}, V_{p1}, V_{p2}, i_{Lr1}, i_{Lr2}, i_{s1}, i_{s2}, V_o, and i_o with the inductive output and capacitive output, respectively. From Fig. 5, it can be observed that 1) with the inductive output, the time periods of the circulating current and duty cycle loss are large as marked by green and red color in Fig. 5(a). 2) With the capacitive output, the time periods of the circulating current are small as marked by green color in Fig. 5(a) and there is no duty cycle loss.

Table III shows the comparison results about the currents on the primary power switches, transformers, and rectifier diodes between the inductive output and capacitive output. From Table III, it can be seen that the RMS value of the currents on $S_1 - S_8$ when using the capacitive output is smaller than that when using the inductive output, which means that the conduction loss of primary power switches would be smaller when using the capacitive output.



(a)



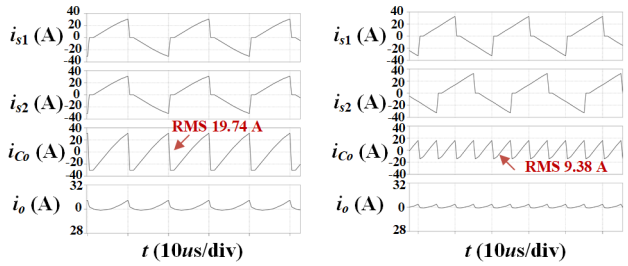
(b)

Fig. 5. Simulation results including V_{ab}, V_{cd}, V_{p1}, V_{p2}, i_{Lr1}, i_{Lr2}, i_{s1}, i_{s2}, V_o, and i_o (P_o = 1500 W) (a) Inductive output (α=1.05 us). (b) Capacitive output (α=1us).

TABLE III. COMPARISON RESULTS ABOUT COMPONENTS' CURRENTS

	Inductive output	Capacitive output
RMS current on S_1 - S_8 (A)	2.608	2.464
RMS current on T_{r1} and T_{r2} (A)	3.69	3.484
Average current on D_{r1} - D_{r4} (A)	7.498	7.49

Figs. 6(a) and 6(b) show the simulation results about the ripple current on the secondary clamping capacitor i_{Co} without and with the interleaving strategy respectively. In Fig. 6, the RMS value of i_{Co} without and with the interleaving strategy are 19.74 A and 9.38 A respectively, which verifies that the proposed converter can effectively reduce the ripple current on the secondary clamping capacitor.



(a) (b)

Fig. 6. Simulation results including i_{s1}, i_{s2}, i_o, and i_{Co} (V_{in} = 550 V, V_o = 50 V, and P_o = 1500 W). (a) w/o interleaving strategy. (b) w/ interleaving strategy.

V. CONCLUSION

This paper proposes a ZVZCS DC/DC converter featuring with 1) capacitive output and 2) input-series output-parallel structure for the high input voltage and high power applications. The advantages of the proposed converter include 1) reduce the circulating current and duty cycle loss when comparing with the conventional converter with the inductive output and 2) reduce the ripple current flowing through the secondary clamping capacitor. Therefore, the proposed converter can not only increase the converter's efficiency, but also improve the reliability of the secondary clamping capacitor. Finally, the simulation results verify the proposed converter.

ACKNOWLEDGMENT

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APPENDIX

The RMS value of i_{Co_rms} when $\Delta t_2 \ge 0$ and $\alpha \le \frac{T_s}{4}$ can be obtained by (25).

$$
\begin{aligned}
a &= \frac{V_{in}/2 - n\cdot V_o}{L_r} - \frac{n\cdot V_o}{L_m} \\
b &= \frac{V_{in}/2 - 2\cdot n\cdot V_o}{L_r} - \frac{2\cdot n\cdot V_o}{L_m} \\
i_{Co\_rms} &= \sqrt{\begin{aligned}
&\frac{2\left[2\cdot\Delta t_2\cdot\left[i_o - a\cdot n\cdot(T_s/4-\alpha+\Delta t_1)\right]^2 + \frac{5\cdot a^2\cdot n^2\cdot\Delta t_2^3}{3} - 3\cdot a\cdot n\cdot\Delta t_2^2\cdot\left[i_o - a\cdot n\cdot(T_s/4-\alpha+\Delta t_1)\right]\right]}{T_s} \\
&+\frac{2\left[\Delta t_1\cdot\left[i_o - a\cdot n\cdot(3\cdot T_s/4-2\cdot\alpha)\right]^2 + \frac{b^2\cdot n^2\cdot\Delta t_1^3}{3} - b\cdot n\cdot\Delta t_1^2\cdot\left[i_o - a\cdot n\cdot(3\cdot T_s/4-2\cdot\alpha)\right]\right]}{T_s} \\
&-\frac{2\left[(\alpha-T_s/4)\cdot\left(i_o - \frac{T_s\cdot a\cdot n}{4}\right)^2 + \frac{4\cdot a^2\cdot n^2\cdot(\alpha-T_s/4)^3}{3} + 2\cdot a\cdot n\cdot(\alpha-T_s/4)^2\cdot\left(i_o - \frac{T_s\cdot a\cdot n}{4}\right)\right]}{T_s} \\
&+\frac{\Delta t_1\cdot\left[L_m\cdot(4\cdot i_o + T_s\cdot a\cdot n - 4\cdot a\cdot n\cdot\Delta t_3) + 4\cdot L_m\cdot n\cdot\left(I_{Lr\_\min} - I_{Lm\_\min}\right) - 4\cdot V_o\cdot n^2\cdot\Delta t_1\right]^2}{8\cdot L_m^2} + \frac{2\cdot b^2\cdot n^2\cdot\Delta t_1^3}{3}}{T_s} \\
&-\frac{b\cdot n\cdot\Delta t_1^2\cdot\left[L_m\cdot(4\cdot i_o + T_s\cdot a\cdot n - 4\cdot a\cdot n\cdot\Delta t_3) + 4\cdot L_m\cdot n\cdot\left(I_{Lr\_\min} - I_{Lm\_\min}\right) - 4\cdot V_o\cdot n^2\cdot\Delta t_1\right]}{L_m} \\
&+\frac{2\cdot\left[\Delta t_2\cdot\left[i_o - a\cdot n\cdot(\Delta t_1 - T_s/4+\Delta t_3)\right]^2 + \frac{a^2\cdot n^2\cdot\Delta t_2^3}{3} - a\cdot n\cdot\Delta t_2^2\cdot\left[i_o - a\cdot n\cdot(\Delta t_1 - T_s/4+\Delta t_3)\right]\right]}{T_s}
\end{aligned}}
\end{aligned}
\tag{25}
$$

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