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Keywords

≪Wide bandgap devices≫, ≪Silicon Carbide (SiC)≫, ≪MOSFET≫, ≪New switching devices≫, ≪EMC/EMI≫

Abstract

This paper investigates gate driver design challenges encountered due to the fast switching transients in medium voltage half bridge silicon carbide MOSFET power modules. The paper presents, design of a reduced isolation capacitance regulated DC-DC power supply and a gate driver with an active Miller clamp circuit for a 10 kV half bridge SiC MOSFET power module. Designed power supply and the gate driver circuit are verified in a double pulse test setup and a continuous switching operation using the 10 kV half bridge silicon carbide MOSFET power module. An in-depth experimental verification and detailed test results are presented to validate the gate driver functionality. The designed gate driver circuit shows satisfactory performance with increased common mode noise immunity and protection against the Miller current induced unwanted turn on.

Introduction

Medium voltage (MV) silicon carbide (SiC) MOSFETs are emerging as promising devices due to their capability of blocking higher voltages and switching at higher frequencies with increased thermal conductivity compared to their Silicon (Si) counterparts [1]. With latest technological improvements these devices are reaching the level of maturity to be considered for medium voltage and high power conversion applications e.g., solid state transformer [2]. Considering high dv/dt switching transients, intrinsic device parasitics together with parasitic capacitance external to the device are crucial and require careful optimization to utilize SiC MOSFETs at their full potential [3], [4]. In a half bridge power module, the mid-point experiences high dv/dt during switching transients. The isolation barriers inside the power modules and interfacing circuitry which experiences the dv/dt, introduces the common mode (CM) currents due to capacitive coupling. One of the dominant paths for this CM current is through an isolation barrier of the DC-DC power supply of high side (HS) gate driver circuit as graphically illustrated in Fig. 1. For reliable operation, and in order to maintain the gate driver control signal fidelity, this CM

current needs to be attenuated. The magnitude of the CM current is directly affected by the dv/dt and isolation capacitance (C_{iso}) based on (1).

$$i_{cm} = C_{iso} \cdot \frac{\mathrm{d}v}{\mathrm{d}t} \tag{1}$$

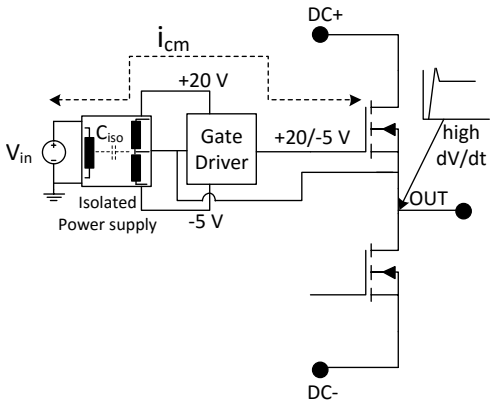


Fig. 1: Schematic representation of common mode current path for the high side gate driver power supply

Fast switching transients in the MV SiC MOSFETs can result in dv/dt as high as 30 kV/μs, which imposes the requirement for a very low isolation capacitance ($<$ 5 pF) in the gate driver circuitry [5]. Readily available galvanically isolated power supplies and driver integrated circuits (ICs) with target application for 6.5 kV IGBTs limits its application for SiC devices with voltage rating of 10 kV and higher. Furthermore, commercially available regulated isolated power supplies with insulation voltage rating of 10 kV or above has an isolation capacitance in the range of 10–20 pF [6]. Recent publications have demonstrated a gate driver power supply for 10 kV SiC MOSFETs/15 kV SiC IGBTs. These are unregulated, which requires an additional stage to achieve voltage regulation [7],[8]. In addition to the CM current, the high dv/dt switching transients can induce undesirable turn on in a half bridge power module due to the Miller effect, when the complementary switch is turning on [9]. Taking these above mentioned considerations into account, this paper presents the design of a regulated power supply with an isolation capacitance of 2.6 pF and a gate driver circuit that incorporates an active Miller clamp functionality for stably driving a 10 kV SiC MOSFET.

DC-DC isolated power supply

This section presents the design of a regulated DC-DC isolated power supply. Design considerations for the high insulation voltage and low isolation capacitance transformer are also discussed with measured key parameters.

Power supply topology

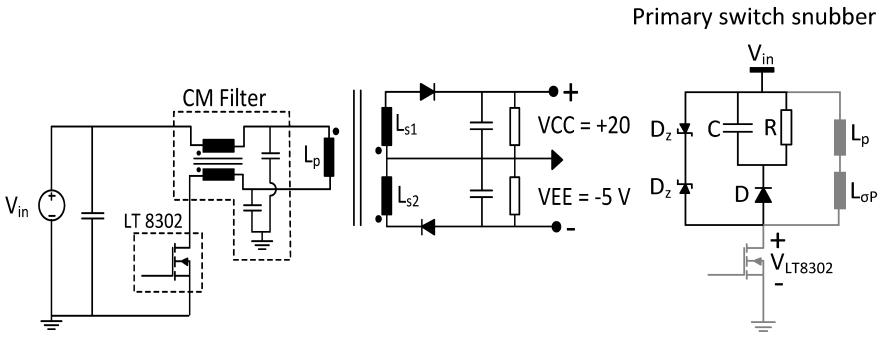


Fig. 2: Schematic of a designed flyback converter

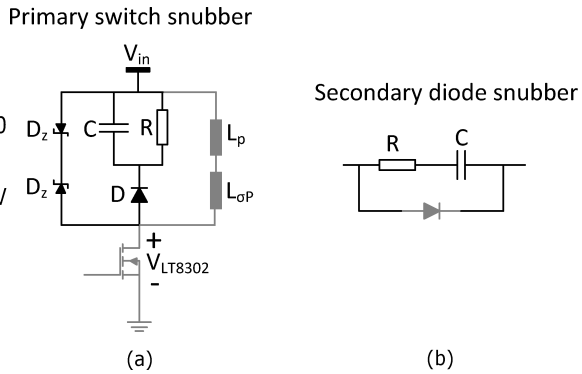


Fig. 3: Schematic of (a) primary switch and (b) secondary snubber circuit

The designed power supply utilises a flyback topology with dual secondary windings as shown in Fig. 2. In order to achieve compact size, a flyback controller IC (LT8302) with an integrated switch is chosen. The IC operates in boundary conduction mode (BCM) or discontinuous conduction mode (DCM) with a variable switching frequency (12 to 400 kHz) and regulates the output voltage by sensing transformer primary winding voltage. Voltage regulation based on primary side sensing eliminates the need of a feedback circuitry from secondary side i.e optocoupler, which would contribute as an additional isolation capacitance. Furthermore, a BCM or DCM in comparison to the continuous conduction mode (CCM) of operation facilitates a reduced requirement of the primary magnetizing inductance. Lower and upper boundary for primary magnetizing inductance of 5.17 μH $\leq L_p \leq$ 931 μH is identified based on: the inductance value for which flyback operates in boundary conduction mode and minimum inductance requirement imposed by the flyback controller. Small magnetizing inductance is desirable because, for a given geometry and magnetic property of a core material, smaller magnetizing inductance yields: fewer number of windings, smaller leakage inductance and lower coupling capacitance. The requirement for the flyback output voltages of $+20$ V and -5 V in reference to secondary mid-point is determined based on the recommended turn on/off driving voltages for a 10 kV SiC MOSFET. A high frequency common mode choke with Y capacitors are placed between the primary winding and control IC to provide a high impedance path for the common mode currents and redirecting it to ground, respectively.

Transformer design

A major requirement for the flyback transformer is to achieve a low coupling capacitance between the primary and secondary windings. This coupling capacitance is dependent on the distance between the primary to secondary windings and the area occupied by the transformer windings on the core. A significant and potentially dominant contribution of capacitive coupling is present between the primary and secondary windings through the transformer core. Graphical representation of the transformer design is presented in Fig. 4 and the electrical parameters for the designed transformer are summarised in Table I. A MnZn toroidal core (TN32/19/13) utilising medium frequency and high permeability magnetic

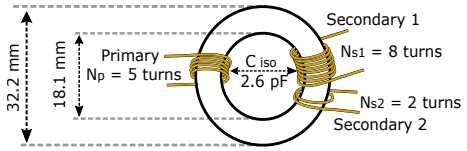


Fig. 4: Graphical representation of the designed transformer

Table I: Measured electrical parameters of the flyback transformer using a keysight E4990A impedance analyser.

Parameters	Values
Isolation Capacitance (C_{iso})	2.6 pF
Primary magnetizing inductance (L_p)	52.7 μH
Secondary 1 magnetizing inductance (L_{s1})	134 μH
Secondary 2 magnetizing inductance (L_{s2})	8.6 μH
Primary leakage inductance ($L_{\sigma p}$)	3.5 μH
Secondary 1 leakage inductance ($L_{\sigma s1}$)	4.5 μH
Secondary 2 leakage inductance ($L_{\sigma s2}$)	0.3 μH

material (3F3) is chosen for the transformer. A high inductance factor $A_L = L/N^2$ of 2270 nH for the chosen core facilitates with the lower number of windings to achieve the required inductance and thereby reducing the area occupied by the winding on the transformer core. The number of turns for primary and secondary windings are determined based on the design constraints imposed by the flyback controller IC, the desired inductance value and the primary to secondary winding voltage ratio. The primary and secondary windings are spaced distantly on the core to increase the physical distance between them, which helps to provide low isolation capacitance but results in an increased leakage inductance of the transformer due to poor magnetic coupling. The core has an insulation coating rated for 2 kV DC. To achieve a higher insulation voltage withstand capability a triple insulated wire is utilised for transformer windings. A layer of insulation tape is placed between the winding and transformer core, lowering the isolation capacitance further by reducing the coupling through the transformer core. Isolation capacitance for the designed transformer is measured to be 2.6 pF using a Keysight E4990A impedance analyser.

Design consideration for primary switch snubber and secondary snubber

Transformer leakage inductance introduces voltage spikes across the primary switch and secondary diodes during turn off. To protect the flyback switch from over voltages and suppress the voltage spikes within allowable limits, an RCD snubber with a Zener clamp and an RC snubber is designed for the switch and diode, respectively [10]. Resistance and capacitance value for RCD snubber is chosen such that the RC time constant is smaller than the blanking time of the flyback controller IC, within which the excess energy form the leakage inductance should be dissipated in order to sense the primary winding voltage correctly. For Zener clamp, the Zener diode is chosen such that the Zener voltage is below the breakdown voltage of the flyback switch.

Design of a gate driving stage with active Miller clamp functionality

A functional schematic of the gate driving circuitry is presented in Fig. 5. A high-speed gate driver IC from IXYS (IXDN614) with peak source/sink current capability of 14 A and a low propagation delay is chosen as a primary driving stage. The output of the driver IC is connected to the gate pad with gate resistance R_g. To isolate the control circuit from the high voltage and remove coupling, the gate signals are transferred optically using an optic fiber link. Preliminary tests showed possibility of unwanted turn on of the SiC MOSFETs due to the Miller effect under high dv/dt switching transients. To mitigate this an active Miller clamp circuit is designed and incorporated into the gate drive [11]. Feedback for

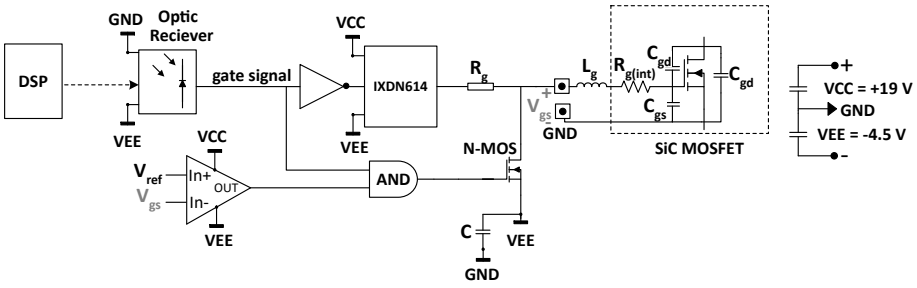


Fig. 5: Schematic of the gate driving stage with active miller clamp circuit

the Miller clamp circuit is provided by utilizing the gate-source voltage and the input gate signal. A comparator circuit compares the gate-source voltage with a reference voltage and outputs logic high, when the sensed voltage reaches below the reference voltage. An additional logic gate is utilized so that the clamp is activated only when the turn off gate command is received and gate-source voltage is below the reference voltage. Reference voltage for the clamp is chosen to be lower than the SiC MOSFETs threshold voltage, meaning that the device turn on/off characteristics are not affected by the Miller clamp and the clamp is only activated after the MOSFET is turned off. To provide a low impedance path for the Miller current, an N - channel MOSFET with low on-state resistance of 50 mΩ is used as a clamping switch. A capacitor with significantly higher capacitance value compared to the device gate-drain capacitance (C_{gd}), is placed between the source of the N - channel MOSFET and ground plane to prevent rise in clamp voltage due to the flow of Miller current. An image of the gate driver and its specification are presented in Fig. 6 and Table II, respectively.

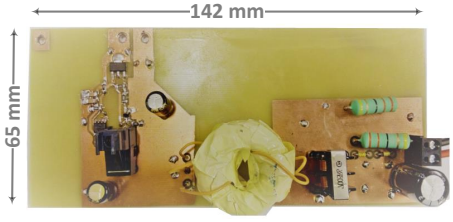


Fig. 6: Image of a designed gate driver circuit

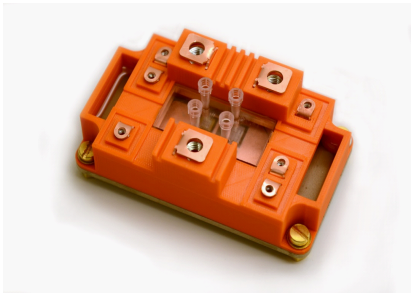
Table II: Gate driver specification

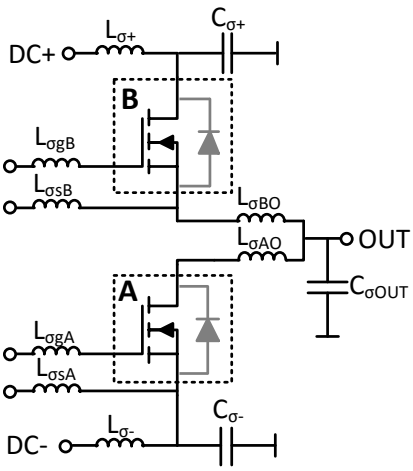
Parameters	Values
Nominal input voltage (V_{in})	12 V
Turn-on gate drive voltage ($V_{gs(on)}$)	+19 V
Clamp voltage (V_{clamp})	−4.5 V
Flyback under voltage lockout	7.5 V
Gate resistance (R_g)	17 Ω / 25 Ω

For a 10 kV SiC MOSFET, a threshold voltage of 2.6 V at the drain current of 1 mA, and internal gate resistance $R_{g(int)}$ of approximately 3 Ω are identified from a static characterisation. This threshold voltage for the SiC MOSFETs may drift due to temperature dependance and application of gate bias stress [12]. Also, the sensed gate-source voltage (V_{gs}) and actual voltage across the device parasitic gate-source capacitance (V_{Cgs}) in reference to Fig. 5 are different due to the internal gate resistance of the device and parasitic inductance in the gate-source loop. An analytical approach considering the SiC MOSFET parasitics as described in [3], [13], [14], was used to study the fluctuation of gate voltage due to Miller current. Taking into account the above mentioned considerations, a reference voltage of 0 V is chosen to avoid an occurrence, where the clamp is turned on before the voltage across the gate-source capacitance C_{gs} reaches below the 2.6 V threshold voltage.

Device under test

For the test two 10 kV/10 A SiC MOSFET half bridge power modules with and without external JBS diodes are utilised. One such module with external SiC JBS diodes is presented in Fig. 7 along with the schematic displaying the power module parasitics extracted form ANSYS Q3D [4]. The shown power module is packaged in-house at Aalborg University and populated with two generation 1 10 kV/10 A SiC MOSFET and 10 kV SiC JBS diode dies from Wolfspeed.





Parasitic	Value
$L_{σ+}$	16.8 nH
$L_{σgB}$	21.3 nH
$L_{σsB}$	17.7 nH
$L_{σBO}$	17.5 nH
$L_{σAO}$	13.9 nH
$L_{σgA}$	21.2 nH
$L_{σsA}$	17.6 nH
$L_{σ-}$	16.3 nH
$C_{σ+}$	100 pF
$C_{σOUT}$	149 pF
$C_{σ-}$	45 pF

Fig. 7: Picture of 10 kV/10 A halfbridge power module populated with generation 1 10 kV SiC MOSFETs and SiC JBS diodes from Wolfspeed and schematic showing power module parasitic with table of values.

Test bench design and experimental results

The designed gate driver circuit and isolated power supply are tested in a double pulse test setup to evaluate CM noise immunity and the Miller effect induced turn on possibility. As presented in Fig. 8 (a), a high side (HS) MOSFET and a low side (LS) diode for freewheeling is utilised in the double pulse test. The CM current for the high side gate driver power supply and gate-source voltage of the low side MOSFET are monitored during the test. To validate the gate driver functionality in continuous switching operation, a test setup as presented in Fig. 8 (b) is used, where the half bridge is switched in an open loop control with a switching frequency of 10 kHz. The power module is attached to a low stray inductance, stacked aluminium bus-bar with low ESR/ESL capacitors. The ceramic substrate layer in the power module DBC forms a parasitc cpacitance between the copper plane on the top of a DBC and the mounting baseplate. The parasitic capacitance $C_{σ(OUT)}$ is a source of EMI that introduces CM current during the high dv/dt switching transitions [15], [16]. For improved EMI performance and owing to safety concerns, the heatsink on which the power module is mounted is grounded using a 278 Ω power resistor based on the analysis described in [3].

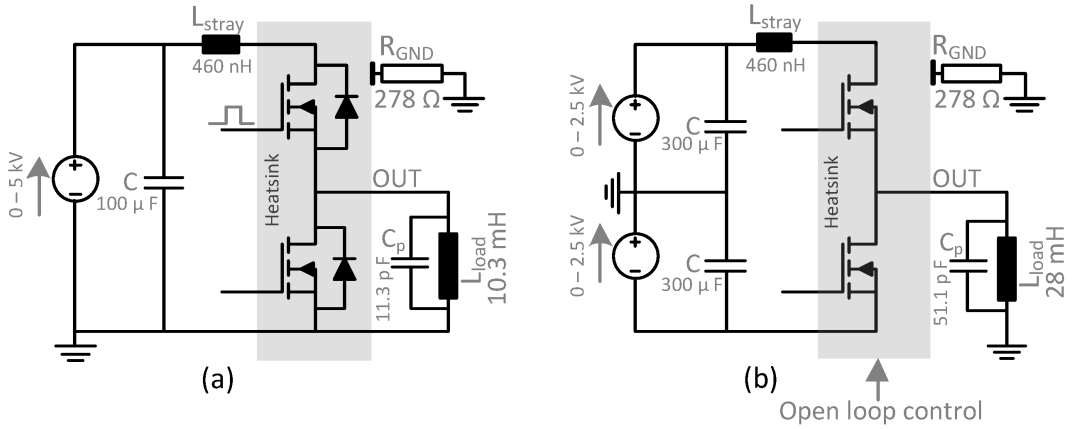


Fig. 8: Simplified schematic of the (a) double pulse and (b) half bridge test setup used to validate gate drive performance

Double pulse test

The half bridge output voltage (V_{OUT}) and gate-source voltage for the low side switch ($V_{\mathrm{gs(LS)}}$) during the first turn off and the second turn on pulse in a double pulse test at 5 kV DC-link voltage ($\mathrm{V_{DC}}$) are shown in Fig. 9. The gate-source voltage during the switching transition is approximately -4.5 V with small oscillations, which is well below the threshold voltage of 2.6 V for a 10 kV SiC MOSFET. The CM current measurement on the input side of the gate driver without any common mode filter on the primary side power supply at a $\mathrm{V_{DC}}$ of 4 kV is presented in Fig. 10. The maximum peak amplitude and mean value of the CM current is approximately 172 mA and 58 mA, respectively for the turn on dv/dt of 16.5 kV/μs, suggesting an isolation capacitance of 3.5 pF being present.

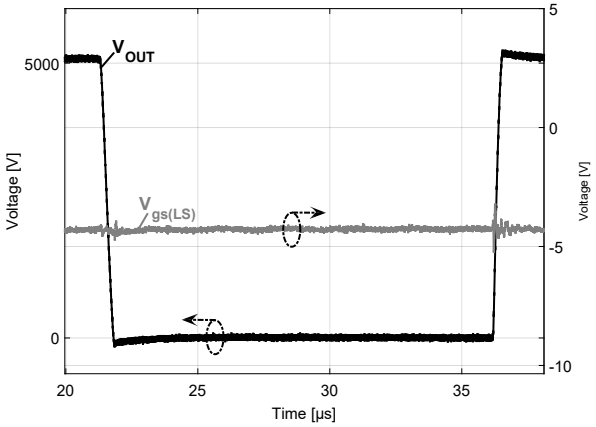


Fig. 9: Measured half bridge output voltage and gate-source voltage of the low side switch in a double pulse test. Test condition: $\mathrm{V_{DC}}$ = 5 kV, Drain current $\mathrm{i_d}$ = 5 A

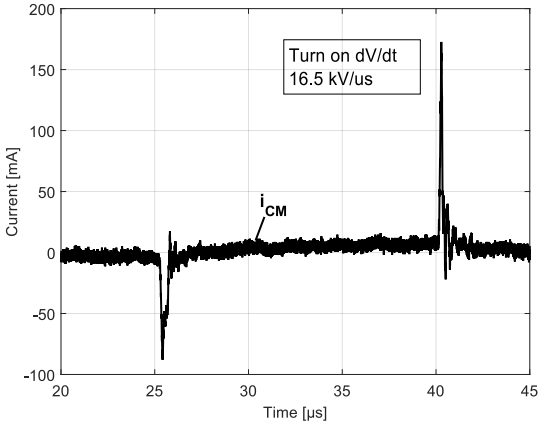


Fig. 10: Measured common mode current in a double pulse test. Test condition: $\mathrm{V_{DC}}$ = 4 kV, Drain current $\mathrm{i_d}$ = 5 A

Continuous switching operation

In the first case, the half bridge is switched with a duty cycle of 0.5. Under, this condition the the load current magnitude is high enough so that the MOSFET output capacitance ($\mathrm{C_{OSS}}$) charges/discharges within the 2 μs deadtime. This implies that the MOSFET turns on with almost zero voltage across it and achieves soft turn on. Fig. 11 and Fig. 12 show the gate current and gate-source voltage for the low side MOSFET, and output voltage of the half bridge module during the turn on and turn off switching transitions. As seen in Fig. 11, due to the zero voltage turn on, the Miller plateau is not present in the

gate-source voltage and the transition is smooth during the MOSFET turn on. With a gate drive voltage of +19/-4.5 V and a gate resistance of 25 Ω, the peak gate current is limited to approximately 1 A. Looking at the turn off switching transition in Fig. 12, when the turn off command is applied, the gate current (i_g) increases from zero to the peak value resulting in a high frequency oscillation in the gate voltage due to voltage drop ($L_g \cdot \frac{di_g}{dt}$) across the parasitic inductance in the gate-source switching loop. The half bridge output voltage starts rising once a gate-source voltage reaches the Miller level. A small delay after the gate-source voltage crosses zero Volts, a steep change in the gate-source and gate current is identified due to the turn on of the Miller clamp. Measured gate-source voltage and the gate current validates the fundamental functionality of the gate driver and DC-DC power supply to operate under continuous switching operation. The measurements presented clearly indicates the satisfactory performance in terms of gate driving voltage and power requirements.

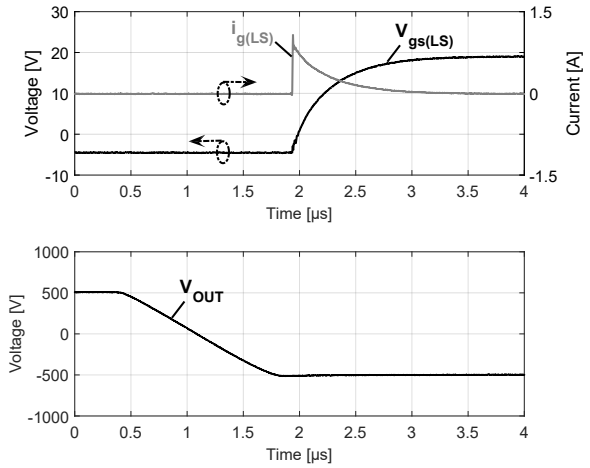


Fig. 11: Measured low side MOSFET gate current, gate voltage and half bridge output voltage during turn on transition.

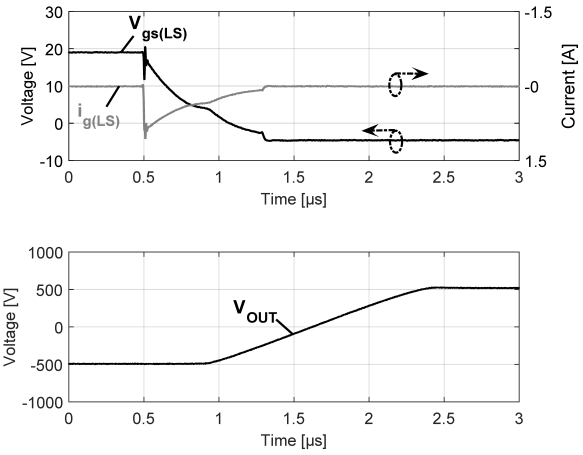


Fig. 12: Measured low side MOSFET gate current, gate voltage and half bridge output voltage during turn off transition.

The test was performed at 5 kV bus voltage. The inductor current and half bridge output voltage, together with the drain current of the high side and low side MOSFETs are presented in Fig. 13. Under this condition, the maximum dv/dt during the switching transition is 5.4 kV/μs. During the switching transition, a finite magnitude and opposite polarity of the drain current is identified in the HS MOSFET as well as the LS MOSFET, which is due to the displacement current charging/discharging the MOSFET output capacitance.

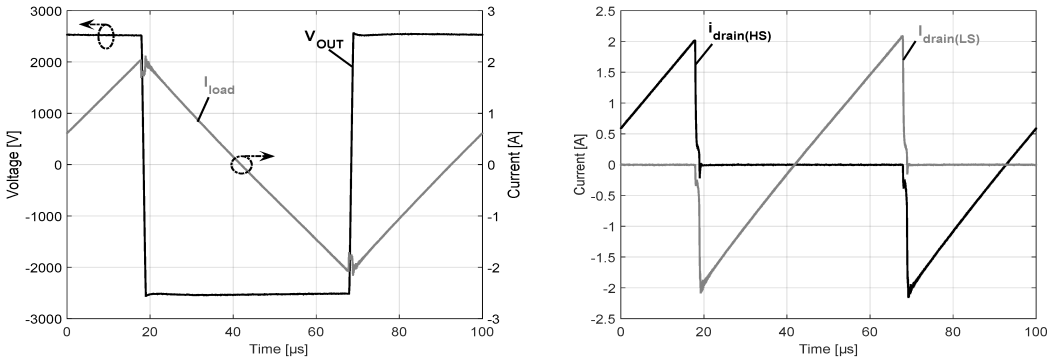


Fig. 13: Measured half bridge output voltage, inductor current, high side and low side MOSFET drain currents

MOSFET first quadrant operation: turn on/off switching transition

To verify the performance under hard commutation, an open loop sine wave pulse width modulation with a modulation index of 0.02 is performed. Fig. 14 shows the drain currents, half bridge output voltage and gate-source voltage during the turn on and turn off switching transitions at a V_{DC} of 4.6 kV. This instant corresponds to the negative cycle of the load current during which the drain current for the low side MOSFET is positive (i.e first quadrant operation). It should be noted that the considerably large difference in the drain current magnitude at the beginning and at the end of the switching period is due to the higher DC link voltage (4.6 kV) and the relatively long switching period (50$\pm$0.02 μs), producing the load inductor (31 mH) ripple current of 2.6 A. As seen in Fig. 14 (a), once the turn on command

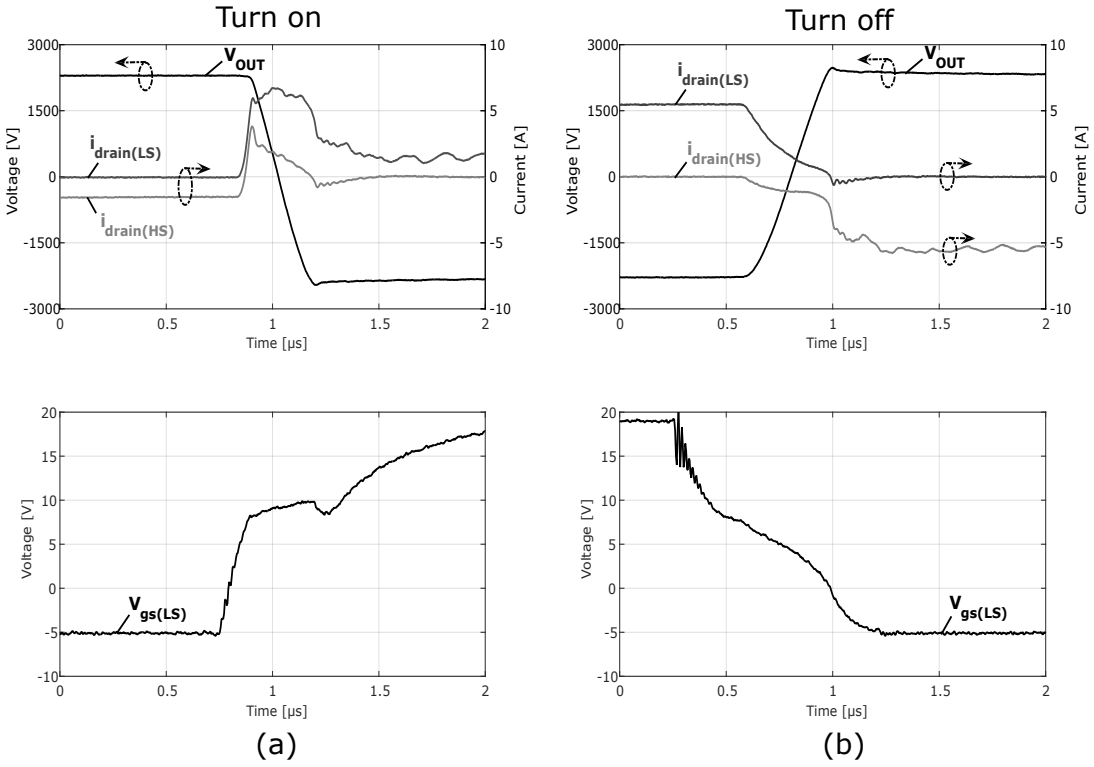


Fig. 14: Measured half bridge output voltage, MOSFET drain currents and low side MOSFET gate-source voltage during (a) turn on and (b) turn off transition.

is received the gate voltage starts to rise. The drain current in the low side switch starts to increase as the gate-source voltage crosses the MOSFET threshold voltage of approximately 2.6 V. The gate-source voltage reaches the Miller level, when the LS MOSFET drain current equals the load current. At this point, the load current is fully commutated from the high side MOSFET body diode to low side MOSFET followed by the reverse recovery process. A non-flat Miller plateau in the gate-source voltage is due to the modest amount of transconductance of a SiC MOSFET in the saturation region [17]. The half bridge output voltage completes its transition during the Miller plateau after which the LS MOSFET is fully turned on and enters into an ohmic region.

The turn off process shown in Fig. 14 (b), is similar to the one described in a previous section. The experimental verification performed, confirms a smooth and typical turn on switching transition under the hard commutation in continuous switching operation.

MOSFET third quadrant operation: turn on/off switching transition

Fig. 15 shows the drain currents, half bridge output voltage and gate-source voltage during the turn on and turn off switching transition at a V_{DC} of 4.6 kV. This instant corresponds to the positive cycle of the load current during which the drain current for the low side MOSFET is negative (i.e third quadrant operation). As shown in Fig. 15 (a), the LS MOSFET achieves zero voltage turn on in third quadrant as

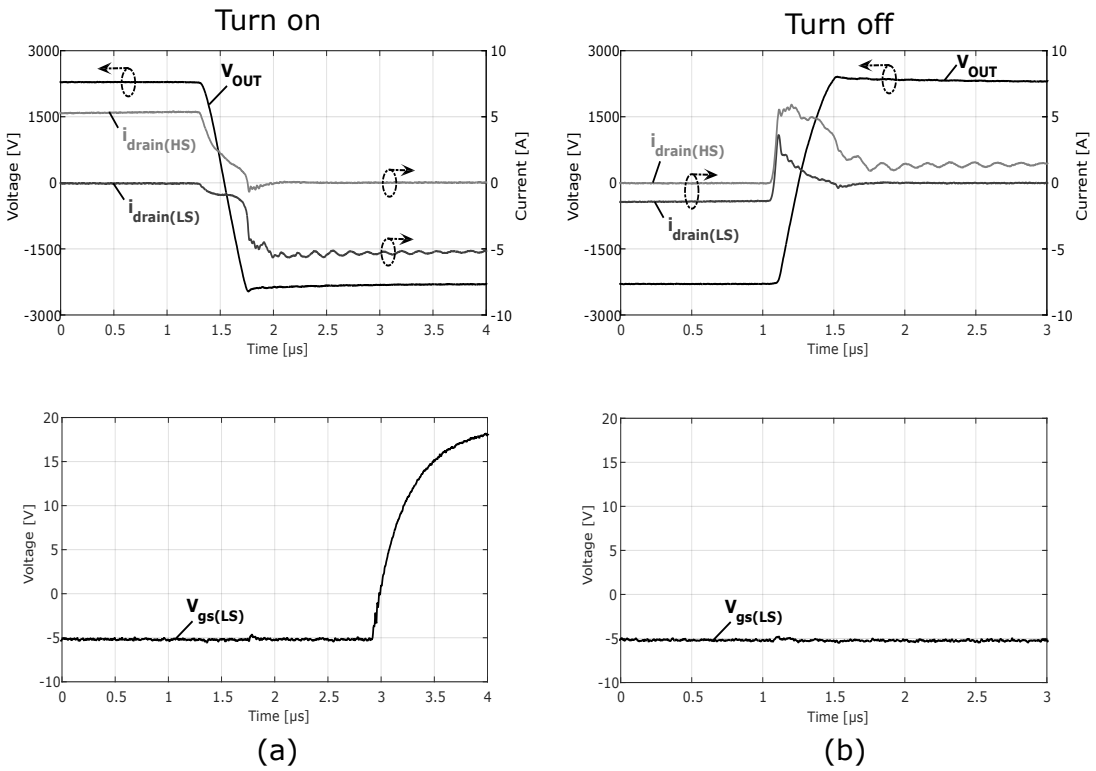


Fig. 15: Measured half bridge output voltage, MOSFET drain currents and LS MOSFET gate-source voltage during (a) turn on and (b) turn off transition.

the drain-source voltage completes its transition during the deadtime and the LS body diode is conducting during the deadtime. The LS MOSFET turns on after this point and operates in the third quadrant.

The dv/dt is high during the hard commutation when, the HS MOSFET turns on and the LS side MOSFET body diode reverse recovers and it is one of the adverse conditions for the Miller clamp in the LS gate driver. This condition is presented in Fig. 15 (b). The LS MOSFET is off after the gate-source voltage has changed from the positive to the negative drive voltage and LS body diode is conducting during the dead time. The moment at which the HS MOSFET is turned on is identified from the HS drain current and change in the half bridge output voltage. During this dv/dt transition, the LS gate-source voltage remains unaffected. The experimental verification performed, confirms the Miller clamp functionality during the hard turn on switching transition of complementary MOSFET in continuous switching operation.

Conclusion

The paper discusses key challenges in designing the gate driver circuit for fast switching MV SiC MOSFET half bridge power modules. The design of an isolated DC-DC regulated power supply and key design considerations for a low coupling capacitance isolation transformer is presented. A prototype for a gate driver circuit with a very low isolation capacitance and the Miller clamp functionality is developed. The gate driver circuit was exposed to dv/dt of up to 20 kV/μs in the double pulse test setup. Further verification was performed in continuous switching operation with switching frequency of 10 kHz. An in depth analysis of the half bridge switching waveforms during the turn on and turn off transition are presented considering different modes of MOSFET operation. The experimental results show that, the design satisfies the gate drive requirements for a 10 kV half bridge SiC MOSFET power module with increased CM noise immunity and protection against the Miller current induced unwanted turn on under the high dv/dt switching transients.

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