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Robust Fault Ride-Through of Converter-based Generation during Severe Faults with Phase Jumps

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***Abstract*—As grid-connected converters are at risk of losing synchronism with the grid when exposed to extreme voltage sags, this might jeopardize the stability during a fault and a converter's ability to comply with fault ride-through requirements. This paper investigates the synchronization stability of grid-tied converters during severe symmetrical faults with phase jumps. To achieve zero-voltage ride-through capability, a frozen PLL structure can be employed to guarantee stability during faults. However, as the frozen PLL approach is unaware of frequency drifts and phase-angle jumps in the grid voltage, its performance during non-constant frequency and phase is unknown. Therefore, this paper investigates and provides new insight into how the frozen PLL performs during phase jumps and reveals whether phase compensation should be utilized to improve the converter response during a severe symmetrical fault. It is disclosed, that even though phase compensation can improve the injected currents during a fault situation including large phase jumps, a non-compensated frozen PLL can inherently ensure stability and allow for zero-voltage ride-through capability at an acceptable current injection. Furthermore, the robustness of the frozen PLL has been analyzed through a comprehensive simulation study where three test cases have been experimentally verified, which confirms the presented findings.**

***Index Terms*—Grid-Connection, Voltage-Source Converter, Grid Fault, Synchronization Stability, Fault Ride-Through**

I. Introduction

With an increasing share of power electronic-based power generation when compared to a conventional synchronous machine-based power system, there is concern about the stability and availability of such systems during abnormal or fault situations. This concern has forced Transmission System Operators (TSOs) and Distribution System Operators (DSOs) to require specific behavior of Distributed Generators (DGs) during irregular events.

For grid-following converters to comply with grid-code directives, an accurate estimation of the phase angle of the grid voltage is essential. During weak-grid or low-voltage grid conditions, the instantaneous location of the voltage at the Point of Common Coupling (PCC) can be significantly distorted or counterproductive due to the Phase-Locked Loop (PLL) being destabilized, which causes instabilities in the current controller [1]. Although analysis of the system performance and stability during nearly zero voltage conditions has not received much attention [1]–[4], a large body of literature describes Low-Voltage Ride-Through (LVRT) capability of Renewable Energy Sources (RES). Several researchers have described Loss Of Synchronization (LOS) of the conventional Synchronous Reference Frame Phase-Locked Loop (SRF-PLL) during very low-voltage situations [5]–[8], and a handful of control scheme recommendations to mitigate LOS have previously been published [7], [9]–[12]. As LOS arises as a result of high network impedances, low grid voltages, and high active/reactive current injection (dependent on the network impedance), most mitigation methods reshape the injected currents during a low-voltage situation in order to stabilize the synchronization process of the converter. This includes limiting or nullifying the current injection [9], injecting a reactive/active current ratio equal to the X/R ratio of the network impedance [10], a voltage-dependent active current injection strategy [11], and methods where the active current injection is adaptively regulated based on the estimated frequency error of the PLL [7], [12].

In the case of a zero-voltage situation, none of the grid-following strategies in [7], [9]–[12] can ride-through the fault since the voltage used for synchronization is not present. A simple approach to deal with this issue is proposed in [13], [14] where the PLL is bypassed or frozen at a predefined or its current state when a low-voltage fault is detected. In this way, the converter can be observed to switch from a grid-following control mode to a grid-forming control mode where its phase angle, obtained for the disabled PLL, happens to be synchronized to the voltage at the PCC. By applying this method, the feedback path within the PLL and the coupling between injected current and estimated voltage phase angle is eliminated, which results in a stable synchronization unit for any low voltage level. This idea was as well patented and published in 2017 [15], where it is stated that when the PLL is frozen during a fault event, it will have substantially the same value as for normal operation. However, as described in [16], this method does not necessarily comply with the grid codes requirements. Moreover, as stated in [17], it cannot avoid phase jumps at the fault occurrence. This is the case as the method is only proven to be effective provided that the voltages at the PCC are not exposed to any phase jumps at the fault instant and that the frequency can be considered constant during the fault. However, if the X/R ratio of the fault impedance is different from that of the equivalent grid impedance, phase jumps will occur and the performance of the frozen PLL structure might be compromised. Therefore, this paper aims to analyze whether or not the benefits of using a

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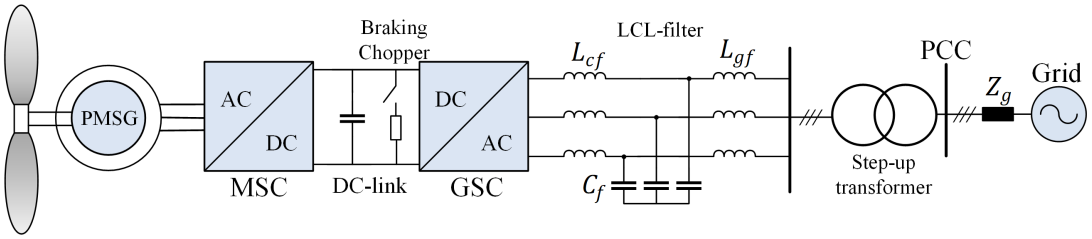


Fig. 1. Type IV wind turbine system with a full-scale power converter connected to the grid through an output LCL filter and step-up transformer. MSC: Machine-side converter, GSC: Grid-side converter.

frozen PLL structure during severe faults can also be extended to handle phase jumps. The contributions of this paper are the following:

1) describing how a phase-angle jump at the fault location propagates to the point of synchronization for different current injections and line impedances.
2) systematically evaluating whether phase compensation should be employed for different line impedances when using a frozen PLL structure during severe symmetrical faults.
3) based on a robustness analysis, a recommendation of how and when to use a frozen PLL during grid faults considering phase-angle jumps is provided.
4) based on these, a more complete picture of the performance of the frozen PLL is given as phase jumps during the fault are considered.

More specifically, the fault condition and the phase jump to be experienced at the fault location and the PCC is described in detail. A phase compensation technique is developed to estimate the phase jump for a comparison to the frozen PLL and a comprehensive simulation study and robustness analysis are conducted to reveal whether improvements in the power injection can be attained by implementing such a phase compensation technique in addition to the frozen PLL structure.

The paper is structured in the following manner: The considered application together with grid requirements are presented in section II. LOS, current injection limits, how the PLL damping influences the system stability, and the frozen PLL structure are discussed in section III. A detailed analysis of what causes phase-angle jumps during faults as well as how it will propagate to the PCC is described in section IV. Section V presents the phase compensation techniques to be used for characterizing the frozen PLL and section VI reveals how a frozen PLL structure with or without phase compensation has advantages compared to state-of-the-art solutions. To that end, section VI includes an extended robustness analysis of the frozen PLL. The disclosures and findings from the comprehensive analysis are experimentally verified in section VII and conclusions are drawn in section VIII.

II. System Overview and Grid Requirements

The system considered in this paper includes a distributed generator such as a wind turbine where a full-scale power electronic converter is used to harvest the energy from renewable energy source and transfer it to the grid, see Fig. 1. The

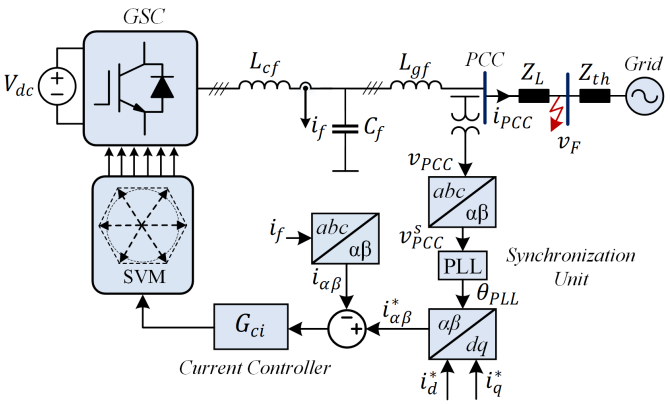
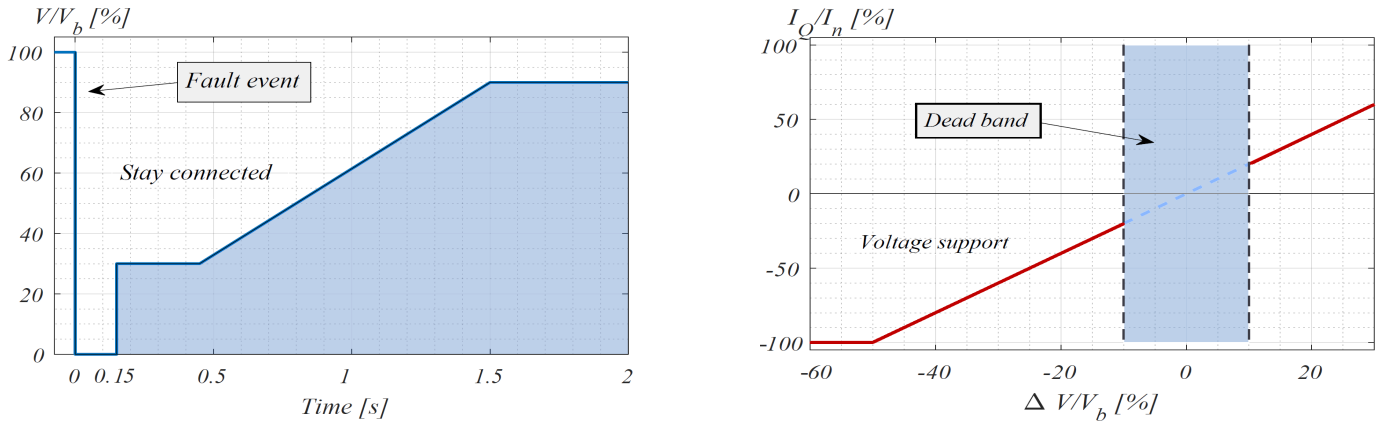


Fig. 2. Structure of grid-side converter control operated in grid-feeding mode. The red arrow indicates the location of a severe symmetrical fault.

physical parameters and control parameters used for the down-scaled system can be seen in Table I. Due to the decoupling between machine-side and grid-side for a wind turbine, only the Grid-Side Converter (GSC) is considered. The machine-side converter, synchronous machine and mechanical circuits of the wind turbine system are realized as a constant voltage source since the aim for this paper is to investigate the synchronization issues associated with severe grid faults and not interactions between the dc and ac side. During a low-voltage situation where the converter current is strongly limited to around 1 pu, the harvested energy from the wind turbine cannot be delivered fully to the grid. This results in surplus energy being accumulated in the DC-link capacitor resulting in over-voltages during the fault. Usually, the DC-side contains a chopper circuit used to dissipate the surplus energy during a fault which facilitates the assumption of a nearly constant DC-link voltage as depicted in Fig. 2 where the control topology used throughout this paper can also be seen.

With the increasing installation of distributed generators, TSOs and DSOs have issued requirements for power converter-based RES. This implies, that such systems should tolerate deep voltage sags and provide voltage support by injecting reactive power into the grid in order to prevent a network to collapse. Such requirements are shown in Fig. 3, where it can be seen that a converter should be able to inject 1 pu of capacitive reactive current during a zero-voltage situation for up to 150 ms.



(a) (b)

Fig. 3. Grid code for wind turbines [18]. (a): Requirement from BDEW for low-voltage ride-through capability during a fault event. V is the line-to-line rms voltage. (b): Voltage support by injection of reactive current. I_n is the nominal line current and I_Q is the required reactive current to be injected.

TABLE I
MAIN PARAMETERS OF THE SYSTEM IN FIG. 1 AND FIG. 2.

Symbol	Description	Physical Value
S_b	Rated power	7.35 kVA
V_b	Nominal grid voltage	400 V
f_n	Rated frequency	50 Hz
V_n	Peak phase voltage	1 pu
V_{tr}	Threshold voltage	0.9 pu
V_{dc}	DC-link voltage	730 V
L_{cf}	Converter-side inductor	0.072 pu
L_{gf}	Grid-side inductor	0.0433 pu
C_f	Filter capacitor	0.0684 pu
f_{sw}	Switching frequency	10 kHz
f_s	Sampling frequency	10 kHz
Z_L	Line impedance	0.04+0.1j pu
$K_{p,ic}$	Proportional gain of G_{ci}	10
$K_{r,ic}$	Resonant gain of G_{ci}	1000
$K_{p,PLL}$	Proportional gain of PLL	58.3
$K_{i,PLL}$	Integral gain of PLL	267.8

III. Loss of Synchronization and PLL Freeze

In order to analyze LOS, the steady-state power flow between two buses is considered as presented in [7]. The power flow between two buses connected to a line, considering the effect of line resistance is shown in Fig. 4(a). In order to analyze feasible operating points of the injected current vector, the phasor diagrams shown in Fig. 4(b) and 4(c) can be constructed. The injected current vector is referenced to the sending end voltage ($\boldsymbol{v_{PCC}}$), which is located on the horizontal axis. The receiving end voltage ($\boldsymbol{v_F}$) can be represented as a vector with a fixed length (V_F) and variable phase angle (θ_g) [19]. In Fig. 4(b), one operating point for an injected current is shown. In Fig. 4(c), the current magnitude is increased causing the operating point to be exactly the limit since the subtraction of $Z_L I_{PCC} e^{j(\theta_I+\theta_Z)}$ from V_{PCC} is equal to the fault voltage (V_F). If the current magnitude is further increased, an infeasible operating point is attempted, which leads to LOS. Using Fig. 4, the current transfer limits for an arbitrary impedance and fault voltage can be derived under steady-state conditions. In order for the subtraction of the voltage drop across Z_L from the PCC voltage to stay within the fault voltage magnitude (V_F), this corresponds to the condition where the vertical component of the impedance voltage drop is equal to the fault voltage magnitude as

$$\begin{aligned} V_F &= Z_L I_{lim} \sin(-\theta_I - \theta_Z) \\ \implies I_{lim} &= \frac{V_F}{Z_L \sin(-\theta_I - \theta_Z)}, \end{aligned} \tag{1}$$

which generally can be expressed as

$$I_{lim} = \frac{V_F}{Z_L |\sin(\theta_I + \theta_Z)|} \tag{2}$$

for any injected current and external grid impedance. When injecting full capacitive reactive current ($\theta_I = -90°$), the denominator in (1) is reduced to the line resistance. This means, that the current transfer limit during reactive current injection is solely determined by the voltage level at the fault location and the line resistance as

$$I_{lim} = \frac{V_F}{R_L}. \tag{3}$$

Actually, it can be deduced from (2) that for purely reactive current injection in either overexcited or underexcited operation, the maximum current magnitude will be constrained by the line resistance given any line impedance. This is the case since this is an inherent limitation of the passive network. I.e. when the fault voltage becomes too low, the active power absorbed by the resistance of the line can no longer be supplied from the grid voltage. This implies that the injection of pure reactive power from the converter at the PCC is no longer possible, resulting in an unstable operating condition if attempted.

An example of this is provided in Fig. 5(a) where the fault voltage magnitude is 0.05 pu and as seen in Table I, the resistance of the line is 0.04 pu. According to (3), a stable operating point should exist since $V_F > R_L$. However, this is

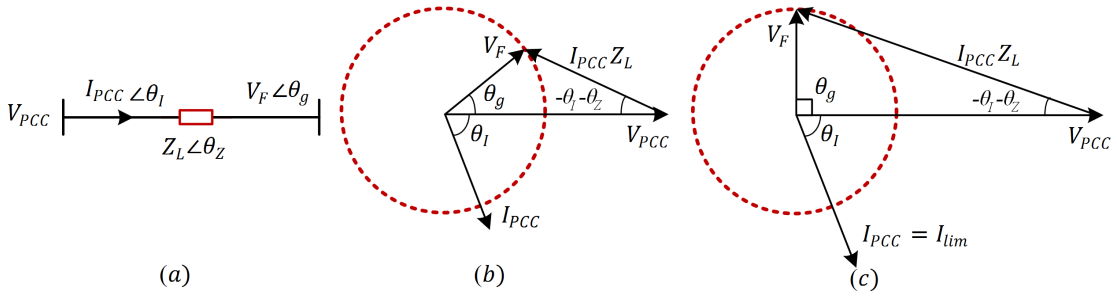
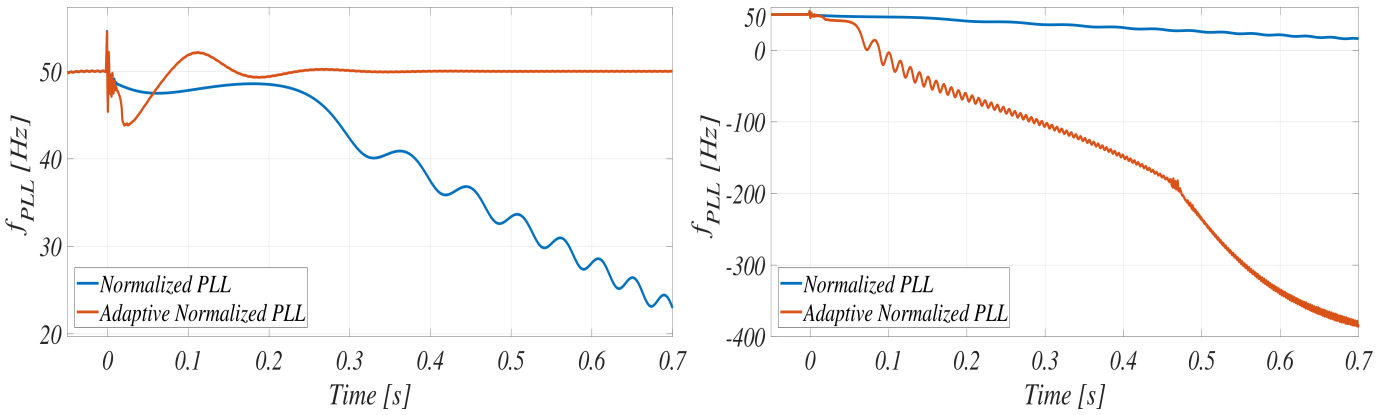


Fig. 4. Power transfer between the wind turbine connection point and fault point represented as a single line diagram and phasor diagram of current injection. The dotted red circle represents a fault voltage with constant magnitude and arbitrary angle and upper case letters denote the magnitude of the complex vector. *(a):* single-line diagram, *(b):* a stable case, *(c):* a limit case where the angle between sending end and receiving end voltage is 90° [7].



(a) Voltage at fault locations drops to 0.05 pu

(b) Voltage at fault location drops to 0.03 pu

Fig. 5. Stability analysis of PLL used to validate current transfer limits presented in (2) during a fault at 0 seconds. PLL saturation limits are not included to show the full effect of LOS.

only true for the case where the input voltage to the SRF-PLL is adaptively normalized as

$$\boldsymbol{v'_{\alpha\beta}} = \frac{\boldsymbol{v_{\alpha\beta}}}{\sqrt{v_\alpha^2 + v_\beta^2}} \cdot \frac{\omega_c}{s + \omega_c} \tag{4}$$

where $\boldsymbol{v'_{\alpha\beta}}$ is the PLL input voltage and ω_c is the cut-off frequency of the low-pass filtered adaptive normalized PCC voltage expressed in the stationary-reference frame. This indicates that besides a feasible steady-state operating point, the dynamics of the PLL strongly affect whether this equilibrium point can be reached. As pointed out in [20]–[22], this happens due to insufficient damping of the PLL control loop. Using the closed-loop small-signal model of the PLL, which is expressed as

$$\frac{\theta_{PLL}(s)}{\theta_g(s)} = \frac{VK_{p,PLL}s + VK_{i,PLL}}{s^2 + VK_{p,PLL}s + VK_{i,PLL}} \tag{5}$$

where V is the magnitude of the normalized voltage sent to the synchronization unit. Considering a fixed normalization term, the PLL input voltage is calculated based on the nominal voltage level at the PCC as

$$\boldsymbol{v'_{\alpha\beta}} = \frac{\boldsymbol{v_{\alpha\beta}}}{V_n}. \tag{6}$$

By comparing (5) to an approximation of a general second-order system

$$G_{2^{nd}}(s) = \frac{2\zeta\omega_N s + \omega_N^2}{s^2 + 2\zeta\omega_N s + \omega_N^2} \tag{7}$$

where ζ is the damping ratio and ω_N is the natural undamped frequency, it can be explicitly observed that by using the adaptive normalized PLL structure (4), the damping ratio is increased compared to the case of the fixed normalization term (6). This is also seen using (5) and (7) from which the damping ratio can be expressed as

$$\zeta = \frac{VK_{p,PLL}}{2\sqrt{VK_{i,PLL}}} = \frac{K_{p,PLL}}{2}\sqrt{\frac{V}{K_{i,PLL}}} \tag{8}$$

which is proportional to the square root of the voltage magnitude V. Considering the adaptive normalized case where it is assumed that $V = 1$ at all time, the damping ratio is explicitly determined by the PLL controller gains as it is evident from (8). Here, it can be seen that an increasing proportional gain will increase the damping ratio proportionally. Also, a decrease in the integral gain will increase the damping ratio.

In Fig. 5(b), the same analysis is performed but with the voltage at the fault location decreased to 0.03 pu which according to (1) should result in an unstable operating point. As anticipated, this holds true, but it can be seen that the

adaptive normalized PLL, in this case, has worse performance. This is due to the fact, that when the input voltage of the PLL is only normalized relative to the nominal voltage, as shown in (6), then for a decreasing voltage, the dynamics of the PLL is reduced which effectively slows down the PLL and increases its robustness to grid disturbances. The settling time of the PLL is inversely proportional to V [23], which satisfies the condition that the normalized PLL is slowed down during the fault, effectively reducing its bandwidth. From the analysis shown in Fig. 5, it could be beneficial to increase the damping ratio of the PLL by using adaptive normalization of the input. However, for very low voltages, it may have the opposite effect. Therefore, in order to circumvent and remove this issue of using current transfer limits to assess stability, the PLL can be frozen during the fault such that ride-through can be accomplished during any voltage level.

The process of freezing the PLL means that the action from the PI controller is bypassed by nullifying the controller error during the fault. This effectively keeps the PLL output at the frequency it had prior to the fault. The activation of the freeze mode can be determined by a fault signal (S_F) and a clear signal (S_C) where the fault signal initiates the freeze mode and the clear signal re-enables the PLL operation after the fault has been cleared. The fault signal is set high when the length of the instantaneous v_{PCC} vector drops below a set threshold value (V_r) and the clear signal is set high when v_{PCC} rises above V_r. The calculation of the clear signal is filtered to slow down its response with 20 ms compared to the fault signal. This is done to improve the resynchronization performance by keeping the PLL frozen during the transient when the fault is cleared. Freezing the PLL is a simple and robust solution to deal with LOS if it can be assumed that the voltages at the PCC terminals do not experience any phase jumps during the fault. If the fault impedance has an X/R ratio different from that of the grid impedance, then phase jumps will be present at the fault instant, which may deteriorate the performance of the frozen PLL. Therefore, the subsequent section aims to analyze how the injected currents during a low voltage situation are influenced by potential phase jumps at the fault instant. Furthermore, a phase compensation technique is developed to analyze whether phase jumps should be compensated when using a frozen PLL.

IV. Phase-Angle Jumps during Symmetrical Faults

As mentioned, during a three-phase fault not only the voltage magnitude is affected, usually so is the phase-angle of the voltage. This section analyzes how the phase-angle experienced at the PCC is influenced by the line impedance, fault voltage magnitude, and injected converter current. Using the simplified circuit diagram of the grid-connected converter system as shown in Fig. 6, the PCC voltage, considering a fault impedance of R_F, can be expressed as

$$\boldsymbol{v_{PCC}} = K_g(\omega_g)V_{th}e^{j(\theta_{th}+\phi_g)} + K_c(\omega_{PLL})I_{PCC}e^{j(\theta_c+\phi_c)} \tag{9}$$

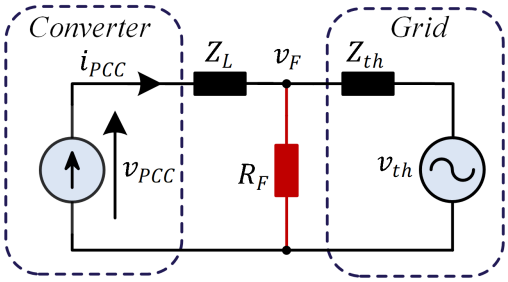


Fig. 6. Simplified circuit diagram of the grid-connected converter during a symmetrical fault where the converter is modeled as a controllable current source and the external grid is represented as a Thevenin equivalent.

where

$$K_g(\omega_g) = \left|\frac{R_F}{R_F + \boldsymbol{Z_{th}}(\omega_g)}\right| \tag{10}$$

$$K_c(\omega_{PLL}) = \left|\boldsymbol{Z_L}(\omega_{PLL}) + \frac{R_F\boldsymbol{Z_{th}}(\omega_{PLL})}{R_F + \boldsymbol{Z_{th}}(\omega_{PLL})}\right| \tag{11}$$

$$\phi_g(\omega_g) = \angle\left(\frac{R_F}{R_F + \boldsymbol{Z_{th}}(\omega_g)}\right) \tag{12}$$

$$\phi_c(\omega_{PLL}) = \angle\left(\boldsymbol{Z_L}(\omega_{PLL}) + \frac{R_F\boldsymbol{Z_{th}}(\omega_{PLL})}{R_F + \boldsymbol{Z_{th}}(\omega_{PLL})}\right) \tag{13}$$

where θ_{th} is the grid voltage angle and the angle of the injected converter current is $\theta_c = \theta_{PLL} + \theta_I$. As described in detail in [19] and utilized in [12], when considering that the fault impedance is highly resistive and that the converter is injecting reactive currents to the grid, the operation of the converter has a negligible impact on the voltage at the fault location during severe faults. Accordingly, the second term in (11) and (13) can be neglected since the converter will only change its local voltage based on the current injected to the line impedance Z_L. This is identical to the analysis of voltage sag characteristics for radial systems, which is usually derived from the voltage divider formula where the injected current from the distributed generation is assumed to be zero [24], [25]. Therefore, by considering that the converter has a negligible impact on the voltage at the fault location (zero converter current), while considering that $\omega_g = \omega_{PLL}$, the PCC voltage can be written as

$$V_{PCC}e^{j\theta_{PCC}} = V_Fe^{j\theta_g} + Z_LI_{PCC}e^{j(\theta_I+\theta_Z)}, \tag{14}$$

where θ_{PCC} is given relative to θ_{PLL} and

$$V_F = K_gV_{th}, \qquad \theta_g = \theta_{th} + \phi_g. \tag{15}$$

When comparing the voltage at the fault location ($\boldsymbol{v_F}$) before and during a fault, the voltage sag and phase jump can be expressed as

$$V_{sag} = 1 - K_g = 1 - \frac{R_F}{\sqrt{(R_F + R_{th})^2 + X_{th}^2}}, \tag{16}$$

$$\theta_\Delta = \theta_g - \theta_{th} = \phi_g = -\tan^{-1}\left(\frac{X_{th}}{R_F + R_{th}}\right). \tag{17}$$

Here it can be seen that if the fault is solid ($R_F = 0$), then the voltage sag will be 1 pu, i.e. the fault voltage magnitude will be zero. Also, it can be noticed that for a positive reactance

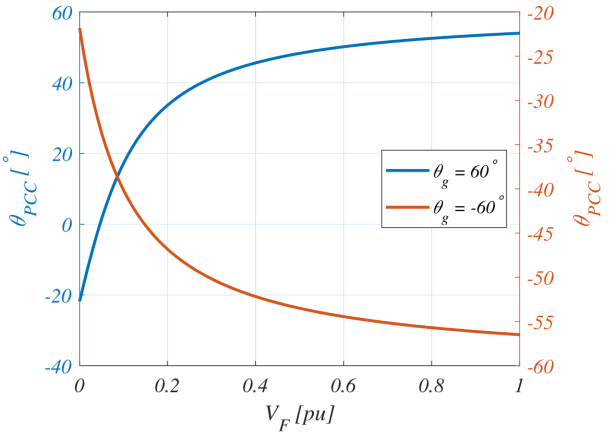


Fig. 7. Phase jump seen at the PCC in Fig. 2 as a function of the fault voltage magnitude and the sign of the phase jump happening at the fault location. The line impedance considered is $Z_L = R_L + jX_L$ and the converter is considered to inject nominal capacitive reactive current.

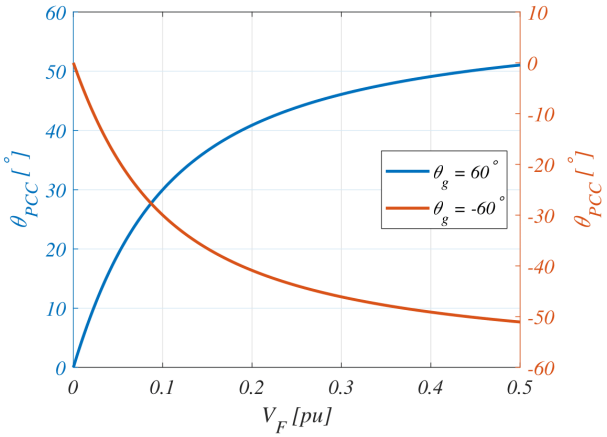


Fig. 8. Identical case as for Fig. 7 but with a purely inductive line impedance.

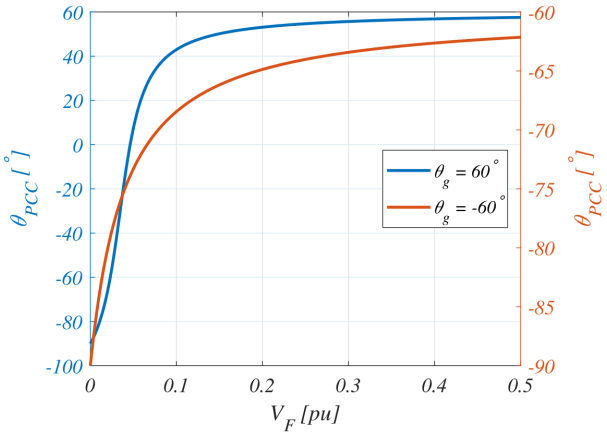


Fig. 9. Identical case as for Fig. 7 but with a purely resistive line impedance.

of the equivalent grid impedance, the phase jump will be negative and considering a solid fault, the phase jump will be the negative of the impedance angle of the equivalent grid. As expected, the phase-angle jump at the fault location will decrease with an increasing Short-Circuit Ratio (SCR) of the external network. Apart from the SCR of the system, the X/R ratio has a large influence on the phase-angle jump. As the fault impedance is highly resistive, the phase jump will increase with an increasing X/R ratio of the equivalent grid impedance. If the fault impedance is considered to have a non-zero X/R ratio, the phase jump becomes

$$\theta_\Delta = \tan^{-1}\left(\frac{X_F}{R_F}\right) - \tan^{-1}\left(\frac{X_F + X_{th}}{R_F + R_{th}}\right) \qquad (18)$$

where it explicitly follows that if $X_F/R_F = X_{th}/R_{th}$, then the phase-angle jump will be zero.

All of this describes the phase-angle jump at the fault location, whereas it is desired to investigate how this phase jump is propagated to the PCC where the converter is connected. Using (14), the phase jump occurring at the PCC as a function of the fault voltage magnitude, line impedance and for both positive and negative phase jumps are graphically shown in Fig. 7-9. For all cases, the converter is injecting nominal reactive current ($\theta_I = -90°$) in compliance with the grid code. As it can be noticed from the line with both resistance and reactance (Fig. 7), the phase jump at the PCC is not symmetrical with respect to the sign of the phase jump at the fault location. Also, the phase change seen on the PCC is highly dependent on the fault voltage magnitude V_F. Actually, in the extreme situation where $V_F = 0$, the phase angle at the PCC must be $\theta_I + \theta_Z$ which during capacitive reactive current injection is $-90° + 68.2° = -21.9°$, which is seen exactly to match θ_{PCC} for either sign of θ_g in Fig. 7. This means, that when the fault voltage is very low, the PCC phase angle is nearly independent on the compensation angle since the converter must supply the resistive losses of the line. For a purely inductive line, the phase jump seen on the PCC is shown in Fig. 8. Here a symmetrical behavior is seen, since the limit angle when V_F approaches zero is also zero. It can be seen for the resistive line in Fig. 9 that a large difference exists between the case of a positive phase jump to the case of a negative phase jump. As anticipated, both cases approach $-90°$ for a solid fault. However, considering a positive phase jump, a large change is seen in the PCC angle for fault voltage magnitudes below 0.1 pu. As mentioned for the case of Z_L, this happens since when the fault voltage magnitude is extremely low, the grid voltage can no longer supply the resistive losses in the line, and therefore the PCC voltage angle has to align with the injected current such that pure active power is injected to the grid as V_F approaches zero.

V. Phase Compensation of Frozen PLL

To be able to assess the performance of the frozen PLL during phase jumps, this has to be compared to a structure which aims to compensate the phase jump and thereby improving the injected currents. When this is done, then it can be determined whether the frozen PLL results in a satisfactory result or not. Therefore, the phase compensation techniques to be presented in this section is not critical for the analysis and focus of the paper but is used for a comparison which facilitates the characterization of the frozen PLL. In order to compensate a potential phase jump, a developed method which estimates the actual phase jump at the fault location is compared with

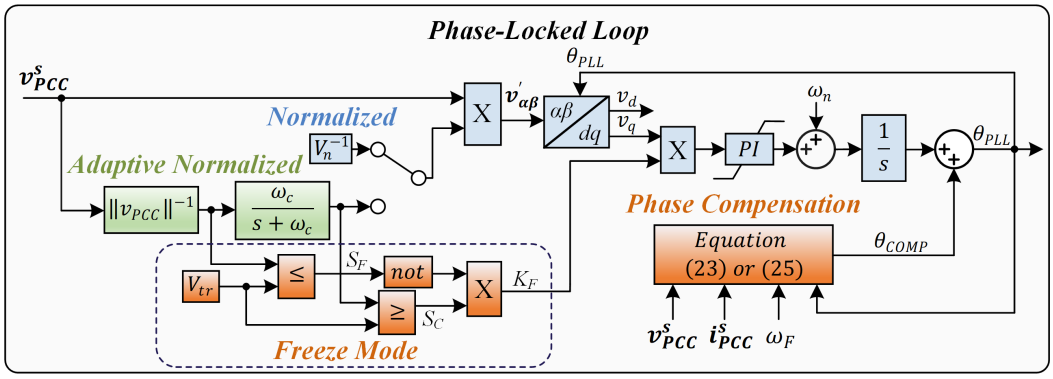


Fig. 10. Structure of PLL used in Fig. 2 with three configurations: normalized, adaptive normalized and freeze mode with phase compensation. ω_F is the frozen PLL angular frequency [26].

a method where the instantaneous phase jump at the PCC is compensated. Using the two-bus diagram shown in Fig. 4(a) and by knowing the PCC voltage, the injected current, and the line impedance, the phase difference between the fault location and PCC voltage can be estimated. The voltage at the fault location can be expressed as

$$\boldsymbol{v_F^s} = \boldsymbol{v_{PCC}^s} - \boldsymbol{i_{PCC}^s}(R_L + sL_L) \tag{19}$$

where superscript s denotes that the complex space vector is expressed in the stationary $\alpha\beta$-reference frame and s is the Laplace variable. By applying Park's transformation matrix on both sides ($s \rightarrow s + j\omega_n$), this is transformed to the synchronous dq reference frame as

$$\boldsymbol{v_F} = \boldsymbol{v_{PCC}} - \boldsymbol{i_{PCC}}(R_L + jL_L \underbrace{(\omega + \omega_n)}_{\omega_F}) \tag{20}$$

which can be represented by a real and an imaginary part as

$$\mathrm{Re}\{\boldsymbol{v_F}\} = v_{PCC,d} + i_{PCC,q}\omega_F L_L - i_{PCC,d}R_L \tag{21}$$
$$\mathrm{Im}\{\boldsymbol{v_F}\} = v_{PCC,q} - i_{PCC,q}R_L - i_{PCC,d}\omega_F L_L \tag{22}$$

where ω_F is the angular frequency of the frozen PLL and R_L, L_L are the resistance and inductance of the line impedance Z_L, respectively.

The term $\omega + \omega_n$ is replaced with ω_F since the estimated frequency of the frozen PLL will not change during the fault. From this, the phase-angle of the fault voltage can be calculated as

$$\theta_{COMP} = \tan^{-1}\left(\frac{\mathrm{Im}\{\mathbf{v_F}\}}{\mathrm{Re}\{\mathbf{v_F}\}}\right). \tag{23}$$

The presented phase compensation technique alongside the freeze mode control and two discussed methods for input voltage normalization (4), (6) are depicted in Fig. 10. In addition to the activation of the freeze mode as dictated by the gain K_F as shown in Fig. 10, an additional feature is introduced to K_F during the re-synchronization procedure. To avoid the frozen PLL to suddenly be re-enabled after the fault has been cleared, the reconnection is performed slowly with a continuous function with continuous derivatives. This smooth transition is obtained by modifying K_F during the re-synchronization process as

$$K_F = \frac{1}{2}\left[1 - \cos\left(\int A \neg S_F S_C \; dt\right)\right] \neg S_F S_C, \tag{24}$$

where $\neg$ denotes the negation of a logical signal. A is the integration gain and it is selected such that the output of the integrator, given that $\neg S_F S_C = 1$, increases to π in approximately 60 ms. The output of the integrator is limited between zero and π and is reset on the rising edge of $\neg S_F S_C$. This effectively gives that the gain K_F will drop to zero when a fault occurs. However, when the fault is cleared and the clear signal S_C takes a logical high, the integrator is reset and the value of K_F will increase smoothly as a sinusoid from 0 to 1. Since the phase-compensation method compensates the phase error in a feed-forward path, a continuous feed-forward will destabilize the system since the terminal voltages and grid currents are directly fed through. To avoid this problem, the phase difference is estimated and corrected once with a single value, 15 ms after the fault, making the converter capable of injecting the desired currents 20 ms after the fault instant. Since the phase angle between the grid voltage and the voltage at the PCC is not zero prior to the fault, only the difference observed in θ_{COMP} is compensated, i.e. the absolute difference is not of interest, only the change.

One might ask why it should be necessary to estimate the phase jump behind the line impedance and not simply inspect the phase change occurring in the voltage at the PCC. In real wind turbine applications, the converter does not have any information about the voltage behind the line impedance and the converter should only react to what is happening at the PCC or local connection point. However, if the phase jump occurring at the PCC is compensated using the same feed-forward structure as shown in Fig. 10, but instead by estimating the phase jump as

$$\theta_{COMP,pcc} = \tan^{-1}\left(\frac{v_{PCC,q}}{v_{PCC,d}}\right), \tag{25}$$

the injection of capacitive reactive current is noticed to be less (closer to the desired response), compared to the method presented in (23), in certain scenarios. Therefore, this method is included to analyze how the injected current vector is

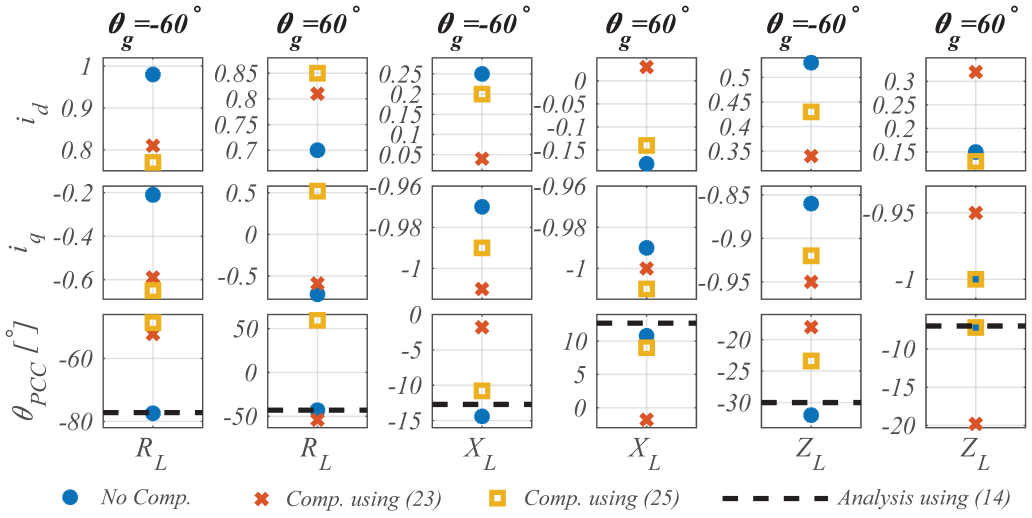


Fig. 11. Simulated case study of resulting active current, reactive current, and PCC voltage angle for different phase jumps and different types of line impedances during a fault where $V_F = 0.03$. Results are shown for the frozen PLL without phase compensation and with phase compensation using (23) and (25). θ_{PCC} is given relative to the constantly increasing θ_{PLL}. The ideal desired response is $i_d = 0$, $i_q = -1$, and $\theta_{PCC} = 0°$.

affected by each compensation scheme and to investigate how the PCC voltage is influenced during a fault including a phase jump. It should be mentioned that when the PLL is frozen during the fault, the converter changes its synchronization method from the voltage-based grid-following synchronization method to a purely grid-forming static reference. This implies, that if a fault occurs and the PLL is frozen, the phase-angle of the injected current vector is changed from injecting active power to capacitive reactive power relative to the pre-fault PLL states. If the static stability requirement in (2) is violated during this movement, the PCC voltage angle will naturally advance to a different location which satisfies the laws of physics. In this way, the PLL freeze method will be stable for any low-voltage condition including zero-voltage conditions. As it is the focus of this work when the fault voltage magnitude is non-zero, it is possible to locate the current vector at a point close to the stability criterion such to comply as much as possible with the grid codes requirements for dynamic voltage support and fast reactive current provision. The relocation of the current vector from the initial frozen PLL state is accomplished using the described phase-compensation method seen in Fig. 10. Accordingly, with the developed phase-compensation method in addition to the PLL freeze, stability will also be guaranteed for any voltage level. This is obviously true as if an infeasible operating point is attempted by modification of the output phase by θ_{COMP}, the PCC voltage angle will position itself independently, as the feedback synchronization loop is eliminated during the fault.

The described re-synchronization process of the frozen PLL structure is here used for improved fault-recovery response and will not change the observations to be seen in the subsequent analysis. Therefore, the transition between grid-forming and grid-following operation is not critical here and other methods for seamless transition may be used as thoroughly studied for microgrid applications, e.g. [27], [28].

A comprehensive simulation study is conducted to reveal whether the injected current vector can be improved by using phase compensation for both positive and negative phase jumps during a fault with a voltage magnitude of 0.03 pu. To that end, the effect is also examined for three different line impedance configurations: purely resistive line, purely inductive line, and a line consisting both of a resistive and a reactive part. This analysis is shown in Fig. 11 where the two compensation methods shown in (23) and (25) are compared to the case without compensation and related to the ideal desired response ($i_d = 0$, $i_q = -1$, and $\theta_{PCC} = 0°$). Regarding the phase change happening on the PCC, it is seen that the case without compensation closely match the predicted phase change calculated from the analysis in (14), which is shown as the black dashed lines and the blue dots in Fig. 11.

For the case with Z_L and $\theta_g = -60°$ and employing the compensation technique in (23) compared to (25), the injected active current can be reduced while the injected capacitive reactive current is increased close to -1 pu. On the other hand, when $\theta_g = 60°$ for the case with Z_L, compensating the phase jump occurring at the fault location results in a decreased power injection accuracy when using (23). Also, it has no effect to compensate for the phase jump using (25). Hence, for positive phase jumps in the case of Z_L, it is recommended not to compensate anything and simply just use a frozen PLL structure during the fault.

For the inductive line and a positive phase jump, the compensation in (23) shows the best performance in the sense that the ideal response ($i_d = 0$, $i_q = -1$, and $\theta_{PCC} = 0°$) is nearly accomplished. For a negative phase jump, the same tendency is evident. For the resistive line, (25) shows the best performance for negative phase jumps whereas no compensation results in the best performance for positive phase jumps.

Based on the inductive and resistive line some detailed comments must be made. As seen from (1), during capacitive reactive current injection into an inductive line, the current transfer limit approaches infinity. This implies that there is no need to freeze the PLL in the first place, i.e. no need for any compensation. Moreover, one should remember, that the

requirements set by the grid code are formed in order for the converter to support the voltage at the PCC. Accordingly, for a resistive grid, this is attained by maximizing the active current injection and not the injection of reactive current. Also, a short circuit fault is mainly resistive [29] which means that for a resistive grid, the phase jump will likely not occur in the first place, i.e. phase compensation is not needed. To that end, by considering that the line and grid impedances in most cases are more inductive than capacitive and knowing that most fault impedances are highly resistive, positive phase jumps are not likely to occur in any practical configuration. Applicable for any line impedance when the fault voltage is extremely low is that it is practically impossible to alter the injected currents to further boost the PCC voltage [11]. Furthermore, the system has negligible sensitivity to voltage phase jumps when V_F is low; therefore even though the current injection can be improved for negative phase jumps for the case of Z_L, one may argue that when looking at the increase in PCC voltage from using no compensation to phase compensation using (23), it is not worth the effort to compensate any phase jump for any line impedance when V_F is low. As an example, the increase in PCC voltage magnitude by using (23) compared to no compensation is only 0.7% for the case of Z_L and a negative phase jump. Putting all of this together, the main claims from this analysis are the following:

- A phase jump seen on the PCC is highly dependent on the line impedance and fault voltage magnitude.
- For a resistive line, phase compensation is not needed.
- For an inductive line, the PLL is not required to be frozen, i.e. phase compensation is not needed.
- Since the PCC phase angle and voltage magnitude are nearly independent of injected currents and line impedance, phase compensation can always be avoided when the fault voltage is extremely low.

Accordingly, since LOS usually occurs when the fault voltage is very low and that the frozen PLL, in that case, do not need to care about phase-angle jumps as just disclosed, the frozen PLL structure actually shows itself as a simple and robust control strategy to avoid LOS while inherently enables the ability to comply with a potential zero-voltage condition.

VI. Comparison and Robustness Analysis

The tests and findings of the frozen PLL with and without phase compensation are yet to be compared to existing solutions for LOS. To that end, an extended robustness analysis is performed to evaluate whether the present disclosures are also valid for different system parameters.

A. Comparison of Frozen PLL to Existing Methods

The analysis performed is now related to the methods proposed in [7], [10]–[12] which all increase the active current injection during the fault to ensure stability. In [11], $i_d > 0.4$ pu during the fault and in [12], an additional control loop is introduced to the PLL, which increases the active current to 0.3-0.4 pu during a fault where $V_F = 0.02$ pu. In [7], the active current is adaptively changed based on the PLL frequency error, which increases the active current to 0.2-0.5 pu dependent on the X/R ratio of the line. Thus, instead of using an additional control loop and having the inconvenience of tuning any additional controller parameters with their own stability issues, freezing the PLL will simply make the PCC voltage shift its phase in order to deliver the needed active power consumed by the line. This is exactly what the methods in [7], [10]–[12] aim to do, but with increased control complexity. Also, the solution provided in [7] may not operate under all conditions since the pre-fault current injection is assumed to be zero. This effectively provides an initial stable operating point for the control which will not be the case for a real application with active power injection prior to the fault.

To exemplify this, when $V_F = 0.03$ pu and no phase jump occurs, the frozen PLL structure alone result in $i_d = 0.3$, $i_q = -0.97$ and $\theta_{PCC} = -18^\circ$ which means that by just freezing the PLL during a low voltage fault, the same or perhaps improved power injection capability can be achieved compared to the more complex methods proposed in [7], [10]–[12]. The only disadvantage of this method is the assumption of a constant grid frequency during the fault which could be violated in future low-inertia grids. Anyhow, to avoid this limitation, a simple frequency estimation algorithm (i.e. zero-crossing technique) can be activated during the fault to correct the frozen PLL frequency if needed.

As mentioned in the introduction, the PLL freeze is partly proposed in [13], [14], however, without investigating the influence of phase jumps. Besides no direct comparable results, the activation of the freeze mode in [13] is based on the PLL error signal instead of the voltage magnitude information, which may trigger the freeze mode unintentionally during a non-severe transient event. Furthermore, as can be seen in [13], the converter current is removed during the synchronization procedure, which cannot be considered acceptable for modern requirements of voltage and frequency support. In [14], the PLL freeze method is recommended for improved fault ride-through capability. Here considering a severe grid fault with $V_F \approx 0$, the injected currents when employing the frozen PLL is $i_q \approx 1.1$ pu and $i_d \approx 0.3$ pu, which in agreement with the presented method shows improved performance with a low control complexity. Nonetheless, as the method in [14] is not experimentally verified, no resynchronization procedure is considered. As is identified through this work, due to the noise contained in experimental fault analysis, a smooth re-synchronization procedure, as included in this presented method, is necessary to obtain a satisfactory fault-recovery performance when examining an experimental test environment. This issue may not have been identified using the frozen PLL in [14] as only simulation results are conducted. As the underlying structure of the PLL presented here and the one in [14] are the same, their performances are surely alike. However, it should be noted, that in addition to what is done in [14], the essential contribution of this paper is the analytical explanation of why the frozen PLL structure works alongside disclosing its performance towards phase-angle jumps. Accordingly, from the presented analysis, a more complete characterization of the abilities of the frozen PLL is therefore given.

Remark: In case one wishes to compensate for a negative

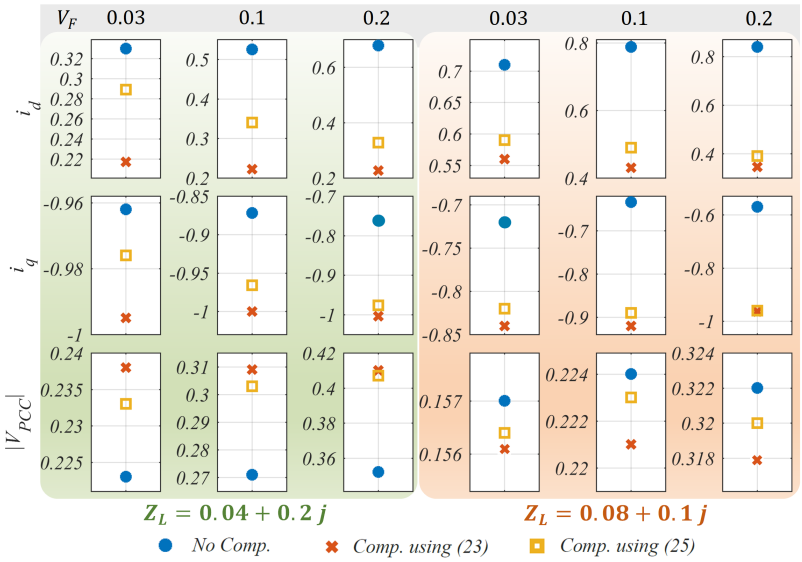


Fig. 12. A simulation study of resulting active current, reactive current, and PCC voltage magnitude for two different types of line impedances and three levels of fault voltage magnitudes. Results are shown for the frozen PLL without phase compensation and with phase compensation using (23) and (25). The phase jump for all cases is $-60°$.

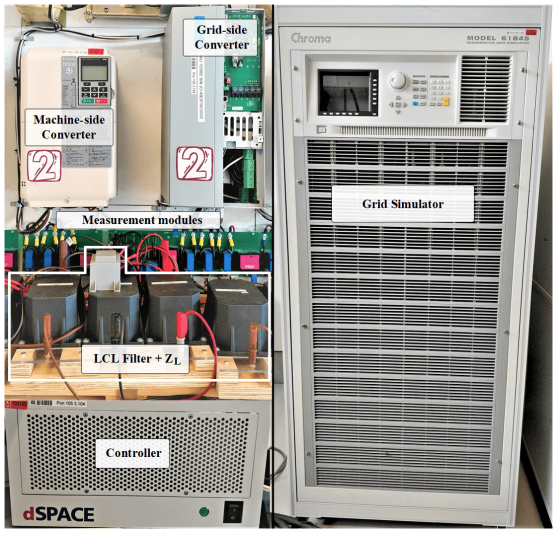


Fig. 13. Laboratory setup used to verify the simulation analysis in Fig. 11. The grid-side converter is regulated using a dSPACE control platform to inject currents through an LCL filter into a grid simulator.

phase jump using (23) to improve the injected currents, an estimate for the resistance and reactance of the line can be estimated as proposed in [30], [31].

B. Robustness Analysis of Frozen PLL

It is claimed in the previous analysis that the frozen PLL structure can be used successfully without any use of phase-compensation methods when the fault voltage is extremely low. This is reasonable as the output of the temporarily blinded converter needs to satisfy (2). This subsection is devoted to analyzing whether this claim is also valid for non-zero fault voltage levels and different line impedances. To verify the robustness of this method, 18 different cases as shown in Fig. 12 have been simulated. These include two different line impedances, each tested for three different fault voltage levels and three different types of control. All tests are for a phase jump of $-60°$ as this was identified to be the case of interest from the analysis of Fig. 11. The green left part of Fig. 12 shows the results of the per-unit active current, reactive current, and PCC voltage magnitude for the case where the line reactance has been doubled from its original value. The orange right part of Fig. 12 shows the same tests but where the line resistance has been doubled. With these tests, both the line impedance and fault voltage magnitude is significantly different from the cases shown in Fig. 11. The findings from this analysis are in strong agreement with what was analyzed previously for nearly zero-voltage conditions. At first, it can be noticed that with a decreased severity of the fault considering the line with increased reactance, the benefits attained by using phase compensation are elevated. This means, that for conditions where LOS may occur for larger voltage levels and for high-impedance weak-grid conditions, the phase-compensation method will provide a larger benefit in terms of dynamic voltage support. Similarly as already experienced for the line with increased resistivity, the non-compensated PLL freeze method will bring the best result. This is intuitive as the phase compensation method aim to inject capacitive reactive current to the grid in compliance with the grid codes. However, for a line with a high resistive part, this is not the optimal current angle location for voltage support. For the right part of Fig. 12, the PCC voltage is nearly independent of the control structure employed as the resistance and reactance are of similar size. For lines dominated by resistance, the non-compensated frozen PLL will provide the highest voltage support. From this, the difference in voltage support among the different methods becomes more pronounced for high network impedances and fault voltage levels. However, even with a doubling in the line impedance and a fault voltage magnitude more than six times the initial value as tested in Fig. 12, the frozen PLL is still seen to provide quite acceptable results without any further information of the grid dynamics.

Remark: It should be noted that other phase-compensation techniques than the ones used for the comparison in this paper may be utilized. However, this will not change the above findings since, for very low fault voltage magnitudes, the phase-angle difference between the PCC voltage and the injected current vector is nearly independent of the compensation. Instead, the phase-angle difference is mainly determined by the network impedances. With a less severe fault where the voltage sag is lower, the utilized phase compensation technique starts to have a larger impact on the improvement in the injected currents. Yet, as freezing the PLL aims to solve the problem of LOS, which usually happens during very deep voltage sags, a frozen PLL may not be initiated in the first place; hence, the phase jump can be accurately tracked. Therefore, the above claims can be considered independent of the phase-compensation technique used.

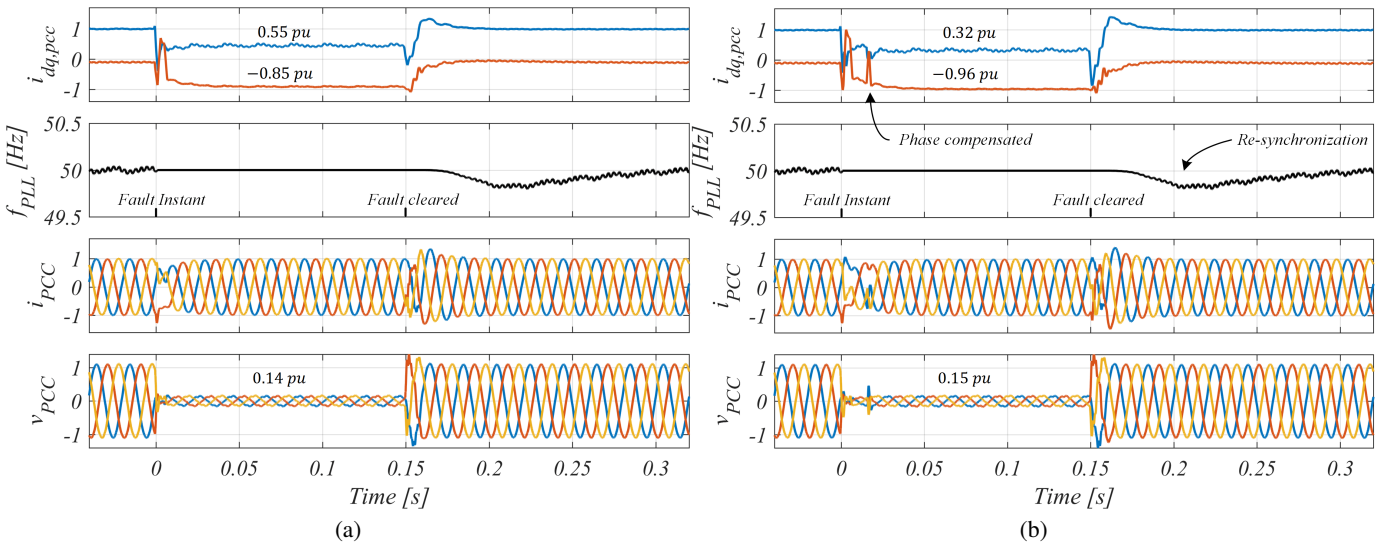


Fig. 14. Experimental validation of Fig. 11 for the Z_L for a $-60°$ phase jump during a fault voltage of 0.03 pu. (a): Fault response of PLL freeze without phase compensation. (b): PLL freeze with phase compensation using (23). The per-unit values of current and voltage during the fault is given in Table II.

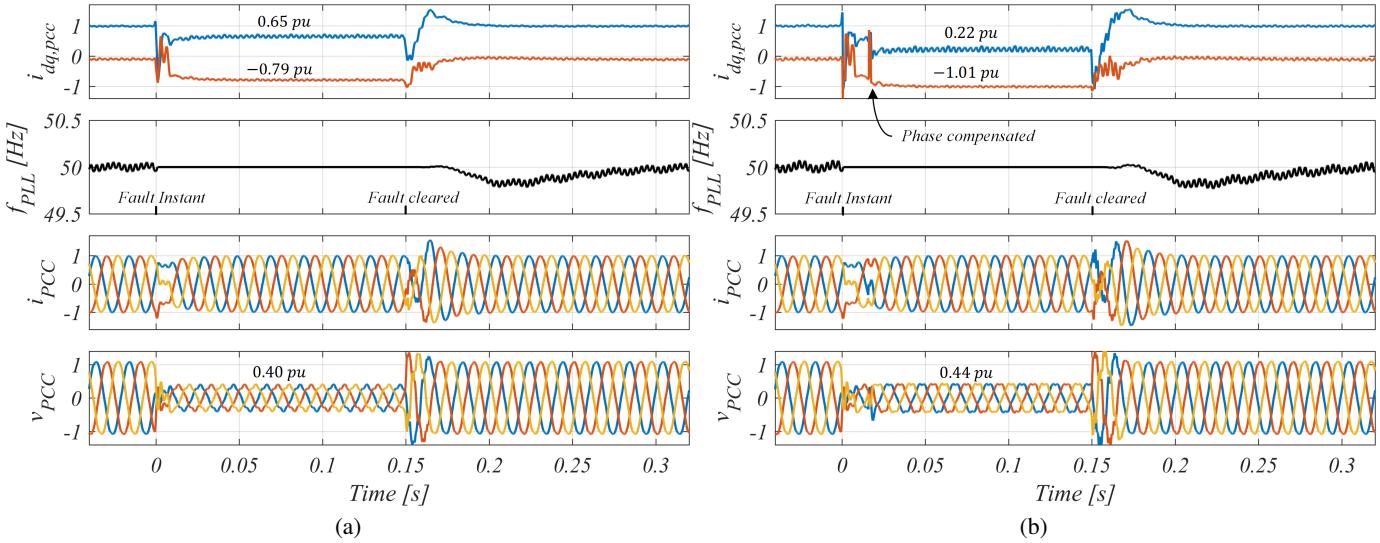


Fig. 15. Experimental validation of Fig. 12 for the $Z_L = 0.04 + 0.2j$ for a $-60°$ phase jump during a fault voltage of 0.2 pu. (a): Fault response of PLL freeze without phase compensation. (b): PLL freeze with phase compensation using (23).

VII. Experimental Validation

The analysis performed in § V is experimentally verified in the laboratory setup shown in Fig. 13 where the grid-side converter is controlled using a dSPACE DS1007 PPC processor board. A severe symmetrical fault with a voltage magnitude of 0.03 pu and a phase jump of $-60°$ is considered for a line impedance consisting of both a resistive and an inductive part. This case is considered since this was the only condition where it could be beneficial to use phase compensation to improve the injected fault currents. The fault voltage waveform is generated using a four-quadrant grid simulator manufactured by Chroma. The test is performed for a frozen PLL structure with and without the aid of the presented phase compensation method in (23). The system and control parameters used for the experimental setup are identical to the ones shown in Table. I. The experimental results are shown in Fig. 14 where values for the injected current and PCC voltage during the fault are listed in Table II alongside the simulated results from Fig. 11. These closely match the analytical results and simulation studies shown in Fig. 11. The small deviations from the simulated case might be due to a low resolution of the voltage measurements when the fault voltage is low and that the wires in the laboratory introduce additional resistance in the setup. As discussed in § V, the re-synchronization procedure of PLL is done softly as described in (24). This can be seen in Fig. 14 which results in a slow and smooth transition from the frozen state back to the normal operating condition. As it is anticipated, even though the phase compensation technique can improve i_d, i_q, and θ_{PCC}, the additional voltage boost at the PCC when using

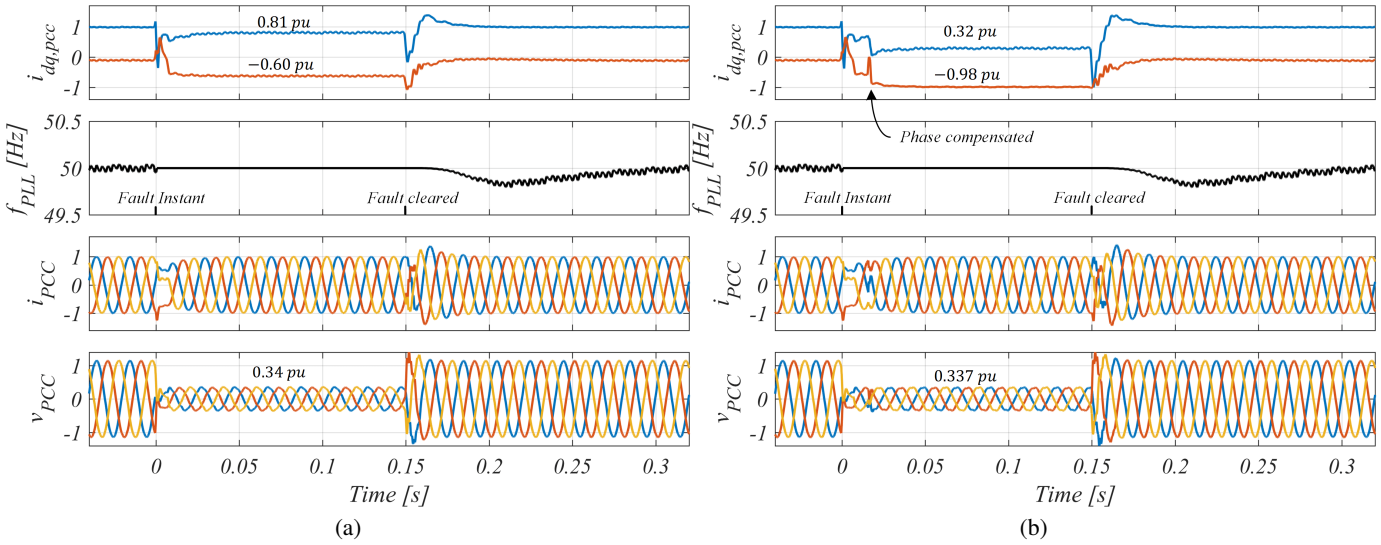


Fig. 16. Experimental validation of Fig. 12 for the $Z_L = 0.08 + 0.1j$ for a $-60°$ phase jump during a fault voltage of 0.2 pu. (a): Fault response of PLL freeze without phase compensation. (b): PLL freeze with phase compensation using (23).

TABLE II
EXPERIMENTAL RESULTS DURING FAULT OF FIG. 14 IN COMPARISON TO SIMULATED RESULTS FROM FIG. 11.

Symbol	No Comp.	Comp. using (23)
Experimental		
i_d	0.55 pu	0.32 pu
i_q	-0.85 pu	-0.96 pu
θ_{PCC}	-32.4°	-21.6°
V_{PCC}	0.14 pu	0.15 pu
Simulation		
i_d	0.53 pu	0.34 pu
i_q	-0.86 pu	-0.95 pu
θ_{PCC}	-32°	-18°

the phase compensation is only 0.01 pu. This again supports the recommendation of simply riding through the low-voltage symmetrical fault without using any phase compensation.

To verify the robustness analysis of the frozen PLL, two different scenarios have been selected for experimental validation. These are the two cases where the line impedance and fault voltage magnitude have been changed the most. The results from the case where the line reactance has been increased are shown in Fig. 15 without and with phase compensation for a fault voltage magnitude of 0.2 pu and a phase jump of $-60°$. It is evident that the inspected i_d and i_q values closely match the ones predicted in Fig. 12. A larger discrepancy is seen in the PCC voltage magnitude, which may result due to the laboratory impedances being a bit larger than the simulation parameters. As anticipated, the voltage boost for the case of higher reactance and higher fault voltage magnitude is increased using phase compensation. However, even with the impedance and fault voltage magnitude being changed significantly, the PCC voltage is only 0.04 pu higher compared to the case without any phase compensation. The second case of the robustness analysis for a line with increased resistance and a fault voltage magnitude of 0.2 pu is shown in Fig. 16. Here, the experimental results closely match the simulation studies from where it can be seen that for the case with $Z_L = 0.08 + 0.1j$, the PCC voltage magnitude is hardly affected by the phase compensation method.

VIII. CONCLUSION

With higher penetration of RES into the power system, stable and safe operation during fault events can be a challenge. During severe symmetrical faults, the voltage at the connection point can reach extremely low values which can cause the control system to become unstable when trying to inject the demanded power. To allow for zero-voltage ride-through capability without the need to consider current injection limits or implementation of additional control loops, a frozen PLL structure is employed in this paper, in which the RES and external power system is represented as a simplified two-bus system. A frozen PLL can ensure stability for any voltage level but how it behaves during phase jumps has not previously been revealed. A comprehensive simulation study is conducted to evaluate how the PCC voltage and current injection capability are influenced during a severe symmetrical fault including voltage phase jumps. Two different phase compensation techniques are compared for the frozen PLL to uncover whether the power transfer can be improved with the aid of phase compensation. This comparison is performed for three types of line impedance configurations to enhance the generality of the study and advice on when to employ the phase compensation for the frozen PLL structure. It is shown that phase compensation should only be performed for negative phase jumps occurring for line impedances consisting of both considerable resistance besides reactance. However, even though a proposed phase compensation technique is shown to improve the power transfer during phase jumps, it is revealed that a frozen PLL structure alone can allow for zero-voltage ride-through, which is robust to phase jumps when the fault voltage is low. To that end, variations in the fault voltage

magnitude and line impedance are performed to visualize the robustness of the frozen PLL. Finally, the performance of the frozen PLL is compared to state-of-the-art solutions to avoid LOS and the power transfer capability of a frozen PLL with and without phase compensation is experimentally verified. From this, the contributions of this paper are as follows:

1) A description of how the PCC voltage phase angle together with injected active and reactive currents are influenced by phase jumps during low-voltage situations for three configurations of line impedances alongside a robustness analysis with varying fault voltage levels and values of line impedances.
2) Based on a comparison between a developed phase compensation technique and a compensation method using the instantaneous phase change at the PCC, it is revealed that phase compensation might not be necessary during any low-voltage situations, and that a frozen PLL structure can by itself allow for zero-voltage ride-through, including phase jumps in a stable, simple, and robust manner. In this way, it is recognized that the drawback of the frozen PLL structure being blind to phase-angle jumps at the PCC, does not seem to be a significant drawback.

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