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Analysis of cascaded silicon carbide MOSFETs using a single gate driver for medium voltage applications

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Abstract: Medium voltage power supplies for applications such as electrostatic precipitators are used in industrial plants to remove particles from fumes. Current solutions based on silicon devices rely on high-voltage transformers to reach the required output voltage levels. New wide band gap materials such as silicon carbide have higher electric breakdown voltage, and thus fewer devices are required in series to withstand the output voltage. Owing to the faster switching speed of silicon carbide devices further demands are put on the serialisation method. In this study, a cascaded series-connection method using only a single external gate signal is analysed in detail, guidelines to size the resistor–capacitor–diode-snubber are proposed and its applicability is experimentally demonstrated. The circuit is tested with four series-connected devices in a double pulse test at 2400 V and current levels of 250–800 mA to show the load dependence. The serialisation technique is tested in a boost converter operating in discontinuous conduction mode but is limited to 1200 V due to an oscillating state occurring after zero current crossing. Finally, the technique is tested at 2400 V and 10 kHz in a synchronous boost converter, which demonstrates the proposed design guidelines.

1 Introduction

New silicon carbide (SiC) devices offer potential advantages in medium voltage power supply design. SiC has higher blocking voltage and faster switching speed when compared to its silicon (Si) counterparts [1, 2]. The increased blocking voltage reduces the required number of devices in series to reach a given voltage rating of a converter. This potentially offers easier entry into the medium voltage range for converter designers. Medium voltage converters are used for electrostatic precipitators (ESPs). ESPs are used to remove particles from fumes in many industrial applications. They rely on medium voltage power supplies to energize the filter, typically to a negative voltage in the range of -40 to -100 kV [3, 4]. The high voltage causes corona discharges in the proximity of the high voltage electrode where the electric field is strongest [5]. This requires controllable medium voltage power supplies. The commonly used technologies are based on Si thyristor or insulated gate bipolar transistors switching sets rated at a few kV, and high voltage transformers are then used to step up the voltage to the required level [4, 6–9]. By utilizing the high voltage blocking capabilities of SiC devices there is a potential to remove the bulky high voltage transformer, improve system efficiency and increase converter power density.

However, reaching the required output voltage rating by series connecting devices is not trivial. Deviations in device parameters and mismatching of gate driving signals result in an unequal distribution of voltage across a string of devices. This leads to failure of devices which are exceeding their individual blocking voltage. Additional circuitry is used to distribute voltages equally between devices during both transients and steady state. However, the high voltage ratings and fast switching speeds of SiC increase sensitivity of parasitics in the circuit design [10], [11]. Reduced switching times requires faster response of passive or active circuitry used to shape the switching transients. Thus serialization techniques that have proven their worth for Si technology might not be beneficial for series connecting SiC devices.

The passive RCD snubber circuit is one of the most popular techniques for series operation of devices. The snubber circuit shapes the transient waveform of each device to minimize voltage imbalances, but increases the total switching time. Passive snubbers reduce switching losses within each device, but losses are moved to the snubber circuit itself. Its simple design and straight-forward implementation is advantageous and offers high reliability [12]. The RCD snubber results in good transient behavior with reduced oscillation and voltage imbalances for even high $\mathrm{d}v/\mathrm{d}t$, but requires isolated synchronous gate driver signals [13]. For SiC devices the requirements on propagation delay are strict. Gate balancing core method balances the voltage and current of each distinct gate driver unit. The method uses transformer cores to magnetically couple the gates [14]. This attenuates the effect of asynchronous gate drive signals without lengthening the total commutation time. The circuit may become bulky by the introduction of transformer cores within the gate drive circuit itself. The performance is limited as new parasitic components are introduced. Parasitic capacitance between transformer windings cause common mode currents to distort the gate balancing [15, 16]. This issue is intensified due to the increased $\mathrm{d}v/\mathrm{d}t$ of SiC devices.

Active gate control methods are used to effectively control the transients of switching devices [17–21]. Common for them is that the cost and complexity of the circuitry is high, and they require high-speed and high-precision analog/digital circuitry for each stacked device [12, 22]. The faster transients of SiC increases requirements for the feedback control circuitry and timing of control signals [23]. Efforts to control the fast transients of SiC devices, may cause oscillations on the gate-source voltage which further induces unattractive ringing of the drain-source voltages [24, 25].

Lately, attention has shifted to cascaded serialization methods [26–29]. This type of serialization technique removes the requirement for both active control circuitry and all switches are turned on/off from a single external gate signal, which is passed on subsequently. One method uses a low voltage Si MOSFET to turn on a string of series-connected normally-on high voltage SiC JFETs. The method shows good balancing between components, and as all devices turn on/off simultaneously, switching speeds are reported as high as 150 kV/μs [26]. Such high switching speed can prove troublesome in circuit design, as parasitic capacitance of devices, gate

driver supplies and filter inductors must be kept extremely low [29]. Capacitance in the gate driver circuit is used to control the switching transients, but matching capacitance for voltage sharing during the turn on transient, does not necessarily ensure balancing during turn off, and vice versa [27]. In [30] a cascaded circuit structure is proposed for normally off devices. In this circuit devices do not turn on/off simultaneously. Instead they turn on/off sub-sequentially, and pass on the gate-driver signal to the next device in the string. In this way the $\mathrm{d}v/\mathrm{d}t$ is limited to the value as a single device. For this reason the cascaded switching sequence increases the total switching time, compared with methods that turn all devices on/off simultaneously. This reduces voltage overshoot issues and ringing, reported as one of the factors limiting the extension of series connection of SiC MOSFETs. The circuit works similarly for Si MOSFETs, but due to the faster switching speed of SiC MOSFET devices they are not as heavily punished for the increased total switching time caused by the cascaded turn on/off behavior. The cascaded circuit structure offers an advantageous approach to easily integrate a series-connection of SiC MOSFETs into medium voltage converter applications, as it mimics the characteristics of a single device but at a much higher voltage rating.

The cascaded circuit structure proposed in [30] offers benefits, but currently lacks guidelines to aid in the design of the circuit. Furthermore, the circuit has only been demonstrated for single switch events in a double pulse test, and no research has yet shown its applicability in a real converter application. The purpose of this paper is to further describe the design of the circuit, demonstrate its load dependence and show its performance during continuous operation in a switch mode power supply. In Section 2 its principle of operation is described and a SPICE simulation is used to aid the sizing of the RCD snubber of the circuit. A modular approach to the design of the circuit is given in Section 3. The operation of the circuit is demonstrated by a double pulse test in Section 4, where the load dependence of the circuit is shown. Furthermore, in Section 5 the voltage balancing capability of the circuit is experimentally tested by using the switch in a boost converter to operate a small-scale model of an ESP.

2 Principle of operation

The cascaded serialization circuit is shown in Fig. 1, extended for a total of four series-connected devices. In the following section, the operation of the circuit will be described in detail.

2.1 Turn-on sequence

Initially all the SiC MOSFETs are turned off. All clamping capacitors C_1, C_2, C_3 and C_4 are charged to one fourth of the total voltage across the string, because of the static voltage balancing resistors R_1, R_2, R_3 and R_4. The gate drive diode D_{G2} is reverse biased by the voltage $V_{\mathrm{G2}} + V_{\mathrm{Z2}} - V_{\mathrm{M1}}$, D_{G3} is reverse biased by $V_{\mathrm{G3}} + V_{\mathrm{Z3}} - V_{\mathrm{M2}}$ and D_{G4} is reverse biased by $V_{\mathrm{G4}} + V_{\mathrm{Z4}} - V_{\mathrm{M3}}$. A positive drive signal is given to the gate of M_1.

State 1: The drain-source voltage across M_1 starts to decrease. The stored charge in the junction capacitance of D_{G2} discharges through Z_2. Thus, already in this state the voltage of the zener Z_2 starts to gradually increase, but has not yet reached the gate-source threshold voltage of M_2.

State 2: As $V_{\mathrm{G2}} - V_{\mathrm{DG2}} - V_{\mathrm{M1}}$ becomes higher than the gate-source threshold voltage of M_2, it starts to turn on and its drain-source voltage gradually decreases. As voltage falls across M_2 the junction capacitance of D_{G3} discharges through Z_3, which gradually increases the gate-source voltage of M_3, but not yet above its threshold.

State 3: The voltage $V_{\mathrm{G3}} - V_{\mathrm{DG3}} - V_{\mathrm{M2}}$ is now higher than the gate-source threshold voltage of M_3, which now starts to turn on and its drain-source voltage drops. The junction capacitance of D_{G4} discharges through Z_4, increasing the gate-source voltage of M_4, but it has not yet crossed the threshold voltage.

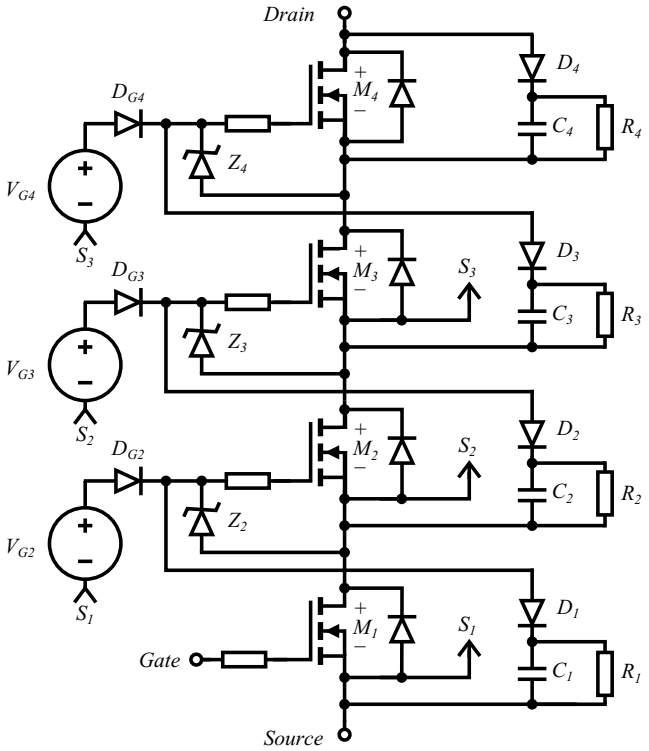

Fig. 1: Schematic of chosen cascaded serialization method requiring only a single external isolated gate driver signal.

State 4: M_4 turns on when the voltage $V_{\mathrm{G4}} - V_{\mathrm{DG4}} - V_{\mathrm{M3}}$ becomes higher than its gate-source threshold voltage. After M_4 is completely turned on the turn-on process of the whole circuit is over.

2.2 Turn-off sequence

All the SiC MOSFETs are in their on state and a current flows from the drain to the source terminal. There is still a voltage stored on capacitors C_1, C_2, C_3 and C_4, but they are slowly discharging through the parallel resistors R_1, R_2, R_3 and R_4, respectively. A negative drive signal is given to the gate of M_1.

State 5: The drain-source voltage across M_1 starts to increase. The speed of the voltage rise is limited by the current, $i(t) = C_{oss}\frac{\mathrm{d}v(t)}{\mathrm{d}t}$, which charges the output capacitance of M_1. The voltage of zener Z_1 decreases, but $V_{\mathrm{G2}} - V_{\mathrm{DG2}} - V_{\mathrm{M1}}$ is still higher than the gate-source threshold voltage of M_2.

State 6: As $V_{\mathrm{G2}} - V_{\mathrm{DG2}} - V_{\mathrm{M1}}$ drops below the gate-source threshold voltage, M_2 turns off and its drain-source voltage starts to increase. Z_2 is forward biased, and thus C_1 starts being charged through D_1. The voltage across zener Z_3 begins to decrease, but because $V_{\mathrm{G3}} - V_{\mathrm{DG3}} - V_{\mathrm{M2}}$ is still above the threshold voltage M_3 has not yet started to turn off.

State 7: The gate-source voltage of M_3 drops below its threshold, and starts to turn off. Z_3 is forward biased. The voltage across Z_4 decreases, but M_4 is still above its gate-source threshold voltage.

State 8: Voltage V_{M3} continuously rises and $V_{\mathrm{G4}} - V_{\mathrm{DG4}} - V_{\mathrm{M3}}$ becomes lower than the gate-source threshold voltage of M_4. M_4 starts to turn off. Zener Z_4 is forward biased and ensures M_4 turns off completely. At this state the gate drive diodes $D_{\mathrm{G}j}$ are all reverse biased by the voltage $V_{\mathrm{G}j} + V_{\mathrm{Z}j} - V_{\mathrm{M}(j-1)}$ for $j = 2, 3, 4$. The

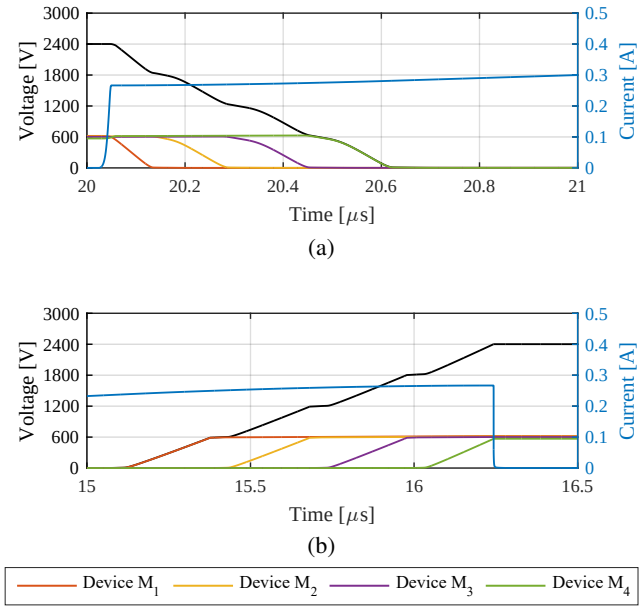

Fig. 2: Simulated drains-source voltages and current during (a) turn-on and (b) turn-off.

voltages across all MOSFETs are balanced by the resistors R_1, R_2, R_3 and R_4.

2.3 Simulation and dimensioning of circuit

The switching speeds and the circuit delays, as described in Section 2.1 and 2.2, are highly dependent on the non-linear device capacitances and internal device delays. Thus the circuit simulation software LTSpice is used to accurately predict the behavior of the circuit. The chosen SiC MOSFET device for M_1 .. M_4 is ROHM SCT2H12NZ, while both gate driver diodes D_{G1} .. D_{G4} and snubber diodes D_1 .. D_4 are 1200 V Si STTH112. The voltage supplied to the gate of the MOSFETs is equal to the supply voltage minus the forward voltage of gate driver diodes D_{G1} .. D_{G4}. Thus, it must be ensured that the forward voltage drop is not excessive to fully operate the chosen MOSFET in its on-state. In such a case the designer must either slightly increase the supply voltage or decrease the forward voltage drop of the gate driver diode by using high voltage diodes with lower forward voltage drop i.e. SiC Schottky diodes. Variations in the forward voltage drop of the chosen diodes, might also result in different turn-on speed of the MOSFET devices in the string. The turn-on/off characteristics for a double pulse test are obtained in a SPICE simulation and results are shown in Fig. 2. The cascaded behavior is clear, as each device is not turned on before the gate-signal is passed on from the subsequent device. The results also show that the device which experiences the highest power loss during the turn-on sequence will have the lowest power loss during the turn-off. This self-balancing mechanism in terms of the switching power loss is strongest when turn-on and turn-off times are equal.

Ideally the capacitor of the snubber of each MOSFET holds a constant voltage, which is equally distributed between each device in the string. However, during turn-on current starts to flow as soon as the driven MOSFET, M_1 is turned on. As the MOSFETs M_2, M_3 and M_4 are still off, the current is conducted through each of their RCD snubbers and charges the capacitors of the RCD snubber. Thus, during turn-on it is the RCD snubber of M_4 which experiences the load current for the sum of turn-on times of both M_1, M_2, M_3 and M_4, denoted t_{on}.

During turn-off the load current starts to conduct through the RCD snubber as soon as MOSFET M_1 is completely off. The load current is conducted through the snubber circuit until all of the remaining MOSFETs M_2, M_3 and M_4 are off. Thus, during the turn-off time it is the snubber of MOSFET M_1 which experiences the current for the longest time, which is the sum of the turn-off time of M_2, M_3 and M_4, denoted t_{off}.

It must be ensured that with non-equal turn-on and turn-off times, that the circuit is designed to withstand the maximum of the two time intervals.

$$t_{max} = max\left\{t_{on}, t_{off}\right\} \tag{1}$$

To size the capacitor, C of the RCD snubber, it is ensured that during t_{max} none of the snubber capacitors will experience a voltage increase of more than a predetermined value denoted Δv_c.

$$C \geq i_L \frac{t_{max}}{\Delta v_c} \tag{2}$$

where i_L is the load current conducted through the switch-leg. The energy added to the capacitor during every switching cycle, must be dissipated in the snubber resistance, R which is connected in parallel. Thus the size of the snubber resistance must allow the average added power, P, to be dissipated, to ensure equal voltage sharing during steady state.

$$R = \frac{V_{ds}^2}{P} = \frac{V_{ds}^2}{\frac{1}{2} \cdot C \cdot ((V_{ds} + \Delta v_c)^2 - V_{ds}^2) \cdot f_{sw}} \tag{3}$$

where V_{ds} is the static drain-source voltage to be maintained across each device, and f_{sw} is the expected switching frequency of the converter of which the switch is to be operated in.

Equations (1)-(3) are based on knowing the switching time of the circuit, obtained through the SPICE simulation switching waveforms. Thus, for the initial run a snubber capacitance and resistance can be chosen based on the approximate switching times given in the datasheet and the guidelines mentioned above. Once the switching speed of the devices is better approximated from the simulated switching waveforms, the size of the RC elements are then determined.

For this paper a voltage increase, Δv_c, of 25 V is deemed acceptable. For the simulation in Fig. 2, the t_{on} is 580 ns and t_{off} is 880 ns. For the case where the load current, i_L, is 200 mA. From (2) the capacitance of the RCD snubbers is determined to be C = 7.3 nF. For this paper, the converter uses a switching frequency, f_{sw} of 10 kHz. Thus the parallel resistance, R, is determined from (3) to be 336 kΩ. The capacitance of the RCD snubber is achieved by three 22 nF C1808V223KDRACTU SMD capacitors from Kemet in series. For the resistors three high voltage 0.5 W 2010 SMD resistors from Bourns CHV-series are used, combined for a total resistance of 330 kΩ. The performance of the static voltage balance is determined by the variation in the resistance of the RCD-snubber. The Bourns CHV-series have a low tolerance of 5 % to ensure a good static voltage balance between devices in the string.

3 Modular cell-based approach

The following section describes the modular cell-based approach which has been used to design the serialized string of switches. The purpose of a modular design is to divide a system into smaller subsystems. Each unit can be developed and manufactured independently, but the overall functionality of the system is maintained. The serialization technique used in this paper has a structure which can be split into different parts that each fulfil a certain feature of the circuit. Modularity enables faster prototyping as each sub-system can be designed and developed one at a time and tested independently. In case of a fault, only single sub-units need to be replaced instead of redoing the entire system.

The string of series connected switches can be divided into two kinds of sub-systems. The switch which is driven by a gate driving signal is one sub-system, while each remaining switch in the string is another (further on labelled as a non-driven, because they are not given an external drive signal). A concept diagram of the connections required between each module is shown in Fig. 3.

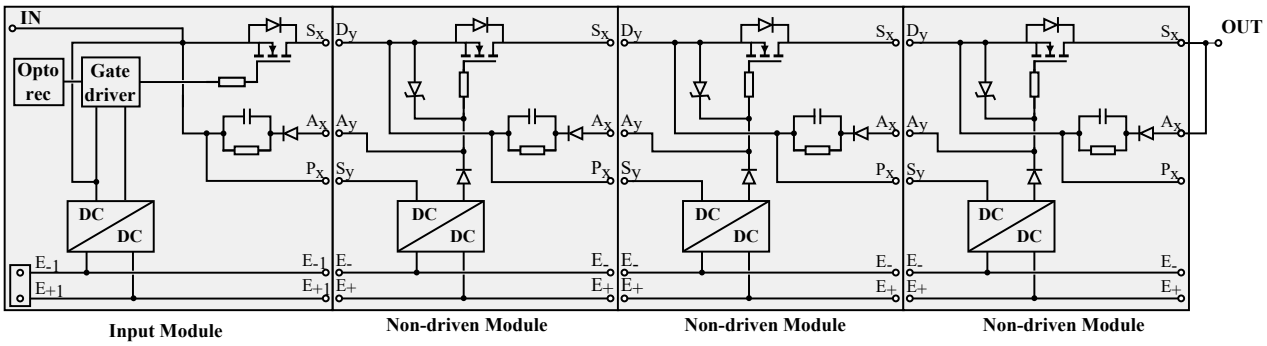

Fig. 3: Concept drawing of the proposed modular PCB layout structure

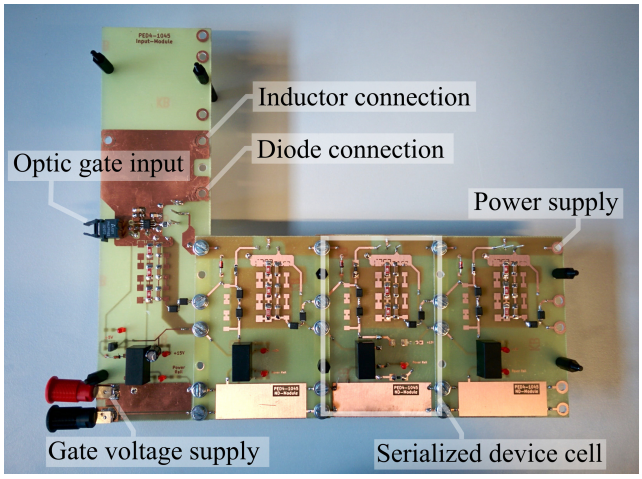

Fig. 4: Photograph of a designed switch with 4 serialized devices.

During development the string of devices is extended one at a time. Thus initially the input module is tested on its own, and then more non-driven modules can be added. The non-driven modules are connected by bolts at the indicated terminal points in Fig. 3.

The gate voltages are supplied using commercially available DC/DC converters. Each voltage supply output is referred to different points, meaning that the supply must be electrically isolated. The fast switching of relatively high voltage levels requires that the solutions have both a high voltage blocking capability and a low parasitic capacitance. The commercially available isolated DC/DC converters are in a form factor that allows them to be directly soldered on the PCB. For this paper the DC/DC supply R12P215S/P1 by RECOM has been chosen, which has a parasitic capacitance rated from 1.5 pF to maximum 10 pF and is tested for an isolation voltage of 6.4 kV. Increasing the isolation voltage and maintaining a low parasitic capacitance involves using a custom built solution [31–34], which has been disregarded for the tests in this paper. The switch is constructed using the modular cell-based approach as shown in Fig. 4, with a total of four serialized devices.

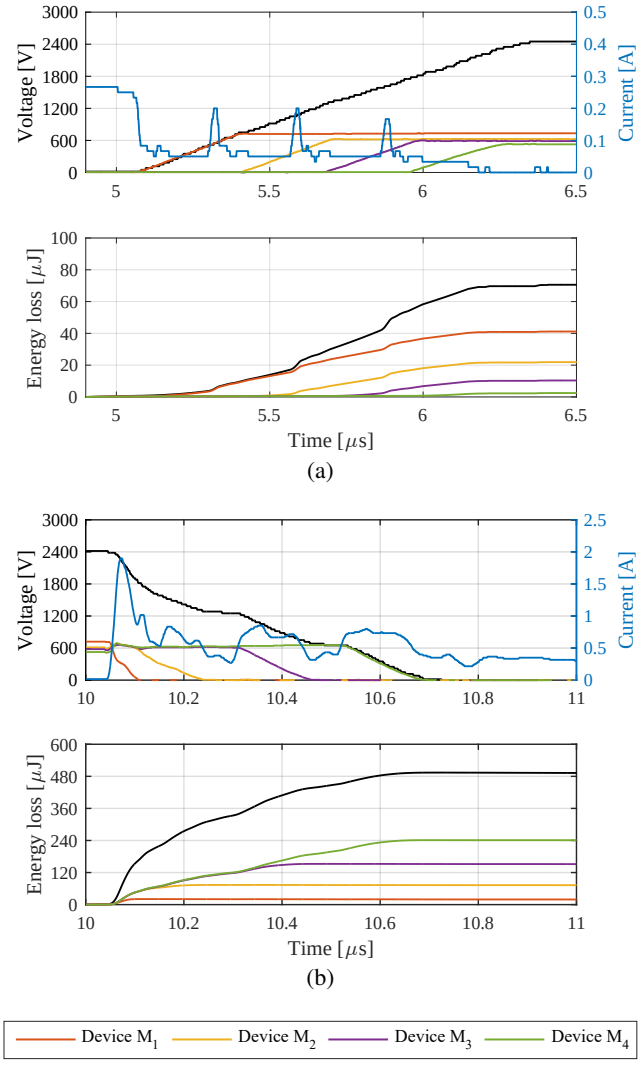

Fig. 5: Measured drain-source voltages, drain current and energy loss during (a) turn off and (b) turn on.

4 Double pulse test results

A double pulse test is used to evaluate the voltage balancing capabilities of the circuit. Indicated in Fig. 4 is the connection points that the switching circuit has with the inductor, diode and the ground of the DC power supply used for the double pulse test setup. The double pulse test is done at a negative DC-link voltage level of 2400 V, to emulate the voltage condition in the ESP application. The drain-source voltage of each MOSFET in the string is measured using a Teledyne LeCroy ADP305 differential probe, and the inductor current is measured using a LeCroy CP030 probe. The current through the inductor is ramped up to 250 mA. The drain-source voltage, drain current and energy loss during turn-off and turn-on is shown in Fig. 5.

The cascaded turn on/off is evident from the switching waveforms. The voltage balancing of the circuit is demonstrated to be good. The timing and duration of the turn on and turn off are similar to what was predicted by the simulation. During the turn-on transient it is noted that some additional delay between turn-on of each MOSFET is present. This causes the experimental turn-on to be an additional 100 ns compared with the simulation of Fig. 2. The delay is dependent on the reverse recovery time of diodes, zener diodes and

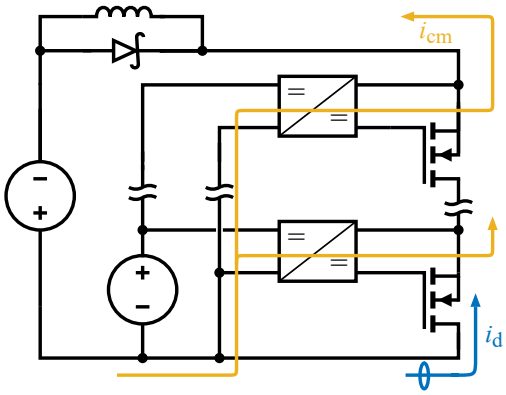

Fig. 6: Common mode current path, i_{cm}, disturbing the measured drain current, i_d during the performed double pulse test.

how they interchange charge with the gate drive diodes [30]. Despite importing the device models this is not accurately modelled by the SPICE models used for the devices in the simulation.

From Fig. 5 it is observed that the measured drain current drops as devices turn off, but increases during turn on transients. The increase/decrease in current happens during the fall and rise times of the switch voltage, and thus is dependent on the $\mathrm{d}v/\mathrm{d}t$. This is caused by a common mode current path through the parasitic capacitance of the isolated gate driver supplies [31], as depicted in Fig. 6. The current in the inductor is constant, but the distribution of current through the MOSFETs and common mode current in the gate drive shifts depending on the $\mathrm{d}v/\mathrm{d}t$. Despite the efforts of choosing gate driver supplies with low parasitic capacitance, the effect of the common mode current is still noticeable. This showcases the importance in maintaining a controlled $\mathrm{d}v/\mathrm{d}t$ and keeping a design of low capacitive coupling.

4.1 Load dependence

In the following section the influence of load current is investigated. The current is ramped up to 250 mA, 500 mA and 800 mA. The total voltage across all switches is shown during turn-off and turn-on in Fig. 7. The results show that the turn-off switching speed is dependent on the load current, as described in Section 2.2. This is caused by charging the output capacitance of each device. When observing Fig. 7 for the turn-on transient it is seen that the first drive switch is independent from the load current. However, the delays between switching transients of each MOSFET is increasing with increasing load current. The time increased from 250 mA to 500 mA is 180 ns, and further 80 ns from 500 mA to 800 mA. Owing to finite $\mathrm{d}i/\mathrm{d}t$ of the diodes and zener diode when they are turned off, the increasing current cause longer delay. The voltage slope during turn on of each individual MOSFET is not significantly affected.

5 Boost converter operation

In the following section, the serialization technique is tested experimentally by utilizing it as a switch in a boost converter. Initially, the single switch of four devices is used in a boost converter, as shown in Fig. 8, where the diode is constructed from a series connection of two CREE C3D10170 diodes. The RC load of the converter mimics a small scale ESP, and uses an output resistance, R_o, and capacitance, C_o, of 19.8 nF and 188 kΩ, respectively.

The switch is operated at a switching frequency of 10 kHz, and the input voltage to the converter is 600 V supplied from a Magna XR2000-1.00/380NEG+LXi power supply. The drain-source voltage of each MOSFET in the string is measured using a Teledyne LeCroy ADP305 differential probe, and the inductor current is measured using a LeCroy CP030 probe. The result of the experiment is shown in Fig. 9.

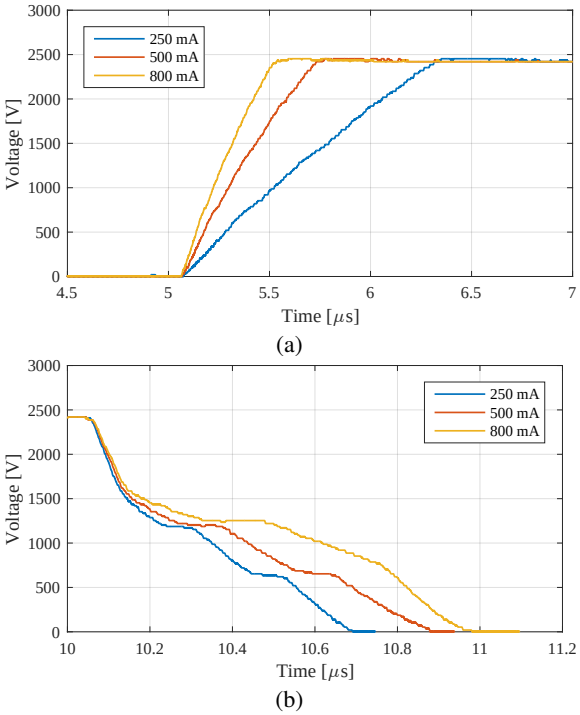

Fig. 7: Drain-source voltage across all devices during (a) turn off and (b) turn on for different load current levels.

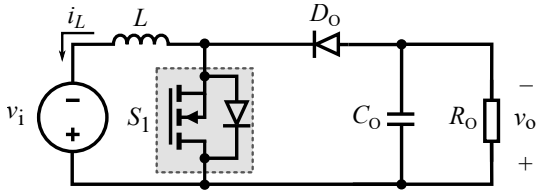

Fig. 8: Schematic of the tested boost converter configuration.

The voltage balancing between devices is not working as intended. As current in the inductor reaches zero, the voltage across the string of devices starts to drop and begins to oscillate. The origin of this ringing is common for boost converters operating in discontinuous conduction mode as described in [35–37], but it has a major impact on the voltage balancing performance of the implemented cascaded serialization technique. The ringing is described using the voltage across the switch during the different states of the boost converter, as shown in Fig. 10. In state B of the circuit, the diode D_o is conducting and the voltage across the switch is clamped at the output voltage v_o. As current reaches zero the diode stops conducting, and the circuit enters state C. The DC-link has a large capacitance and is maintained at v_i. The capacitance of the switch initially maintains a voltage of v_o, which is not in equilibrium with the input voltage v_i and they start to interchange charge through the inductance, L. This causes an oscillatory current to flow.

The result of this oscillatory behaviour, is that effective balancing between serialized devices in the switch does not occur. During turn-on and turn-off transients the current conducted through snubber capacitors result in an unequal charging. Thus ideally during state B, the output voltage v_o is across the switch, conducting current through the snubber capacitors and their parallel resistors to ensure balancing. But when voltage across the switch drops to v_i in state C, the diode in the snubber circuit becomes reverse biased and there is limited balancing.

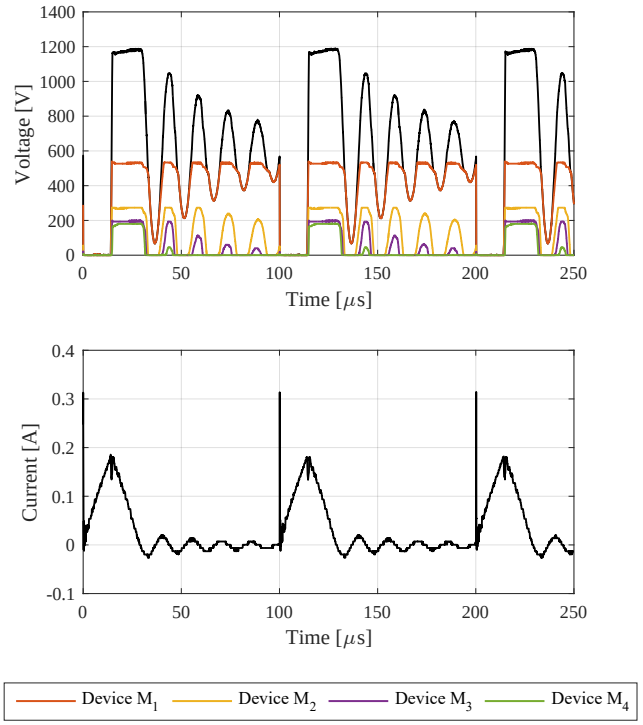

Fig. 9: Drain-source voltages and inductor current during discontinuous conduction mode of the boost converter.

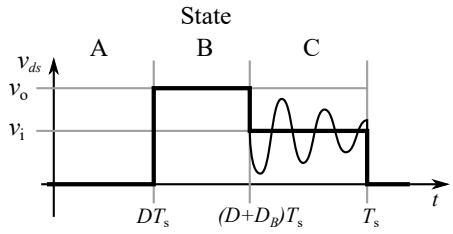

Fig. 10: Switch voltage during circuit states of a boost converter operating in discontinuous conduction mode.

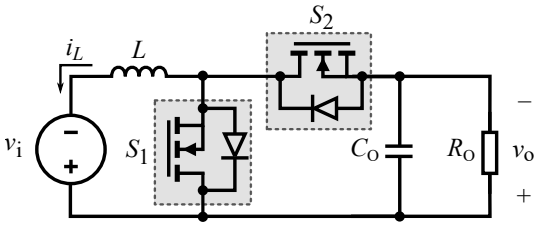

Fig. 11: Schematic of the tested synchronous boost converter configuration.

5.1 Synchronous boost operation mode

The converter is changed to a synchronous boost converter configuration, as shown in Fig. 11, as the diode is replaced with another switch, S_2, which is constructed by another string of four devices. The physical converter is depicted in Fig. 12. The converter is constructed in the same modular concept, where each SiC MOSFET and its associated snubber components are implemented on separate boards. Except from the boards containing the input and output connections, each non-driven board is identical in structure.

The synchronous boost topology, eliminates state C shown in Fig. 10, because the converter can be operated in continuous conduction mode no matter the duty cycle or load. The switching frequency

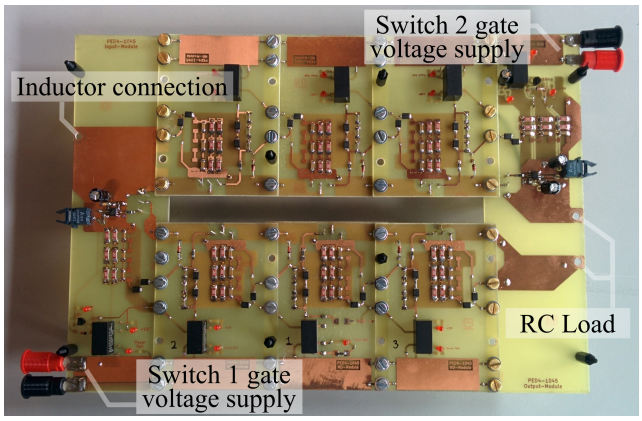

Fig. 12: Photograph of the designed synchronous boost switch circuit.

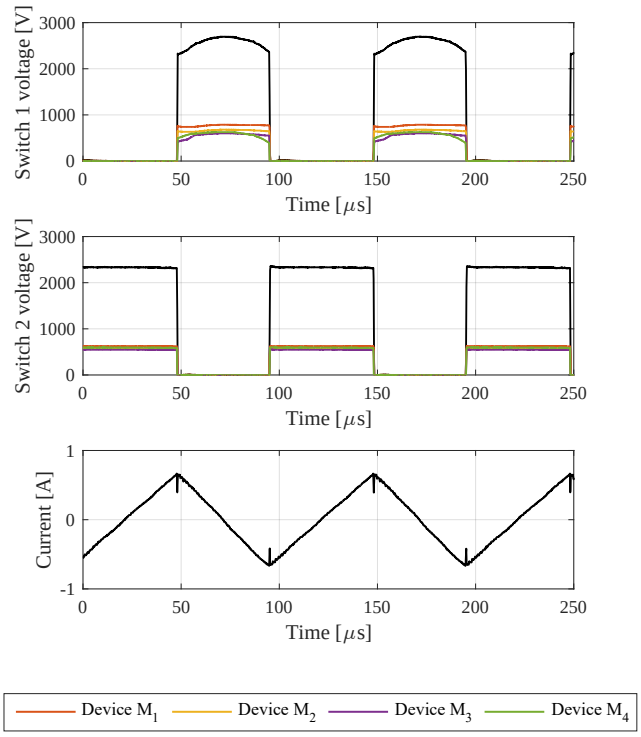

Fig. 13: Drain-source voltages and inductor current during continuous conduction mode of a synchronous boost converter.

is kept at 10 kHz, but due to better voltage balancing across the devices, the input voltage is increased to 1200 V and a duty cycle of 50 % is used. The obtained drain-source voltage across each device and the measured inductor current is shown in Fig. 13.

It is observed that voltage balancing between devices is significantly improved. During the off-state of switch 1 its voltage is clamped at the output voltage v_o. However, during this state the inductor current is conducted to the output capacitance, C_o, which increases the output voltage. The voltage starts and ends at approximately 2380 V, but peaks at 2693 V in the middle of the S_1 off-state period. Owing to this, the voltage balancing is not as effective for switch 1 as it is for switch 2. For switch 2, during its off state the voltage is similarly clamped at the output voltage v_o, but this voltage is kept constant by the output capacitor that is only slowly discharged through the relatively large output resistance R_o. From the experimental results it is concluded that good voltage balancing can be achieved by using the cascaded series-connection structure. By comparison of the results of the boost converter operating in

discontinuous and continuous conduction mode, it is found that a constant off-state voltage is important to achieve good balancing between devices in the string.

6 Conclusion

In this paper the operation of a cascaded series-connection has been analyzed, and design guidelines of the circuit have been proposed. The switching performance of individual devices in the string is investigated in a double pulse test, which clearly shows a staircase-shape of the voltage waveforms. It is demonstrated that the full string operates with similar $\mathrm{d}v/\mathrm{d}t$ as each single device. Good voltage balancing between devices is achieved during the switching transient. The transition period of turn on/off was demonstrated in the double pulse test, which is tested for load current levels of 250 mA, 500 mA and 800 mA. It is concluded that turn-off speed is highly dependent on the load current, while turn-on is only affected by a slightly added delay between each device conducting in the string. The serialization technique is tested during 10 kHz operation. At first a single switch of four series connected devices is tested in a boost converter topology operating in discontinuous operation mode. When the inductor current reaches zero the circuit enters an oscillating state, which results in poor voltage balancing across the string of devices. The circuit is expanded to include two sets of serialized switches in a synchronous boost converter, enabling operation in continuous conduction mode and bidirectional power transfer. The continuous conduction mode eliminates the oscillating state, and results in good voltage balancing behaviour. The relatively low output capacitance, due to the modelling of a small scale electrostatic precipitator results in a voltage ripple of approximately 300 V on the output voltage, which is reflected on the voltage balancing between devices in one of the switches. Despite this voltage ripple, the voltage balancing of individual devices is good compared with other techniques and implementations found in literature. It works well for the medium voltage, low current conditions found in the application of electrostatic precipitators. The paper demonstrates that the cascaded serialization technique has advantages for new high voltage and fast switching SiC devices.

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