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Performance analysis of commercial MOSFET packages in Class E converter operating at 2.56 MHz

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Abstract

Wide bandgap (WBG) power electronic devices realized using silicon carbide (SiC) and gallium nitride (GaN) are increasingly replacing their silicon (Si) counterparts in power electronics applications. The obvious advantages of these devices with their higher switching speeds, lower on state resistance and high temperature operation over Si devices have aided in the paradigm shift towards wide bandgap devices. The low gate charge requirements of SiC MOSFETs enables use of these devices in radio frequency (RF) converters using resonant topologies operating at MHz frequency range. The RF converters employed in various industrial applications are currently realized with vacuum tubes. Replacing vacuum tubes with solid state devices provides greater reliability. This requires power switches transferring high power at high switching speeds. Wide bandgap devices operating at these specifications are not commercially available and power modules have to be custom designed for these applications. This work demonstrates performance of various commercial MOSFET packages at frequency of 2.56 MHz. Commercial SiC MOSFETs in TO-247 and D2Pak packs are tested in Class E resonant converter operating at 2.56 MHz and compared with DE-275 Radio Frequency (RF) package performance under same operating conditions. Design considerations deduced from results can then be used in design of custom low voltage SiC RF modules and eventually can be used in the design of high voltage modules.

Introduction

Resonant converters operating in the RF frequency range (> 1MHz) are used in various industries for processes employing induction and dielectric heating. These heating methods are employed mainly in semiconductor industries in float zone process for generating ultra-pure silicon wafers [1], in wood industries for drying of wood and in food processing industries [2]. The induction heating employs the principle of electromagnetic induction where the element to be heated is passed through coils supplied by an alternating supply. The varying electromagnetic field generated by these coils will induce an alternating current in the element, the eddy currents, resulting in heat generation through resistive heating [3]. Dielectric heating uses the principle of oscillating bipoles in a dielectric material by applying an alternating field across the dielectric material to generate heat through friction of the oscillating elements [4]. The RF converters are needed for these applications ensuring the process heat generation [3][4]. The industries, as mentioned above, which are dependent on the RF converters are currently using vacuum tube in their converters which have efficiencies in the range of 50-60%. These converters are susceptible to many catastrophic and degenerative failures. RF converters realised with solid state devices are smaller, cheaper, reliable and more efficient (> 85%) [5]-[9]. The solid state converters currently used at high frequencies but at low voltage levels are more reliable than their vacuum counterparts by a factor as much as 2.5 [7]. Therefore, the transition to the solid state counterparts provides the obvious economic advantages to these industries. The conventional Si based power electronics devices are not capable of operating at such high switching frequencies (> 1 MHz) and transfer the high power level needed for these application and as such these industries continue to rely on the vacuum tube based converters [10].

The WBG devices using SiC and GaN have resulted in devices with superior operating capabilities than their Si counterparts [11]. These WBG devices have low gate charge requirements, lower intrinsic carrier concentration, higher electric breakdown field, higher thermal conductivity and large saturated electron drift velocity. The low gate charge requirement enables higher switching speeds while the higher electric breakdown field enables reduction in drift layer thickness bringing a significant reduction in on state resistance. They are also capable of operating at higher junction temperatures resulting in reduced cooling requirements [11][12]. The above advantages enable them to be used in high switching frequency, high power applications for the industries mentioned above using high power density power electronics converters [13].

The WBG devices despite their obvious advantages has had significant difficulties in penetrating the market. The major factor in the early days was the difficulty in developing high quality SiC wafers on insulator substrates as highlighted in [11]-[15]. The recent advances in the manufacturing process have helped overcome these issues but still the large scale penetration of the WBG devices in the market needs overcoming the challenges in term of cost, reliability as highlighted in [16]. However, with the advancement in technology in the manufacturing process the SiC MOSFET with prices comparable to that of their Si counterpart are available in market. The maximum available voltage rating with SiC MOSFET commercially is from Wolfspeed and Rohm with voltage rating at 1700 V. The Wolfspeed MOSFETs are available in D2Pak with current rating of 5.4 A and in TO-247 pack with a current rating of 72 A.

RF application needs MOSFET that can switch at high speeds which comes down to low gate charge requirements which will be met by the new SiC devices mentioned above. The packaging of the MOSFET is another integral feature which enables the operation of MOSFETs at high frequencies. MOSFET packaging with large stray inductance can lead to poor performances at high frequencies. IXYS has its RF MOSFETs using their patented DE-275 pack with different ratings capable of operating up to 45 MHz using Si MOSFETs. These MOSFETs though are available at voltages only up to 1 kV. The industrial application requires converters capable of delivering power more than 100 kW. This requires the need for high voltage high current MOSFETs capable of operating at high frequencies. Wolfspeed claims the third generation MOSFETs from them in the range of 900V - 15 kV. These are pre-release SiC devices available only in its die form. The proper packaging of these MOSFETs have to be done in ensuring their operation at RF range and this calls for the need of developing custom RF packages for these applications. A 1.2 kV custom package SiC MOSFET employed in a 3.38 MHz resonant converter is presented in [17]. The objective of this paper is to draw conclusions on optimal packaging requirements for custom made SiC MOSFETs. The aim is to test different commercial SiC MOSFETs of different packaging, which are not designed for RF applications, in converter operating at 2.56 MHz. Their performances are studied and conclusions drawn will be used as design considerations for packaging custom SiC MOSFET modules which can be used in RF environment.

The rest of the paper is arranged as follows. The next section will describe the basic operating principle and the design of the class E converter. The third section will describe the methodology used in the testing of the different MOSFET packs. The results will be presented and discussed in the fourth section. Finally, the paper will be concluded in the last section.

Class E resonant converter

The resonant converters are some of the most widely used topologies for high frequency switching applications. This is mainly because of the soft switching capabilities of these converters namely zero voltage switching (ZVS) or zero current switching (ZCS). The soft switching methods in comparison to the hard switching techniques employed in standard converters reduces the switching losses. The switching loss becomes significant at high frequency since hard switching leads to proportional increase in switching losses leading to lower efficiencies and higher cooling requirements for the converters [18].

The class E resonant converter is the simplest of the resonant topologies employing a single switch in MOSFET. The apparent easiness of developing a class E converter and the single switch power module was the reason behind choosing this topology for the testing purpose. The Fig. 1 shows a class E schematic with the values of the tank elements used in this converter. The L_f represents a choke inductance and the value of it is high enough to ensure that the ripple in the current drawn from the DC supply is minimal. The L-C-R_i represents the tanks components. C_1 includes the MOSFET output capacitance and additional external capacitance which will be added. This ensures that the MOSFET output capacitance is included the design considerations. When the MOSFET turns on it bypasses the capacitance C_1 resulting in a resonant network formed by L, C, R_i with a resonant frequency of f_{01}. When the MOSFET turns off the resonant network is formed by series network of L, C, R_i and C_1 with resonant frequency of f_{02}. The class E switching frequency f_s is between f_{01} and f_{02}. Detailed description on the working of class E converter is presented in [18] and is not discussed here as it is beyond the scope of this paper. The class E converter is designed for a DC link voltage of 200 V. This because as highlighted in [19] the voltage across the switch will come around 3.5-times DC link voltage in class E converter. The converter is designed for a power transfer capability of 1 kW. The design equations of the converter is followed as highlighted in [8].

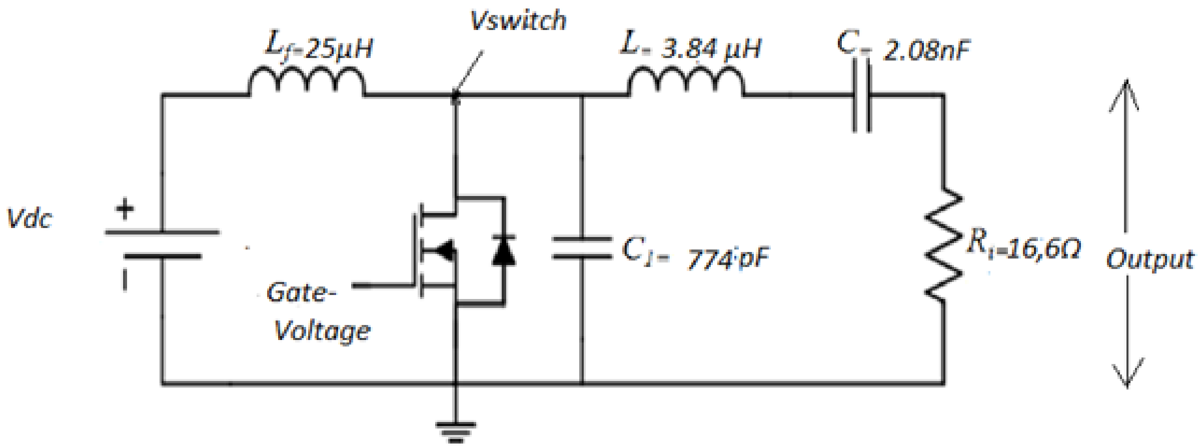


Fig. 1: Class E resonant converter.

Methodology

In this work the resonant class E converter, described above, is realized with three different MOSFETs namely, the DE275X2-102n06A silicon MOSFET from IXYS rated at 1 kV, C2M0040120D SiC MOSFET from CREE rated at 1.2 kV with TO-247 pack and C3M0065090J SiC MOSFET from CREE rated at 900 V with D2Pak. In these the IXYS MOSFET is an RF MOSFET capable of working up to 45 MHz. The MOSFETs are shown in Fig. 2. These CREE SiC MOSFETs have been chosen since their gate and drain capacitances are comparable or lesser than the RF MOSFET from IXYS. The low output capacitance value of the SiC MOSFET make them ideal for RF operation but the layout of their package and the stray lead inductances may not be optimized for the RF operation.

These MOSFETs are tested by operating them in the class E converter. The MOSFETs in the converters are subjected to a drain voltage of a maximum around 500 V to ensure that there is sufficient margin from the rated values for these MOSFETs and thereby preventing over stressing of these devices. The drain waveforms at 2.56 MHz for the different MOSFETs are observed. The drain waveforms can provide significant insight into the effect of parasitics in the operation of MOSFET at 2.56 MHz. The effects of the parasitic elements are expected to be more significant in the SiC MOSFETs as their packaging is not suited for RF operation. The drain waveforms of the SiC MOSFETs are then compared with IXYS MOSFET as it is expected to show the best operation with its RF layout in package. The deductions from the comparisons are expected to give insight into the modifications in the layout of the existing package for the SiC MOSFETs to make them operate efficiently at RF frequencies. The driving of these devices are done using a quasi-resonant gate driver which is not presented here as it is beyond the scope of the topic.

Fig. 2: IXYS RF MOSFET, CREE MOSFET TO-247 and D2Pak

Results and discussion

V_{DSS} = 1000 V
I_{D25} = 8 A
$R_{DS(on)}$=1.6 Ohm

C_{iss} = 1800 pF at 600 V
C_{oss} = 120 pF at 600 V
C_{rss} = 22 pF at 600 V

Fig. 3: IXYS RF MOSFET with its specifications.

The results of the testing of the MOSFETs will be presented here. First the results of the IXYS MOSFET with RF packaging will be presented. The Fig. 3 shows the RF package with its parameters. The parameter shown are the V_{DSS} the maximum drain source voltage, I_{D25} the maximum current rating for a case temperature of 25 deg, $R_{ds(on)}$ the on state channel resistance and C_{iss}, C_{oss}, C_{rss} are the input, output and gate drain capacitance respectively. The RF pack comes with symmetrical layout for the MOSFET both at the control (gate) and power side along with Kelvin connected source for the gate side which helps in decoupling the gate current from the source. The Fig. 4 shows the gate and drain voltage for the class E converter using the IXYS RF MOSFET. The converter was tested for a DC link voltage of 150 V and a power input of 531 W and output of 464 W. The output power was obtained by using RMS value of the current going into the load resistor of 16.6 ohms using the current probe CP030 from Teledyne Lecroy. The electrical efficiency calculated was 87 percent. The electrical efficiency is less since the power board is not optimized in terms of layout and main focus here is to study how the switching waveforms are affected due to the MOSFET package. As can be seen from Fig. 4 the distortion in the gate voltage is minimal with the RF MOSFET under loaded condition. This indicates the effectiveness of the RF package. The lead inductance for the RF package is 1 nH in the drain side as suggested by the model provided by IXYS. The low lead inductance coupled with the significantly low output capacitance of the MOSFET allows the MOSFET to be operated at the RF frequency of 2.56 MHz without any distortion in the voltage waveforms.

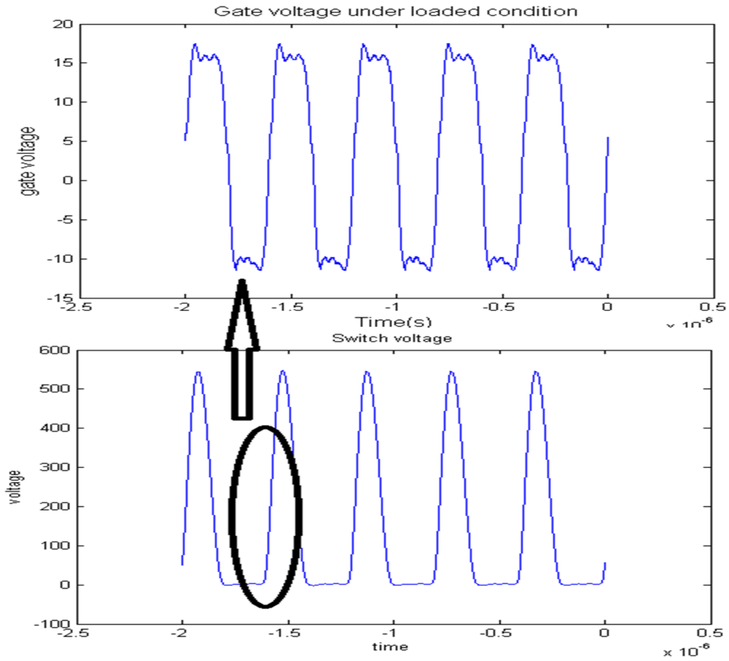
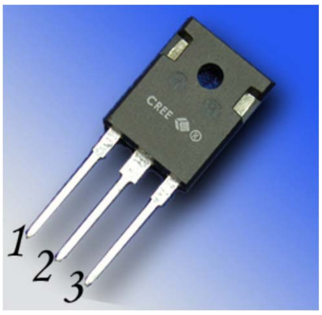


Fig. 4: Gate voltage and drain voltage across the IXYS RF MOSFET under loaded condition.



V_{DSS} = 1200 V I_{D25} = 60 A $R_{DS(on)}$ =40 mOhm	C_{iss} = 1900 pF at 1000 V C_{oss} = 150 pF at 1000 V C_{rss} = 10 pF at 1000 V

Fig. 5:TO-247 package MOSFET from CREE and the parameters.

The Fig. 5 shows the CREE TO-247 pack MOSFET, C2M0040120D, used as the second device for testing. The similar conditions as with the RF MOSFET have been imposed on this MOSFET also. The Fig. 6 a and b shows the results with the TO-247 pack of the CREE MOSFET. The gate voltage under unloaded condition without any DC link voltage being applied to the MOSFET is shown in Fig. 6a. The Fig. 6b shows the same gate voltage under loaded conditions. It can be noted that in comparison with the RF pack there is significant distortion in the gate voltage of the TO-247 pack MOSFET. The through hole layout of the TO-247 pack with the high lead inductance of 11nH and 6 nH at the source and drain terminals, provided in MOSFET model, usually makes this pack unsuited for high frequency applications. The MOSFET when tested in the class E converter, as the drain voltage started getting higher it can be noticed from the Fig. 6b that the gate voltage started getting distorted but it should be noted that the drain voltage is still smooth without ringing. The distortion in the gate voltage is more prominent at the turn off instant of the MOSFET. It can be noticed that at the turn off of the MOSFET the gate voltage resembles a quasi-sine wave similar to that of the drain voltage with superimposed ringing. At the DC link voltage of 112V and 3.24A the distortion in the gate voltage results in positive values at MOSFET off state even though it can be noted from the gate voltage in the unloaded condition, Fig. 6a, that the gate off state voltage is at -5 V. The main difference in the TO-247 pack compared to the RF pack is the lack of symmetry in packaging, the absence of Kelvin connected source and the high lead inductance. The Kelvin connection is very important as it enables in decoupling of drain source current from the gate source side. In the absence of the Kelvin connection the ringing which can arise at the drain side due to the current cut off will appear in the gate source voltage. The lack of symmetry in the layout is another important factor as it can lead to higher stray inductance. The placement of the forward and return path of the currents close to each other helps in reducing the stray inductances. This is achieved in the RF MOSFET by placing the gate, Kelvin connected source terminals near to one another in control side and the drain, the source terminals near to one another in the power side. The emphasis of the Kelvin connection can be seen in the testing of D2Pak

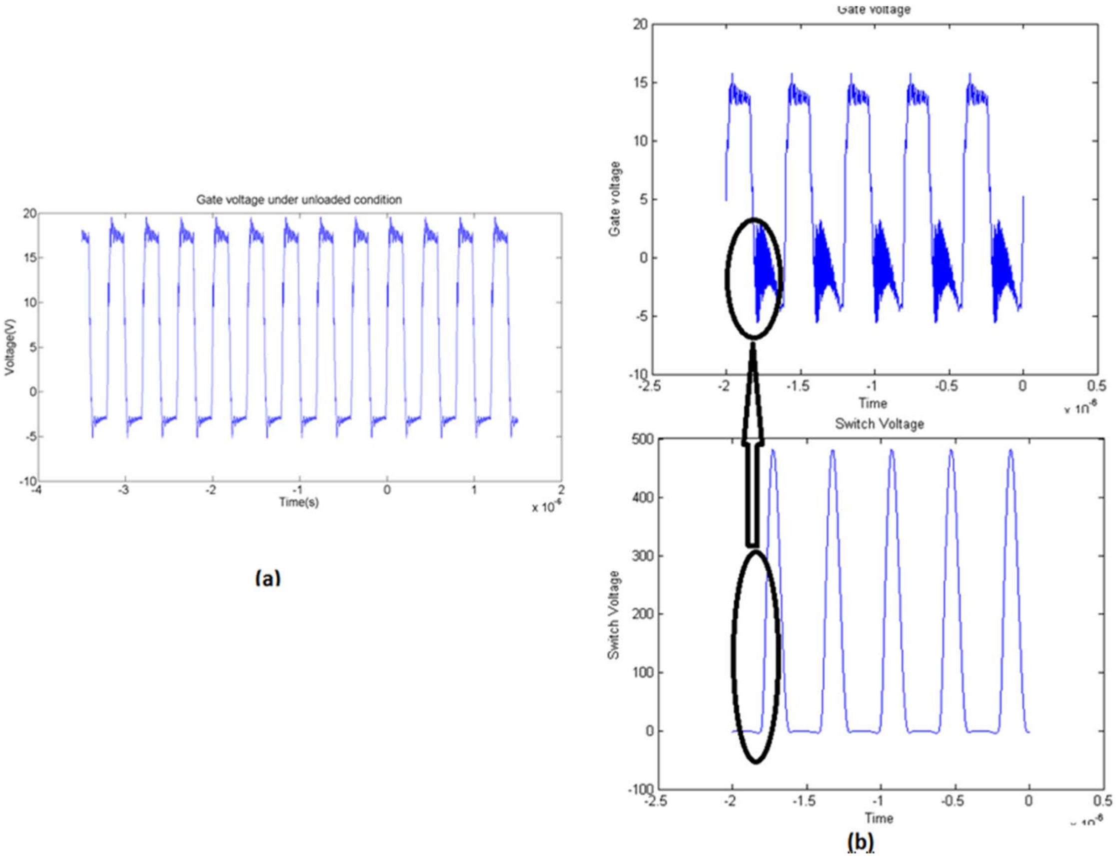


Fig. 6 (a): Gate voltage with drain voltage zero and (b): gate voltage distortion with drain voltage for TO-247 pack

V_{DSS} = 900 V I_{D25} = 35 A $R_{DS(on)}$ =65 mOhm	C_{iss} = 660 pF at 600 V C_{oss} = 60 pF at 600 V C_{rss} = 4 pF at 600 V

Fig. 7: D2Pak package MOSFET from CREE and the parameters.

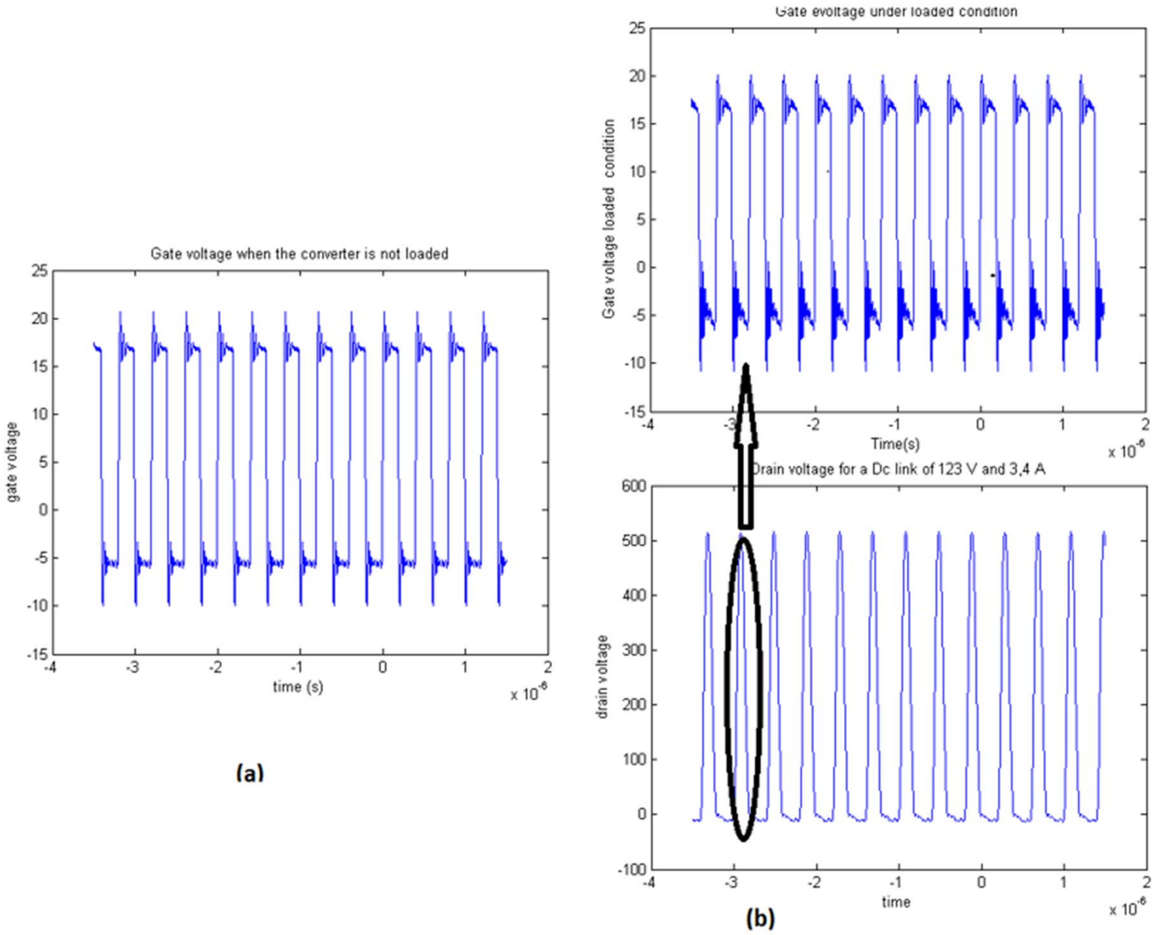


Fig. 8 (a): Gate voltage with drain voltage zero and (b): gate voltage distortion with drain voltage for D2Pak

The Fig. 7 shows the CREE D2Pak MOSFET, C3M0065090J, along with its parameters. The testing of the MOSFET is done in the same way as for the RF and the TO-247 pack MOSFETs discussed above. The D2Pak as can be noted from Fig. 7 has one drain tab and 7 terminals of which one is gate, one is Kelvin connected source for gate side and the remaining drain side sources. The results shown here are for a DC link of 123 V and 3.4 A resulting in an input power of 418 W and output of 371 W with an electrical efficiency of 89 percent. The Fig .8a shows the gate voltage applied to the MOSFET without any DC link voltage applied. The Fig. 5b shows the gate voltage under the loaded condition of the MOSFET. Unlike the case of the TO-247 pack the distortion is not very high. This shows the emphasis of the Kelvin connection which helps in decoupling the gate and drain side current thereby preventing the distortion in the gate voltage. The lead inductance of the pack compared to the TO-247 pack is low as suggested by the MOSFET model provided by CREE. The inductance is still higher than that of the RF pack from IXYS and in comparison to the waveforms from the RF MOSFET the distortion of the gate voltage is higher in the D2Pak. It should be noted the D2Pak layout is not symmetrical as the RF pack. As mentioned symmetry is an important criterion in the development of RF MOSFET packs as it enables field cancelling by placement of forward and return path of currents close to each other. It can also be noticed from the gate waveforms that the distortion is also contributed by the Miller effect which becomes prominent at this frequency. The Miller effect can be reduced by providing a low impedance path for the Miller feedback current thereby preventing voltage distortions. The Miller clamp or an integrated driver placed close to the MOSFET bare die can help achieve this.

Conclusion

The comparison of the MOSFET packaging has pointed to the obvious fact that the RF package provides the best performance and this was expected. The purpose of doing the test was to verify how much impact packaging will have on the operation of the MOSFET at RF frequencies even if MOSFETs have very low stray capacitances at the gate and drain as is evident from the SiC MOSFETs. It can be concluded that the packaging of the MOSFET plays as important a role as the MOSFET parameters. It was also interesting to see how much modifications have to be made on the existing packs to make it work at RF frequencies. The TO-247 pack is very reliable in high power application mainly due its reduced mechanical stress on the die during mounting and improved heat dissipation properties as highlighted in the application note SNOA460 from Texas instruments. Infineon has developed TO-247 pack with Kelvin connection which might overcome the issue of the gate voltage distortion but the lack of symmetry which reduces the stray inductance and the ringing needs to be addressed. The D2Pak though has the Kelvin connected source for the gate side cannot be considered as a good option for high power application mainly due the issues in integrating an effective heat dissipation system due to the surface mounted nature of the packing. The RF pack design is therefore the best solution but the mounting of the MOSFET can lead to significant stress on the die due to solder of pad which will be connected to the die and the surface mounted nature. The integration of the gate driver into the MOSFET packing is also a good solution. The resonant gate driver used in this case gave good performance but by integration of the driver within the pack will help reduce the Miller effect substantially.

Therefore, it can be concluded that the RF package with the symmetric layout will provide best performance in the RF range. To ensure efficient operation at high voltage the RF package has to be modified to withstand the high voltage keeping the symmetrical layout intact. It should also be considered to improve the mounting by avoiding surface mounted structure with solder pads as it can lead to increased stress on die and also to include an integrated drive into package to reduce stray effects. As future work it will be interesting to develop a custom RF module for low voltage level (1 kV) taking into account the above considerations, test it under similar conditions and then develop a high voltage module (10 kV) .

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