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FS-MPC Algorithm for Optimized Operation of a Hybrid Active Neutral Point Clamped Converter

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***Abstract*—The design for reliability has gained a lot of attention in power electronic community in the past few years. The aim is to optimize the design in order to achieve desired reliability goals with minimum margins. However, in most applications, there are stressing conditions, which result in high stress and therefore require higher margins. As an opportunity, adapting the control of the power electronic converters to equally redistribute the stress of the devices can reduce the stressing conditions and also reduce the design margins. This is of great importance for multilevel topologies and in particular the Active Neutral Point Clamped (ANPC) topology. This paper introduces a Finite-Set Model Predictive Control algorithm designed for achieving a balanced device junction temperature in a Hybrid SiC ANPC converter. The inner switches of the converter are replaced by SiC MOSFETs and the control algorithm is designed to utilize the low switching losses of the devices. The obtained experimental results are compared to carrier based benchmark algorithm. It is demonstrated that the temperature difference between the devices is within 1°C and the dc-link voltage deviation is within 0.5V.**

***Index Terms*—Active Neutral Point Clamped converter (ANPC), Finite-set Model Predictive Control (FS-MPC), hybrid power stage, multilevel converter, SiC**

I. Introduction

In 1980s the three level neutral point clamped (NPC) converter was introduced for the medium-voltage large variable speed drives to improve the conversion efficiency [1]. Nowadays, the application has also spread in the low voltage range, particularly for interconnection of renewable energy sources [2]–[4]. It was soon noticed that although the topology has brought many benefits such as lower harmonic distortion of the output voltages/currents, smaller and cheaper filters, the maximum output power was still limited by the unbalanced stress distribution of the power components [5], [6]. Efforts have been made to solve the problem by sizing the components for the expected stress [7]. However the problem was still not solved as a different operating point of the converter presented different temperature distributions. For low amplitude modulation indexes the inner devices are more stressed due to increased usage of the small voltage vectors e.g. low voltage ride through in [8], while for high modulation indexes the situation will change due to more frequent application of the large voltage vectors. We can conclude that for solving this problem not only the hardware needs to adapted but also the designed control algorithm needs to take into account different stress distributions in the operating points of the converter.

One of the most popular solutions was the active neutral point clamped (ANPC) topology, first introduced in [5]. By replacing the clamping diodes with the active switches, more redundant switching states can be achieved to balance out the loss distribution. Different commutations and zero states are used to distribute the losses more evenly. In [9] online calculations of the switching and conduction losses are used for the estimation of the junction temperatures, which are fed back to the control unit. In the next step, the applied switching state is selected from the decision chart for commutations to the zero states. Loss distributions of six PWM-based control strategies are compared in [10]. The proposed method has managed to outperform the other PWM modulation methods and balance out both the conduction and switching loss distribution, however the method was not experimentally validated in that paper. In [11] authors propose an adaptive double frequency PWM (ADF-PWM) that can adapt the duty cycles of every switching cycle to optimize the loss distribution. Nevertheless, it is not shown whether the algorithm also can balance the neutral point voltage or another control loop is necessary. Algorithms based on Finite-set model predictive control (FS-MPC) have the possibility to include multiple objectives in a single cost function without the necessity of additional control loops [12]–[14]. In [12] the FS-MPC is divided into two stages: in the first stage the cost function that includes the current control and DC-bus balance control is used and in the second a cost function that manages the loss energy balancing is used. Therefore, in the first stage 27 different voltage vectors are evaluated and in the second stage if the zero voltage vector is selected, predictions for 4 possible zero vectors are calculated. Both cost functions have two weighting factors, however it is not described how they should be optimally selected. The algorithm was modified in [13] where now only one cost function is used and the power losses are predicted using a function that contains the most stressed devices according to the switching transition. In this way the search time and the calculation time of the algorithm are reduced, though the weighting factor tuning still remained as the most difficult part of the control design. The control method presented in [14] Predictive Active Loss Balancing (PALB) is a combination of SHE-PWM and MPC. Despite the fact that the method showed decreased maximum junction temperature and increased output power, it was not

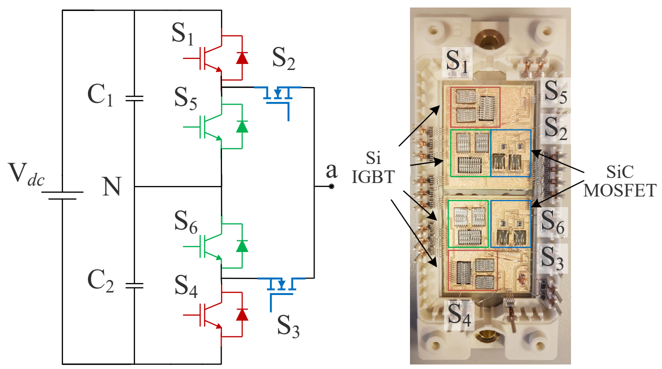


Fig. 1. One phase ANPC open module.

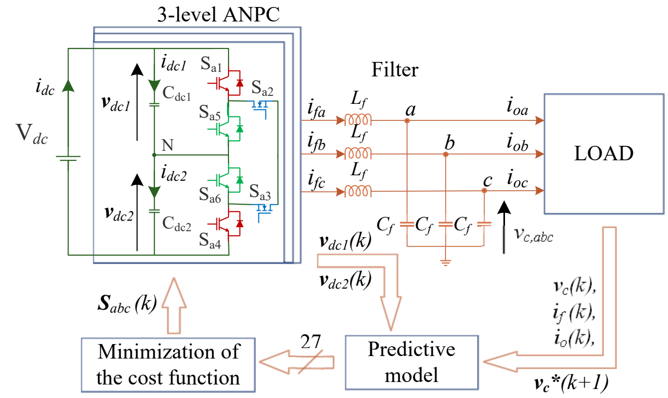


Fig. 2. Simplified system model scheme of ANPC converter using model predictive control.

validated experimentally due to high computational burden in the implementation.

Although the maximum power rating of the ANPC converter was increased in aforementioned publications, the market still demands for an even higher power density converters with smaller and lighter filters. To achieve this, the switching frequency of the converter would need to be increased, which on the other hand will introduce higher switching losses. Here, strategically by replacing just some of the devices with wide band gap (WBG) devices and combining an efficient use of their low switching losses and Si-IGBT's conduction characteristics, especially for high currents [15]–[17].

In this paper the loss distribution of a hybrid ANPC converter will be investigated. The module consists of four Si IGBTs and two SiC MOSFETs used as the inner switches as shown in Fig. 1. Two control algorithms will be compared in this paper: a carrier based modulation presented in [17] and a new FS-MPC based algorithm. The MPC algorithm was chosen due to the very simple inclusion of additional objectives in the cost function [18]–[20]. In this way, in one control loop three different objectives can be fulfilled: control of the output voltage, DC-bus voltage and loss distribution. This will be the first attempt to experimentally validate the use of FS-MPC algorithm on a three level hybrid ANPC converter and record the junction temperatures of the hybrid open module during operation. The structure of the paper is the following. In Section II we introduce the hybrid SiC ANPC converter. The control algorithm is explained in the Section III. Evaluation of the loss distribution is done in Section IV. Conclusions and future research aspects are given in the last section.

II. Hybrid SiC ANPC converter

As mentioned in the introduction, in order to comply with market's need for high power density converters with small and lighter output filters, the switching frequency needed to be increased. To reduce the switching losses WBG devices must be used. Replacing all the devices with WBG devices would be an expensive solution and it may not be necessary if we know which devices are the ones that suffer under high switching losses. In our case we are looking at applications for unidirectional power flow with high modulation index like e.g. photovoltaic or UPS, where the inner devices of an ANPC have the highest losses. Thus we have decided to use a hybrid SiC ANPC converter, that was build using the open modules shown in as Fig. 1. The module contains two SiC MOSFET's S_2 and S_3 which have two parallel connected chips (V_{DS} = 650 V, $R_{DS(on)}$ = 23 mΩ) and four IGBT's which are also realized as parallel connected chips (V_{CE} = 650 V, I_C = 75 A). For one phase module, 8 different switching combinations can be applied, two combinations that connect the output to the positive DC voltage, two combinations that connect to the negative and four combinations that can realize the zero voltage [10], [21]. However, in our case only one positive, one negative and two redundant zero voltage combinations will be used as shown in Table I. It can be noticed that devices $S_1 - S_6$, $S_4 - S_5$ share the gate signals and that $S_2 - S_3$ are complementary pairs. The zero voltage state "0^+" is only used in the positive cycle and zero voltage state "0^-" in the negative cycle. In this way only two switches need to change the state while transitioning from "P" state to "0^+" and "N" to "0^-" respectively. Moreover, only inner switches ($S_2 - S_3$) are changing the states during the half cycle i.e. the MOSFETs are switched with a higher switching frequency to take the advantage of the low switching losses of the devices.

Table I: Switching states of the 3L ANPC converter.

Switching state	S_1	S_2	S_3	S_4	S_5	S_6
P	1	1	0	0	0	1
0^+	1	0	1	0	0	1
0^-	0	1	0	1	1	0
N	0	0	1	1	1	0

III. Control algorithm

For the hybrid ANPC prototype we have chosen to develop a control algorithm based on the FS-MPC because, the algorithm

Table II: System parameter values.

Parameter	Value
DC-link voltage and capacitance (V_{dc}, $C_{dc1,2}$)	700 V, 2.8 mF
Filter inductance (L_f, C_f)	2.4 mH, 15 μF
Load resistance (R_{load})	2.16 Ω
Sampling time (T_s)	20 μs

offers a simple inclusion of multiple objectives in the control cost function and a fast transient response [22]. The objectives that need to be taken into account in the control design are: voltage reference tracking, neutral point balancing and device temperature balancing. As stressed in the previous sections, depending on the application (modulation index, power factor) the stress distribution of the ANPC converter will change. In our case, the converter is expected to be working with a high modulation index and unidirectional power flow. This means that the most stressed device will be the outer devices (S_1, S_4) [21]. Therefore, the algorithm needs to reduce the switching stress of these devices and distribute it to the inner SiC devices, which can operate on high switching frequencies with lower losses.

The schematic of the system can be seen in Fig. 2. In each sample period the FS-MPC controller collects the measurements of the DC-link voltages ($v_{dc1,2}$), converter output current ($i_{f\,abc}$), filter capacitor voltage ($v_{c,\,abc}$) and load current ($i_{,\,abc}$) to calculate the propagations of the voltages for 27 possible switching states of the three phase converter. Using the Clark transformation the control variables are transformed from time domain components of the three phase abc system to the stationary $\alpha\beta$ reference frame. The propagations for the next sample period are calculated using the discretized system equations given in (1) - (3). Euler forward method is used to obtain the discrete system equations. Once the predictions are calculated, they are used in the cost function, which defines the desired behaviour of the converter.

$$v_{dc1,2}(t) = C_{dc1,2}\frac{di_{dc1,2}(t)}{dt} \quad (1)$$

$$i_{f\,\alpha\beta}(t) = C_f\frac{dv_{c\,\alpha\beta}(t)}{dt} + i_{o\,\alpha\beta}(t) \quad (2)$$

$$v_{i\,\alpha\beta}(t) = L_f\frac{di_{f\,\alpha\beta}(t)}{dt} + v_{c\,\alpha\beta}(t) \quad (3)$$

Three objectives will be used in the cost function (4): output voltage control, DC-link balancing and penalization for the switching of the outer switches i.e. favouring the switching of the inner switches $S_2 - S_3$:

$$g = (v^*_{c\alpha\,\beta} - v^P_{c\alpha\,\beta})^2 + \lambda_{dc}g_{dc} + \lambda_p g_p \quad (4)$$

$$g_{dc} = (v^P_{dc1} - v^P_{dc2})^2 \quad (5)$$

$$g_p = \sum_{x=a,b,c}(1 - |S_{2x}(k) - S_{2x}(k-1)|) + \quad (6)$$

$$(1 - |S_{3x}(k) - S_{3x}(k-1)|), \quad (7)$$

where weighting factors λ_{dc} and λ_p define the importance of each objective, $S_x(k-1)$ represents the previous and $S_x(k)$ the current switching state for all converter phase legs $x \in a, b, c$. The optimum weighting factors can be determined by using the Artificial Neural Networks approach presented in [23].

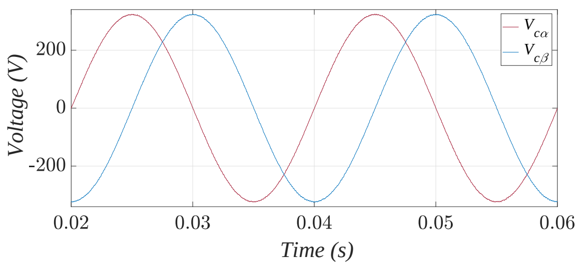
IV. Loss distribution and device junction temperature comparison

A simulation model of the system presented in Fig. 2 and FS-MPC algorithm explained in the previous section were created in MATLAB Simulink. The thermal modeling of the devices was done in PLECS Blockset using the manufacturer datasheets. In Table II system parameters used for simulations to analyze the device stress under high power loading are presented. The weighting factors in the cost function (4) were set to λ_{dc} = 5 and λ_p = 1. A benchmark model using the carrier based algorithm based on phase disposition of the carriers presented in [17] was used for comparison. Due to the lack of modulator in the FS-MPC algorithm, the switching frequency of the converter is variable, therefore only the average switching frequency per device can be calculated using the following expression:

$$f_{sw_{avg}} = \sum_{i=1}^{6}\frac{f_{sw_{ai}} + f_{sw_{bi}} + f_{sw_{ci}}}{3} \quad (8)$$

A. Simulation results

In Fig. 3 filter capacitor voltage and reference tracking error are shown. Even with the two secondary objectives in the cost function it can be noticed that the reference tracking of the algorithm has a good performance. The obtained simulation results of the loss distribution and device junction temperatures are shown in the Fig. 4. For the FS-MPC algorithm an average switching frequency of 14 kHz was calculated and for the benchmark model 15 kHz switching frequency was used. The total losses for the nominal output power of 73 kW for FS-MPC algorithm were 883 W (η = 0.988) and 1110 W (η = 0.985) for benchmark algorithm respectively. Although the overall efficiency was not significantly increased, lower losses per device can be noticed in the Fig. 4a. We can also notice that for the benchmark algorithm the only device producing the switching losses is the inner MOSFET and the total switching losses for FS-MPC algorithm are the same but they are spread over all devices. This difference can be explained by the fact that the switching sequence of the benchmark algorithm is fixed and it is always following the same pattern from Table I, whereas FS-MPC is evaluating in every sample step if it is possible to avoid switching the outer devices without significantly degrading the reference tracking performance and DC-link voltage balance. Moreover, it can be seen that the clamping switches are also being used more often than in the benchmark algorithm, but also the outer switches are producing lower conduction losses. All of this is mirrored into the junction temperatures of the devices, which are for the proposed algorithm lower. Lower and balanced device temperatures can increase both the lifetime of the converter and also the maximal power output.



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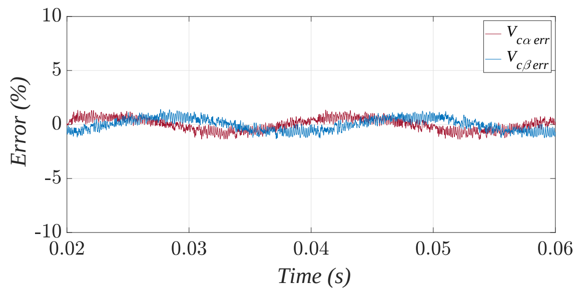

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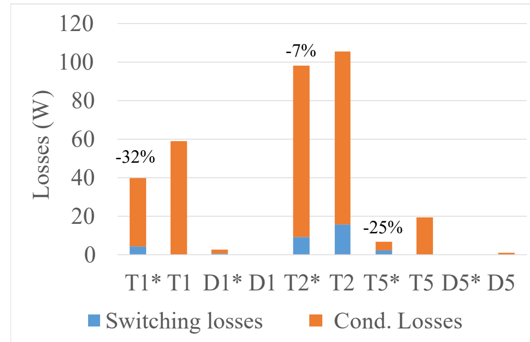
Fig. 3. Simulation results for the proposed FS-MPC algorithm: (a) capacitor voltage (b) voltage reference tracking error in $\alpha\beta$ reference frame.



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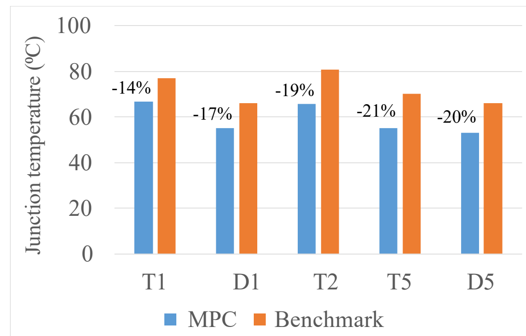


(b)

Fig. 4. Simulation results for one phase module: (a) device losses in a hybrid module for MPC (*) and benchmark algorithm. (b) device junction temperatures in a hybrid module MPC (*) and benchmark algorithm used in [17].

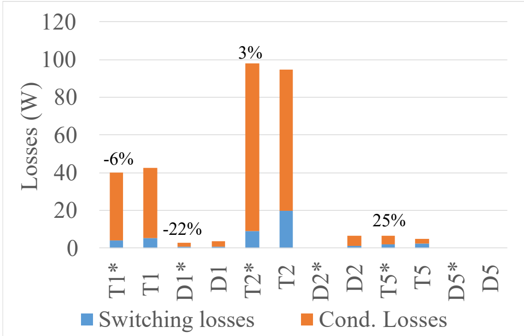
It also needs to be noticed that the benchmark algorithm needs an additional control loop to maintain the DC-link balance, while in the FS-MPC algorithm this is already included in one control loop. This would have impact on the transients as the FS-MPC controller will have a faster response than in the benchmark model. The results are also compared to the loss distribution and junction temperatures of full Si ANPC module with MPC algorithm. In the loss distribution chart in Fig. 5a it can be seen that for the hybrid module the switching losses of the inner device and total losses on the outer device are lower. The positive effects are also visible in the thermal stress distribution given in Fig. 5b where the lower junction temperatures of the devices can be noticed.

B. Experimental results

In Fig. 6 the three phase prototype ANPC converter can be seen. The control algorithm is implemented using the MicroLabBox DS1202 PowerPC DualCore 2 GHz processor board and DS1302 I/O board from dSpace. The generated gate signals are then connected to the connector board from which the signals are guided through optic fiber cables to the converter board. To compensate the computational delay of the FS-MPC algorithm the predictions were calculated one step further ahead and applied at the beginning of the next time sampling interval as proposed in [22]. It was not possible to use the nominal current values in the experiments due to the set-up limitations (PCB design, DC-supply capacity, protection), therefore the testing was done for the I_o = 30 A and V_{dc} = 260 V.

Measured phase load currents and DC-link voltages can be seen in Fig. 7. It can be noticed that the algorithm can keep a good balance of the DC-link voltages. An average switching frequency of 5.8 kHz was measured per device, the outer and clamping IGBT's (S_1,S_4,S_5,S_6) were switching with 1 kHz, while the MOSFET's (S_2,S_3) were switching with 15 kHz. For a comparison we will also show IR measurements of the conventional carrier based modulation with f_{sw} = 5.8 kHz and f_{sw} = 15 kHz. Here, it needs to be noticed that in this modulation scheme the outer and clamping IGBT's switch with 50 Hz and the MOSFET's with 5.8 kHz and 15 kHz respectively. Which of the two comparison metrics (average switching frequency per device or switching frequency of the MOSFET) should be used for a fair comparison opens up a lot of questions, therefore we will focus more on the temperature distribution rather then on the absolute values of the obtained temperatures.

In Fig. 8 a snapshot from the infrared camera can be seen for the proposed algorithm and the benchmark control algorithm. It can be seen that the temperatures of the upper device S_1 and inner device S_3 are very good balanced for all 3 control strategies. We can also notice that the distinction is found in the clamping device temperature as seen in Fig. 9. For the proposed algorithm the temperature difference of the clamping



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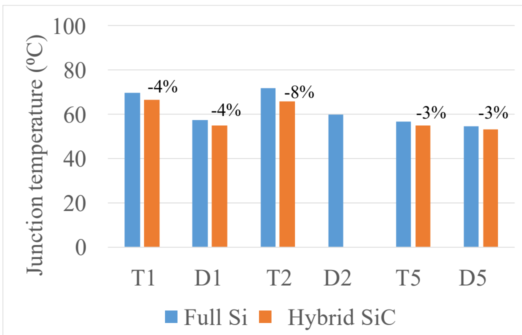


(b)

Fig. 5. Simulation results for one phase module: (a) device losses for MPC in a hybrid ANPC module (*) and in full Si (b) device junction temperatures in a hybrid ANPC module (*) and in full Si.

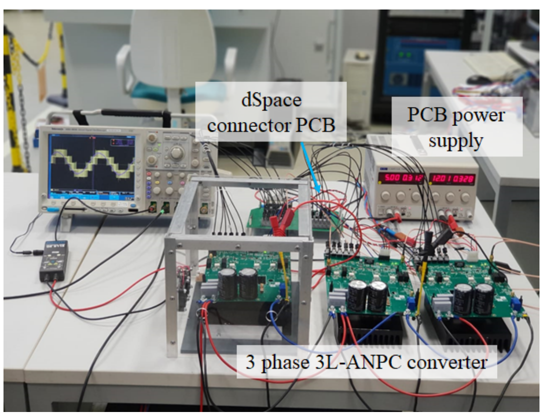
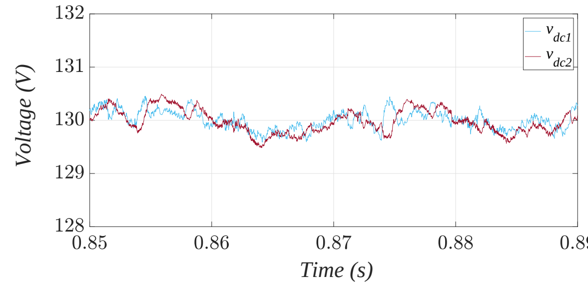


Fig. 6. Three phase ANPC experimental set-up

device and the outer device is 1.6°C, while for the benchmark model the difference is 3.8°C, see Table III . This result was expected as the proposed algorithm is switching the clamping device with a higher switching frequency providing better distribution of the losses among the devices.

V. Conclusion

A Finite Set Model Predictive Control algorithm is proposed to balance the temperatures in a hybrid ANPC module. This is achieved by penalization of the switching combinations that



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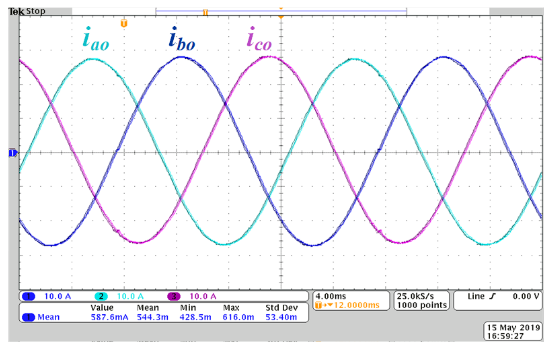


(b)

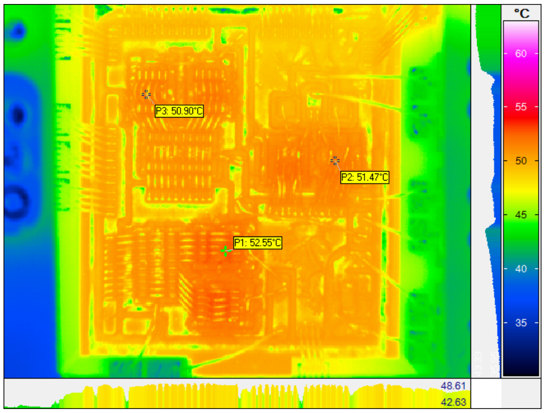
Fig. 7. Experimental measurements: (a) DC-link voltages $v_{dc\,1,2}$, (b) phase load currents $i_{o\,abc}$ [10 A/div] at P = 4 kW.

Table III: Comparison of the measured junction temperatures for the three control strategies (P = 4 kW).

Control	Switching freq.	T_{j4}	T_{j4}	T_{j4}
FS-MPC	5.8 kHz	52.55°C	51.47°C	50.9°C
Bench. PWM	5.8 kHz	53.56°C	52.43°C	49.76°C
Bench. PWM	15 kHz	54.14°C	53.78°C	51.81°C

switch the outer switches more often in the cost function. As a consequence, the switching frequency of the inner switches will increase while in outer devices it will decrease. In this way the advantage of low switching losses of the SiC MOSFETs will be utilized. Simulation results for the nominal converter power showed that the proposed algorithm can provide balanced stress distribution and good reference tracking performance. This was also confirmed with experimental measurements which showed that the difference between the inner and outer device temperature is within 1°C. Moreover, it was showed that the proposed algorithm can maintain the DC-link voltages in good balance with voltage deviation bellow 0.5 V. An improvement compared to the conventional carrier based algorithm is also seen in the clamping device temperature which had a lower temperature difference to the outer device then when using the conventional algorithm.

It this paper only a unidirectional power flow was investigated for e.g. photovoltaics application, in future work the thermal analysis of the hybrid ANPC converter using the



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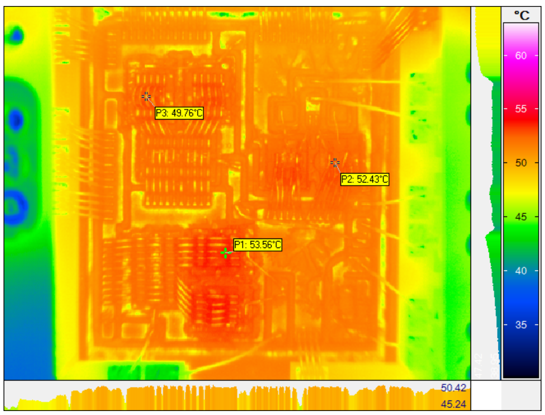

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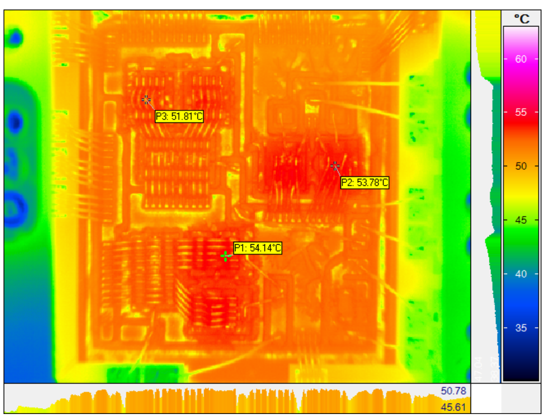
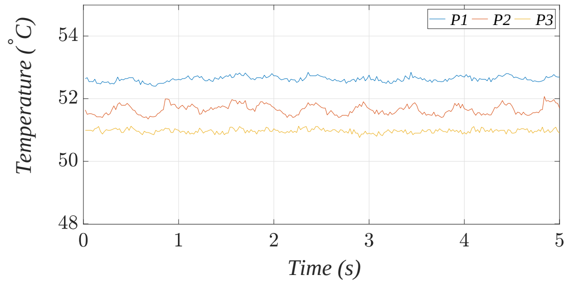


(c)

Fig. 8. IR snapshot of the one phase ANPC open module during operation, V_{dc} = 260 V, I_o = 30 A: (a) with the proposed FS-MPC algorithm, (b) with benchmark algorithm, f_{sw} = 5.8 kHz, (c) with benchmark algorithm, f_{sw} = 15 kHz.



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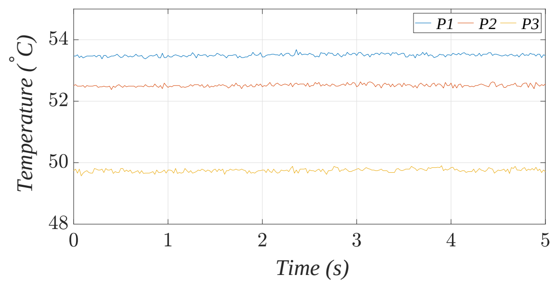

(b)

Fig. 9. Junction temperature measurement for (P1 $\rightarrow$ S4 (outer switch), P2 $\rightarrow$ S3 (inner switch), P3 $\rightarrow$ S6 (clamping switch)) in steady state, V_{dc} = 260 V, I_o = 30 A: (a) with proposed FS-MPC algorithm, (b) with benchmark algorithm, f_{sw} = 5.8 kHz (see Fig. 8).

proposed algorithm will be extended for reverse power flow and low modulation indexes.

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