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Implications of short-circuit events on power cycling of 1.2-kV/ 20-A SiC MOSFET power modules

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Abstract

When the device works in the real-field application, short-circuit events could happen along the whole lifetime of the component. In order to investigate the degradation effects of short-circuit events on power cycling, a mixed accelerated aging test combined with a repetitive short-circuit test has been performed for the 1.2-kV/ 20-A SiC MOSFET power module. The short-circuit robustness and repetitive short-circuit performance are analysed on the fresh device at first in order to understand the different levels of degradation. Then, the power cycling test is performed for two matched devices with the selected test conditions; one of them undergoes a number of short-circuit events and the other one, without short-circuit stress, is used as the reference. The experimental results exhibit a major implication of short-circuit degradation on power cycling and it would accelerate the degradation process of SiC MOSFETs.

1. Introduction

Silicon Carbide (SiC) power devices have drawn extensive attention for future power electronic systems thanks to their superior material properties. Compared with silicon devices, the emerging SiC MOSFETs have promising capability especially in the high temperature and high switching frequency operations. Despite their inherent advantages, the reliability becomes a critical issue at both chip and package level.

By means of accelerated power cycling test, the wear-out reliability issues can be investigated within very short time [1]. The on-state drain and source voltage (V_{DS}), which mainly consists of the voltage across die, solder layer and bonding wires, is used as an indicator to evaluate the degradation. Due to the different thermal expansion coefficient of the different materials, the bonding wires [2] and solder layers [3] become degraded over long-term operation. Since the high-temperature environment could cause the threshold voltage (V_{th}) shift in SiC MOSFETs, the die degradation effect has also been investigated in [4].

On the other hand, the reliability of SiC MOSFETs under Short-Circuit (SC) conditions still remains a challenge due to the smaller die area and thinner gate oxide. A thermal runaway could happen when the drain leakage current is high enough, which would trigger a positive temperature feedback [5]. In order to analyse the degradation mechanisms of SiC MOSFETs, some repetitive SC aging tests have been performed on fresh devices [6] [7]. Furthermore, the degradation indicators including threshold voltage, gate leakage current, output characteristics are evaluated in [8] [9].

With the aid of power cycling tests at various conditions (i.e. mean temperature T_{jm} and junction temperature ΔT_{j}), the lifetime of component could be estimated based on application requirements [10]. However, when the power devices work in the real application, several times of SC events could appear [11]. Therefore, the degradation effects of SC events on the lifetime need to be considered.

In this paper, a mixed accelerated aging test combined with repetitive short circuit is performed in order to investigate the degradation effects of short-cicuit events on the power cycling of SiC MOSFETs.

2. Test setup

2.1. Device under test

The Device Under Test (DUT) is a commercial 1.2-kV/ 20-A three phase six-pack SiC power module which could be used in motor drives and

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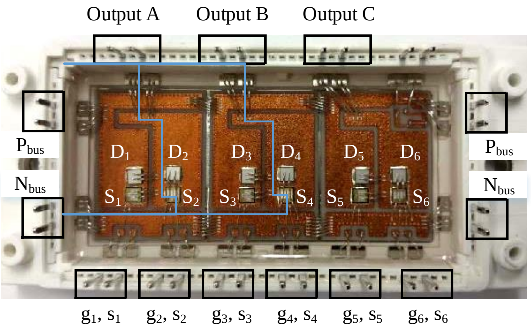


Fig. 1. 1.2 kV/ 20 A three phase six-pack SiC power module and its layout.

solar inverters. The layout inside the power module is shown in Fig. 1. The positive and negative bus terminals (P_{bus}, N_{bus}) are located on the left and right side. The module has three substrates (i.e. three phases) and each one consists of two SiC MOSFETs and two diodes. The S_1, S_3 and S_5 are the upper-side SiC MOSFETs and the lower side are named as S_2, S_4 and S_6. Furthermore, there are Kelvin-source terminals (from s_1 to s_6) as can be seen in the bottom of Fig. 1.

2.2. Power cycling test setup

The principle schematic of the DC-based power cycling test is shown in Fig. 2. The DC current source supply (DELTA SM 45-140) provides a constant current I_{load} and two independent commercial gate drivers (CREE CRD-001) with adjustable output voltage are used for two switches separately. The used gate resistance (R_G) is equal to 20 Ω and the control signals G_1 and G_2, provided by a Field-Programmable Gate Array (FPGA), are operated in a complementary mode with 1 ms overlap in order to keep the I_{load} stable during switching time. The junction temperature swing ΔT_j is controlled by adjusting the I_{load} and turn-on/off time duration (t_{on}/t_{off}). The mean temperature T_{jm} is achieved by the external heater and force air cooling system. An optical fiber condition unit (Opsens) with two fiber thermal sensors (OTG-F-10) are used to measure the junction temperature. Both drain-source voltage (V_{DS}) and gate-source voltage (V_{GS}) are monitored during the whole power cycling test.

2.3. Short-circuit test setup

The repetitive short-circuit tests have been performed by a 2.4-kV/ 10-kA Non-Destructive Tester (NDT) [12]. The basic schematic of short-circuit test is shown in Fig. 3. The goal is to test the SiC MOSFET under extreme conditions in order to assess the SC capability avoiding explosions. A series protection, consisting of four IGBT power modules in parallel, works as a circuit breaker. The busbar has low inductance (10 nH) to avoid the high voltage spikes when the device turns off. A FPGA provides the control signals to the gate drivers for both the series protection and the DUT, which is driven by a +20 V/ –5 V gate voltage. A MATLAB GUI is used to adjust the SC pulse time duration (t_{SC}), number of repetitions (N_{SC}) and interval time between consecutive tests (t_{int}). During each SC test, the drain-source voltage (V_{DS}), gate-source voltage (V_{GS}) and the drain current (I_D) are measured by the oscilloscope.

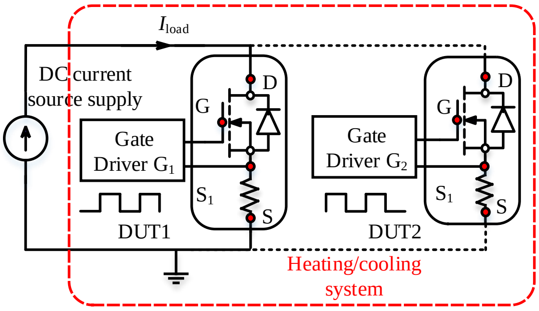


Fig. 2. Schematic of DC-based power cycling test.

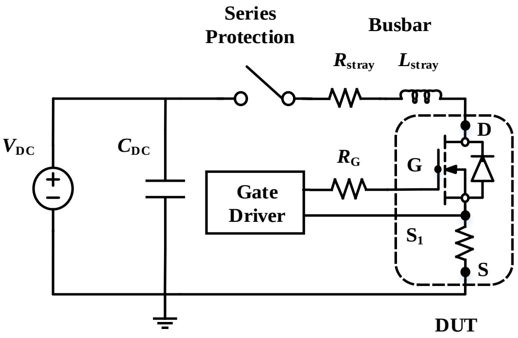


Fig. 3. Schematic of the short-circuit test.

3. Mixed accelerated aging test approach

3.1. Selected test conditions

First, power cycling tests have been done as described in the following. A power supply provides a constant current of 20 A to each of the two DUTs for a period of 2 seconds, alternately. The temperature of external heater is set to 98 ºC in order to achieve the required initial minimum junction temperature (T_{j_min}). The gate-source voltage (V_{GS}) is set with different values in order to have the same on-state drain-source voltage (V_{DS}) and operate under the same thermal stress (ΔT_j). The summary of the test conditions for the power cycling test can be found in Table 1.

Table 1
Test condition for the power cycling test

Parameters	Value (unit)
Load current I_{load}	20 A
t_{on}/ t_{off}	2s/ 2s
Initial maximum T_{j_max}	162 ºC
Initial minimum T_{j_min}	104 ºC
Initial ΔT_j	58 ºC

To figure out the short circuit test condition for the mixed accelerated aging test approach, one of the SiC MOSFETs (S_5) has been tested with increasing short-circuit pulse time (t_{SC}) in steps of 0.2 μs. During the test, the V_{DS} is set to 600 V, the V_{GS}= +20 V/ –5 V and the junction temperature is 25 ºC. The experimental results can be seen in Fig. 4, where the on-state V_{GS} starts to decrease at the end of the short circuit pulse, i.e. t_{SC}= 3.6 μs. When the short circuit pulse is further increased to 4.4 μs, the V_{GS} is no longer 20 V but 18.5 V, which is in agreement with the results in [13], indicating that the SiC MOSFET presents a permanent gate oxide degradation and metal deformation by failure analysis. Therefore, it is considered as the critical short circuit energy for this device and the junction temperature during SC test could reach more than 600 ºC according to [14].

For the repetitive SC test during the mixed accelerated aging approach, the short circuit energy has been selected below the point where degradation has been observed, therefore the short circuit test conditions are: V_{DS}= 600 V, V_{GS}= +20V/ –5 V, t_{SC}= 3 μs and T_{case}= 25 ºC.

3.2 Lifetime consumption due to repetitive SC test

The lifetime consumption due to repetitive SC tests has been assessed for the S_6 device with the selected test condition (i.e. V_{DS}= 600 V, V_{GS}= +20V/ –5 V, t_{SC}= 3 μs and T_{case}= 25 ºC). The aging indicator to assess the end-of-life is the reduction of the on-state gate source voltage at the end of the short circuit pulse, since it shows a strong correlation with the number of repetitions. The results can be observed in Fig. 5, where the on-state V_{GS} decreases with increasing number of repetitions. This phenomena has been investigated in [6] – a gate oxide damage leads to the increase of gate leakage current, resulting in the on-state gate voltage reduction. This effect indicates that leakage current increases with the number of repetitions. The end-of-life is selected when the V_{GS} reduces 2 V (i.e. V_{GS}= 18 V) and this situation occurs after 143 short circuit repetitions as shown in Fig. 5.

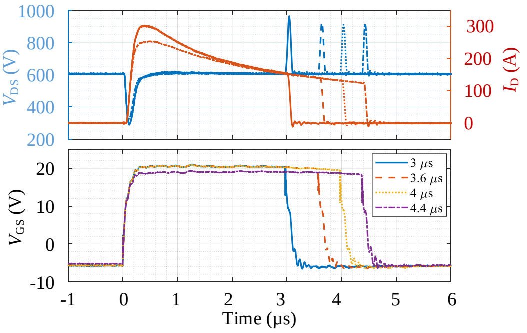


Fig. 4. Short-circuit waveforms (V_{DS}, I_D and V_{GS}) of 1.2 kV/ 20 A SiC MOSFET (S_5) with increasing t_{SC}.

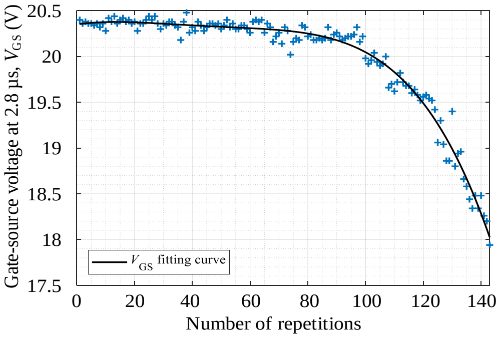


Fig. 5. Decrease of gate-source voltage during SC tests with increasing number of repetitions increasing (S_6).

3.3. Test approach

A static characterization on two of the fresh SiC DUTs (S_2 and S_4) has been performed by means of a power device analyser (Keysight B1506A). It has been observed that the DUTs have slightly unmatched on-state voltage drop; therefore, the V_{GS} is adjusted before the mixed accelerated test in order to keep the DUTs at the same initial on-state voltage and temperature swing (i.e. S_2 is set to V_{GS}= 18 V and S_4 is set to V_{GS}= 20 V).

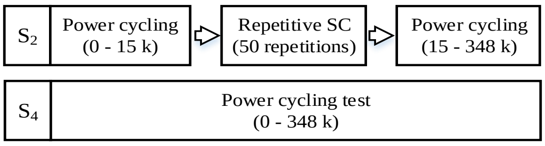
After the initial calibration, the two DUTs (S_2 and S_4) have been tested under power cycling up to 15 k cycles with the aim of having a device which has not been degraded yet, according to the experimental results presented in [4].

Then, the repetitive short circuit tests are performed for one of the DUTs (S_2) under the tests conditions mentioned above (i.e. V_{DS}= 600 V, V_{GS}= +20 V/ –5 V, t_{SC}= 3 μs and T_{case}=25 ºC). The number of repetitions has been set to 50, which corresponds to 35% of the total consumed life of the SiC MOSFET according to Fig. 5.

After the repetitive short circuit activity, power cycling tests have been again performed on device S_2 until failure. Meanwhile, the SiC MOSFET DUT S_4 has been only tested under power cycling tests in order to compare the results with device S_2.

The flow chart of test approach is shown in Fig. 6 and it allows to investigate the degradation effects of repetitive SC events and understand which parameters show a major shift with the mixed accelerated aging test.

4. Experimental results and discussion



S2
Power cycling (0 - 15 k)
Repetitive SC (50 repetitions)
Power cycling (15 - 348 k)
S4
Power cycling test (0 - 348 k)

Fig. 6. Flow chart of mixed accelerated aging test combined with short-circuit events.

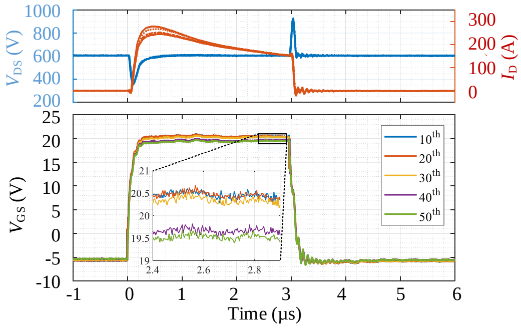


Fig. 7. Short-circuit waveforms (V_{DS}, I_D and V_{GS}) of 1.2 kV/ 20 A SiC MOSFET (S_2) from 10th to 50th SC event.

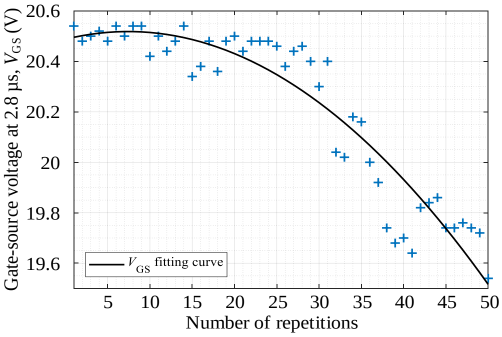


Fig. 8. Gate-source voltage at 2.8 μs during SC tests decreases with the increasing number of repetitions (S_2).

Before starting power cycling test, 1 k cycles have been used to ensure the stable thermal condition. The repetitive short-circuit tests for S_2 have been performed after 15 k cycles and the SC waveforms from 10th to 50th in step of 10 repetitions are shown in Fig. 7 for the sake of clarity. An obvious gate voltage reduction of device S_2 could be observed at 40th SC repetition. Similar to the device S_6 in Fig. 5, the on-state V_{GS} at 2.8 μs of the device S_2 deceases with the SC repetitions increasing as present in Fig. 8. During the 50th SC event, the on-sate V_{GS} decreases to 19.5 V.

The static characteristics of device S_2 have been measured before starting the tests, after the power cycling stress (15 k) and again measured after the SC repetitive stress. Fig. 9 shows the variation of both I_D-V_{GS} and I_D-V_{DS} curves, which reveals that the on-state resistance increases slightly after the SC repetitive stress. In Fig. 10, the gate leakage current (I_{GSS}) of the device S_2 increases from 3.84 pA to 42.62 mA (when the V_{GS} is equal to 20 V) after the SC test and in this case, the gate oxide degradation could be confirmed. The V_{th} shifts positively from

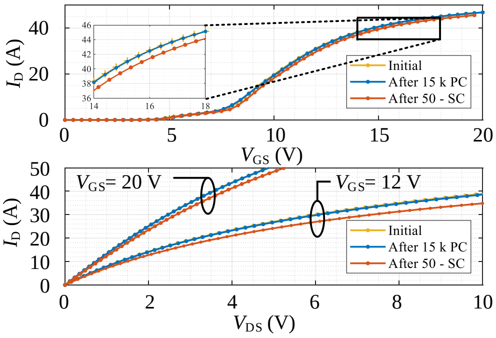


Fig. 9. I_D-V_{DS} and I_D-V_{GS} characteristics variation of the device S_2 before test, after 15 k power cycling test and after 50 short-circuit repetitions.

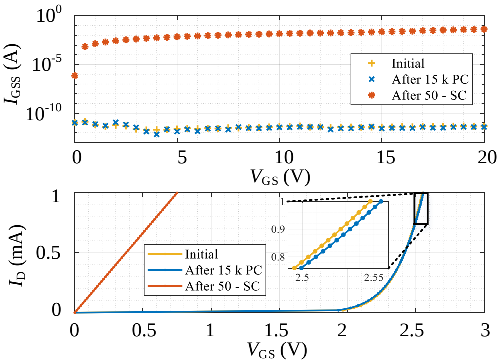


Fig. 10. Gate leakage current increase and threshold voltage variation of the device S_2 before test, after 15 k power cycling test and after 50 short-circuit repetitions.

2.547 V to 2.555 V after the 15 k cycles and this is most likely affected by the trapping and de-trapping phenomena at the SiC/SiO$_2$ interface, which has been investigated in [15]. The V_{th} curve becomes linear after repetitive SC test because of the gate-oxide degradation, indicating constant resistance and the current increases linearly with voltage.

The effect of repetitive SC tests on the on-state voltage ($V_{DS,on}$) can be observed in Fig. 11. In the beginning, the device S$_2$ and S$_4$ have the same $V_{DS,on}$, which is equal to 3.12 V. After 15 k power cycling test, repetitive SC tests are applied to the SiC MOSFET S$_2$ showing that the $V_{DS,on}$, jumps to 3.34 V. Thereafter, the $V_{DS,on}$ shows a sharp increase with the increasing number of cycles until failure at 348 k. On the other hand, the S$_4$, which has been exposed to the power cycling test without SC stress remains at 3.12 V and it shows a gradual increase of $V_{DS,on}$ with the increasing number of cycles. Therefore, it is observed that when the SC stress is applied, the $V_{DS,on}$ shows a faster increasing trend, which indicates that the SC events exacerbate the degradation process.

Additionally, during the power cycling test, the junction temperatures (T_j) of S$_2$ and S$_4$ are measured separately by an optical fiber sensor. According to the experimental curves in Fig. 12, it could be observed that an obvious maximum junction temperature (T_{jmax}) increase appears for the device S$_2$ after SC stress and then it also increases gradually throughout the following cycles (100 k, 250 k and 334 k). At the same time, the temperature swing of the device S$_4$ (T_{jmax} and ΔT_j) remains constant. In Fig. 13, the measured junction temperature (T_{jmin} and ΔT_j) of S$_2$ and S$_4$ are presented together for comparison.

It can be concluded that the short-circuit events have a strong effect on the on-state voltage increase. It is worth to note that the gate oxide degradation, induced by the SC events, results in a lower gate-source voltage during power cycling test due to the non-negligible gate leakage current and then leads to the higher $V_{DS,on}$ at the same time. Once the $V_{DS,on}$ is increased, its conduction loss P_{loss} increases and then leads to the T_{jmax} and ΔT_j increase, as explained in Fig. 14. Therefore, higher T_{jmax} and ΔT_j accelerate the degradation process. The experimental tests for all the DUTs are listed in Table 2.

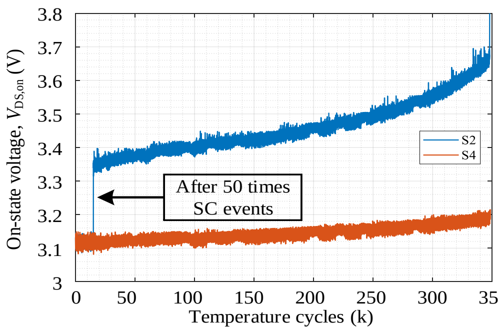


Fig. 11. Evolution of the on-state drain-source voltage (S$_2$) throughout the power cycling test combined with 50 SC repetitions at 15 k cycles.

Table 2
Summary of experimental tests for S$_2$, S$_4$, S$_5$ and S$_6$

No.	Experimental test	Results
S$_2$	Mixed power cycling and short-circuit test	$V_{DS,on}$ had a sharp increase after 50 SC.
S$_4$	Power cycling test	$V_{DS,on}$ had a gradual increase.
S$_5$	Short-circuit test with increasing pulse time	V_{GS} starts to decrease at t_{SC}= 3.6 μs.
S$_6$	Repetitive short-circuit test (t_{SC}= 3 μs)	V_{GS} decrease to 18 V after 143 repetitions.

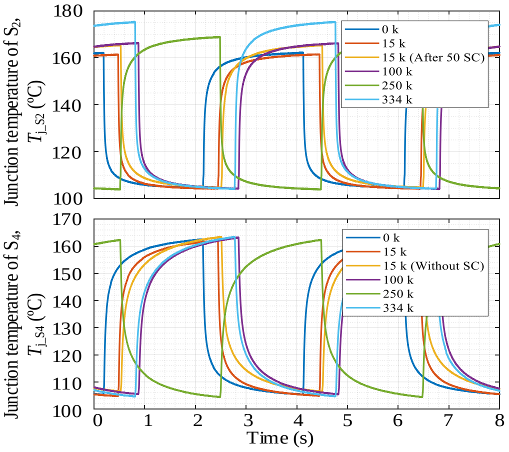


Fig. 12. Junction temperature waveforms of the device S$_2$ and S$_4$ throughout the power cycling test at 0 k, 15 k, 15 k with/without 50 SC, 100 k, 250 k and 334 k.

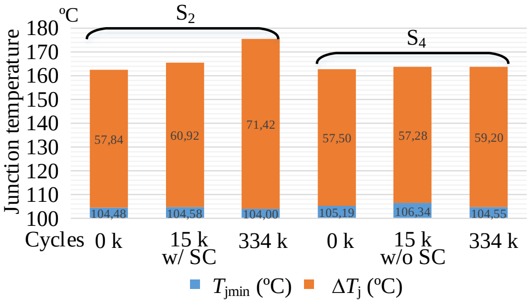


Fig. 13. Measured junction temperature (T_{jmin}, ΔT_j, and T_{jmax}) during power cycling test for S$_2$ (with 50 SC test) and S$_4$ (without SC test).

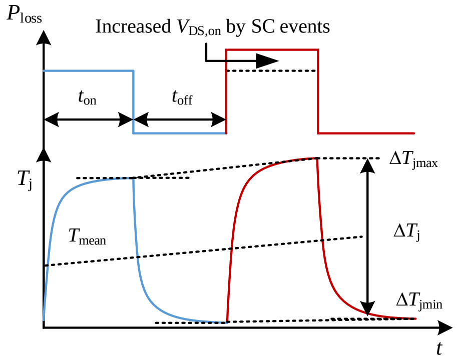


Fig. 14. Implication of short-circuit events on the temperature conditions of power cycling test.

5. Conclusions

This paper investigates the implications of short-circuit events on the power cycling of 1.2 kV / 20 A SiC MOSFET power module thanks to the mixed accelerated aging test approach. After 15 k power cycling test, the experimental results of 50 repetitive short-circuit tests for the device S_2 determine the reduction of on-state V_{GS} as a consequence of gate oxide degradation. Together with the increase of I_{GSS}, the variation of I_D-V_{DS} and I_D-V_{GS} curves have been observed by means of static characterization before and after the short-circuit events.

Thereafter, it has been demonstrated that the short-circuit events have a significant effect on this power cycling test. The V_{DS} of the device S_2 jumps from 3.12 V to 3.34 V and then it continues to increase sharply until failure. In contrast, as a reference device without short-circuit stress, the device S_4 shows a gradual increase in the V_{DS} with the increasing number of cycles. This phenomenon could be explained by the higher T_{jmax} and ΔT_j for S_2 due to the increased conduction loss after short-circuit events. The more severe temperature conditions result in a positive feedback to V_{DS} and it accelerates the degradation process.

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