# EMI Modeling of Three-Level Active Neutral-Point-Clamped SiC Inverter Under Different Modulation Schemes

Pan, Donghua; Chen, Mengxing; Wang, Xiongfei; Wang, Huai; Blaabjerg, Frede; Wang, Wei

*Published in:*
ICPE 2019 - ECCE Asia - 10th International Conference on Power Electronics - ECCE Asia

*Publication date:*
2019

*Document Version*
Accepted author manuscript, peer reviewed version

# EMI Modeling of Three-Level Active Neutral-Point-Clamped SiC Inverter Under Different Modulation Schemes

Donghua Pan[1], Mengxing Chen[1], Xiongfei Wang[1], Huai Wang[1], Frede Blaabjerg[1], and Wei Wang[2]
[1] Department of Energy Technology, Aalborg University, Denmark
[2] School of Electrical Engineering & Automation, Harbin Institute of Technology, China

***Abstract*--This paper investigates the electromagnetic interference (EMI) emission in three-level active neutral-point-clamped (3L-ANPC) silicon carbide (SiC) inverter. Four typical modulation schemes of 3L-ANPC inverter are considered. An EMI model is established by including all the system parasitics and noise sources. Based on this model, a comparison of different modulation schemes on EMI emission is carried out. Simulations are performed in a case study to confirm the theoretical expectations.**

***Index Terms*--3L-ANPC, EMI, modulation scheme, SiC.**

## I. Introduction

The recent evolution of photovoltaic (PV) panel has raised its open-circuit voltage from 1000 V to 1500 V [1]–[3]. A higher DC input voltage can lower power losses in DC transmission cables, which is an impending trend in next-generation PV inverters [4], [5]. At such a voltage level, the three-level neutral-point-clamped (3L-NPC) topology is the most promising option due to its low device stress [6]. The conventional 3L-NPC topology adopts two diodes to clamp the neutral point, which is called the three-level diode neutral-point-clamped (3L-DNPC) [7]. To solve the uneven loss and voltage stress distribution in the 3L-DNPC topology, the three-level active neutral-point-clamped (3L-ANPC) topology is proposed by replacing clamping diodes with active switches [8], [9].

Besides the topology, the selection of power devices is also important in PV inverters. Recently, the new generation of power devices based on silicon carbide (SiC) has drawn more and more attention [10], [11]. As a wide bandgap material, SiC has several superior properties in comparison with the traditional silicon material, e.g., higher thermal conductivity, breakdown field, and energy gap level [12]–[14]. These super properties enable a fast switch transition and a high switching frequency, which push the PV inverters toward high efficiency and high power density, but on the other hand, generate more electromagnetic interference (EMI) noises [15], [16]. Moreover, with the high 1500-V input voltage, the EMI issue becomes especially challenging.

This paper investigates the EMI emission in three-phase 3L-ANPC SiC PV inverter. The four typical modulation schemes of 3L-ANPC inverter are reviewed, and their impacts on EMI noise sources are analyzed. An EMI model that accounts for all the parasitics and noise sources is constructed. Based on this model, a comparative analysis of different modulation schemes on EMI emission is carried out. A case study is presented, and simulation results are provided to verify the theoretical analysis.

This work was support by Innovation Fund Denmark under Grant 5185-00006B (HER-SiC).

## II. Modulation Schemes of 3L-ANPC Inverter

Fig. 1(a) shows a three-phase 3L-ANPC PV inverter feeding into the grid. SiC MOSFETs $S_1$ – $S_6$ and their antiparallel diodes are adopted to form the inverter phase leg. An *LCL* filter is employed at the inverter output due to its superior harmonic attenuating ability [17]–[22]. $L_1$ is the inverter-side inductor, $C$ is the filter capacitor, and $L_2$ is the grid-side inductor. A line impedance stabilization network (LISN) provides the specified impedance at the testing terminal. In the LISN, $R_{LN}$ = 50 Ω, $L_{LN}$ = 50 $\mu$H, $C_{LN1}$ = 1 $\mu$F, and $C_{LN2}$ = 0.1 $\mu$F. $C_{P1}$ – $C_{P6}$ are the parasitic capacitors of SiC MOSFETs and their antiparallel diodes. $C_s$ is the dc bus stray capacitor.

In the 3L-ANPC inverter, there are two neutral current paths, which are the upper path formed by $S_5$ & $S_2$ and their antiparallel diodes and the lower path formed by $S_6$ & $S_3$ and their antiparallel diodes. These two current paths provide alternatives to clamp the neutral point n [23]. The neutral current can flow through any of the upper path, the lower path, or both of them, which leads to different modulation schemes consequently, as shown in Fig. 2.

### A. Scheme I: DNPC Modulation

The DNPC modulation, as its name implies, is to control the ANPC inverter as the DNPC one by keeping the two clamping switches $S_5$ and $S_6$ OFF constantly. The gate signals for $S_1$ – $S_6$ in a line cycle are generated with the phase disposition method, as shown in Fig. 2(a). It is clear to see that $S_1$ is switched in complementary with $S_3$, and $S_2$ and $S_4$ follow the same manner. Each complementary switch ($S_1$ – $S_4$) is modulated at high switching frequency in half line cycle and remains constant in the other half. During the neutral state, where $S_2$ and $S_3$ are ON, the neutral current path is determined by the load current direction.

### B. Scheme II: ANPC Modulation With Same-Side Clamping

With the ANPC modulation, the neutral current path can be intentionally configured, which allows more possibilities in the modulation schemes. One method is called “same-side clamping”, which means to use the upper neutral path for the top cell commutation and the lower neutral path for the bottom cell commutation. Its gate signals are given in Fig. 2(b), where three pairs of

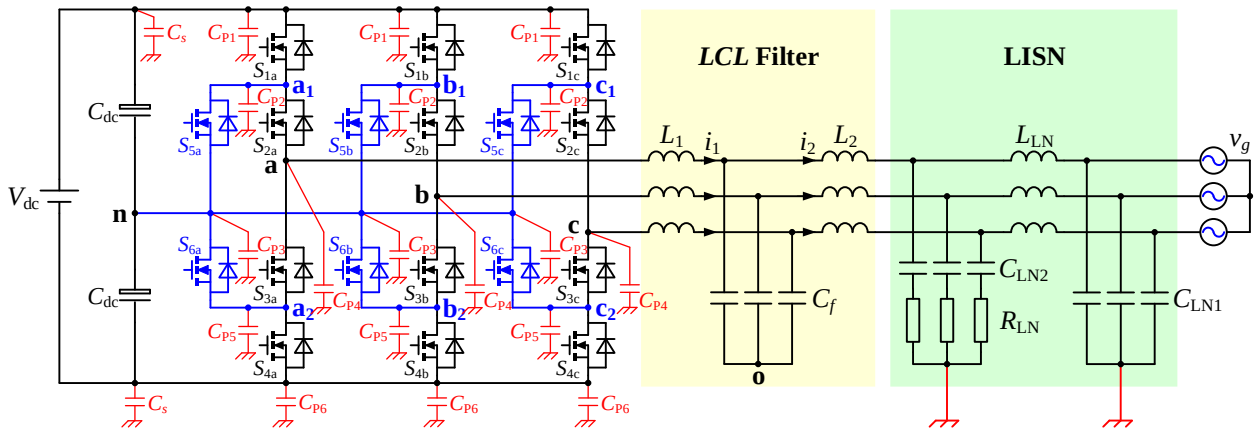


Fig. 1. A three-phase 3L-ANPC SiC inverter with an *LCL* filter.

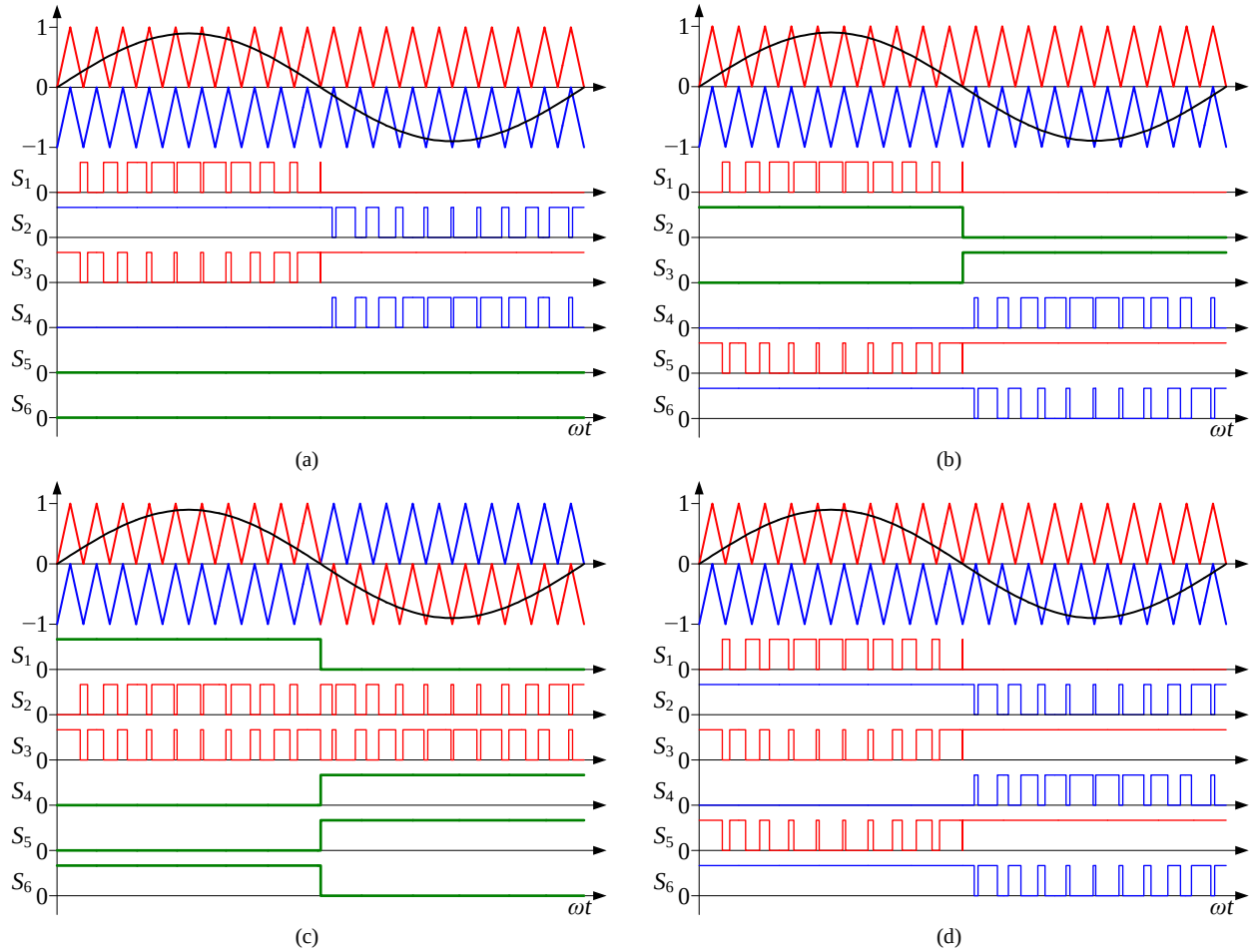


Fig. 2. Modulation schemes of 3L-ANPC inverter. (a) Scheme I: DNPC modulation. (b) Scheme II: ANPC modulation with same-side clamping. (c) Scheme III: ANPC modulation with opposite-side clamping. (d) Scheme IV: ANPC modulation with full-path clamping.

complementary switches, i.e., $S_1$ and $S_5$, $S_2$ and $S_3$, and $S_4$ and $S_6$, can be observed. The outer switches $S_1$ & $S_4$ and the clamping switches $S_5$ & $S_6$ are modulated at high switching frequency in half line cycle and remains constant in the other half. The inner switches $S_2$ & $S_3$ are switched at only the line frequency.

### *C. Scheme III: ANPC Modulation With Opposite-Side Clamping*

On the contrary, we can use the lower neutral path for the top cell commutation and the upper neutral path for the bottom cell commutation, which is called “opposite-side clamping”. As shown in Fig. 2(c), the same complementary switch pairs exist, but the switching patterns are quite different. Only the inner switches $S_2$ & $S_3$ are modulated at high switching frequency. The outer switches $S_1$ & $S_4$ and the clamping switches $S_5$ & $S_6$ are all switched at line frequency.

### *D. Scheme IV: ANPC Modulation With Full-Path Clamping*

Besides using only one current path during the neutral states, the upper path and the lower path can be used together, which is called “full-path clamping” [24]. The two paralleled current paths can reduce the on-state

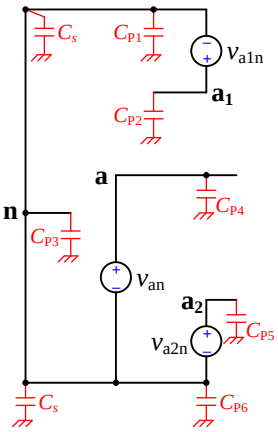


Fig. 3. EMI noise sources in one phase leg of the 3L-ANPC inverter.

resistance and thus the conduction loss during the neutral states. This benefit is especially appealing when SiC MOSFETs are used, since they have excellent current sharing capabilities. As shown in Fig. 2(d), $S_3$ is switched in the same pattern with $S_5$ but in complementary with $S_1$, and $S_2$ is switched in the same pattern with $S_6$ but in complementary with $S_4$. The inner switches $S_2$ & $S_3$ and the clamping switches $S_5$ & $S_6$ are all turned ON during the neutral states.

## III. EMI Modeling of 3L-ANPC Inverter

In the 3L-ANPC inverter, there are three voltage changing ($dv/dt$) nodes in each phase leg, i.e., the midpoint of phase leg (a, b, and c), the midpoint of upper cell ($a_1$, $b_1$, and $c_1$), and the midpoint of bottom cell ($a_2$, $b_2$, and $c_2$). Usually, only the $dv/dt$ at the midpoint of phase leg is considered as the EMI noise source. However, recent analysis in 3L-DNPC topology finds that the other two $dv/dt$ nodes also contribute to the EMI noise [25]. As discussed above, the 3L-DNPC is just a special case of the 3L-ANPC. With various modulation schemes, the EMI emission in the 3L-ANPC inverter will be much more complicated.

To illustrate, a single phase leg of the 3L-ANPC inverter is extracted. Fig. 3 shows the equivalent circuit of phase leg A. The dc link is treated as a short circuit due to its constant dc voltage. The three $dv/dt$ at points a, $a_1$, and $a_2$ are denoted by three voltage sources $v_{an}$, $v_{a1n}$, and $v_{a2n}$, respectively. Combining the counterparts of phase B and phase C, and separating the common mode (CM) and the differential mode (DM) noises, three-phase EMI models of the 3L-ANPC inverter can be obtained, as shown in Figs. 4(a) and (b), where the LISN is simplified as a pure resistor $R_{LN}$, and the CM and DM noise sources are expressed as

$$\begin{cases} v_{CM} = \dfrac{v_{an}+v_{bn}+v_{cn}}{3} \\ v_{CM1} = \dfrac{v_{a1n}+v_{b1n}+v_{c1n}}{3} \\ v_{CM2} = \dfrac{v_{a2n}+v_{b2n}+v_{c2n}}{3} \end{cases} \tag{1}$$

$$v_{DM} = v_{an} - v_{CM}\,. \tag{2}$$

$C_n$ is the total parasitic capacitor connected to the dc bus and the neutral point n, which is expressed as

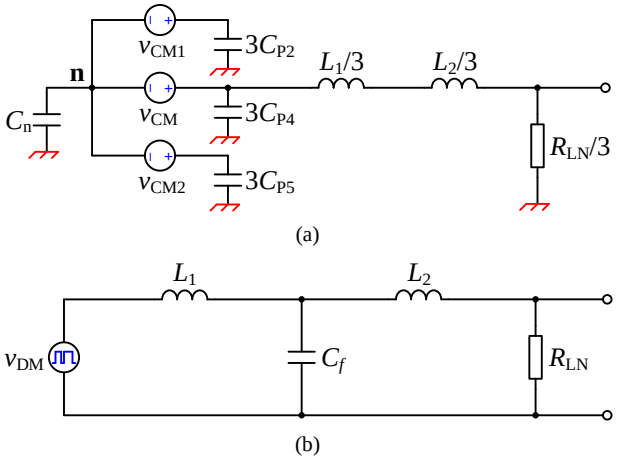


Fig. 4. EMI model of three-phase 3L-ANPC inverter. (a) CM. (b) DM.

$$C_n = 2C_s + 3C_{p1} + 3C_{p3} + 3C_{p6}\,. \tag{3}$$

From the analysis in Section II, it can be found that the modulation schemes only change the neutral current path, but do not affect the voltage output in each phase leg, which means that $v_{an}$, $v_{bn}$, and $v_{cn}$ stay unchanged for different modulation schemes. Consequently, $v_{CM}$ and $v_{DM}$ will keep the same according to (1) and (2). However, $v_{CM1}$ and $v_{CM2}$ do not follow this manner. As shown in Fig. 3, $v_{CM1}$ ($v_{a1n}$) and $v_{CM2}$ ($v_{a2n}$) are determined by the switching patterns of $S_1$ and $S_4$, respectively, which according to Fig. 2, may vary with different modulation schemes. Therefore, it is necessary to evaluate the impacts of modulation schemes on EMI noise sources.

## IV. Impacts of Modulation Schemes on EMI Emission

From Fig. 2, it can be found that the switching patterns of $S_1$ and $S_4$ stay unchanged for Scheme I, Scheme II, and Scheme IV. Thus, $v_{CM1}$ and $v_{CM2}$ will also stay unchanged for these three modulation schemes. However, in Scheme III, $S_1$ and $S_4$ are switched complementarily at line frequency, which means they will not generate EMI noises, i.e., $v_{CM1} = v_{CM2} = 0$.

For Scheme I, Scheme II, and Scheme IV, the relationships among $v_{CM1}$, $v_{CM2}$, and $v_{CM}$ can be further identified. Taking Scheme I as a case, the following equation can be obtained due to the complementary switching of $S_1$ and $S_3$ ($S_2$ and $S_4$).

$$v_{a1n} = v_{an} - v_{a2n} \;\Rightarrow\; v_{CM1} + v_{CM2} = v_{CM}\,. \tag{4}$$

Due to the symmetric circuit in each phase leg, $C_{P2} \approx C_{P5}$. Under this condition, the CM noise model in Fig. 4(a) can be further simplified. Specifically, for Scheme I, Scheme II, and Scheme IV, the two paralleled CM branches of $v_{CM1}$ and $v_{CM2}$ can be combined into one, where the equivalent noise source is $(v_{CM1} + v_{CM2})/2 = v_{CM}/2$, and the equivalent CM capacitance is the summation of $3C_{P2}$ and $3C_{P5}$, i.e., $3C_{P2} + 3C_{P5} \approx 6C_{P2}$, as shown in Fig. 5(a). For Scheme III, the noise sources $v_{CM1}$ and $v_{CM2}$ can be removed as $v_{CM1} = v_{CM2} = 0$. At one moment, either $3C_{P2}$ or $3C_{P5}$ is connected to the neutral point due to the complementary switching of $S_1$ and $S_4$. Here, it is represented by $3C_{P2}$, as shown in Fig. 5(b).

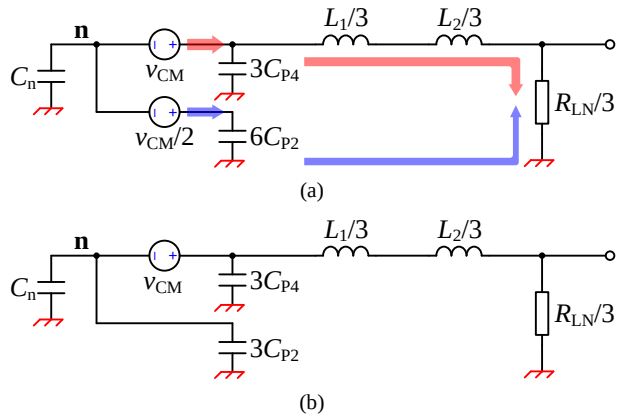


Fig. 5. Simplified CM EMI model. (a) Scheme I, Scheme II, and Scheme IV. (b) Scheme III.

TABLE I
SYSTEM PARAMETERS IN CASE STUDY

| Parameter | Symbol | Value | Parameter | Symbol | Value |
|---|---|---|---|---|---|
| DC voltage (nominal) | $V_{dc}$ | 1140 V | Inverter-side inductor | $L_1$ | 250 $\mu$H |
| Grid voltage (RMS) | $V_{g(LL)}$ | 600 V | Grid-side inductor | $L_2$ | 40 $\mu$H |
| Output power | $P_0$ | 12 kW | Filter capacitor | $C$ | 5 $\mu$F |
| Fundamental frequency | $f_0$ | 50 Hz | Switching frequency | $f_{sw}$ | 48 kHz |

Although there are two equivalent CM noise sources in Fig. 5(a), i.e., $v_{CM}$ and $v_{CM}/2$, their impacts on the EMI emission are opposite. As indicated by the lines with arrow, the CM currents generated by these two noise sources are partly cancelled out at the testing terminal, which helps to reduce the CM EMI noise measured by LISN. Therefore, it can be concluded that:

- The CM EMI emission is the same for Scheme I, Scheme II, and Scheme IV, which is lower than that in Scheme III.
- The DM EMI emission is the same for the four modulation schemes.

## V. CASE STUDY

To verify the theoretical analysis, a case study is presented in this section. The system parameters are listed in Table I. For the PV inverter, the maximum DC input voltage is 1500 V, and there is a DC voltage operating range around a nominal value, which is set as $V_{dc}$ = 1140 V.

The *LCL* filter is designed with well-known constraints [17], [22]. Specifically, $L_1$ = 250 $\mu$H is obtained for an average current ripple of 23% of the rated peak current, $C$ = 5 $\mu$F is designed to limit the reactive power to 5% of the rated output power, and $L_2$ = 40 $\mu$H is set to attenuate the switching harmonics to 0.3% of the rated peak current.

Figs. 6 and 7 give the measured EMI noise spectra at the testing terminal. For the CM noise, as shown in Fig. 6, almost the same spectra are obtained for Scheme I, Scheme II, and Scheme IV, and they are nearly 20 dB lower than that in Scheme III. For the DM noise, as shown in Fig. 7, the same spectra are observed for the four modulation schemes. Simulation results verify the theoretical analysis.

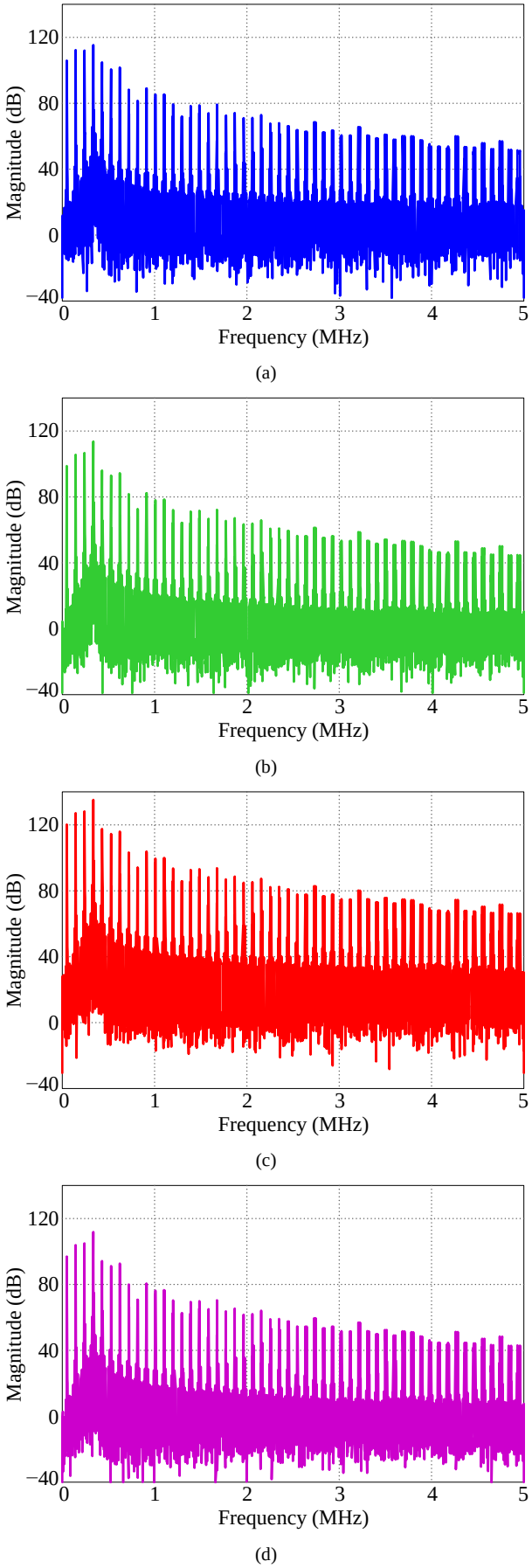


Fig. 6. Measured CM EMI noise spectra by LISN. (a) Scheme I. (b) Scheme II. (c) Scheme III. (d) Scheme IV.

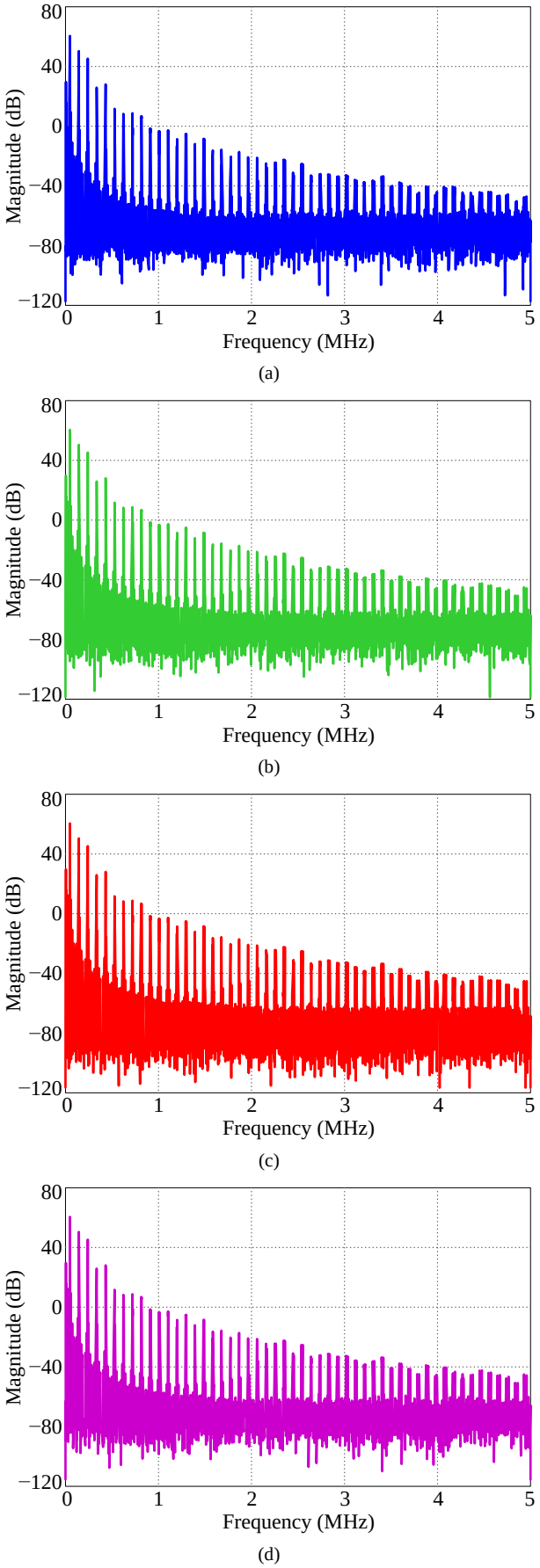


Fig. 7. Measured DM EMI noise spectra by LISN. (a) Scheme I. (b) Scheme II. (c) Scheme III. (d) Scheme IV.

## VI. Conclusions

In this paper, EMI modeling of the 3L-ANPC SiC inverter has been studied under different modulation schemes. It reveals that the CM noise is the same for DNPC modulation, ANPC modulation with same-side clamping, and ANPC modulation with full-path clamping, which is lower than that in ANPC modulation with opposite-side clamping. While the DM noise is the same for all the four modulation schemes. Simulation results from a case study verify the theoretical analysis.

## References


[1] E. Serban, M. Ordonez, and C. Pondiche, "DC-bus voltage range extension in 1500 V photovoltaic inverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 4, pp. 901−917, Dec. 2015.

[2] Z. Čorba, B. Popadić, V. Katić, B. Dumnić, and D. Milićević, "Future of high power PV plants — 1500 V inverters," in *Proc. 19th International Symposium on Power Electronics (Ee)*, Novi Sad, Serbia, Oct. 2017.

[3] *True 1500 V Technology for the New Gneration of PV Power Plants*, SMA Solar Technology AG. [Online]. Available: https://www.sma.de/fileadmin/content/global/specials/1500V/Whitepap1500V-AEN1639.pdf

[4] E. Gkoutioudi, P. Bakas, and A. Marinopoulos, "Comparison of PV systems with maximum DC voltage 1000 V and 1500 V," in *Proc. IEEE 39th Photovoltaic Specialists Conference (PVSC)*, Tampa, FL, USA, Jun. 2013.

[5] R. Inzunza, R. Okuyama, T. Tanaka, and M. Kinoshita, "Development of a 1500 Vdc photovoltaic inverter for utility-scale PV power plants," in *Proc. IEEE 2nd International Future Energy Electronics Conference (IFEEC)*, Taipei, Taiwan, Nov. 2015.

[6] X. Hao, K.-W. Ma, Y. Yang, and J. Zhao, "1500 V solar inverter at megawatts level in NPC1 topology enabled by high-density IGBT module," in *Proc. IEEE Region 10 Conference (TENCON)*, Singapore, Nov. 2016.

[7] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. 17, no. 5, pp. 518−523, Sep./Oct. 1981.

[8] T. Brückner, S. Bernet, and H. Güldner, "The active NPC converter and its loss-balancing control," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 855−868, Jun. 2005.

[9] J. Rodriguez, S. Bernet, P. K. Steimer, and I. E. Lizama, "A survey on neutral-point-clamped inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2219−2230, Jul. 2010.

[10] M. Chen, H. Wang, F. Blaabjerg, X. Wang, and D. Pan, "A temperature-dependent thermal model of silicon carbide MOSFET module for long-term reliability assessment," in *Proc. IEEE 4th Southern Power Electronics Conference (SPEC)*, Singapore, Dec. 2018.

[11] M. Chen, H. Wang, H. Wang, F. Blaabjerg, X. Wang, and D. Pan, "Reliability assessment of hybrid capacitor bank using electrolytic- and film-capacitors in three-level neutral-point-clamped inverters," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2019, pp. 2826−2832.

[12] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si − evaluation of potentials for performance improvement of inverter and DC-DC converter systems by SiC power semiconductors," *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2872−2882, Jul. 2011.

[13] J. Millán, P. Godignon, X. Perpiñà, A. P.-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor

devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155−2163, May 2014.

[14] X. She, A. Q. Huang, Ó. Lucía, and B. Ozpineci, "Review of silicon carbide power devices and their applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8193−8205, Oct. 2017.

[15] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, "An experimental investigation of the trade-off between switching losses and EMI generation with hard-switched all-Si, Si-SiC, and all-SiC device combinations," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2393−2407, May 2014.

[16] Z. Fang, D. Jiang, Z. Shen, and R. Qu, "Impact of application of SiC devices in motor drive on EMI," in *Proc. IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2017, pp. 652−658.

[17] D. Pan, X. Ruan, C. Bao, W. Li, and X. Wang, "Magnetic integration of the *LCL* filter in grid-connected inverters," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1573−1578, Apr. 2014.

[18] D. Pan, X. Ruan, C. Bao, W. Li, and X. Wang, "Capacitor-current-feedback active damping with reduced computation delay for improving robustness of *LCL*-type grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3414−3427, Jul. 2014.

[19] D. Pan, X. Ruan, C. Bao, W. Li, and X. Wang, "Optimized controller design for *LCL*-type grid-connected inverter to achieve high robustness against grid-impedance variation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 3, pp. 1537−1547, Mar. 2015.

[20] D. Pan, X. Ruan, X. Wang, H. Yu, and Z. Xing, "Analysis and design of current control schemes for *LCL*-type grid-connected inverter based on a general mathematical model," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4395−4410, Jun. 2017.

[21] D. Pan, X. Ruan, and X. Wang, "Direct realization of digital differentiators in discrete domain for active damping of *LCL*-type grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8461−8473, Oct. 2018.

[22] D. Pan, X. Ruan, X. Wang, F. Blaabjerg, X. Wang, and Q. Zhou, "A highly robust single-loop current control scheme for grid-connected inverter with an improved *LCCL* filter configuration," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8474−8487, Oct. 2018.

[23] Y. Jiao, S. Lu, and F. C. Lee, "Switching performance optimization of a high power high frequency three-level active neutral point clamped phase leg," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3255−3266, Jul. 2014.

[24] D. Barater, C. Concari, G. Buticchi, E. Gurpinar, D. De, and A. Castellazzi, "Performance evaluation of a three-level ANPC photovoltaic grid-connected inverter with 650-V SiC devices and optimized PWM," *IEEE Trans. Ind. Appl.*, vol. 52, no. 3, pp. 2475−2485, May/Jun. 2016.

[25] H. Zhang, L. Yang, S. Wang, and J. Puukko, "Common-mode EMI noise modeling and reduction with balance technique for three-level neutral point clamped topology," *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 7563−7573, Sep. 2017.