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***Abstract*— This paper proposes a physics-level modeling method for analyzing the primary to secondary-side (common-mode) parasitic capacitance of the transformer for the Medium-voltage SiC MOSFETs gate drivers. The lumped circuit-based physics-model of the turn-to-turn capacitance, turn-to-core capacitance, and self capacitance of the core are derived, and it is found that the turn-to-core capacitance mainly contributes to the total equivalent parasitic common-mode capacitance. The measured common-mode impedance of the transformer shows high agreements with the calculated value, where the accuracy of the proposed modeling method can be proved based on the experimental results.**

Keywords—common-mode capacitance, SiC MOSFETs gate drivers, lumped circuit-based physics-level model, turn-to-core capacitance.

I. INTRODUCTION

Medium-voltage (MV) converters are getting increased attention as a grid interfaces to the MV power grids (1 kV- 35 kV) with typical line-to-line voltages of 3.3 kV, 4.16 kV, 6.6 kV, and 10 kV. Thanks to the recent advances in SiC Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), the blocking voltage for the Wolfspeed 3rd generation SiC MOSFET dies have been increased to 10 kV and 15 kV [1] which makes it possible to design the MV converters by using the simple two-level voltage source converter (VSC) topology. However, due to the high *dv*/*dt* operations of SiC MOSFETs, the parasitic elements of active and passive components utilized in the converters should be considered and analyzed [2].

Gate drivers play an important role in providing reliable and continuous operation for the semiconductor switches. The high *dv/dt* switching transient causes the transient common-mode (CM) current to flow through the high side gate driver in a two-level VSC, which may result in the false turn-on switching instant and disturb the reliable operations of gate driver ICs and power supply controller [3].

It is known that the CM capacitance of the gate driver is majorly contributed by the parasitic primary to secondary side capacitance of the high voltage isolation transformer of the DC-DC power supply [3]. The peak amplitude of the CM current is in direct proportion to the transformer CM capacitance and therefore larger CM capacitance of the transformer will contribute to the increased transient CM current [4].

Several modeling methods are reported for modeling the CM capacitance of transformers. In [5] the authors proposed an accurate equivalent circuit model of the transformer by measuring the impedance between the terminals separately. In [6] the physics-based model of inductors for calculating the theoretical parasitic capacitance based on the energy conservation law was derived, where the electrical potential difference between the two analyzed terminals was assumed to be known. However, how to accurately and reasonably define the voltage drop between the two terminals of the analyzed capacitor is still a challenge for this type of modeling method [7].

Another popular physics-based modeling method is built on the lumped circuit-based modeling of the electromagnetic devices [8, 9]. This type of modeling method does not require any prior knowledge of the voltage potential difference between the analyzed terminals, but the disadvantage of this method is that the total equivalent capacitance is calculated by solving the complex lumped circuit models.

J. Biela et al. comprehensively review the physics-based modeling methods for calculating the stray capacitance of transformers and they indicate the CM capacitance of the transformer is majorly contributed by the primary-side layer to secondary-side layer capacitance [10]. However, for the transformers utilized in gate drivers, A. Anurag et al. in [4] point out that the CM capacitance is majorly contributed by the capacitance from the winding to the core. Since the derivations of the physics-based models are based on the geometrical structure, these models are useful for the optimized design of the transformer [7].

None of the known papers have physically modeled the parasitic CM capacitance of the transformer by considering the turn-to-core capacitance. In order to fill this gap, the geometry-based physics-level models of parasitic capacitances are derived in this paper, to develop the theoretical model for the transformer parasitic capacitances. Then, an efficient and simple method is proposed for calculating the total equivalent parasitic CM capacitance of the transformer by simplifying the complex

lumped circuit model. The valid frequency range of the proposed method is also given in this paper. Finally, the experimentally measured impedance of the transformer is compared with the calculated equivalent parasitic CM capacitance to validate the accuracy of the proposed modeling method.

II. MV SiC MOSFETs Gate Driver Power Supply

Fig. 1 shows the schematic of the designed gate driver power supply, which has been introduced in detail in [3]. A flyback converter is used for supplying the voltage to the gate driver IC. A high-frequency and high isolation voltage toroidal core transformer is used in the designed flyback converter.

It is known that one of the biggest challenges for designing the gate drivers prone to high dv/dt switching transients is the CM current due to the transformer primary to secondary side (CM) parasitic capacitance. Based on $i = C \cdot dv/dt$, the CM current will be smaller for the smaller value of the CM capacitance [3, 4]. Therefore, it is meaningful to have a physics-based model for calculating and optimizing the parasitic CM capacitance of the transformer.

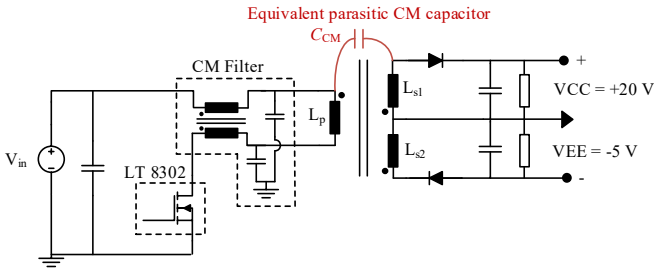


Fig. 1 Schematic of the MV SiC MOSFET gate driver power supply [3]

III. Modeling of Parasitic Capacitance

The parasitic capacitances of the transformer include turn-to-core capacitance C_{tc}, turn-to-turn capacitance C_{tt} and self capacitance of the core C_{core}. A toroid-type core transformer (primary side: 2 turns, secondary side: 2 turns) is selected as an example in this section. The equivalent circuit including the parasitic elements for the analyzed transformer is presented first, after which, the theoretical equations for the parasitic capacitances are derived.

A. Key assumptions

Several key assumptions have been made for the modeling, which are the same assumptions as in [8, 9] and are summarized below:

1) The inductance and parasitic capacitance are linear, and not voltage and frequency-dependent. The reactance of the parasitic capacitance is infinite and doesn't affect the performance of the inductance at low frequency [8].

2) The elementary parasitic turn-to-turn, turn-to-core capacitances, and inductances in one turn can be represented as a single equivalent turn-to-turn, turn-to-core capacitance, and inductance [8, 9].

3) The elementary capacitance between two adjacent turns or between the turn-to-core can be an equivalent series combination of several elementary capacitors, each with uniform dielectric material [9].

4) The lines of the electrical field are orthogonal to the conductor surfaces. The length of the electrical field in coatings and bobbins is considered to be equal to the thickness of the respective material. The length of the electrical field in the air gap is assumed to be the shortest distance between the two calculated points [8, 9].

5) The efficient angle range for integration is selected as $-\pi/2$ to $\pi/2$, which is the same as Ref. [9].

B. The equivalent circuit for the toroidal core transformer with parasitic elements

A toroidal core transformer with two turns in each side is selected as an example in this section. The schematic of the researched transformer with parasitic elements is shown in Fig. 2, where L_{tt} and C_{tt} are the equivalent inductance and capacitance between the two neighbor turns, C_{tc} is the equivalent capacitance between the single turn and core, and C_{core} is the equivalent capacitance between the mapping points of the individual turn.

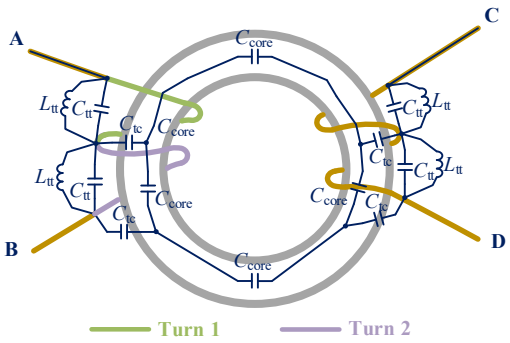


Fig. 2 Schematic of the transformer with parasitic elements

C. Modeling of turn-to-turn capacitance

In a cross-sectional view as shown in Fig. 3, the capacitance between the two neighbor turns (Turn 1 and Turn 2) can be expressed as a series combination of several equivalent capacitances between the two conductors [8, 9].

Based on the [8, 9], the equations of $C_c(\theta)$ which is the equivalent elementary capacitance between the conductor and insulated coating and $C_{g1}(\theta)$ which is the equivalent elementary capacitor between the two turns contributed by the air gap with per unit angle can be given as

$$dC_c(\theta) = \varepsilon_r \varepsilon_0 d\theta \int_0^{l_t} dl \int_{r_0}^{r_c} \frac{r}{dr} = \frac{\varepsilon_r \varepsilon_0 l_t}{\ln \frac{r_0}{r_c}} \quad (1)$$

$$dC_{g1}(\theta)=\frac{\varepsilon_0\int_0^{l_t}dl}{p_1+2x_1(\theta)}r_0d\theta=\frac{\varepsilon_0 l_t r_0}{p_1+2r_0(1-\cos\theta)} \quad (2)$$

where r_c is the diameter of the conductor, r_0 is the diameter of the conductor with coating, p_1 is the air gap between the two turns, l_t is the length of one turn, ε_r is the relative permittivity of the coating of turns, and ε_0 is the vacuum permittivity. For any angle θ, there exists a corresponding element equivalent capacitance.

The equivalent elementary capacitance $C_{tt}(\theta)$ between the Turn 1 and Turn 2 can be presented as

$$dC_{tt}(\theta)=dC_c(\theta)//dC_{g1}(\theta)//dC_c(\theta) \quad (3)$$

where the symbol "//" represents the mathematical calculation symbol for the capacitances in series.

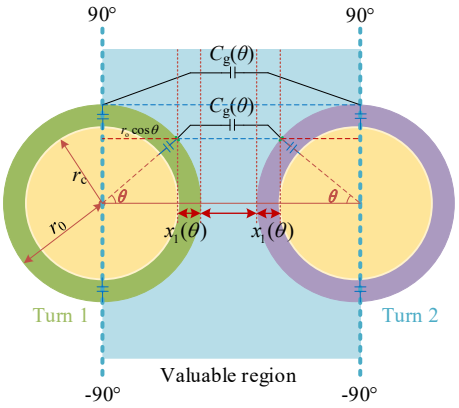


Fig. 3 Schematic of the two adjacent turns with parasitic elements in 2-Dimension

Integrating the Eq. (3) from -90° to +90° [9], the equivalent turn-to-turn capacitance can be expressed as

$$C_{tt}=\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}}dC_{tt}(\theta) \quad (4)$$

D. Modeling of turn-to-core capacitance with bobbins

In [8], the turn-to-core capacitance is calculated to be twice of the measured capacitance, based on the assumption that there is no air gap between the turn and the core. For the modern power electromagnetic devices, bobbins, core coating, and even more complex structures are designed. In this section, the turn-to-core capacitance models considering the impacts of bobbins and core coating are derived.

In practice, there is an insulated coating on the surface of the toroid core. The thickness of this coating is usually large so that its impact on capacitance cannot be neglected. Therefore, Case B is aimed to illustrate the parasitic turn-to-core capacitance with both bobbins and core coating. The turn-to-core capacitance, in this case, can be presented in a cross-sectional view as shown in Fig. 4. $C_{g2}(\theta)$ is the equivalent elementary capacitor contributed by the airgap, $C_b(\theta)$ is the equivalent elementary capacitor contributed by the bobbins, and $C_i(\theta)$ is the equivalent elementary capacitor contributed by the coating of the core.

The extra elementary capacitance contributed by the core coating and the bobbin with per unit angle can be presented as

$$dC_i(\theta)=\frac{\varepsilon_i\varepsilon_0\int_0^{l_t}dl}{l_i}r_0d\theta \quad (5)$$

$$dC_b(\theta)=\frac{\varepsilon_b\varepsilon_0\int_0^{l_t}dl}{l_b}r_0d\theta \quad (6)$$

$$dC_{g2}(\theta)=\frac{\varepsilon_0\int_0^{l_t}dl}{p_2+x_2(\theta)}r_0d\theta=\frac{\varepsilon_0 l_t r_0}{p_2+x_2(\theta)}d\theta=\frac{\varepsilon_0 l_t r_0}{p_2+r_0(1-\cos\theta)} \quad (7)$$

where l_i is the thickness of the core coating, ε_i is the relative permittivity of the coating of the core.

Therefore, the total elementary capacitance per angle can be expressed as

$$dC_{tc}(\theta)=dC_c(\theta)//dC_{g2}(\theta)//dC_b(\theta)//dC_i(\theta) \quad (8)$$

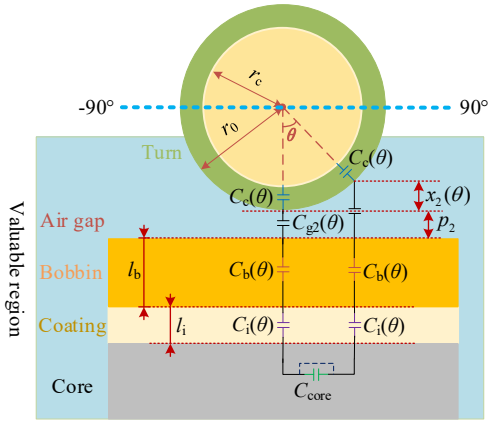


Fig. 4 Schematic representation of the turn-to-core capacitance in 2-Dimension considering bobbins and coating of the core elements (C_{core} can be neglected in most situations)

Integrating the Eq. (6) from -90° to +90°, the equivalent turn-to-core capacitance can be obtained as

$$C_{tc}=\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}}dC_{tc}(\theta) \quad (9)$$

E. Modeling of the self-capacitance of the core

Considering the two cross-sections A and B of the toroid core is presented in Fig. 5, the total equivalent capacitance C_{core} can be expressed as a parallel combination of the two separate capacitors (C_{core1} and C_{core2}). C_{core1} is the capacitor contributed by the minor circle, and C_{core2} is the capacitor contributed by the major circle on the core as shown in Fig. 5.

The total capacitance can be expressed as

$$C_{core} = C_{core1} + C_{core2} \tag{10}$$

C_{core1} and C_{core2} can be approximately expressed as

$$C_{core1} \approx \frac{\varepsilon_0 \varepsilon_c wh}{l_{c1}}, \quad C_{core2} \approx \frac{\varepsilon_0 \varepsilon_c wh}{l_{c2}} \tag{11}$$

where ε_c is the relative permittivity of the core, l_{c1}, and l_{c2} are the average lengths from points A to B of the minor arc and major arc respectively.

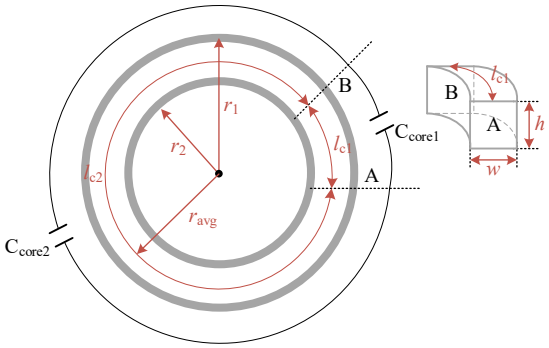


Fig. 5 Schematic representation of the self-core capacitance between surface A and B

IV. Calculation of CM Capacitance

In practice, one of the methods to obtain the CM capacitance of transformers is to measure the impedance between the primary and secondary side winding using an impedance analyzer.

In Fig. 2, A and B are the two ends of the primary winding, C and D are the two ends of the secondary winding. If the terminals A and C are connected to the impedance analyzer, and the terminals B and D are left floating, then the equivalent schematic can be represented as shown in Fig. 6.

While the signal is injected at the Terminal A, and the Terminal B is floating, the circuit of the primary side can be divided into the two identical sub-circuits.

For one of the sub-circuits shown in Fig. 6, the impedance between the Rp1 and Rp2 can be written as

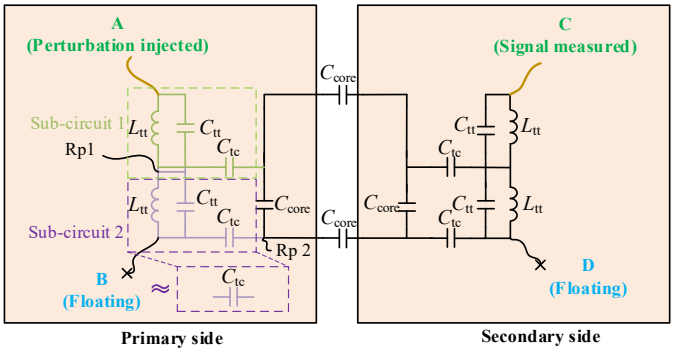


Fig. 6 The equivalent CM impedance between the terminals A and C of the toroidal transformer

$$\begin{aligned} Z_{RP1\_2} &= (Z_{Ltt} // Z_{Ctt}) + Z_{Ctc} \\ &= \frac{j\omega L_{tt} \times \frac{1}{j\omega C_{tt}}}{j\omega L_{tt} + \frac{1}{j\omega C_{tt}}} + \frac{1}{j\omega C_{tc}} \end{aligned} \tag{12}$$

If the frequency range of Z_{RP1_2} below $0.1 \times w_{tt}$, where w_{tt} is the characteristic frequency of the paralleled circuit of L_{tt} and C_{tt}, the Z_{RP1_2} can be rewritten as

$$Z_{RP1\_2} \approx j\omega L_{tt} + \frac{1}{j\omega C_{tc}}, \quad \omega \le 0.1 \times \frac{1}{\sqrt{L_{tt} C_{tt}}} \tag{13}$$

In further, if the frequency range of Z_{RP1_2} is also below $0.1 \times w_{tc}$, where w_{tc} is the characteristic frequency of the L_{tt} and C_{tc} in series, the Z_{RP1_2} can be further simplified into

$$Z_{RP1\_2} \approx \frac{1}{j\omega C_{tc}}, \quad \omega \le 0.1 \times \min\left(\frac{1}{\sqrt{L_{tt} C_{tt}}}, \frac{1}{\sqrt{L_{tt} C_{tc}}}\right) \tag{14}$$

Besides that, the relative permittivity of the core material is usually much higher than the relative permittivity of the insulating material and bobbins. According to the reference [10], the relative permittivity of the MnZn core is 2×10^5 at 0.1 MHz, whereas the relative permittivity of the core enabled by NiZn core is 50 at 0.01 MHz.

For the MnZn core, the capacitance C_{core} can be regarded as short since C_{core} is much larger than the C_{tc}. Then the simplified equivalent circuit of transformer for calculating the CM capacitance can be presented as Fig. 7.

Based on the simplifications, the CM capacitance calculated from terminal A to terminal C can be presented as

$$C_{CM} = \frac{nm}{n+m} C_{tc}, f \le 0.1 \times \min\left(\frac{1}{2\pi\sqrt{L_{tt} C_{tt}}}, \frac{1}{2\pi\sqrt{L_{tt} C_{tc}}}\right) \tag{15}$$

where n is the number of turns of the primary winding, m is the number of turns of the secondary winding, f is the valid frequency range which is smaller than the minimal characteristic frequency of the windings.

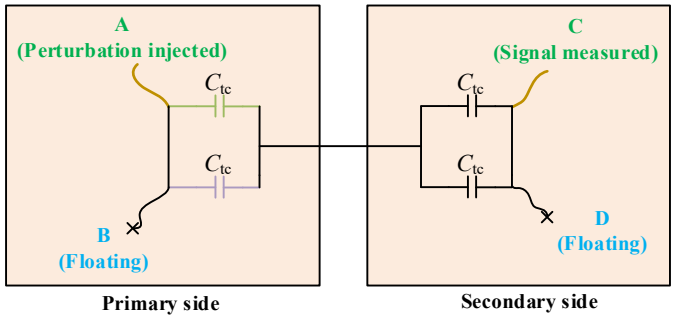


Fig. 7 The simplified equivalent CM impedance between the terminal A and C of the transformer

According to the Eq. (13), for the certain frequency range, the value of CM capacitance of transformer is only related to the

primary side and secondary side number of turns and the equivalent turn-to-core capacitance.

V. Case Study and Experimental Results

The key parameters of the designed transformers are listed in Table I.

Table I: Key parameters of the researched transformers

Parameters	Value
Core material [11]	3F3
Primary-side turns	5
Secondary-side turns	10
Relative permittivity of the turn coating [12]	3.3
Relative permittivity of the core coating [13]	4.0
Relative permittivity of the bobbins [14]	2.7
Relative permittivity of core @ 0.1 MHz [11]	MnZn = 2×10^5
Size of core [11]	Dia. 32 mm Inner Dia. 19 mm Thick. 13 mm
Thickness of the core coating [11]	0.3 mm
Diameter of the conductor	0.65 mm
Diameter of the conductor including insulation	0.85 mm
Inductance factor (Al) [11]	2270 nH/per turn

The magnetizing inductance for primary and secondary side windings are calculated as 11.35 uH and 22.7 uH per turn respectively. The triple-insulated wire is used for winding the transformer, which has a breakdown voltage rating of 15 kV.

Since the relative permittivity of the core is much larger than the relative permittivity of the bobbin and coating, the equivalent capacitance of C_{core} is very high and can be regarded as a short based on the analysis presented Section IV.

The CM impedance of the designed transformer is measured by the impedance analyzer E4990A using an adaptor 16047 from Keysight Technologies. The image of the test set up for experimental measurements is shown in Fig. 8.

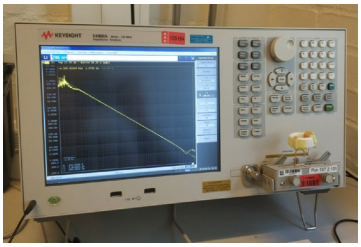


Fig. 8 Image of the experimental test setup

The picture of the designed transformer with bobbins is shown in Fig. 9(a). The schematic diagram of the core with bobbins is shown in Fig. 9(b).

The measured average length of the single turn is 5.1 cm. The air gap length between the turn and core is measured using the caliper, and the average length is calculated as 0.36 mm. The theoretical CM capacitance can be obtained by calculating the several capacitors in series combination, due to the different thickness and width of bobbins.

Thus, according to Eq. (9), the theoretical turn-to-core capacitance C_{tc} can be calculated as

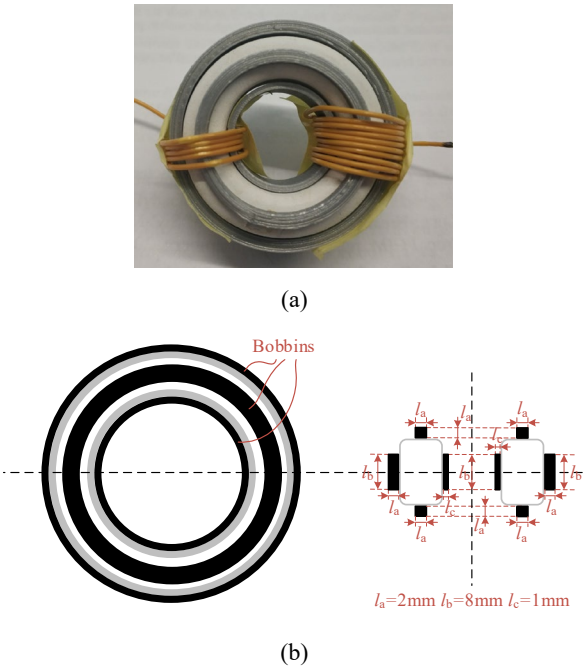
$$C_{tc} = 0.32 \text{ pF} \tag{16}$$

For the frequency range of up to $0.1\times f_c$ (2.4 MHz), the calculated parasitic CM capacitance is shown in Eq. (17) based on Eq. (15).

$$C_{CM} = 1.07 \text{ pF} \tag{17}$$

The measured and calculated impedance for the CM capacitance for the transformer with bobbins are compared in Fig. 10.

According to Fig. 10, the calculated impedance matches the measured impedance up to the frequency range of 2.4 MHz.



(a)

(b)

Fig. 9 (a) The image and (b) schematic for the transformer design with bobbins

Due to the capacitive coupling of the PCB, the total CM capacitance of the gate-driver is measured as 3 pF. For comparing, Table II gives the comparisons of the CM capacitance among the designed transformer and other commercial products with MV insulation. According to the comparisons, the designed low CM capacitance transformer helps to significantly reduce the total CM capacitance of the power supply for the gate driver.

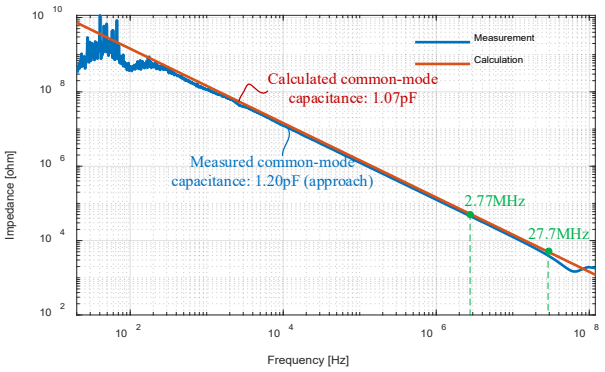


Fig. 10 The measured impedance and calculated equivalent parasitic CM capacitance (with bobbins)

Table II: The comparisons of the CM capacitance among the designed transformer and commercial productions

	CM capacitance
Designed transformer	1.2 pF
Gate driver with the designed transformer	3 pF
Concept ISO5125I DC-DC power supply[15]	4 pF
RECOM REC6/R DC-DC power supply[16]	20 pF
Concept Scale 2 1SC0450 gate driver[17]	8 pF

VI. Sensitivity Analysis of Assumptions

In this paper, the permittivity and permeability of materials are found from the datasheet, technical report, and previous publications. However, none of them is constant, and most of them vary with frequency, temperature, current and voltage. The measured or estimated length of the geometrical structure may also introduce some error to the calculated results.

The sensitivity of two parameters is discussed in detail, which is the estimated length l_{tb} between the turn and bobbin and integrating angle range θ.

Table III presents the calculated results with the fixed integrating angle (from $-\pi/2$ to $\pi/2$) and different estimated length l_{tb}. It can be found that there is a 16% difference between the calculated capacitance with l_{tb} = 0.1 mm and l_{tb} = 0.36 mm. The best fit results when l_{tb} is equal to around 0.2 mm.

Table III: The comparisons of the CM capacitance of transformer for a different turn-to-core length

	l_{tb} = 0.1mm	l_{tb} = 0.2mm	l_{tb} = 0.36mm	Meas.
Cap.	1.27 pF	1.18 pF	1.07 pF	1.2 pF

Table IV presents the calculated results with fixed estimated length l_{tb} = 0.22 mm and different integrating range (from $-\pi/2$ to $\pi/2$, $-\pi/3$ to $\pi/3$, $-\pi/6$ to $\pi/6$).

Table IV: The comparisons of the CM capacitance of transformer with different integrating angle ranges

	$-\pi/2$ to $\pi/2$	$-\pi/3$ to $\pi/3$	$-\pi/6$ to $\pi/6$	Meas.
Cap.	1.07 pF	0.75 pF	0.39 pF	1.2 pF

It can be found that the calculated capacitance is smaller with the smaller angle range, which means the calculated capacitance is sensitive to the angle range. The best fit results when the integrating angle range is even wider than $-\pi/2$ to $\pi/2$. It is worth noting that the integrating angle range might be different for different practical applications.

VII. Conclusions

This paper proposes a complete modeling method for calculating the equivalent transformer CM mode parasitic for MV SiC MOSFETs gate drivers. The turn-to-turn, turn-to-core, and self- capacitance of the core are modeled considering several practical problems. A novel simplified method is used for calculating the equivalent parasitic CM capacitance in a certain frequency range, where the frequency range is determined based on the minimal characteristic frequency of the system. A transformer low CM capacitance is examined using the proposed modeling method, and it is found that the major CM capacitance of the transformer is contributed by the turn-to-core capacitance in the valid frequency range. The experimental results show good agreements with the theoretical analysis. The theoretical analysis and experimental results also prove that the transformers with bobbins have 1.1 pf-1.2 pF CM capacitance, which is a significant improvement compared to the previous research [3]. The total capacitance of gate driver with the designed transformer is 3 pF, respectively, which are considerably smaller compared to the commercial productions in 10 kV voltage class [15 - 17].

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