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System and Circuit Design Aspects for CMOS Wireless Handset Receivers

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TITLE

System and Circuit Design Aspects for CMOS Wireless Handset Receivers

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ABSTRACT

The work documented in this dissertation deals with system and circuit design aspects for *Complementary Metal Oxide Semiconductor* (CMOS) implementations of wireless handset receivers. The work has been divided into three parts: Part I of the dissertation is concerning CMOS as an RF technology, Part II deals with receiver architectures on a system level, and Part III considers RF circuit and device implementations in CMOS. Through comparison a historic background to the use of CMOS in cellular applications is provided. The tremendous developments in CMOS technology are considered and the analog short-comings are evaluated. The lack of high quality passive devices, inductors in particular, is found to be one of the major obstacles in achieving a fully integrated RF design based on CMOS. Part II starts with an overview of different receiver architectures and a discussion of some fundamental problems in relation to CMOS integration. Based on the standards provided for *Universal Mobile Telephone System* (UMTS) requirements are derived for a UTRA/FDD (UMTS Terrestial Radio Access - Frequency Division Duplex) direct-conversion receiver. The direct-conversion receiver is chosen in spite of the well-known problem with DC-offset. The wideband nature of the UMTS signal opens up for simple DC-offset cancellation schemes. In line of this the effect of highpass filtering as a means to reduce the DC-offset is pursued. Based on link-simulations a correlation between DC-offset cancellation and *Bit Error Ratio* (BER) is established. To be used in the receiver planning it is found that a third to fourth order Butterworth filter provides sufficient DC-offset cancellation while degrading E_b/N_0 only by 0.2 – 0.3dB. When an implementation performance surplus is available it is common practice to simplify receiver planning and employ a full separation of different distortion mechanisms. This approach is not an option when a low-cost silicon technology is the target. For a UTRA/FDD receiver the disturbance scenario is complicated as a consequence of continuos transmission and reception. To manage this a simple voltage domain approach to receiver planning is presented. The method allows all interferring components to be considered simultaneously whereby a more optimum receiver design results in comparison with traditional calculations based on manual distribution of distortion effects. Aiming for CMOS implementation the UTRA/FDD requirements are used to specify requirements for all receiver stages in the direct-conversion receiver. Having requirements for both low noise and especially high linearity the mixer stands out as one of the more challenging blocks and has therefore been selected for CMOS implementation in Part III. A modified Gilbert cell mixer topology forms the basis for the quadrature mixer design. The modification is shown to have a 3dB noise advantage over traditional quadrature mixers. As a drawback the mixer is sensitive towards imbalance in the LO voltage levels and for that matter it is necessary to have an accurate LO feed. For direct-downconversion mixers LO leakage represents a significant source to performance degradation. Due to antenna-like characteristics and typically large areas the inductor is especially prone to crosstalk. To minimize the coupling to and from inductors the traditional approach is to surround these by guard-ring structures. While guard-rings improve isolation they also form a trade-off between device area and performance. The relation between guard-ring area and inductor performance is evaluated and it is shown that, depending on the size of the guard-ring, the Q-value reduction may be as high as 16% at 2GHz. In continuation of this, various coupling effects for CMOS on-chip co-planar spiral inductors are presented. Simple guard-rings are shown to improve isolation between closely spaced adjacent inductors by approximately 10-15dB. At larger distances the gain of having a guard-ring reduces and is eventually found to be zero at a distance of 1000μm. For modeling purposes an extended lumped element model is proposed and found to fit very well with measurements.

TITEL

System- og Kredsløbs-designaspekter vedrørende CMOS Håndsæt til Trådløs Kommunikation

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RESUMÉ

Arbejdet dokumenteret i denne afhandling omhandler aspekter af system og kredsløbsdesign for trådløse modtagere og implementering af disse i *Complementary Metal Oxide Semiconductor* (CMOS) teknologi. Arbejdet er delt op i tre dele, hvoraf del I omhandler RF egenskaberne for CMOS teknologi, del II omhandler radio-modtagere på arkitekturnivau, og del III omhandler implementation af RF kredsløb og komponenter i CMOS teknologi. Gennem sammenligninger præsenteres et historisk forløb, hvor anvendelsen af CMOS til implementering af trådløse applikation er i fokus. Den intense udvikling CMOS har gennemgået beskrives, og begrænsningerne i forhold til analog kredsløbsdesign vurderes. Her viser det sig at, manglen på spoler med tilstrækkelig høj Q-faktor er en af de væsentligste problemer i forhold til at kunne realisere fuldt integrerede RF kredsløb i CMOS. Del II starter med en gennemgang af forskellige modtager-arkitekturer og en diskussion af deres fundamentale problemer i relation til en integration i CMOS. Ud fra standarderne for *Universal Mobile Telephone System* (UMTS) udledes kravene til en direct-conversion-modtager til UTRA/FDD (UMTS Terrestial Radio Access - Frequency Division Duplex) systemet. Direct-conversion-modtageren vælges til trods for det velkendte problem med DC-offset. Den store båndbredde anvendt i UMTS gør det muligt at anvende simple teknikker til reduktion af DC-offset. I forlængelse af dette undersøges

det om højpas-filtrering er en farbar vej til reduktion af DC-offsettet. Baseret på link-simulering etableres en sammenhæng mellem DC-offset-reduktion og bitfejl-sandsynlighed (BER). Til brug i den efterfølgende modtager-designfase afdækkes, at et tredie- eller fjerde-ordens Butterworth filter giver tilstrækkelig reduktion af DC-offsettet samtidig med at E_b/N_0 kun reduceres med 0.2 – 0.3dB. Forudsat at den anvendte implementeringsteknologi kan levere et performanceoverskud, er det normal praksis at simplificere modtager designet ved at betragte de forskellige forstyrrende mekanismer seperat. Denne praksis er ikke mulig når en low-cost Silicium-implementering er målsætningen. I UTRA/FDD-systemet foregår signal-transmission og modtagelse samtidigt hvilket øger kompleksiteten af modtager-designopgaven. Til håndtering af dette benyttes en fremgangsmetode, der bygger på spændingsdomæne-beskrivelser. Metoden gør det muligt at betragte samtlige forstyrrende signaler samtidigt, hvorved et mere optimalt modtagerdesign kan opnås til sammenligning med traditionelle teknikker baseret på en manuel fordeling af de forstyrrende effekter. Med en implementering i CMOS for øje specificeres kravene til alle modtagerblokke i en direct-conversion-modtager ud fra UTRA/FDD-kravene. Med krav om både lav støj og høj linearitet skiller mixeren sig ud som en udfordrende blok, hvorfor denne vælges til implementering i del III. Her danner en modificeret Gilbert-cell-mixer basis for et quadratur-mixerdesign. Modifikationen vises at have en støjfordel på 3dB i sammenligning med mere traditionelle implementeringer. En ulempe ved den valgte topologi er, at den er følsom overfor ubalance i LO-signalet. For en direct-conversion-modtager er LO-overhør en væsentlig kilde til performancereduktion. På grund af dens antennelignende udformning og relativt store størrelse er spolen særdeles tilbøjelig til skabe overhør. For at minimere overhør til og fra spoler benyttes normalt guard-ringstrukture. Udover at reducere overhør medfører guard-rings også et trade-off mellem komponent-areal og performance. Sammenhængen mellem guard-ringareal og spole-performance analyseres og det vises, at afhængig af størrelsen på guard-ringen, kan reduktionen i Q-faktor være helt op til 16% ved 2GHz. I forlængelse af dette gennemgås forskellige kilder til overhør og det vises, at simple guard-rings kan reducere overhør mellem tætplacerede spoler med omkring 10 – 15dB. Ved større afstande reduceres effekten af guard-ringen og for en afstand på 1000μm ses ikke længere nogen effekt. Til anvendelse i simuleringer foreslås en model baseret på passive komponenter, og modellen viser sig at stemme særdeles godt overens med målinger.

Preface

This dissertation is submitted to the Faculty of Technology and Science at Aalborg University in partial fulfillment of the requirements for the PhD degree. The work has been carried out in the Department of Communication Technology, at Institute of Electronic Systems, at Aalborg University.

The work presented in the dissertation is part of a larger research project running within the *RF Integrated Systems & Circuits* (RISC) Division, also Aalborg University. The overall goal is here to exploit the characteristics of state-of-the-art CMOS processes for RF applications. To accomplish this the RISC Division conducts research on all levels of RF integrated circuit design, i.e. system, circuit, and device level. The basis of the work presented in this dissertation falls within all three research areas, a fact also reflected by the structure of the dissertation. The dissertation is divided into an introductory part and subsequently two parts that each provides an extended summary of the work done within the system level as well as the circuit and device areas.

- The first part, the introduction, presents the concept of CMOS integrated circuit design by a short historical introduction followed by an example of the current state-of-the-art for commercially available RF CMOS design. CMOS as a vehicle for digital and analog integrated circuit design is considered and a few considerations related to the much debated single-chip vision is presented. This is followed by an evaluation of the RF potential of CMOS by considering its characteristics in relation to traditional radio design metrics.

- The second part addresses the system level aspect of IC design. In particular, the system level design of receiver architectures for modern cellular system handsets. The available receiver architectures are considered. A system level design for a direct-downconversion receiver for WCDMA (UTRA/FDD) is conducted. As part of this the DC-offset problem related to the direct-downconversion receiver is addressed. A DC-offset model is presented and using this the robustness of a WCDMA signal is evaluated using link-simulations. This leads to a set of filter requirements that form a compromise between overload protection of baseband circuits and signal degradation.

- The third part of the dissertation focuses on the implementation level of RF IC design. The mixer is an essential circuit block in any direct-downconversion receiver and as a natural extension of part two, the design of a direct-downconversion mixer is the target of part three. In addition to the actual circuit design of a mixer it is essential that any unwanted signal leakage is minimized. Therefore, this part of the dissertation also considers crosstalk and minimization of this. To increase isolation between devices and circuits guard rings are often used. The use of guard rings results in either an inductor performance penalty or an additional area requirement. Using simulations and experimental set-ups the effectiveness of guard rings is evaluated. The device degradation is analyzed and different coupling mechanisms are evaluated to form a lumped element crosstalk model for the inductor-to-inductor coupling.

Including this preface the three parts form a 58 page extended summary of the work. Each part is completed with a summary and the overall achievement summary of the dissertation is provided at the end of this preface. The dissertation is based on a total of 14 selected publications, of which seven are first-authored and the remaining seven are co-authored. All 14 publications are included as part of this dissertation. The included papers span a total of six years and for that reason it should be expected that in some cases the background for certain assumptions and motivations may have changed over time.

Publications

1. J.H. Mikkelsen, "Evaluation of CMOS Front-End Receiver Architectures for GSM Handset Applications," in *IEEE International Symposium on Communication Systems and Digital Signal Processing (CSDSP)*, (Sheffield Hallam University, Sheffield, England), pp. 164–167, April 1998.

2. T.E. Kolding, J.H. Mikkelsen, and T. Larsen, "CMOS Technology Adjusts to RF Applications," *Microwaves and RF*, vol. 37, pp. 79–88, June 1998.

3. J.H. Mikkelsen, T.E. Kolding, and T. Larsen, "RF CMOS Circuits Target IMT-2000 Applications," *Microwaves and RF*, vol. 37, pp. 99–107, July 1998.

4. J.H. Mikkelsen, "CMOS Low-Noise Asymmetric Poly-Phase Filter for GSM Low-IF Radio Receivers," in *European Conference on Circuit Theory and Design (ECCTD)*, (Stresa, Italy), pp. 221–224, August–September 1999.

5. J.H. Mikkelsen, T.E. Kolding, T. Larsen, T. Klingenbrunn, K.I. Pedersen, and P. Mogensen, "Feasibility Study of DC Offset Filtering for UTRA-FDD/WCDMA Direct-Conversion Receiver," in *17th IEEE NORCHIP Conference*, (Oslo, Norway), pp. 34–39, November 1999.

6. O.K. Jensen, T.E. Kolding, C.R. Iversen, S. Laursen, R.V. Reynisson, J.H. Mikkelsen, E. Pedersen, M.B. Jenner, and T. Larsen, "RF Receiver Requirements for 3G WCDMA Mobile Equipment," *Microwave Journal*, vol. 43, pp. 22–46, February 2000.

7. P. Madsen, O.K. Jensen, T. Amtoft, R.V. Reynisson, J.H. Mikkelsen, S. Laursen, C.R. Iversen, T.E. Kolding, T. Larsen, and M.B. Jenner, "RF Requirements for UTRA/FDD Transceivers," in *Conference Proceedings for Wireless Personal Multimedia Communications (WPMC)*, vol. 1, (Aalborg, Denmark), pp. 197–202, , September 2001.

8. J.H. Mikkelsen and T.E. Kolding, "Accurate Computer-Assisted Planning of Integrated Radio Receivers," in *19th IEEE NORCHIP Conference*, (Kista, Sweden), pp. 167–172, November 2001.

9. P. Madsen, O.K. Jensen, T. Amtoft, R.V. Reynisson, J.H. Mikkelsen, S. Laursen, T.E. Kolding, T. Larsen, and M.B. Jenner, "UTRA/FDD RF Transceiver Requirements," in *Wireless Personal Communications*, vol. 23, no. 1, pp. 55–66, Kluwer Academic Publishers, October, 2002.

10. J. Bøjer, M.B. Gentsch, O.K. Jensen, J.H. Mikkelsen, K.Aa. Pedersen, and S. Lindfors, "An UTRA/FDD Direct-Downconversion Mixer in 0.25μm CMOS," in *20th IEEE NORCHIP Conference*, (Copenhagen, Denmark), pp. 259–264, November 2002.

11. N. Sainz, O.K. Jensen, and J.H. Mikkelsen, "Evaluation and Modeling of Guard Ring Related Device Performance Degradation," in *21st IEEE NORCHIP Conference*, (Riga, Latvia), pp. 228–231, November 2003.

12. J. Bøjer, M.B. Gentsch, O.K. Jensen, J.H. Mikkelsen, K.Aa. Pedersen, and S. Lindfors, "An UTRA/FDD Direct-Downconversion Mixer in 0.25μm CMOS", in *Analog Integrated Circuits and Signal Processing*, vol. 38, pp. 27–33, Kluwer Academic Publishers, January, 2004.

13. J.H. Mikkelsen, O.K. Jensen, and T. Larsen, "Measurement and Modeling of Coupling Effects of CMOS On-Chip Co-Planar Inductors," in *IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, (Atlanta, Georgia, USA), pp. 37–40, September 2004.

14. J.H. Mikkelsen, O.K. Jensen, and T. Larsen, "Crosstalk Coupling Effects of CMOS Co-Planar Spiral Inductors," in *IEEE Custom Integrated Circuits Conference (CICC)*, (Orlando, Florida, USA), pp. 371–374, October 2004.

Summary of Publications

The included papers all have CMOS implementations as a common focal point. Apart from that, the contributions aim at both system, circuit, and device levels. In the following, summaries of the papers are presented to provide an overview of the scientific contributions combined in this dissertation. The order of the paper summaries is according to the list of publications as just mentioned above.

1. **Evaluation of CMOS Front-End Receiver Architectures for GSM Handset Applications**
   The paper presents the first direct evaluation of the potential of RF-CMOS for implementing highly integrated receivers for the Global System for Mobile-communication (GSM). Also, the paper is the first to report results of RF-CMOS receiver evaluations where the performance of the data receiver is included. The two most promising architectural candidates for implementing highly integrable receivers are identified to be the direct-downconversion receiver (DCR) and the low intermediate frequency (Low-IF) receiver. Both receiver architectures are analyzed and link simulations are conducted based on contemporary CMOS performance. The simulations show that an all CMOS Low-IF receiver solution for GSM is realistic. The DCR is shown to suffer from low-frequency noise problems that lead to de-sensitization causing it to fail to meet specifications. The paper concludes that when using contemporary CMOS performance an all-CMOS Low-IF receiver is potential while the DCR presents problems that still need to be solved.

2. **CMOS Technology Adjusts to RF Applications**
   This paper is the first part of a two-part feature that takes a first look at RF CMOS technologies and circuits aiming for IMT-2000. This, the first part, provides an overview of advances in CMOS technologies and their importance in relation to analog circuit design. Normally the minimum feature size of a given technology is used as a technology performance indicator. For digital designs this is an appropriate measure as a number of important parameters is positively affected by the continuous downscaling. Traditional analog RF performance metrics, such as gain, noise and linearity are not necessarily improved in the same way. Instead the paper argues that analog improvements come from other digital improvements than downscaling. For instance, as CPU speeds enter the 1 - 2GHz range, design techniques previously considered to be exotic analog techniques are finding way into digital designs. As an example, to reduce interconnect resistivity the use of copper is considered as a replacement of alumina and to ease interconnectivity in extremely dense digital designs several metal layers are needed. Both of these, in principle, digital improvements have direct effect on analog circuit performance as the potential inductor performance is significantly improved. Despite such improvements the paper argues that the major limitation is related to the low-resistivity substrate. An overview of the achievable RF performance for CMOS passive devices is provided to illustrate the limitations in device performance. The paper concludes that all the technological innovations are only useful as long as they maintain the low cost advantage of CMOS.

3. **RF CMOS Circuits Target IMT-2000 Applications**
   This paper is the second part of the feature looking at RF CMOS technologies and circuits aiming for IMT-2000. The paper is the first to consider the requirements for the coming 3G systems (IMT-2000) while drawing relations to the achievable RF performance of CMOS. Since IMT-2000 requirements are not yet finalized GSM-like RF requirements are expected. In that sense the step from 2G towards 3G should only be a minor

one. However, the increased bandwidth and the air interface flexibility (4MHz, 6MHz, 12MHz) impose big challenges. The paper points at the increased bandwidth as being the major challenge as the present f_T and g_m/I_D characteristics of MOS devices are more suited for narrow-band design. Some of the limitations of CMOS are that the CMOS devices introduce significant noise and distortion into the signal path. The paper identifies two very different design approaches that aim to solve this; simplicity in design and advanced signal processing. Simplicity in design implies that the number of devices used in the signal path is to be minimized – the philosophy being that fewer non-ideal components are going to provide a minimum of degradation of signal quality. In direct contrast to this, advanced signal processing may be used to mitigate the short-comings of CMOS. Here, circuit complexity is added to implement complex signal processing in the analog domain. The important point is made, that for a majority of the CMOS designs reported, the performance has been obtained in controlled environments. Stable-design innovations are required to mature CMOS to a state where packaging effects and process variations become manageable. The paper concludes that issues besides pure circuit performance must be considered to close the gab between current TDMA systems and the coming IMT-2000 system.

4. **CMOS Low-Noise Asymmetric Poly-Phase Filter for GSM Low-IF Radio Receivers**
   The key component in any low-IF receiver is the poly-phase filter. This paper provides the first comparison of different implementations of active poly-phase filters. To achieve high levels of image-rejection using traditional poly-phase filtering a high filter-order is needed. High-order filtering normally comes at the expense of increased noise levels and for that reason the paper looks at low-noise implementations. The traditional active-RC implementation is compared with two new current-mode topologies, a $G_m - C$ based implementation and a current-adder topology. For the Active-RC implementation only moderate gain may be implemented while low noise performance is preserved. Further, low noise performance and low frequency operation imply large capacitors which require a large area. For the $G_m - C$ approach the paper proposes an enhanced G_m cell with dual output whereby matching performance is improved. Based on the principle of simplicity in design the paper also proposes a poly-phase filter topology based on differential current adding. This topology improves noise performance significantly but suffers from the fact that the cut-off frequency depends on transistor matching. The paper concludes that the active-RC topology has the best signal handling performance of the three implementations. In its current implementation the $G_m - C$ topology has inferior performance compared to the two other implementations. The current-adder topology has the best noise performance and offers potential for implementing low-noise poly-phase filters even at high frequency.

5. **Feasibility Study of DC-Offset Filtering for UTRA-FDD/WCDMA Direct-Conversion Receiver**
   One of the strongest contenders for a completely integrable receiver architecture has long been the DCR. The DCR has a number of inherent short-comings with DC-offset being one of the more severe issues. This paper is the first to present a study of the DC-offset

problem for UTRA-FDD/WCDMA DCRs. The paper takes a look at the root of the DC-offset problem and provides the first reported model for DC-offset. The causes of DC-offset are characterized as being either largely time-invariant or time-variant. The largely time-invariant contributions may be mitigated in production-line calibration or through power-up calibration. For that reason the DC-offset model only considers the time-variant parts. The DC-offset model is specified in a manner that provides for a worst-case scenario with the maximum frequency content determined by the maximum Dopler shift. To prevent saturation of receiver stages following the mixer the paper shows that 60 - 80dB attenuation at 1kHz is required. Based on extensive link-simulations the paper is the first to provide an evaluation of the robustness of the WCDMA signal against removal of low frequency signal content. The paper concludes that a third to fourth order Butterworth filter with a cut-off frequency around 10kHz provides for a good compromise between BER degradation and saturation protection.

6. **RF Receiver Requirements for 3G WCDMA Mobile Equipment**
   The paper provides the first reported analysis of the RF receiver requirements for 3G WCDMA mobile equipment. Two very important considerations affect the analysis presented in the paper. First, unlike the traditional TDMA systems, the considered WCDMA system employs simultaneous transmission and reception which requires a duplex filter. Secondly, it is expected that WCDMA mobile equipment must be able to operate using the already existing 2G network. This requires a transceiver configuration capable of supporting both the TDMA and the WCDMA systems. The paper concludes that noise figure and adjacent-channel rejection requirements are not directly affected by the presence of the TX leakage signal. Considering second-order non-linearities two sources of interferers are identified; unwanted channels in the receive band and the TX leakage signal and it turns out that the TX leakage signal by far represents the worst case. In addition to the intermodulation test prescribed, the presence of the TX leakage forms and additional requirement. Any CW signal to arrive at the receiver at an offset of 67.4MHz is going to mix with the TX leakage which at an offset of 135MHz is to give third order intermodulation. This adds to the list of specifications. In conclusion, the continuing presence of a TX leakage signal complicates the task of receiver specification. However, the paper shows that a DCR with reasonable requirements is capable of meeting derived specifications when an interstage bandpass filter is used to attenuate the TX leakage signal.

7. **RF Requirements for UTRA/FDD Transceivers**
   This paper provides an extension to the work presented in publication 6. The receiver analysis is refined and a transmitter analysis is added to provide the first published requirements for a complete UTRA/FDD handset. The receiver calculations are some of the first to be published and the transmitter calculations are the first published. Based on a realistic duplex arrangement all receiver requirements are derived for the interface between the RX output of the duplexer and the input to the actual receive path. Furthermore, it is assumed that all disturbing signals that are not located at the channel frequency of the wanted signal are removed by filtering in the digital baseband part. This

implies that any distortion resulting from second order non-linearities is significantly reduced. Also, using highpass filtering to attenuate any DC-offset also improves the performance. For the transmitter analysis the standard dictates the overall requirements to EVM, ACLR and spurious emission. In addition to this, the receiver analysis adds an additional requirement by specifying the maximum amount of transmitter noise that can be tolerated in the receive band. These specifications form an overall budget for the transmitter which is used to derive requirements for the different receiver blocks. The requirements are given in terms of I/Q-imbalance, in-band ripple, LO phase noise and leakage, and compression points. It is found that a baseband filter is needed before the PA in order to meet the requirement for transmitter noise in the receive band.

8. **Accurate Computer-Assisted Planning of Integrated Radio Receivers**
   In this paper a general methodology for accurate and fast planning of integrated low-cost receivers is presented. The proposed method is based on a loop-form voltage domain extension of traditional microwave theory and the method is the first to include general selectivity and non-50Ω interface transitions in a simple and manageable way. The presented approach allows the designer to consider all interferring components simultaneously thereby optimizing the receiver planning to minimize the effect of implementation impairments. To exemplify the approach, the paper makes use of a CMOS-based UTRA/FDD RF/baseband receiver case study. The receiver is required to operate at a BER of less than 10^{-3}. To simplify the receiver planning this BER requirement is mapped into a 7dB SIR requirement. A simulation model is built for each of the different test scenarios. It is emphasized that it is important to ensure that the model includes all simultaneously active disturbance effects that contribute to the overall performance degradation. The case study shows that it is not possible to have all test scenarios exactly match the 7dB requirement but using the proposed method a close-to optimum receiver specification results where over-specification is avoided.

9. **UTRA/FDD RF Transceiver Requirements**
   This paper is a reprint of publication 7. The original paper was selected for a reprint in a special issue of Kluwer Academic Publishers *Journal of Wireless Personal Communication*. The reprint is shorter than the original paper and a major revision was therefore needed. Compared to the original paper a few changes are made; the compression point requirements are replaced with ACLR requirements and it is described how ACLR requirements for cascaded blocks may be used to calculate a resulting ACLR measure.

10. **An UTRA/FDD Direct-Downconversion Mixer in 0.25μm CMOS**
    This paper presents the design of a 2GHz direct-downconversion mixer for a UTRA/FDD receiver. The mixer is implemented using a standard low-cost 0.25μm, single-poly, six-metal CMOS process. The implemented topology is a modification of the well-known Gilbert cell mixer. To provide for a quadrature output, as required in a DCR, the mixer uses a shared differential transconductance stage as input. This approach implies that only the switching core mismatch add to imbalance in the mixer output. Compared

to a single Gilbert cell mixer, the noise performance of the proposed mixer topology is inferior when instantaneous switching is assumed. However, for non-switching LO signals the proposed topology holds a noise advantage over the Gilbert cell mixer. The usual current-source bias approach is abandoned in favor of a LC resonator. With the input stage based on a LC resonator, common-mode rejection is provided without the loss of voltage headroom. The input also includes an on-chip balun to provide a single-ended to differential transformation of the input signal. Based on measurements the mixer is found to offer a voltage gain of 15dB, a state-of-the-art noise figure of 8dB, and an iIP3 of around -1dBm.

11. **Evaluation and Modeling of Guard Ring Related Device Performance Degradation**
In this paper the importance of distance between guard ring and device is evaluated. This is done by quantifying the variations in inductor and capacitor performance for different guard ring distances. For this purpose several test structures are implemented using a 0.25μm, single-poly, five-metal layer, CMOS technology. To explain the relation between guard ring and device performance both the magnetic and the electrical fields are considered. Based on this it is argued that the guard ring is of insignificant importance for capacitor performance. This argument is supported by measurements. For inductors the situation is more complicated and 2.5D simulations are used to support and help understand measurements. The distance between inductor and guard ring is found to be of significant importance and as expected, the inductance values are found to decrease when the distance to the guard ring is reduced. Consequently, the Q-value of the device also degrades. At 5GHz it is found that a 35% reduction in component area due to reduced guard ring distance may cause a reduction of approximately 16% in Q-value.

12. **An UTRA/FDD Direct-Downconversion Mixer in 0.25μm CMOS**
This paper is a reprint of publication 10. The original paper was selected for a reprint in a special issue of Kluwer Academic Publishers *Journal of Analog Integrated Circuits and Signal Processing*. The reprint is longer than the original paper and offers the opportunity of further explanations. The receiver set-up and mixer requirements are explained in more detail and, more importantly, the mixer topology is explained in greater detail. The nature of the mixer in switching versus non-switching LO scenarios is given more attention. In a switching scenario it is explained how the proposed topology has an increased sensitivity towards LO amplitude mismatch in comparison with two separate mixers. For a sinusoidal LO input this impairment is significantly reduced. It is also explained how the quadrature topology holds a noise advantage over two separate mixers for sinusoidal LO inputs. Because of the shared input stage, noise in I- and Q-branches is correlated and consequently there is a 3dB noise advantage.

13. **Measurement and Modeling of Coupling Effects of CMOS On-Chip Co-Planar Inductors**
This paper evaluates the coupling effects between two planar inductor structures. The evaluation considers the effect of different distances between the structures and also the effect of having a guard ring or not. For this purpose an experimental set-up is

implemented using a 0.25μm, single-poly, five-metal layer, CMOS process. The test structures are also evaluated using 2.5D simulation to support measurements. The test fixtures are found to affect measurements significantly and to solve this, laser cutting is used to break an unintended coupling path. With the test fixture problem solved it is found that the coupling depends significantly on the distance between inductors. The nature of the correlation between coupling and distance is highly dependent on whether a guard ring is used or not. When using guard rings the resulting isolation is found to be independent of distance unless the inductors are placed at a very short distance to one another. For all the tested distances an isolation of approximately 30dB results. The same trend is not seen when no guard ring is used. For an increase in distance from 190μm to 290μm around 20dB of reduction is provided while an increase from 190μm to 1090μm results in approximately 35dB additional isolation.

14. **Crosstalk Coupling Effects of CMOS Co-Planar Spiral Inductors**
This paper may be considered to be an extension of publication 13. This paper builds on the same measurement set-up as publication 13 but the focus here is on the modeling of the crosstalk coupling between two planar inductors. Often crosstalk is assumed to result only from substrate carried effects. In this paper an extended model including magnetic as well as direct capacitive coupling is used to evaluate the crosstalk effects when no guard ring is used. The extended lumped model is shown to provide a very good fit to measured data for all four different distances. In contrast to previous reports the substrate-related coupling is found to have only minor effects from 10GHz to 12GHz. The direct capacitive coupling is found to have virtually no effect at all. The majority of the crosstalk coupling is found to be a result of inductive coupling between the two inductors.

Achievement Summary

As part of the work documented in this dissertation a number of contributions has been made. Some of these findings and achievements are as followingly summarized:

Part I:

- A survey of CMOS technology and its performance and shortcomings in relation to RF design requirements is provided.
- Trends and technology developments for digital IC design are put into an analog perspective.

Part II:

- A survey of receiver architectures and their characteristics from an IC implementation point of view is given.

- The direct-conversion receiver is shown to be an interesting architecture for implementing UTRA/FDD receivers, allowing for high integration and holds potential for multi-mode operation.
- A DC-offset model is developed and used to set requirements to DC-offset cancellation schemes.
- Link-level simulations are used to show that the UTRA/FDD signal may be subject to highpass filtering without significant signal-quality degradation. It is found that a third to fourth order Butterworth filter with a 3dB cut-off frequency of 10kHz provides a good compromise between DC-offset cancellation and signal degradation.
- Based on voltage domain expressions, allowing for non-50Ω impedances and receiver stage selectivity, a simple method for receiver planning is proposed. The method allows all noise and distortion components to be considered simultaneously whereby a close-to-optimum receiver planning is possible.
- An UTRA/FDD direct-conversion receiver is proposed. It is shown that the receiver is able to meet the UTRA/FDD requirements when based on block performance that seems to be within reach of CMOS.

Part III:

- A CMOS 2GHz quadrature down-conversion mixer is designed, implemented, and tested. Measured results are: 13.8dB voltage gain, 8dB noise figure, 25dBm input second order intercept point at 15MHz offset, and -3.1dBm input third order intercept point at 10/20MHz offset. These data are obtained for a supply voltage of 2.5V and a current consumption of 6mA.
- The effect of guard ring area is analyzed and shown to have significant impact on inductor performance.
- It is shown that reducing the distance between coil and guard ring from 32μm to 10μm (corresponding to an area reduction of 32%) results in 5.8% reduction in inductance values and 16% reduction in quality factor at 2GHz. At 5GHz the inductor value is found to be reduced by 8.1% and the quality factor by 15.8%.
- To determine if the use of guard rings is justified, experiments on inductor isolation are conducted to determine the degree of inductor cross-talk.
- It is shown that the test set-up for doing isolation measurements is very important. Specific problems and how to solve these are described.
- It is shown that guard rings provide around 10 – 15dB improvement in isolation for closely spaced inductors. At larger distances the improvement is shown to reduce to zero. It is found that a doubling of distance provides an additional 20dB of isolation.

- An extended lumped-component model is proposed to model the crosstalk between inductors. Mutual coupling is found to be the most significant source of crosstalk. The model provides very good fit to measurements.

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Jan Hvolgaard Mikkelsen, Aalborg, February 2005

Contents

I CMOS Technology
RF IC Design for Wireless Applications 1
1.1 A World gone Wireless 3
1.2 Integrated Circuit Design for Cellular Applications – State-of-the-art 4
1.3 Complementary Metal Oxide Semiconductor 6
    1.3-1 CMOS – a Digital IC Technology 6
    1.3-2 CMOS – an Analog IC Technology 7
1.4 Choosing the Appropriate Technology 8
    1.4-1 The Single-Chip Vision 10
1.5 CMOS as an RF Technology – Performance vs. Requirements 11
    1.5-1 High frequency gain 12
    1.5-2 Low Noise 13
    1.5-3 High Linearity 14
    1.5-4 Low Power 15
    1.5-5 Low Voltage 16
    1.5-6 Passive Devices 17
1.6 Summary 19

II CMOS Aware Receiver Planning
Receiver Architectures and DC-Offset Cancellation 21
2.1 Receiver Architectures and General Considerations 23
    2.1-1 Poly-Conversion Receivers 24
    2.1-2 Single-Conversion Receivers 26
    2.1-3 Subsampling Receivers 29
    2.1-4 Choosing the Appropriate Architecture 31
2.2 Receiver Structure for UTRA-FDD 32
2.3 DC-Offset Filtering of W-CDMA Signals 34
    2.3-1 DC-Offset Model and Cancellation 35
2.4 Receiver Planning 37
    2.4-1 Test Scenarios and Work-Flow 39
2.5 Summary 40

III CMOS Circuit and Device Design

UTRA-FDD Mixer Design and Inductor Crosstalk Issues 43

- 3.1 Mixer Design for a UTRA-FDD Direct-Downconversion Receiver 45
  - 3.1-1 Switching Core 46
  - 3.1-2 Input Stage 46
  - 3.1-3 Measurement Results 47
- 3.2 Circuit Isolation and Inductor Design Trade-off 49
  - 3.2-1 Inductor Performance and Guard-Rings 50
  - 3.2-2 Inductor Crosstalk 53
- 3.3 Summary 57

Part I

CMOS Technology

RF IC Design for Wireless Applications

"In modern wireless communication systems a given performance at a low cost is almost always preferred to improved performance at a greater cost".

L.M. Burns

Communication technology as a general concept has evolved immensely over the last couple of decades. New system concepts have been engineered and the implementation technologies have seen an almost explosive development. This part of the dissertation takes a look at the "Wireless World" concept followed by an example of state-of-the-art in RF-CMOS design today. The development of CMOS as both a digital and an analog technology is considered and the RF characteristics of CMOS are evaluated.

1.1 A World gone Wireless

There is little question that the world is going wireless. Since the mobile communication revolution started in the early 80s through the introduction of the *Nordic Mobile Telephone* (NMT) system, a wide range of systems and applications based on wireless communication has emerged. Intended as a digital replacement for NMT, the *Global System for Mobile communication* (GSM) was introduced in the early 90s as a first real attempt at a truly global communication standard [1, 2]. GSM did not succeed in becoming a global standard but it saw a significant penetration in Europe and with its 72% share of the world's wireless market it is today by far the most wide-spread cellular system [3]. Almost simultaneously with the introduction of GSM the first *Digital European Cordless Telephony* (DECT) system saw operation.

To provide for better services and especially to offer higher data rates, a second generation of GSM, the *Enhanced Data rate for GSM Evolution* (EDGE) system, was developed. With EDGE a maximum bandwidth of 384Kb is possible which is a significant improvement over GSM. With GSM being labeled as a second generation (2G) cellular system, EDGE is considered to be a 2.5G system. Even before mobile operators had started to offer EDGE based services, a third generation (3G) system was being drafted. The new system, *Universal Mobile Telephone System* (UMTS), is the second attempt for a global standard [4]. Once again political and commercial interests prevented UMTS from being a unified global standard. Instead several sub-standards have been formed and these have then been incorporated as options within the UMTS standard. There is a lot of dispute regarding the 3G system and a majority of the mobile operators has disregarded 3G and instead focuses on GSM and EDGE. In Denmark, a single operator has only recently started to offer 3G services and this with a very limited success as public interest has been very scarce. Despite the limited interest in 3G, industry and academia are already highly focused on forming and developing the next mobile communication system, the 4G system [5].

In parallel with the expansions within the area of mobile telephone communication a number of wireless computing applications has been developed. This includes applications such as *Wireless Local Area Network* (WLAN), Bluetooth, and ZigBee [6–8]. All three standards are basically intended as cable replacements offering very different bandwidths, data rates, and power consumption levels. Location applications such as the *Global Positioning System* (GPS) have been matured and fairly cheap handheld terminals have been commercially available for some years. As a further note, GPS is currently being incorporated into a number of other applications. As an example, in the United States the *Federal Communications Commission* (FCC) has an ongoing initiative (E911) to provide positioning information to for instance rescuers in emergency situations. The intention is that a positioning service with an accuracy in the order of 50m – 150m should be a required and integrated part in all new cellular phone handsets by the end of year 2005. To meet this, GPS and *Assisted-GPS* (A-GPS) in particular, is suggested [9]. This is a clear advocate for increased functionality and complexity in handheld wireless communication.

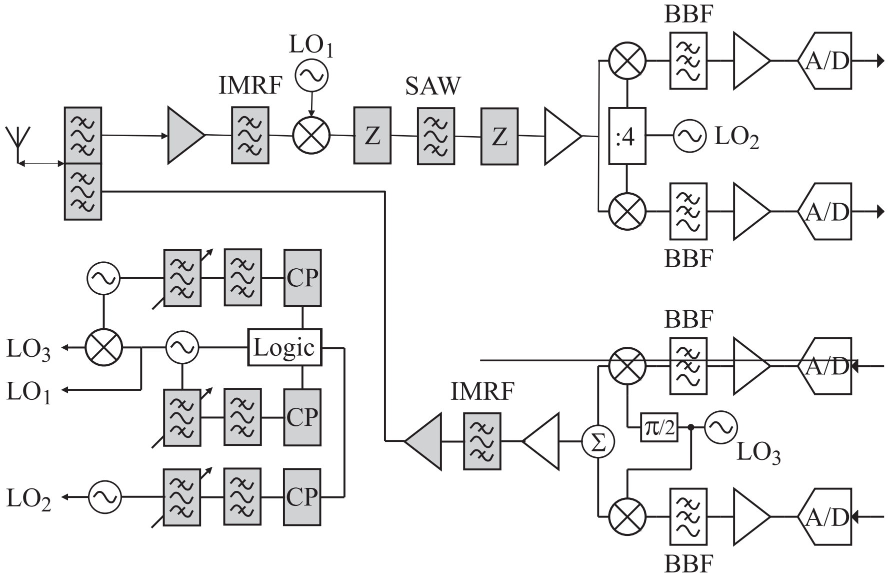
More recently the concept of a *Personal Area Network* (PAN) is being accepted as a potential scenario for a future wireless world [10]. Based on user-centricity, such PANs are to support user activities by enabling seamless and possible ad-hoc based communication to (and between) all of a user's devices capable of network connection whether at home, at the office, or in the wireless vicinity of the user. In such a scenario a vast number of wireless communication devices is to co-exist. This covers both ends of the bandwidth-scale including very low data-rate sensory nodes to very high data-rate 4G systems. For full user-centricity, a single device should enable transparent communication to and from all user devices. This calls for an unprecedented level of flexibility in the handset design.

1.2 Integrated Circuit Design for Cellular Applications – State-of-the-art

As a whole, the development in integrated circuit design has found good use in wireless applications, hand-portable communication equipment in particular. In fact, for the last 5-10 years applications based on wireless communication technology have represented the fastest growing market segment within the electronic industry [11]. During this time cellular handsets have gone from being mainly discrete implementations using hundreds of components to highly compact solutions based on three to four chips [12]. To illustrate this significant increase in system and circuit integration, an early single-chip GSM transceiver example is shown in Figure 1.1.

The design makes use of a heterodyne receiver architecture where a single intermediate frequency of 71MHz is used before the signal is downconverted to baseband. The transmitter is based on the direct-upconversion architecture where offset-LOs are used to prevent injection pulling. The extensive use of off-chip components results in a bulky and expensive implementation. Considering that even a \$2 external component may be objectionable by manufactureres, the solution in Figure 1.1 is hardly desirable. However, at the time of its introduction the implementation of Figure 1.1 took cellular handset design integration to a new level.

With cost, form factor, and a reduced *Bill of Material* (BoM) being driving factors, a majority of the high-cost components had to be eliminated. In this sense the most successful product to date is the GSM transceiver, *Aero*^{TM}, offered by Silicon Laboratories. The transceiver, illustrated in Figure 1.2 consists of three CMOS chips; a Low-IF receiver and offset-PLL transmitter (Si4200), a digital downconverter and channel select chip (Si4201), and a separate frequency


BBF
LO1
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Z
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:4
LO2
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BBF
CP
LO3
Logic
LO1
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CP
BBF
A/D
IMRF
Σ
π/2
LO3
A/D
BBF

Figure 1.1: *Example of an early GSM transceiver based on a 1.5μm silicon bipolar technology. Shaded blocks represent off-chip components [13].*

synthesizer chip. Despite its increased complexity, a direct result of its multi-mode capability, the chip-set offers a significantly higher degree of integration compared to the early attempt in Figure 1.1 as it only occupies $2.4cm^2$ and requires only 20 external components. By mid 2003 this GSM transceiver, Silicon Laboratories' first generation design, had been sold in over 30 million samples leaving little doubt about the commercial capabilities and success of RF CMOS design [14].

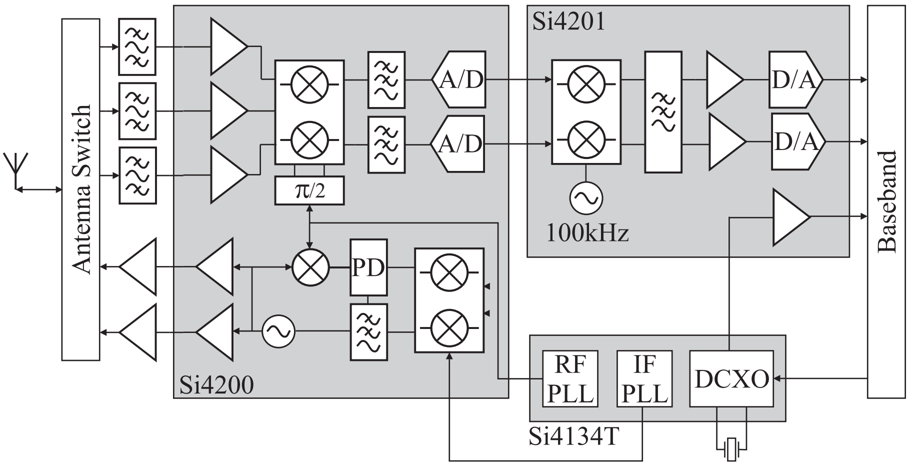

Antenna Switch
A/D
A/D
π/2
PD
Si4200
Si4201
D/A
D/A
100kHz
RF PLL
IF PLL
DCXO
Si4134T
Baseband

Figure 1.2: *Silicon Laboratories' CMOS chip-set with support for GSM, DCS, and PCS [15].*

On June 7, 2004, Silicon Laboratories announced the third generation of their $Aero^{TM}$ chipset. By combining the functionality of the earlier three-chip solution in a single chip, the resulting highly integrated solution takes up only $1cm^2$ and requires only 19 external components to form a complete quad-band GSM transceiver [15]. With its *Aero*^{TM} chipsets Silicon Laboratories have managed to transform CMOS from initially being largely an academic oddity to its new-found status as a commercially proved technology for cellular applications.

1.3 Complementary Metal Oxide Semiconductor

For a large number of years CMOS has been the preferred technology for implementing digital designs. During this time CMOS as a technology has been developed significantly, a development fueled by digital design requirements. In the early 90s analog designers started to present results that have eventually caused CMOS to develop into an analog IC technology [16, 17].

1.3-1 CMOS – a Digital IC Technology

The appearance of the *bipolar junction transistor* (BJT) in the 40s and the *monolithic integrated circuits* (MICs) during the 50s and 60s, more or less formed the foundation for integrated circuit design [18, 19]. Despite initially emerging as an analog design invention, semiconductor developments have been driven largely by digital design requirements. As a result *Very Large Scale Integration* (VLSI) circuits, containing hundreds of thousands of transistors, have become standard in most digital designs. The transition from VLSI to *Ultra Large Scale Integration* (ULSI), containing more than half a billion transistors per chip, has long since been achieved. As an illustration the first microprocessor, the *Intel* 4004 introduced in 1971, contained 2300 transistors occupying 12mm^2 in a 10μm*P-channel Metal Oxide Semiconductor* (PMOS) technology [19]. The original *Intel* 8086 processor had some 29,000 transistors while the Pentium and the Pentium Pro have around 1 million and some 5.5 million transistors on-chip [20, 21]. By 1992, high-end microprocessors, such as the 21164 Alpha chip, contained 9.3 million transistors occupying 209mm^2 in a 0.35μm CMOS technology [22]. The number of transistors per area obviously differs significantly for the Alpha chip and the *Intel 4004*. The density is in fact improved by a factor of approximately 230 when the two designs are compared. This is partly due to technology improvements such as scaling where a shift from a minimum feature size of 10μm to 0.35μm, alone, provides for a significant reduction in area.

At the time of writing, state-of-the-art microprocessors are breaking the 3GHz boundary [23]. One of the more recent processors on the market to do so is the Intel Pentium 4 - *Prescott*. As seen from Table 1.1 the number of transistors has increased by more than a magnitude when comparing the P4 to the Alpha. Despite this growth in complexity the overall chip area has in fact been reduced as a result of the continued aggressive technology scaling.

The high packing density has helped CMOS become today's preferred technology in terms of digital circuit designs. The high packing density leads to reduced volume costs which is a primary design parameter today. Also, zero static power consumption and high yield characterize CMOS [25, 26]. These characteristics make CMOS an extremely valuable

Table 1.1: *Performance comparison of the early Intel 4004, the 21164 Alpha microprocessor, and the newer Intel Pentium 4 - Prescott processor [24]. NoT = Number of Transistors.*

Design	Year	Technology	Area	NoT	Clock
Intel 4004	1971	10μm PMOS	12mm^2	2300	0.108MHz
DEC Alpha	1992	0.35μm CMOS	209mm^2	$9.3 \cdot 10^6$	500MHz
Intel P4	2004	0.09μm CMOS	112mm^2	$125 \cdot 10^6$	3.2GHz

technology. By completely dominating the world of digital designs, CMOS is currently the most widespread semiconductor technology [27, 28].

Looking at processor road-maps from major microprocessor suppliers such as Intel and *Advanced Micro Devices* (AMD), a change of technology is forseen [29]. Using conventional transistor technology the power consumptions of future processors could increase exponentially to reach as much as 100W/cm [30]. Because of this manufacturers of high performance microprocessors are turning towards *Silicon on Insulator* (SOI) as their new technology platform. It would appear that due to power dissipation issues, standard CMOS has outplayed its role as the vehicle for high performance microprocessor design.

1.3-2 CMOS – an Analog IC Technology

The BJT was the first transistor to be successfully integrated and a long experience with bipolar based analog circuit designs exists. One reason for the success of the bipolar technologies is that the BJT has a number of nice analog features. For instance, the BJT displays a high transconductance value per DC bias current, g_m/I_C, which makes it an attractive technology for high gain amplifier implementations [25]. Further, BJT technologies also provide low flicker noise corner frequencies, typically in the order of 1 – 10kHz [31].

Due to the semi-conducting nature of silicon technologies these generally experience higher losses than the more sophisticated technologies, such as GaAs. This is a serious impairment, especially at high frequencies where the substrate effects are more pronounced. The actual resistivity level of silicon is, however, highly dependent on the particular technology. For CMOS the resistivity is around 5–20Ωcm, with 10Ωcm as a typical level [32]. The low substrate resistivity for CMOS is a legacy from its digital heritage where latch-up issues are important. For analog purposes the disadvantages connected to the low resistivities come two-fold. First, the low-resistivity substrate causes loading of high frequency signals, and secondly, it offers a significant electrical coupling path for both signals and noise. While such characteristics speak against CMOS for analog designs its low cost potential is of great interest to the industry. For that matter substrate-related coupling issues have been, and continue to be, an ongoing research topic where the aim is to mature CMOS for analog high frequency applications [33–41].

Compared to the high frequency performance of bipolar technologies CMOS leaves much to be desired. This lack in high frequency performance of CMOS is caused by a number of factors. For instance, the analog performance of CMOS is limited by the low transconductance of PMOS devices [42]. In general the low g_m/I_D is of concern in CMOS designs. A general impediment of analog CMOS is the reduced device-to-device matching compared to bipolar technologies [43]. In addition, both resistive and capacitive parasitics, related to the aforementioned substrate effects, limit the attainable bandwidths of CMOS designs. Further, while the high frequency noise of the MOSFET is slightly lower than that of the BJT, the flicker noise performance is inferior to that of bipolar technologies [44]. Typical corner frequencies for CMOS are 0.1 – 1MHz [45]. Technology improvements in terms of down-scaling do not affect the BJT in a degree even comparable to the effect it has on a MOSFET device. For the MOSFET, down scaling, while preserving the current consumption level, results in an increased gate overdrive voltage, V_{od}, which in turn results in increased linearity of the device [45].

Over the last decade a third technology, *bipolar CMOS* (BiCMOS), has evolved. BiCMOS is a result of merging processing steps from bipolar and CMOS technologies. This merger combines advantages from both processes in terms of speed and power handling [42]. In a BiCMOS technology the disadvantages of MOSFETs may consequently be alleviated by using BJTs whenever these outperform MOSFET performance. However, combining bipolar and CMOS technologies involves some compromises and as a result, transistors found in state-of-the-art BiCMOS processes have reduced performance compared to their counterparts manufactured in their pure technologies [46]. This is partly due to the fact that state-of-the-art BiCMOS processes are typically lagging state-of-the-art CMOS processes by a technology node or two. Still, having both BJTs and MOSFETs available often eases some design tasks. This approach provides for optimum circuit implementation and from a circuit designer point of view, BiCMOS appears to be the better choice [47, 48]. Manufacturing of BiCMOS circuits requires more processing steps than regular CMOS thus adding to production costs. Furthermore, digital circuit implementations in BiCMOS need larger areas than equivalent CMOS implementations. Some of the short-comings of BiCMOS are illustrated by two Bluetooth transceiver design examples from the public literature [49, 50]. Reaching comparable performance levels the 0.18μm CMOS implementation provides a 40% area reduction compared to the BiCMOS implementation. Therefore, despite claims that aggressive scaling of CMOS adds to processing costs and that the cost advantage is weakening, CMOS still remains the most cost effective technology [46, 51–53].

1.4 Choosing the Appropriate Technology

It has been claimed that for modern wireless communication systems a given performance at a low cost is preferred over improved performance at a greater cost [43]. That is, if a functionality is implemented using any number of technologies, at sufficient performance, the cheaper solution always wins. In today's practical cellular networks the scenario is not quite as simple as that. To increase their market shares network operators have been engaging in costly discount campaigns for the last five to ten years. The result is that operators sell selected handsets at prices that are significantly lower than the cost price of the handset. Customers often tend to blame the network operators if they experience performance reductions and with this in mind the operators are of course interested in promoting only handsets with good performance. As a consequence, low cost on its own is not a sufficient performance parameter. Low cost has to come together with good performance, a low form factor, and low power operation if the product is to become successful.

Independently of technology, integrated design has potential for meeting all these requirements. Still, as already stated, clearly there is a number of tradeoffs involved in choosing the right technology for any given application. Only within the last decade CMOS has seriously been considered an analog high frequency technology option [54–56]. Through enginuitive designs, limitations have been negotiated to make the available CMOS performance sufficient for many applications [51]. Still, depending on a particular application either technology, bipolar or CMOS, may be favored. If, for instance, low current consumption is required, MOS has a switching speed advantage over the BJT. The opposite is the case if instead low voltage is of prime concern [57]. When cost is considered the raw technology expense is unfortunately not a sufficient parameter. If this was indeed the case, every IC design would then be implemented in a standard digital CMOS process.

While academia can afford to look at the cheapest as well as the most expensive and exotic technologies, industry must ensure competitiveness. Consequently, industry has time-to-market as one of its major design factors. For that matter the net cost of a product may in fact be optimized short term by selecting the more superior technology despite its excess cost. Here, the additional design effort required with using a cheaper technology may exceed its cost advantage. Another approach to cost reduction is through system level design optimization. In an attempt to mitigate some of the expensive external components, architectures have been revised over time. This is also apparent when Figures 1.1 and 1.2 are considered. Here, not only a change in implementation technology makes the difference, the system architectures of the two transceivers also differ.

Two of the more popular outcomes of the research on receiver and transmitter architectures are the reintroduced *Direct-Conversion Receiver* (DCR) topology and also the *Low Intermediate Frequency* (Low-IF) topology. The transceiver in Figure 1.2 makes use of the latter topology. When an optimum receiver topology is considered, the DCR stands out as being the most obvious choice. By converting the incoming RF signal down to baseband in a single step, high frequency signal processing is minimized, the image-reject filter at RF is mitigated and the same goes for the IF filter. However, the DCR concept suffers from a number of inherent disadvantages such as sensitivity towards DC-offset and low frequency noise. When both these issues are considered bipolar devices are favored over CMOS. Due to its inferior matching performance, CMOS designs result in higher DC-offset levels and due to flicker noise performance CMOS also produces more low frequency noise.

This lack in performance combined with the picture of the DCR as the optimum topology did not favor CMOS for RF-IC design. Based on a principle of concurrency in design the Low-IF is found to favor CMOS [58]. This is especially the case for narrow-band systems where signal modulations with a significant DC and/or low frequency content are used. This is also reflected by the success of the design in Figure 1.2. For narrowband systems the disadvantages of the DCR are outspoken and generally favors a bipolar implementation. If instead a Low-IF topology is used the main limitations of the DCR are mitigated and a CMOS solution becomes feasible. One reason for this is the use of poly-phase filtering which allows for image-signal rejection using analog signal processing in the complex domain [59–61]. When considering wideband systems the DCR offers better performance. One reason for this is that the wideband nature of the signals makes these more robust towards removal of low frequency content. In such cases it is possible to compensate for the short-comings of CMOS which makes this the favored technology. This fact is clearly reflected by the many WLAN [62–65] and WCDMA [66–70] designs presented in the public literature over the last couple of years. A majority of these utilize the direct-downconversion principle.

1.4-1 The Single-Chip Vision

There is a great tendency towards single-chip transceiver integration in the published RF-CMOS work. The basic philosophy being that the full potential of CMOS is unleashed only when analog RF and digital baseband are integrated on a single die. Such a design would in principle only require the addition of a display and a keypad to form a complete handset solution. While the single-chip vision represents a common goal for a majority of researchers, the viability of the single-chip idea remains a much debated issue. At least two important issues fuel the debate; i) design yield and ii) processing yield.

One of the major concerns related to design yield is the isolation properties of the substrate. With requirements for higher digital operating frequencies and increased analog accuracy, precise modeling of the substrate and all coupling effects is mandatory for the single-chip ever to become realistic. Processing yield is another limiting factor for the single-chip vision. In any IC fabrication process a number of error spots is going to exist on the wafers. Despite the significant improvements in feature-size the number of error spots per wafer has not seen the same improvement. For a typical CMOS process the defect density is around one per cm^{-2} [71]. For a 12” wafer this would imply that approximately 730 error spots would be spread across the wafer. Assuming a die area of 5mm x 5mm a total number of 2920 dies would be on the wafer. With 730 error spots this would result in a 75% yield. Such error spots set a limit on the resulting yield according to [72]

$$\text{Yield} = \frac{\text{Number of functional chips}}{\text{Total number of chips}} \approx \exp\left(-l \cdot A\right), \tag{1.1}$$

where A is the chip area and l is a function of the defect density for the given fabrication process. According to Equation (1.1), for a 95% yield design a doubling of the area would result in a yield of 86%. In high volume productions a 9% drop in yield represents a significant loss.

As a result of such practical problems single-chip design for wireless communications is still not a cost effective solution [73]. The standing question is then whether or not a single-chip solution is ever to become cost effective.

1.5 CMOS as an RF Technology – Performance vs. Requirements

From being mostly a low and medium frequency technology, CMOS is already targeting a number of RF applications. One of the driving factors behind this is the on-going development in semiconductor technology. This has resulted in the RF potential of CMOS processes becoming more evident than ever. The major achievement here being the continuous decrease in minimum feature size. Only a few years ago did the *Semiconductor Industries Association* (SIA) start to define CMOS processes in terms of nanometer rather than micrometers and already the 0.1μm milestone has been reached. This illustrates the swift evolution in CMOS technology. In contrast to digital design requirements, the technical requirements for analog transceiver functions are considerably more complicated [57]. Where speed, yield, and power dissipation are the major performance metrics for digital designs, analog designs face additional metrics such as noise, accuracy, linearity, selectivity, and high frequency gain. If CMOS can adjust to those RF needs, it has the potential of dominating analog RF design as well as digital design.

To indicate the analog performance of a given technology two parameters, f_T and f_{max}, are particularly popular. The first, f_T, represents the frequency at which the extrapolated current gain of the MOSFET reaches unity. The second one, f_{max}, represents the frequency at which the power gain falls to unity. Simplified expressions for the aforementioned f_T and f_{max} are given as [74]

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + [1+g_m]C_{gd}\right)} \quad \text{[Hz]} \tag{1.2}$$

$$f_{max} \approx \frac{1}{4\pi}\sqrt{\frac{2\pi f_T}{r_g \cdot C_{gd}}} = \frac{1}{4\pi}\sqrt{\frac{g_m}{r_g(C_{gd}\cdot C_{gs} + [1+g_m]C_{gd}^2)}} \quad \text{[Hz]}, \tag{1.3}$$

where C_{gs} is the gate-to-source capacitance, C_{gd} is the gate-to-drain capacitance, r_g is the gate resistance, and g_m is the transconductance of the device. The down-scaling into deep sub-micron leads to f_T and f_{max} values in excess of requirements which, as a conservative measure, is ten times the operating frequency of the circuit. As Figure 1.3 illustrates, 5GHz operation is well within the capabilities of modern CMOS processes.

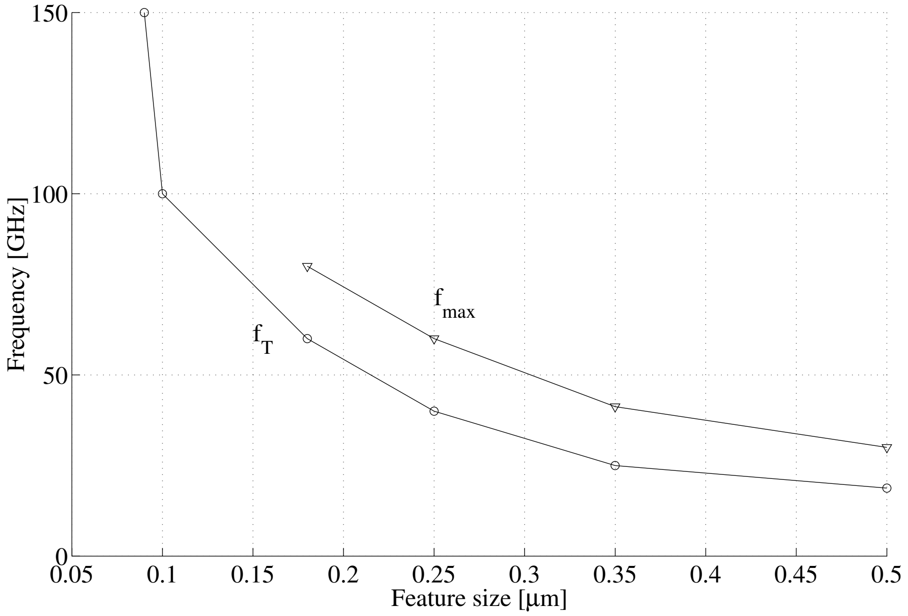


***Figure 1.3:** Measured CMOS f_T and f_{max} values versus feature size [75].*

1.5-1 High frequency gain

To provide for high frequency operation sufficient gain is crucial. This is particularly the case when implementing active circuits as the gain has to come at low current levels to save power. With f_T values of silicon processes, sub-micron CMOS processes in particular, reaching levels comparable to GaAs devices, sufficient high frequency gain is provided. However, the f_T measure ignores any effects the gate resistance, r_g, and drain-to-source junction capacitance, C_{ds}, have on high frequency performance. In that sense, the f_{max} measure is a more appropriate measure as this includes the gate resistance and thereby takes layout effects into account. In fact, the high f_{max} values reported for CMOS result primarily from lowered gate resistances due to fingered transistor layout [57]. From the first-order approximation in Equation (1.3) it is clear that f_{max} is increased either by reducing the gate resistance, the gate-drain or gate-source capacitances, or by increasing g_m.

In providing RF gain, sufficient transistor performance is not always enough. As many RF circuits, such as LNAs and oscillators, are tuned to some narrow frequency band using an LC resonator type load, the performance of these reactive components also plays an important part in ensuring ample RF gain. Take for instance a single-FET LNA where the parasitic capacitances are used in conjunction with a load inductor to implement the LC tank. The resulting peak voltage gain for this circuit may be expressed as g_m times Z_0 where Z_0 is the impedance of the tank at resonance. The attainable impedance is here often limited by the quality factor, Q, of the inductor. The resonance impedance may be written as

$$Z_0 = Q \cdot \omega_0 \cdot L = \frac{Q}{\omega_0 \cdot C} \qquad [\Omega], \tag{1.4}$$

where L is the resonator inductance, C is the resonator capacitance, and ω_0 is the resonance frequency. Based on this the voltage gain may be expressed as

$$A_V = g_m \cdot Z_0 = \frac{g_m \cdot Q}{\omega_0 \cdot C} \qquad [\text{–}] \tag{1.5}$$

From this it appears that a high RF gain requires low loss passive devices and tight control of parasitic capacitances if power consumption is to remain reasonable. However, increasing the Q-value is also governed by a compromise. Circuits based on large loaded Q-values are highly susceptible to de-tuning due to either component spread or simply from insufficient estimation and modeling of parasitics [76]. As an example, for any given circuit with a gain tolerance specification there is a technology dependency as component spread sets a limit on how high the Q is allowed to go. In turn this means that there is also a limit to how low the power consumption may go.

1.5-2 Low Noise

Apart from amplification of the wanted signal RF front-ends also need to display low-noise performance in order to meet sensitivity requirements. Typical front-end noise figure requirements range from 5–10dB when measured at the antenna terminals [77, 78]. As the LNA has significant influence on the overall noise performance this is a key circuit element in meeting noise figure requirements. Typically LNAs must display noise figures of less than 3dB for the overall receiver to meet specifications [57]. Eventually at some point the incoming signal is translated to baseband in the receiver chain. Depending on the nature of the receiver architecture, input-referred noise from baseband circuits may drown the weak input signals. At the expense of increased power consumption a high gain LNA may help overcome this. However, to prevent the need for very high gain in RF stages baseband circuits must also be low noise. This relation is an often neglected issue in the public literature.

Considering the noise performance of the MOSFET, a simplified expression for the minimum noise figure is given as [57]

$$NF_{min} \approx 1 + k \cdot g_m \cdot r_g \cdot \left(\frac{f}{f_T}\right)^2 \qquad [\text{–}], \tag{1.6}$$

where r_g is the gate resistance of the device, k is a unitless technology dependent constant, and g_m is the device transconductance. Equation (1.6) illustrates the importance of having both a low gate resistance and a high f_T. While technology scaling has a significant positive effect on f_T the reduced feature sizes increase r_g to form a trade-off in noise performance. The minimum noise figures for MOS devices are in the order of 0.6 – 0.8dB which is slightly lower than for bipolar devices [45]. That CMOS is capable of producing low noise LNAs is evident from various reported works where noise figures around 1.2dB – 3dB have been reported [79–82]. In fact, CMOS is gradually approaching the sub-1dB NF range [45, 83, 84].

A low NF_{min} for a circuit does not on its own guarantee a resulting low noise figure. It is also crucial to know the optimum source impedance, Z_{SOF}, for the device as well as the spacings of the noise circles as these determine how easy optimum noise matching may be attained. The performance gap between reported NF_{min} values and actual circuit noise figures relates to the fact that low noise input matching to 50Ω is hard for MOS devices. This is partly due to the inherent capacitive nature of the MOSFET and partly due to the large component variations. This implies that a degradation of noise or power dissipation performance results from moving the input impedance closer to 50Ω. So once again a tradeoff is the result. To understand these trade-offs consider the thermal noise for a MOS device given as [85]

$$v_t = \sqrt{\frac{\langle |e_{tn}|^2 \rangle}{\Delta f}} = \sqrt{\frac{4kT \cdot \gamma \cdot g_{d0}}{g_m^2}} = \frac{2\sqrt{kT \cdot \gamma \cdot g_{d0}}}{g_m} \qquad \left[\frac{\mathrm{V}}{\sqrt{\mathrm{Hz}}}\right], \tag{1.7}$$

where k is Boltzmann's constant and g_{d0} is the drain-source conductance at zero V_{DS} voltage. The parameter γ equals unity at zero V_{DS} and, for long-channel devices, decreases to approximately 2/3 in saturation. For short-channel devices γ takes on a value of two to three or even larger [74]. According to Equation (1.7) a large g_m value helps to reduce thermal noise. Another important noise source results from the generation of flicker noise. The flicker noise adds a noise current to the drain-source current of the MOSFET. The spectral characteristics of flicker noise follow a $1/f$ characteristic that, when reflected back to the gate, is described as [85]

$$v_f = \frac{i_f}{g_m} = \frac{1}{g_m \cdot L}\sqrt{\frac{KF \cdot I_D^{AF}}{f \cdot C'_{ox}}} \qquad \left[\frac{\mathrm{V}}{\sqrt{\mathrm{Hz}}}\right], \tag{1.8}$$

where the flicker noise coefficient, KF, typically is in the order of $10^{-25}\mathrm{V}^2\mathrm{F}$, the flicker noise exponent, AF, is around 0.5 to 2, C'_{ox} is the gate oxide capacitance, and I_D is the DC drain current. Hence, in reducing the flicker noise contribution long devices with large transconductances are needed. Comparing Equations (1.6) and (1.8) reveals that the overall noise performance may be improved only through the use of long devices or by a combination of large g_m and large f_T.

1.5-3 High Linearity

Linearity is another important performance parameter for front-end designs as the receiver is normally required to receive and demodulate weak incoming signals, typically around -100dBm or lower, in the presence of powerful interfering signals located at nearby adjacent channels. The large dynamic range in the combined input signal makes it difficult to extract the weak wanted component without distorting this to some degree.

When the linearity performance of a FET is considered it is actually found to be better than the BJT device. Both the FET and the BJT are basically non-linear voltage controlled current sources and their transfer function may be approximated by a power series expansion

$$i_O = I_{DC} + f' \cdot v_s + \frac{1}{2!} \cdot f'' \cdot v_s^2 + \frac{1}{3!} \cdot f''' \cdot v_s^3, \tag{1.9}$$

where v_s represents the peak input voltage and the function f describes the transfer function of the device. f' represents the first derivative of the transfer function with respect to the device input. When exited by a high power input signal the second and third order components can be found from Equation (1.9). The ratio between the fundamental component and the second and third order components provides measures of the *Harmonic Distortion* (HD) levels of the device. These measures, HD_2 and HD_3, are indicators of the single-tone second and third order non-linearity performance of the device respectively. When calculating the harmonic distortion components for both the FET and the BJT a significant difference is found as Equations (1.10) and (1.11) show

$$HD_2 = \frac{1}{4} \cdot \frac{f''}{f'} \cdot v_s \quad \Rightarrow \quad \begin{cases} HD_{2,BJT} = \frac{1}{4} \cdot \frac{v_s}{V_T} \approx \frac{v_s}{100mV} \\ HD_{2,FET} = \frac{v_s}{4 \cdot (V_{GS} - V_t)} \end{cases} \tag{1.10}$$

$$HD_3 = \frac{1}{24} \cdot \frac{f'''}{f'} \cdot v_s^2 \quad \Rightarrow \quad \begin{cases} HD_{3,BJT} = \frac{1}{24} \cdot \left(\frac{v_s}{V_T}\right)^2 \approx \frac{v_s^2}{15mV} \\ HD_{3,FET} = 0, \end{cases} \tag{1.11}$$

where V_T is the thermal voltage, v_t the MOS threshold voltage, and v_s the input voltage signal. Based on harmonic distortion properties the FET is seen to provide, ideally, zero third order distortion while the BJT suffers from a fundamental limit. A simple rewriting of Equation (1.11) shows that the IP_3 for a BJT corresponds to an input level of 87mV$_{rms}$. In terms of second order distortion the BJT is found to have an IP_2 of 71mV$_{rms}$. These values represent fundamental device limitations. For the FET it is seen that IP_2 may be controlled by the gate over-drive voltage given by $V_{GS} - V_t$. With typical values of V_t around 0.5 – 0.6V the second order distortion performance of the FET is easily better than that for the BJT.

The harmonic distortion concept applies to single-tone excitation only. Consequently, the output signal may consist only of the fundamental frequency, f_c, and its harmonics, $2 \cdot f_c$, $3 \cdot f_c$ and so on. In a practical wireless system several high power signals may interfere with the wanted signal. By a non-linear combination of two or more of such interfering signals the receiver generates interference on any number of frequencies. A receiver's tendency to degrade performance through such non-linear combinations is referred to as intermodulation.

Traditionally IP_3 has been sufficient in describing receiver linearity. Depending on the choice of receiver architecture another important effect is even order distortion as this results in the generation of DC signal components. Therefore, to quantify the amount of DC-offset produced, IP_2 is also required to fully specify receiver performance.

1.5-4 Low Power

Second only to low cost, the major consumer requirement relates to the time between battery recharges. The time between the battery recharges is a performance metric that enabels customers to an easy comparison of competing commercial products. Hence, prolonged recharge cycle time is an important performance measure for today's battery driven devices. Also, portability places severe constraints on the physical size and weight of handsets. As a result the available battery power is limited due to the bulky nature of battery cells. The fundamental limit of power consumption is directly linked to circuit performance. Low voltage and low power are interlinked features as reduced supply voltages lead to reduced power dissipation. In fact, for digital designs the power consumption scales quadratically with the supply voltage [19]. Low voltage and low power are already mastered in CMOS digital designs. This trend is also seen in analog designs where both very low voltage operation and low power is seen.

As mentioned previously, the noise of a MOSFET device is inversely proportional to g_m. Furthermore, the linearity performance is found to depend on the gate over-drive voltage, V_{od}, applied to the device. As a result g_m and V_{od} determine the dynamic range capabilities of the MOSFET. Extended a bit further this means that the minimum drain current is determined by the dynamic range requirement. This may be illustrated by

$$I_D = \frac{1}{2}\mu \cdot C'_{ox}\frac{W}{L}(V_{gs} - V_T) = \frac{1}{2}g_m V_{od}, \tag{1.12}$$

which represents the drain current of a MOSFET operated in saturation. Clearly with g_m and V_{od} determined by dynamic range requirements the resulting I_D is given by Equation (1.12). Even more important is that this is a fundamental relation that is independent of feature size and other technology scaling effects [76].

1.5-5 Low Voltage

With the ever decreasing feature sizes of CMOS technologies lower device breakdown voltages result. This is a consequence of the reduced gate oxide thickness and reduced channel lengths [86]. Reduced channel lengths result in punch-through if supply voltages are not adjusted accordingly and a reduction of the power supply voltage is therefore necessary. A reduction of the power supply voltage means that the battery size may be reduced as fewer cell elements are required. Another benefit is as mentioned, that for digital logic the power consumption scales with the supply voltage. However, for analog designs lowering the supply voltage does not necessarily imply a reduction in power consumption. As low voltage requirements severely affect circuit dynamic range, bias current levels may need to be increased to meet performance requirements. This must be taken into consideration during design as traditional circuit topologies may prove unfit in a low voltage environment [86]. For instance, switched capacitor circuits do not operate optimally at low voltages due to insufficient operation of CMOS switches [87]. Also, transistor stacking is no longer viable as this reduces the available output signal swing.

1.5-6 Passive Devices

A highly linear receiver may be able to accommodate weak incoming signals with only a limited amount of distortion. Still, in order to amplify the wanted signal without overloading receiver stages due to interfering signals, some filtering is required. In modern cellular systems the available frequency bands are split into channels for improved capacity. As such, frequency selectivity is an important measure of a receiver's ability to demodulate weak signals in high power interference environments. Depending on the implementation, different filter requirements are found. These are, however, generally rather steep which calls for high quality passive devices for adequate filtering.

High frequency filtering considered, the availability of quality passive RF devices is of key concern in RF-CMOS design. Traditionally, high quality passives are extensively used in RF design. The limitations in design of passive devices, inductors in particular, are here mainly associated with substrate losses as well as high resistivity interconnects. Typical CMOS performances for various implementations of passive devices are listed in Table 1.2.

Table 1.2: *Achievable RF performance for passive devices in CMOS technology [75, 88–90]. Only implementations based on standard CMOS implementations are included.*

Component	Value	Accuracy [%]	Performance
Resistors			
Polysilicon	5 – 10 Ω/□	30 – 40	Good Linearity
Well (n or p type)	1 – 10 Ω/□	50 – 80	Large parasitics and voltage coefficient
Capacitors			
Fractal	1 – 2 fF/μm^2	2	Q ≈ 60 @ 2GHz
MOS	1 – 5 fF/μm^2	15	Q ≈ 15 @ 2GHz
MIM	50 – 200 aF/μm^2	20	Q ≈ 30 @ 2GHz
Interdigital/MIM	1 – 2 fF/μm^2	n/a	180 @ 2GHz
Inductors			
Bondwire	1 – 5 nH/mm	1 – 100	Q ≈ 60 @ 2GHz
Spiral	1 – 10 nH	5 – 10	Q ≈ 3 – 6 @ 2GHz
Enhanced spiral	1 – 100 nH	3 – 5	Q ≈ 7 – 9 @ 2GHz

Resistors

For resistors, absolute tolerances can be as large as 40% [75]. The relative matching performance is usually much better, typically in the order of a few per cent. It should here be noted that die-die versus wafer-wafer matching and tolerance may show notable differences. The relatively poor matching performance of both active and passive components may be improved as device matching improves with the inverse of the square-root of their physical area [80].

Capacitors

When implementing passive devices in CMOS technologies the same design problems are faced as with bipolar technologies. Fortunately, due to the accurate oxide control, capacitors implemented in CMOS technologies have benefits over bipolar implementations. Here the very thin gate oxide allows for high capacitance per area implementations which is important [43]. In the context of integrated design it is therefore relatively easy to fabricate well-defined capacitors. With typical tolerances of 15% both the accuracy and the quality factors of integrated capacitors are found to be acceptable.

Exploitation of lateral flux capacitors is another high performance option in CMOS where the many metal layers and the very narrow metal spacings improve performance. In keeping the flux away from the substrate, bottom plate capacitances and substrate losses may be minimized and fairly high-Q capacitances can be implemented [45, 88].

Inductors

While both resistors and capacitors of reasonable performance may be implemented with CMOS technologies, the inductor represents a severe problem. One explanation is that the inductor was never a part of the initial CMOS idea. And since the development of CMOS has been largely motivated by digital design requirements there has been no need for inductors. However, to meet the stringent requirements for filtering and power efficient gain optimization in analog applications, high quality passives including inductors are essential.

In a standard silicon technology, quality factors of passive spiral inductors are limited to approximately 3 – 9 within the frequency range 0.5 – 2GHz which is rather poor. The two most viable inductors result from either bondwires or from spiral inductors. From Table 1.2 the bondwire inductor is found to give good quality factors while the accuracy here is unacceptable for most purposes. Furthermore, bondwire inductors may only implement relatively small inductance values. In contrast spiral inductors provide for significantly larger inductance values and also better accuracy. The quality factor, on the other hand, is very low. Being relatively large structures spiral inductors also invite to parasitic coupling with substrate as well as other adjacent circuits which compromises both device and circuit isolation. Optimized inductor layout where multi-layer inductor design strategies are exploited improves the inductance value while reducing the inter-trace capacitance [90, 91]. Despite shielding and even removing the underlying substrate the parasitic capacitance between the metal traces remain a limitation to the performance of the planar spiral implementation. The solenoid-type inductor addresses this issue [92]. Recently, solenoid-type inductors have been implemented in standard CMOS using the obvious vertical approach [89]. This provides for an area efficient implementation while improving both quality factor and self-resonance frequency compared to an equal-inductance planar structure.

Ingenious design techniques based on post-processing have been developed in an attempt to improve on the performance of the inductor. One example is the technique of suspended inductors [93]. Using post-fabrication etching, quality factors may be improved by removing part of the lossy substrate. Despite such efforts to improve performance, inductor values up to approximately 10nH seem to be the limit at 2GHz. At the same time quality factors remain as low as 3 – 10 which drastically limits on-chip resonator performance. In comparison, off-chip high-Q resonators, such as coax-resonators, can provide quality factors better than 10,000 in the same frequency range. In recent years *Micro Electro Mechanical Systems* (MEMS) have been pursued as a vehicle to obtain better overall performance in inductors [94–96]. As MEMS technology is maturing its potential for improving the inductor performance is unquestionable. However, even though the MEMS approach is completely compatible with existing standard CMOS technologies, it still adds extra processing steps to the fabrication process [92].

1.6 Summary

The lack of high quality passive devices, inductors in particular, represents one of the major obstacles in achieving a fully integrated RF design based on CMOS. However, as RF CMOS is currently among the most actively researched areas in integrated circuit design, CMOS is likely to acquire many of the required qualities over time.

Using traditional RF circuit design techniques, high-quality inductors remain mandatory in a large host of circuits for receiver applications. To enable a successful CMOS implementation of integrated transceivers, a different approach to system level architectures needs to be taken. Instead of focusing on traditional approaches new radio architectures must evolve around the strengths and weaknesses of CMOS.

In addition, the requirement for multi-standard transceivers calls for a degree of flexibility that is in excess of what is possible with today's receivers if parallel and therefore expensive receivers are to be avoided. Consequently, future transceiver architectures need to provide vast flexibility while requiring only mediocre performance from their functional blocks. With the power amplifier as a questionable part of a single-chip design it is argued that a single-technology CMOS solution for the remaining transceiver blocks is a very plausible contender. Especially since the full potential of RF CMOS is only unleashed in single-chip solutions where DSP algorithms may be exploited to adapt the analog circuit blocks to changing conditions [80, 97]. One important limitation to this development is that RF CMOS innovations must not come at the expense of cost as CMOS has to be the cheaper technology to remain competitive.

Part II

CMOS Aware Receiver Planning

Receiver Architectures and DC-Offset Cancellation

"An attractive receiver design must effect a compromise between physics and economics".

U.L. Rohde

This part addresses aspects of direct-downconversion receiver planning for RF-CMOS implementation. First an overview of different receiver architectures is provided. Following this, the potential of the direct-conversion receiver architecture is presented using UTRA-FDD as a vehicle. With a performance surplus in the implementation technology it is common practice to simplify receiver planning and employ a full separation of different distortion mechanisms. However, low-cost silicon technologies, applied for todays RF and baseband circuitry offer only limited design performance. This means that the block requirements resulting from over-specification may be very difficult to meet using low-cost technologies. Another approach to receiver planning is therefore needed. Based on voltage domain expressions a simple receiver planning method is presented. As part of this the DC-offset problem is analyzed and the effect of a DC-offset cancellation for a UTRA-FDD DCR is pursued. Requirements for a DC-offset cancellation system are found and the possibilities of use of a simple highpass filter are analyzed.

2.1 Receiver Architectures and General Considerations

The lack of high quality passive devices, inductors in particular, represents one of the major obstacles in achieving a fully integrated RF design based on CMOS. Considering this, the extensive use of high quality inductors in traditional RF designs therefore does not match with the fact that silicon technologies only provide poor quality inductors. Using traditional RF circuit design techniques, high-quality inductors remain mandatory in a large host of circuits for receiver applications. Despite continuous efforts to overcome this limitation the lack of high quality passives still remains a bottleneck. Therefore, to enable the implementation of integrated transceivers, a different approach to system level architectures has to be made. To ensure success these architectures must be designed within the limitations of integrated technologies, in this case CMOS. Consequently, architectures based on extensive high-selectivity filtering should be avoided.

A wide range of receiver architectures is already available to the designer. Based on basic functional differences, such as the frequency translation principle utilized, the receiver architectures may be separated into one of three categories; i) poly-conversion, ii) single-conversion, and iii) sub-sampling structures. In Figure 2.4 a number of architectures is illustrated and organized according to this principle. Some of the architectures are well-known while others still represent somewhat novel structures.

The term poly-conversion indicates that the frequency translation is spread over more than one functional block in the analog part of the receiver chain. Single-conversion, on the other hand, implies that only one analog down conversion step is used. After this down conversion the wanted signal is located at a frequency where traditional A/D conversion is possible. By this the demodulation or the final down conversion to baseband, if required, may be implemented digitally. The last family member included in Figure 2.4 is the sub-sampling receiver. This includes any receiver where, at any point in the receiver chain, the analog signal undergoes down conversion to digital baseband using the principle of sub-sampling.

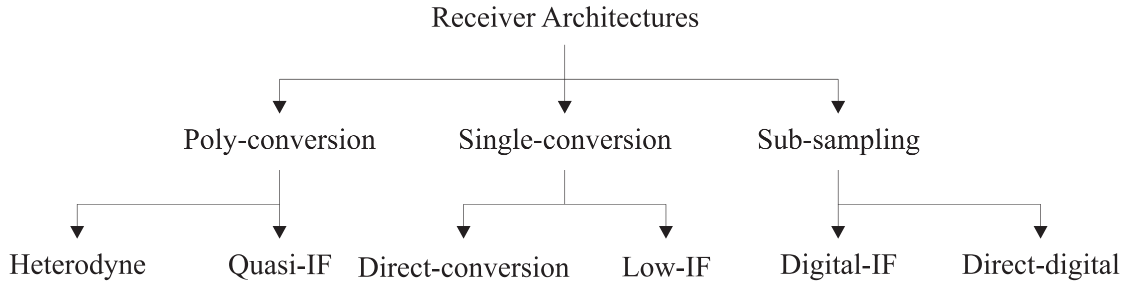

Receiver Architectures
Poly-conversion
Single-conversion
Sub-sampling
Heterodyne
Quasi-IF
Direct-conversion
Low-IF
Digital-IF
Direct-digital

Figure 2.4: *Some of the most common receiver architectures arranged in families based on common functional characteristics.*

The illustrated receiver architectures all provide for different trade-offs, such as degree of filtering and ADC requirements just to mention a few. For any given application the advantages and disadvantages of the architectures must be evaluated to enable an optimum receiver selection. In the following sections the different members of the receiver family are investigated further.

2.1-1 Poly-Conversion Receivers

The most well-known poly-conversion receiver architecture is the *HeteroDyne Receiver* (HDR). This structure was introduced as early as 1918 and by now it represents a well-known solution to the task of radio reception [98]. Figure 2.5 shows an example of a poly-conversion receiver where only a single IF is used before the down-conversion to baseband. The topology illustrated in Figure 2.5 requires three external filtering components to meet the filtering requirements. The first of these filters, the duplex filter (Rx/Tx), attenuates all out-of-band signals. In theory this ensures that only the wanted signal band enters the receiver. The second filter, the image-rejection filter (IMRF), suppresses the image signal while the third filter, the IF-filter (IFF), provides for channel selection filtering.

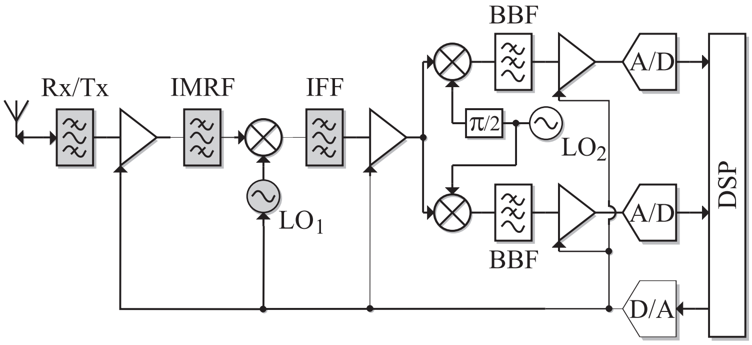

BBF
Rx/Tx
IMRF
IFF
π/2
LO₂
LO₁
A/D
A/D
DSP
BBF
D/A

Figure 2.5: *Traditional heterodyne receiver architecture. Shaded blocks are traditionally implemented off-chip.*

The working principle of poly-conversion receivers is to translate the high frequency input signal to baseband via two or more conversion stages. By exploiting high quality filtering and amplification in between frequency conversion stages, it is possible to progressively isolate the wanted signal from various interferers and thereby provide the desired performance. Receivers based on this principle generally provide for very good sensitivity performance.

Selecting the proper IF involves a number of important trade-offs, the majority of which is centered around the mixers as well as the image-reject and IF filters. Considering mixers, the specific choice of IF, and indirectly the LO, has a major effect on the performance. To attain optimum mixer performance a square-wave switching signal is required [99]. If the switching transistors are not driven fully on/off, that is if they are soft-switched, they are all partly open for fractions of the switching period. These devices thereby contribute with both shot and thermal noise to the mixer output whereby noise levels are raised in excess of hard-switched mixers [100]. Any diversion from hard-switching causes distortion and noise levels to rise and the conversion gain is reduced. At high frequency attaining a perfect square-wave LO signal is harder to generate which results in soft-switching of the mixer with reduced mixer performance as a result [80]. This calls in favor of a low LO frequency and accordingly a large IF. A large IF is also favored for reasons of image rejection. Here, a large IF results in a large image distance whereby the requirements for the image-reject filter may be relaxed accordingly. On the other hand, having to operate at a high IF implies that all the IF stages, including both the LNA and the first mixer, must operate at high frequencies where power efficiency is harder to obtain. Thus, while large IFs reduce requirements for preceding filtering additional high frequency signal processing is required whereby the power consumption is increased.

The heterodyne receiver is limited by its traditional approach to image-rejection. Having to combat the image-signal through traditional RF filtering is a great hindrance to further promotion of integrated receivers. Using image-rejecting mixers the image signal may be attenuated whereby filtering requirements can be relaxed. Another way to mitigate part of this problem is to make use of quadrature down-conversion and then recombine the resulting two-phase signal. This approach allows for image-rejection after the down conversion and the IF frequency tradeoff is virtually removed. Two well-known single-sideband receiver architectures, the Hartley receiver and the Weaver receiver, are based on this principle of quadrature signal processing. Where the Hartley receiver makes use of passive RC-networks to provide for the image suppression, the Weaver receiver uses a second quadrature mixer. A common feature for both receivers is that they suffer from effects of gain and phase mismatch. The typical component mismatch in integrated circuits limits image suppression to 30 – 40dB [101]. Combining two Hartley or two Weaver receivers in a double quadrature manner results in an improved image-rejection mixer. When based on the Weaver receiver, like the topology illustrated in Figure 2.6, the resulting receiver is known as a *Quasi-IF Receiver* (QIFR).

Just as for the heterodyne receiver, a duplex filter selects the wanted frequency band. However, after the low-noise amplification the quasi-IF receiver down-converts the information signal using quadrature mixing. This results in a complex signal representation at the IF just as it is the case for the basic Hartley and Weaver topologies. Without any IF filtering each of the signal branches is down-converted to baseband using yet another quadrature mixer stage. This

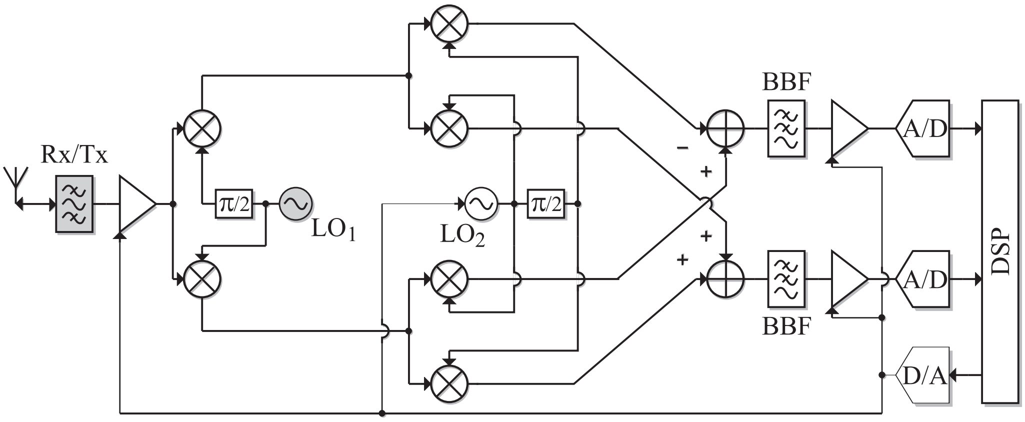


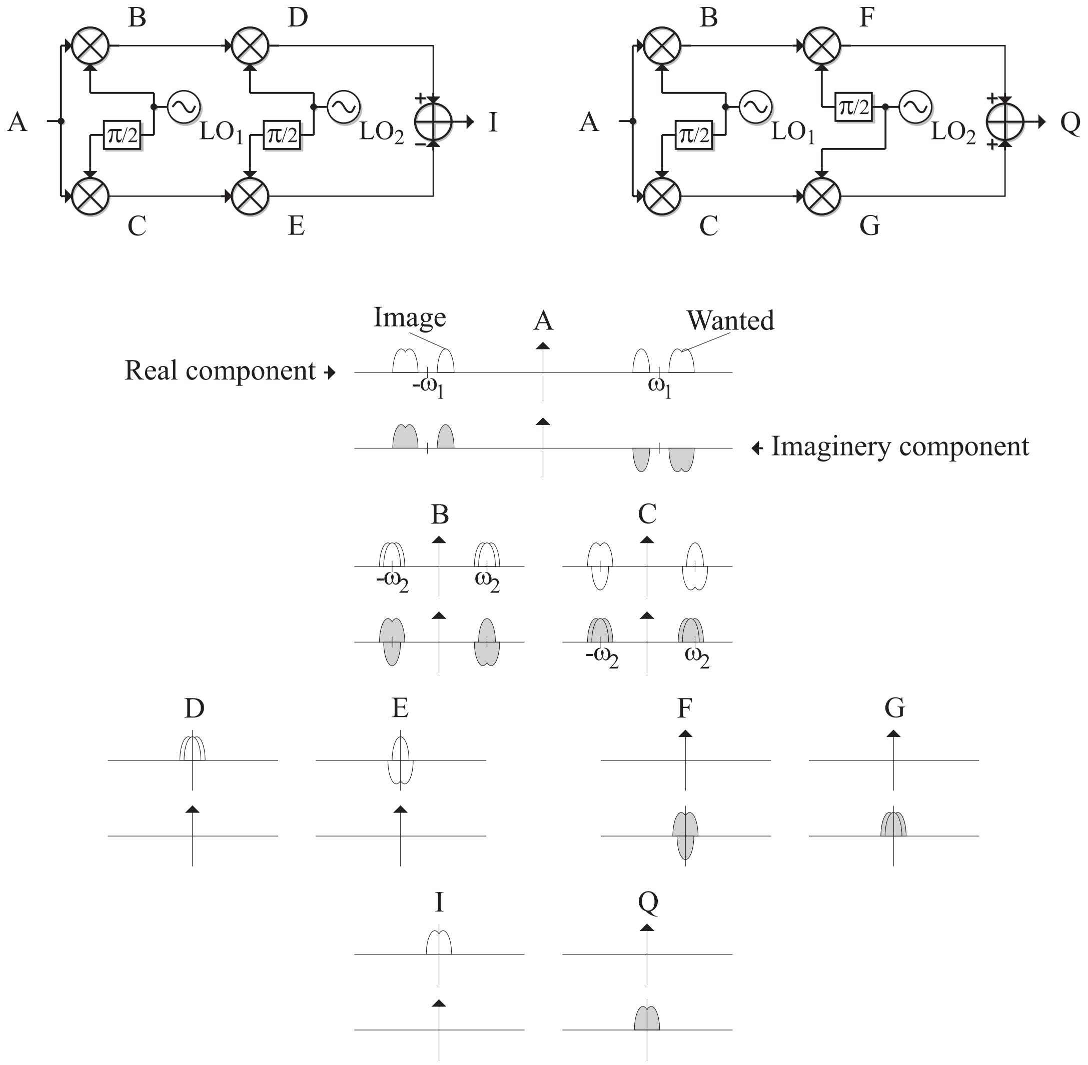
Figure 2.6: *Quasi-IF receiver architecture. Shaded blocks are traditionally implemented off-chip.*

way both sidebands are available as a quadrature baseband signal. To graphically illustrate the operation of the quasi-IF receiver the core of the receiver is split into two parts in Figure 2.7. From this illustration the signal phasing operation resulting from the signal processing through the quasi-IF receiver is revealed. Having the wanted and the image signals available at different phases, at points B and C, makes it possible to down-convert and combine the signals resulting in a suppression of the unwanted component. Using the quasi-IF approach 40 – 50 dB of image rejection is possible without any filtering at IF [60]. In practice some processing may be required prior to the second set of mixers, most likely some amplification to combat low frequency noise [102].

Besides eliminating the need for an image-reject filter the quasi-IF receiver has a number of other advantages compared with the heterodyne receiver. By allowing the first LO to be fixed and letting the low frequency second LO be tunable both may be optimized with respect to phase noise [60, 103]. The absence of the IF-filter is another advantage as only one off-chip filter is required. The penalty is the added complexity of the receiver due to the extra mixers required. In addition the RF mixers must be highly linear to reduce intermodulation distortion in the IF mixers. The additional circuitry also increases the power consumption of the receiver as a whole. This puts extra focus on low-power mixer implementations.

2.1-2 Single-Conversion Receivers

Both the traditional heterodyne receiver and the quasi-IF receiver make use of extensive analog signal processing at both RF and IF. This is a common feature that applies to most of the poly-conversion receiver topologies. An obvious way to reduce the amount of analog signal processing is to reduce the number of IF stages. Reducing the number of IF stages means fewer receiver stages and hence less circuitry. What is equally important is that of the remaining stages fewer now have to operate at high frequencies. Reducing the number of IF stages not only decreases the power consumption. The reduced area consumption may also help to minimize


B
D
A
π/2
LO1
π/2
LO2
+
−
I
C
E
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F
A
π/2
LO1
π/2
LO2
+
+
Q
C
G
Image
A
Wanted
Real component
-ω1
ω1
Imaginery component
B
C
-ω2
ω2
-ω2
ω2
D
E
F
G
I
Q

Figure 2.7: *Graphical illustration of the quasi-IF receiver (QIFR) operation. Signals are split into real and imaginary components with the latter being marked using a dark shade.*

the cost of the handset. In continuation of this, the single-conversion receiver represents an optimum solution as only one frequency conversion stage is made use of here. The specific choice of IF is not the important part as single-conversion receivers may convert directly to baseband or any other IF carrier frequency for that matter. If the incoming signal is converted directly down to baseband the architecture is known as a *Direct-Conversion receiver* (DCR). As a concept the DCR was considered as early as 1924 but it was not until 1947 that the structure saw its use to full effect [104]. That the DCR architecture indeed represents a less complicated design is evident from Figure 2.8.

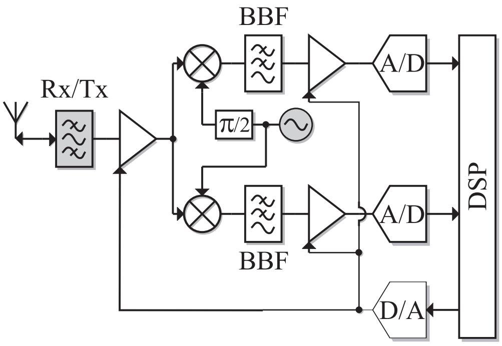

Figure 2.8: *Direct conversion receiver architecture. Shaded blocks are traditionally implemented off-chip.*

Compared to Figure 2.6 the DCR may be viewed as a stripped down quasi-IF receiver where the four quadrature mixers are here omitted. This is possible as the image-signal is non-existing when the wanted signal is down-converted directly to baseband [98]. Still, there is a need for tight matching between I and Q branches to prevent signal leakage. As a consequence the task of image discrimination becomes significantly easier and sufficient performance is attainable in the mixer alone. For the DCR to match the image rejection performance of the QIFR the gain and phase match must be better than 0.1dB and 0.5° respectively [44].

In a direct-conversion receiver the wanted signal is selected with a lowpass type baseband filter (BBF). Another characteristic of the direct-conversion receiver is that most amplification and filtering are now performed at baseband rather than at RF. This enables lowered current drain in amplifiers and active filters whereby power consumption may be reduced. There are, however, several drawbacks connected to the DCR architecture. In fact when compared to the previously discussed poly-conversion receivers, the DCR combines the disadvantages of both. Here, the RF-LO selects the wanted channel and tuning range versus phase noise tradeoff must be negotiated. Furthermore, LO frequency deviation and spurious LO leakage also represent challenges in a DCR design. Just as for the quasi-IF receiver the reduction in RF and IF filtering means that the linearity performance of any low frequency blocks needs to be improved in comparison to the requirements in the heterodyne topology. This problem is especially severe for the direct-conversion receiver as the RF gain must be fairly high for the signals to successfully combat low frequency noise resulting from mixer and baseband circuits. However, the most important limitation connected to the DCR architecture is the much talked about DC-offset. Due to mostly even-order non-linearities and component mismatch in I and Q branches, DC components are generated internally in the receiver paths. Not only does this distort the wanted signal, it may also result in overloading of receiver circuits. As such, the reduced circuit complexity of DCR architectures generally comes at the expense of reduced performance. Thus for a given application a trade-off exists between complexity and performance.

Moving on to a non-zero IF a number of the problems related to the DCR may be mitigated. If the IF is kept at low or moderate frequencies the resulting topology is known as a *Low-IF Receiver* (LIFR). As Figure 2.9 shows the low-IF topology is very similar to that of the DCR.

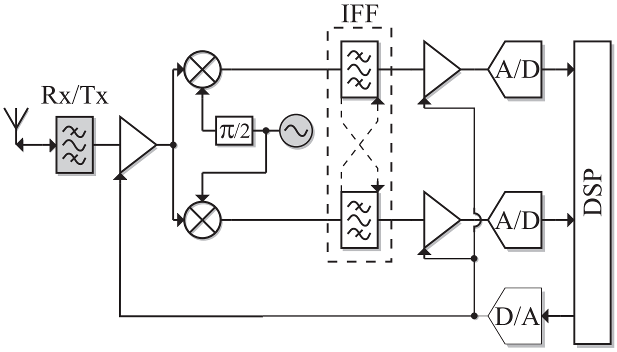

Figure 2.9: *Low-IF receiver architecture. Shaded blocks are traditionally implemented off-chip.*

Like the direct-conversion receiver the LIFR architecture also makes use of quadrature down-conversion to produce a low frequency complex representation of the incoming RF signal. As a result the mixer-related concerns of the DCR are also found here. Moving from a zero-IF to a low-IF of course re-introduces the image signal problem. This means that the severe IF tradeoff displayed in poly-conversion receivers applies here as well. Since a part of the image discrimination must result from the mixers the I/Q matching is important. Again, this places soft-switching of FET mixers as a concern as the exposed mismatches limit image rejection [80]. Having the signals represented as complex signal allows for the image signal to be attenuated using complex post-processing. This may either be implemented using additional mixers as in the quasi-IF receiver or by using complex analog filters. A third option is to postpone the image-rejection until after the ADC whereby the operation may be implemented digitally [106]. Determining where to place the image-rejecting operation involves dynamic range performance tradeoffs. If implemented digitally the dynamic range of the ADCs becomes extremely important.

2.1-3 Subsampling Receivers

All the previously discussed receiver architectures suffer from the limited performance of CMOS devices. As a solution to a number of these practical problems, subsampling has been suggested [98]. Where traditional architectures solely operate the MOSFETs as active analog devices, sampling architectures exploit the excellent sampling properties of MOSFET switches [98]. Unlike traditional signal sampling, where the sampling frequency is according to Nyquist, subsampling makes use of a sampling rate that is much lower than the signal frequency. The principle here being that any signal of a given finite bandwidth, $B = (f_h - f_l)$, may be sampled using any sample rate, f_s, that is equal to, or greater than, twice the signal bandwidth while also satisfying [107]

$$\frac{2f_h}{k} \leq f_s \leq \frac{2f_l}{k-1} \quad \text{, with} \begin{cases} 2 \leq k \leq \dfrac{f_h}{B} \\ B \leq f_l \end{cases} , \tag{2.13}$$

where k is an integer value. By complying with both Nyquist and Equation (2.13), subsampling produces a series of non-overlapping replica of the incoming signal at multipla of the sampling frequency. Anyone of the replicas may be selected but from a implementation and power consumption point of view selecting to baseband replica may be advantageous. The structure of a receiver based on subsampling is not much different from anyone of the previously discussed receivers. Much like the poly-conversion receiver any number of traditional analog down conversion steps may take place prior to subsampling. If an analog IF is used the receiver is categorized as a *Digital-IF Receiver* (DIFR) structure. If no analog conversion takes place and the sample-rate is furthermore an exact sub-harmonic of the incoming RF signal, a *Digital Direct-Conversion Receiver* (DDCR) is the result. The latter topology is illustrated in Figure 2.10.

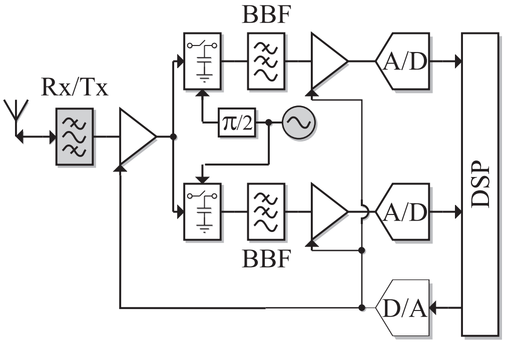

Figure 2.10: *Subsampling receiver architecture. Shaded blocks are traditionally implemented off-chip.*

Just as the direct-conversion receiver suffers from a number of practical problems, a number of problems arises in practice in a digital direct-conversion receiver. The sub-sampling approach is bandwidth limited as only narrow band signals may feasibly be down-converted using this approach [108]. This results in the need for high-quality RF filtering which may not be implemented in an integrated way. For that reason the additional filtering requirements must be incorporated into the duplexer or as a prefilter stage preceding the LNA. Another more severe disadvantage related to sub-sampling is noise [98]. The problem is that the sub-sampling mixer also acquires wide-band noise which then folds into the frequency band of the down-converted signal [109]. The noise in question results both from the input signal and from the preceding receiver stages. The effect of this is that the baseband noise spectral density is raised by the ratio of the track bandwidth to the sample-rate [110]. On the other hand, a subsampling mixer tends to be more linear in terms of RF-to-IF magnitude transfer than traditional analog multipliers [110]. Provided a high gain LNA precedes the sub-sampling mixer, its noise effects are reduced to provide for large dynamic range operation [110]. Also, it is adventegous that a high frequency LO sinusoid is no longer required as a low frequency pulse train is used instead [57].

2.1-4 Choosing the Appropriate Architecture

The presented architectures do not represent an exclusive listing of available architectures. However, most architectures do share a number of common characteristics which allow for categorization. As such, most architectures may be derived from one of the aforementioned families of receiver architectures. Despite the characteristics of each family being more or less known in advance, the task of selecting the most suited receiver architecture is generally still no easy task. However, if a fully integrated solution is the goal, the number of realistic candidates quickly reduces.

An important issue here is the filtering requirement. Selective filtering, in integrated form, is hard to achieve and compared to off-chip solutions the performance is feeble. On top of that the frequency range for passive solutions is limited. While spiral and bondwire inductors are useful in providing limited selectivity at around 1GHz and up, they are not viable options at lower frequencies [112]. As a result image rejection and channel selection filters are typically implemented using expensive off-chip *Surface Acoustic Wave* (SAW) filters. Not only do these add to the end price of the handset, they also require low ohmic interfaces leading to more severe trade-offs between gain, noise performance, and power dissipation. Any receiver architecture that mitigates the use of off-chip filters is advantageous. While this again excludes the heterodyne receiver, the quasi-IF receiver holds a slight advantage by its immediate down-conversion from IF to baseband. In terms of both reduced RF signal processing and filtering, the DCR and the LIFR present themselves as close to ideal architectures for full integration by relocating the majority of the signal processing to low frequencies or even baseband. The same applies for the subsampling receivers.

When using receiver architectures that translate the incoming signal to low frequencies early on in the receive path, noise is of great concern. Considering the inferior flicker noise performance of the MOSFET, this is especially important for CMOS receivers. As signals here must compete with noise generated in both mixers and baseband blocks, severe design requirements are placed on the LNA. While increased LNA gain improves overall receiver noise performance, it also compromises linearity. This also places a requirement for highly linear mixers in order to suppress unwanted intermodulation products resulting from interferers [98, 110]. To efficiently detect advanced modulation forms it may be necessary to run at an IF well above the flicker noise corner frequency [80]. Noise performance is also of great importance to the last candidate architecture, the subsampling receiver. This is illustrated by a reported subsampling receiver structure that acquires samples of a 900MHz carrier at a 50MHz rate while displaying an 18dB noise figure [110]. This is around 8 – 9dB more than reported continuous-time mixers display for the same frequency band [113].

Catching up on the aforementioned, the quasi-IF, the low-IF, and the direct-conversion receiver stand out as the most suited receiver architectures for a full CMOS integration. All three share the characteristic that they make use of complex signal representation early on in the receiver path. As no image signal is present in the direct-conversion receiver, I/Q mismatch is not as great a concern as for the quasi-IF and the low-IF receivers. Extensive I/Q processing invites to phase and gain mismatch problems and should be avoided. For that matter the LIFR is favored over the QIFR in this work.

Everything considered, the advantages and disadvantages of the different receiver architectures seem to speak in favor of single-conversion receivers as the best choice for a fully integrated CMOS receiver. Both the DCR and the LIFR have great potential in this relation. Only, they each favor different applications. For narrow band systems, such as GSM, the LIFR architecture would appear to be the preferred choice. It allows for a fast transition from RF to LF while at the same time avoiding a number of the disadvantages of the DCR. The potential of the DCR is not to be neglected, however, its characteristics are best suited for wideband applications.

2.2 Receiver Structure for UTRA-FDD

When engaging in receiver design for 3G systems it is important to realize that 2G systems are already well-established. Until the newer systems can deliver sufficient coverage and services, handsets have to support both. The presented receiver design is intended for multi-mode operation based on GSM and W-CDMA.

For RF designers experienced with TDMA/FDMA-based second generation wireless systems, the introduction of W-CDMA presents some new challenges. Rather than being separated in time or in frequency, CDMA users are separated by orthogonal codes. The use of high bit rate codes implies a spectral spreading of the user signals and due to the noise-like characteristics of the codes the signal attains the characteristics of band-limited white noise. Using gold-code scrambling on top of the orthogonal spreading codes, several CDMA channels are multiplexed onto the same frequency channel. Consequently, the signal received by a CDMA handset consists of many simultaneous transmitted signals all located on the same carrier frequency.

GSM is based on time division duplex (TDD) as well as frequency division duplex (FDD) which allows a duplex switch to select between transmit and receive modes. Having a duplex switch ideally allows for perfect isolation between transmitter and receiver. In contrast the considered W-CDMA system, UTRA-FDD, only uses FDD which implies that simultaneous transmission and reception takes place. This introduces a new set of problems due to spurious leakage which complicates the process of receiver planning significantly. For 2G systems it has largely been possible to consider the transmitter and receiver designs seperately. For UTRA-FDD this is not the case. Besides amplification of the wanted transmit signal any noise generated in the transmitter path is also amplified and transmitted. Such noise emissions are of course critical for the spurious emission test approval. It is also very important for the receiver design as excess transmitter noise appearing within the receive band could degrade receiver performance significantly. Naturally, all this has to be considered when selecting a receiver architecture for UTRA-FDD.

Due to its good noise performance and its high selectivity, the heterodyne receiver architecture has been the preferred architecture for 2G systems. However, with issues such as power consumption, cost and especially form factor becoming increasingly important, alternative architectures are being explored. Despite its many short-comings, direct-conversion receivers have emerged for the GSM market. One of the many obstacles has here been the narrow-band nature of the GSM signal combined with a receiver architecture that suffers from nonlinear distortion and DC-offset issues. Based on the large signal bandwidth, W-CDMA systems are less susceptible to low frequency noise and other limiting characteristics of the direct-conversion receiver. Consequently, many consider this architecture the better choice for the W-CDMA 3G systems. Based on previous experience and studies the receiver structure and interface definitions illustrated in Figure 2.11 are therefore chosen. The receiver contains both RF and baseband blocks as the entire chain is important in a CMOS implementation.

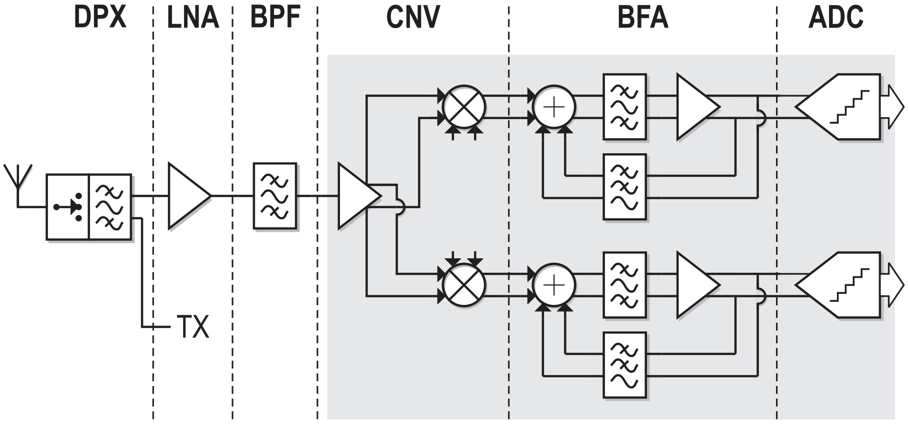

Figure 2.11: *System diagram of the UTRA/FDD receiver. Shaded blocks are intended for CMOS implementation.*

The first stage is a duplexer (DPX) including a multi-mode selection switch. Using a duplexer is the only practical way to obtain the required isolation between the transmitter and the receiver. Despite intentions of a fully integrated CMOS receiver, initial evaluations show that with the available CMOS RF filter performance, an off-chip bandpass filter (BPF) following the LNA is needed to attenuate transmitter leakage. Following the BPF there is a quadrature down-converter (CNV) with an active phase splitter as input, and two parallel baseband filter and amplifier (BFA) paths. The BFA includes a servo-type feedback loop to compensate for low frequency distortion and DC-offset generated in both the CNV and the BFA.

As mentioned, the continuous presence of the transmitter signal constitutes an important issue for UTRA receiver specification. Any TX signal leaking to the receiver part is going to generate intermodulation distortion together with blockers, direct second-order distortion, as well as direct distortion. Another interference component of particular concern for the direct-downconversion is low-frequency second-order products generated by adjacent channels and intermodulation disturbances. In addition to this there is the problem of DC-offset which needs to be considered. Independent of the method used during receiver planning, the effect of these low frequency disturbances must be evaluated if over-specification is to be avoided. It is very important to uncover the options at hand in terms of cancellation techniques and how these affect the W-CDMA signal. It is therefore necessary to address this issue prior to engaging in any receiver link-budget calculations.

2.3 DC-Offset Filtering of W-CDMA Signals

The causes to DC-offset are numerous but may be characterized as being either largely time-invariant or time-variant. Largely time-invariant effects are caused by effects such as process mismatch, drift of analog circuitry that varies slowly versus temperature, aging, and gain setting. Using a slow-update adaptive correction algorithm these issues may be mostly alleviated. Time-variant errors are of greater concern as these may not be compensated for during for instance fabrication or during power-up. As illustrated in Figure 2.12, the time-variant errors are caused mainly by parasitic LO signal coupling to mixer RF port (I''_{lo}), LNA input-port ($I'_{lo}/2$), and antenna ($\alpha I'_{lo}/2$).

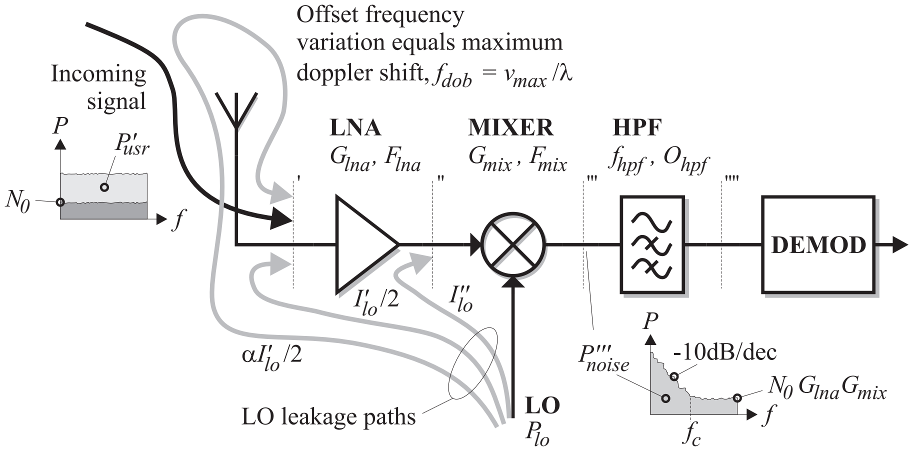

Figure 2.12: *Illustration of the DC-offset problem in direct-conversion receiver.*

The attenuation factor α used in Figure 2.12 describes (i) antenna impedance mismatch and (ii) the fraction of leakage at LNA input port which is radiated from the antenna and then subsequently reflected back from nearby moving objects to the receiver. Further, f_{hpf} is the 3dB cut-off frequency for the filter and O_{hpf} is the corresponding filter order.

The LO leakage depends on the actual implementation and is typically due to substrate, capacitive, and bond-wire coupling [115]. Any leakage between LO and RF ports of the mixer causes self-mixing which produces an undesired DC component. The instantaneous amount of self-mixing is assumed to be dominated by antenna movement and, hence, the associated Doppler shift [116]. To consider a worst-case scenario, it is assumed that the content of all time-variant offset errors falls at a single frequency determined by the maximum Doppler shift $f_{dob} = v_{max}/\lambda$ where v_{max} is the maximum vehicle speed allowed according to the specifications. As Figure 2.12 illustrates, a simple highpass filter (HPF) is used to cancel the DC-offset. A number of more or less sophisticated adaptive schemes based on DSPs has been proposed [67, 117, 118]. Compared to these schemes the HPF approach may seem hopeless. However, while the advanced cancellation schemes often require additional DACs, the HPF approach is very simple and straight forward. It also has potential for attenuating the low frequency second-order distortion component.

2.3-1 DC-Offset Model and Cancellation

The major concern is that DC-offsets can easily reach values that are large enough to saturate stages following the mixer. For sufficient performance the total DC-offset power should be around 20dB lower than the total down-converted signal power [119]. Based on the notation of Figure 2.12 and neglecting the largely time-invariant errors, a worst-case scenario as shown in Figure 2.13a may be derived. Here the full dynamic offset power, $\alpha I'_{lo} P_{lo} G_{lna} G_{mix}/2$, is shown at the the maximum Doppler shift frequency. In Figure 2.13b the resulting attenuation at 1kHz is shown for different 3dB cut-off frequencies and different filter orders.

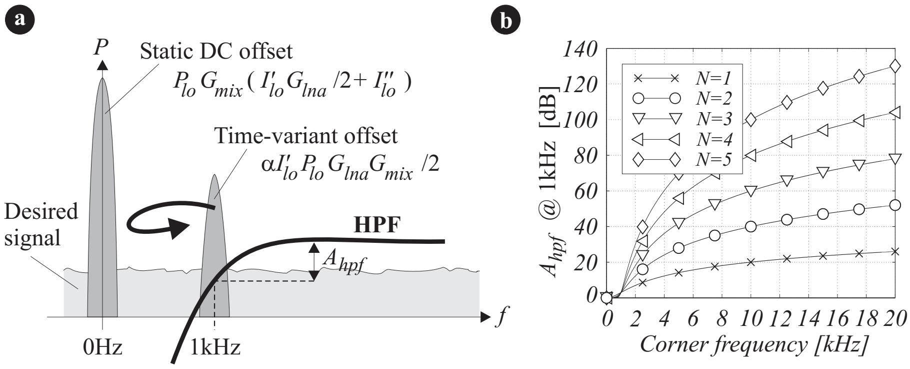

Figure 2.13: *Illustration of (a) static and dynamic offset with HPF characteristic and (b) HPF attenuation at 1kHz for various Butterworth filter orders, N, and 3dB corner frequencies.*

Based on typical values the ratio of time-variant offset power to signal power is found to be as high as 40 – 60dB. The HPF should therefore be able to reach a target value of 60 – 80dB at 1kHz. It is seen from Figure 2.13b that such an attenuation can be obtained only with filter orders of four, or higher, if a maximum corner frequency of 10kHz is required. At a corner frequency of 20kHz a filter order of three also meets the requirements. In either case this is a steep filtering requirement and it may lead to signal degradation due to group-delay.

To determine the sensitivity of the UTRA-FDD signal towards removal of DC and low frequency information through highpass filtering, a simulation platform has been developed. Based on this simulation set-up a number of simulations is conducted using different filter configurations and different channel fading profiles. The results of these simulations are combined in Figure 2.14.

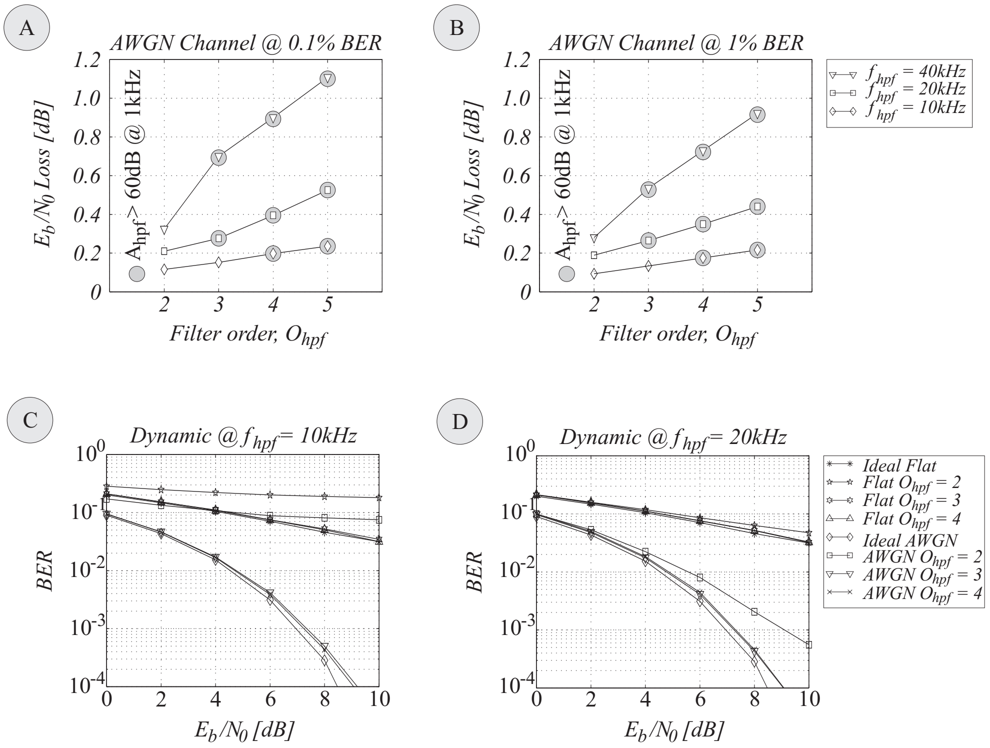

Figure 2.14: *Simulation results for various HPF and system configurations using a spreading factor of 128. a) Signal degradation at 0.1% BER without offset, b) Signal degradation at 1% BER without offset, c) BER performance with a HPF cut-off at 10kHz, d) BER performance with a HPF cut-off at 20kHz.*

The results shown in Figure 2.14a and Figure 2.14b are based on the AWGN channel and they have been conducted without the time-variant offset. Hence, the results show the signal degradation caused by the HPF alone. The E_b/N_0 degradation due to the HPF is shown for two BER reference values and in both cases it is found to increase with both corner frequency and filter order. As a higher filter order leads to an increased group-delay and a higher corner frequency removes more signaling information, this is as expected. For the HPF to provide the full DC-offset suppression of 60 – 80dB, it seems as if a choice of O_{hpf} equal to four and a f_{hpf} to 10kHz gives the least distortion. If 0.3dB E_b/N_0-degradation is acceptable, the combination of a O_{hpf} of three and a f_{hpf} at 20kHz is a possible way to reduce group delay. In conclusion, the target value of 60 – 80dB attenuation is achievable using a HPF while degrading E_b/N_0 by only 0.2 - 0.3dB.

To evaluate the DC-offset canceling effect of the HPF a time-variant offset at 60dB above the reference signal level is added to the signal. For reference, a simulation is conducted without including the HPF and the time-variant offset is found to completely corrupt the reception quality (BER=50%). When the HPF is introduced, performance improves significantly. The results shown in Figure 2.14c and Figure 2.14d illustrate the performance of the HPF for both types of channels. It appears that for $O_{hpf} \geq 3$ the HPF is able to almost remove the effect of the 1kHz offset component.

At a BER of 10% the degradation of the fourth order 10kHz HPF is less than 0.2dB. Here it is important to note that these results are based on the maximum spreading factor of 128. As the spreading factor is reduced so is the processing gain of the system. To evaluate the effect of a reduced processing gain a simulation is conducted using a minimum spreading factor of 4. In this case the second and third order filters fail while a fourth order filter sees a relative E_b/N_0 loss of only 0.2dB for a BER of 10%. This is not as bad as could be expected from a 15dB reduction in processing gain. The explanation is found in the frame structure where a change at low spreading factors adds pilot bits to improve the channel estimate and an overall E_b/N_0 gain of 0.5dB results. In general it appears that a filter order around three or four and a corner frequency around 10kHz serve as a good compromise. Based on this it is possible to do a receiver planning where the performance of the data receiver is exploited.

2.4 Receiver Planning

Traditionally the use of high performance discrete components and exotic integrated solutions has allowed designers to consider non-ideal effects separately while obtaining full receiver compliance with specifications. Designers have had to identify a benchmark test from the specifications and based on this all remaining radio parameters have been derived. For GSM it has typically been the *Co-Channel Rejection Ratio* (CCRR) that has been used as the benchmark test. However, for low-cost integrated receivers, such as the DCR and LIF types, where baseband circuits seriously degrade overall performance, performance surplus is not in abundance which prevents the non-ideal effects from being considered separately. Instead the technology limitations call for a non-trivial tradeoff among gain-distribution, noise, nonlinearities, and selectivity. Hence, receiver planning must consider interstage selectivity and baseband performance in order to reach a balanced tradeoff between the different radio parameters.

For a system such as UTRA-FDD the increased complexity in receiver planning is even more apparent as the transmitter is constantly being operated. This is very unlike TDMA-based GSM where the receiver and transmitter are prevented from being operated simultaneously. Having an always present TX signal adds complexity to the whole process of receiver planning. It is of course possible to use a traditional approach despite the complexity of the problem. One way is to assign different contribution percentages to the different distortion components and have the combined effect meet specifications. This approach is illustrated in Figure 2.15.

The many interferring components make it difficult to achieve an optimum solution when distribution factors are set manually. To ease this process a computer-assisted methodology

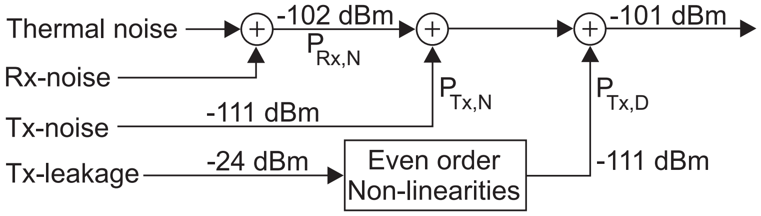

Figure 2.15: *Illustration of how noise and disturbance power contributions may be handled.*

is therefore proposed. Using this simple scheme the otherwise complicated task of receiver planning becomes manageable.

To consider all the different distortion mechanisms simultaneously, absolute signal levels of desired response, noise, intermodulation products, and interferers/blockers are preferable over standard cascade measures. In the case of receiver planning the optimization procedure may conveniently be based on an effective *signal-interference ratio* (SIR) defined at the input of the demodulator just before the ADC. As it is customary in specifications, all performance requirements are given in BER. In case of UTRA-FDD the test scenarios require an overall receiver performance to meet a BER of less than 10^{-3} [4]. In order to simplify the process, the baseband processing should be discluded. Therefore the BER value needs to be mapped to a corresponding SIR referred to the input of the ADC. From system simulations it has been determined that the BER requirement is met for a SIR of 6dB – 6.2dB [120]. Based on the link-simulations presented in Section 2.3-1 the requirements for DC-offset filtering have been found and more importantly, the resulting penalty in terms of E_b/N_0 degradation is found. In addition to the 6.2dB another 0.2 – 0.5dB degradation is expected to result from the DC-offset filtering in the BFA. Based on this the resulting performance requirement is 6.7dB. Hence, when adding some margin the overall design target to the demodulator is calculated as

$$\begin{aligned}\mathrm{SIR} &\simeq \frac{|A_{usr}|^2}{n_{out}^2\Delta f + \sum_r |A_r|^2} \\ &\simeq \frac{\mathrm{PG}\cdot|A_{usr}|^2}{n_{out}^2\Delta f + |A_{blck}|^2 + |A_{adjc}|^2 + |A_{2,\mathrm{BFA}}|^2 + |A_{3,\mathrm{BFA}}|^2 + |A_{\mathrm{mai}}|^2} \geq 7\mathrm{dB}, \qquad (2.14)\end{aligned}$$

where A_{usr} is the RMS amplitude of the desired signal before the demodulator, n_{out} is the effective noise amplitude, Δf is the baseband signal bandwidth, PG is the processing gain, A_{blck} is the RMS amplitude of all blockers/interferers (including spurious TX), A_{adjc} is the RMS amplitude of adjacent channels, $A_{2,\mathrm{BFA}}$ and $A_{3,\mathrm{BFA}}$ are the RMS amplitudes of all second and third order products, and A_{mai} is the multiple access interference (MAI) from all other code channels. All amplitude powers in Equation (2.14) are added in-phase assuming no correlation regardless of the frequency location within the Δf band.

The next step is to derive expressions for the different terms that go into Equation (2.14). When doing this it is important that an extended version of traditional microwave theory that incorporates general selectivity is used [121]. This is necessary since when the baseband circuitry in DCR architectures contributes heavily to the overall receiver performance, the performance envelope of CMOS technology is being pushed. In this case even the slightest degree of attenuation of interferers may benefit the overall performance.

The adopted theory is based on voltage domain calculations [122]. Here, the loaded voltage gain, for block k, is denoted by $G_k(f)$, where f is the frequency. The gain functions denote the full frequency dependent gain and, hence, selectivity is considered. To handle frequency translating devices, each block k is denoted by its input-referred passband frequency f_k. In this way interferers and other intermodulation products may be treated by their absolute offset to the passband frequency which enables a simplified notation. Further, the adopted expressions have been rewritten to form loop-form equations which makes for an easy computer implementation. Based on these definitions the total noise output from a cascade of K stages is given as

$$n_{out} = \sqrt{\sum_{k=1}^{K} n_k^2 \left(\frac{r_{i,k}}{r_{i,k}+r_{o,k-1}}\right)^2 \cdot \prod_{r=k}^{K} \alpha_r G_r^2(f_r)}, \tag{2.15}$$

where n_r is the equivalent mean square noise voltage density (referred to zero source impedance) for block r, $r_{i,k}$ and $r_{o,k}$ are the input and output resistance for block k respectively, and α_r is a factor denoting the type of frequency translation in block r. The second order distortion that originates from an interferer placed at a frequency δf away from the passband frequency may be calculated as

$$A_{o,2} = A_i^2 \left(\prod_{k=1}^{K} G_k(f_k)\right) \sum_{k=1}^{K} \frac{1}{\mathrm{iIP2}_k} \left(\prod_{r=1}^{k-1} \frac{G_r^2(f_r+\delta f)}{G_r(f_r)}\right) \left(\prod_{r=k+1}^{K} \frac{G_r(f_{im})}{G_r(f_r)}\right), \tag{2.16}$$

where $iIP2_k$ is the second order input intercept point for block k, and f_{im} represents the absolute output frequency at which the distortion arrives. For the DCR this distortion is usually a low-frequency contribution. A similar expression exists for the third order intermodulation distortion. In this case the distortion is created by two interferers located at δf and $2\delta f$. With amplitudes given by A_1 and A_2 the expression is given as

$$A_{o,3} = A_1^2 A_2 \left(\prod_{k=1}^{K} G_k(f_k)\right) \sum_{k=1}^{K} \frac{1}{\mathrm{iIP3}_k^2} \left(\prod_{r=1}^{k-1} \frac{G_r^2(f_r+\delta f) G_r(f_r+2\delta f)}{G_r(f_r)}\right), \tag{2.17}$$

where $\mathrm{iIP3}_k$ is the third order input intercept point for block k.

2.4-1 Test Scenarios and Work-Flow

The different test scenarios described in the standardization document may be boiled down to the three major distortion groupings illustrated in Table 2.3. This table provides an overview of which interference and distortion mechanisms are present during the different tests.

By considering all interfering components simultaneously, the designer can utilize advantages and minimize the effect of impairments of the applied technology. This philosophy forms the basis of the methodology illustrated in Figure 2.16.

Table 2.3: *Indication of effects included in the various simulation tests. '+' indicates that the effect is active while '–' indicates that it has been omitted.*

Test	**Desired**	**Direct Distortion**					**2nd Order**			**3rd Order**	
	User	Noise	MAI	Blk1	Blk2	Tx	Blk1	Blk2	Tx	Blk1/Blk2	Blk1/Tx
Sensitivity	+	+	+	–	–	+	–	–	+	–	–
ACS	+	+	+	+	–	+	+	–	+	–	–
Blocking	+	+	+	+	–	+	+	–	+	–	–
IMD1	+	+	+	+	+	+	+	+	+	+	–
IMD2	+	+	+	+	–	+	+	–	+	–	+

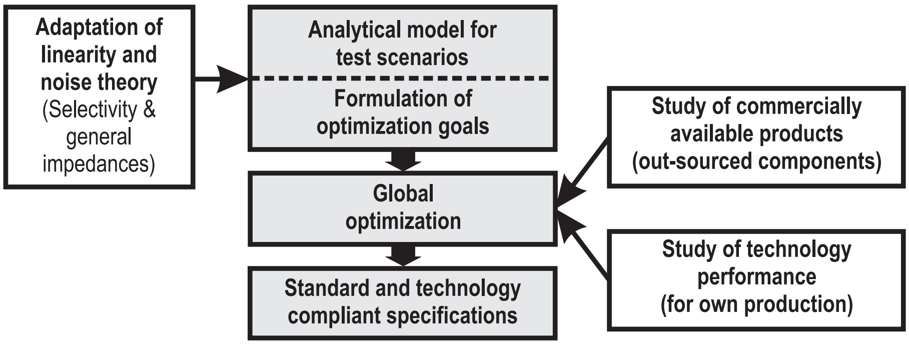
Adaptation of linearity and noise theory (Selectivity & general impedances)
Analytical model for test scenarios
Formulation of optimization goals
Global optimization
Standard and technology compliant specifications
Study of commercially available products (out-sourced components)
Study of technology performance (for own production)

Figure 2.16: *Representation of the work-flow used for the receiver planning.*

Accordingly, a computer model is built for each of the test-scenarios to which compliance must be guaranteed. During the optimization, a number of parameters is swept to search the performance space for a optimum combination of receiver block performance. Block parameters open for optimization include gain, selectivity, and linearity. All combinations of gain and gain margin are used as noise and linearity are weighted randomly which prevents the identification of a worst-case set-up. Realistic ranges for available block performances are determined using public literature and previous design experience.

The entire scheme is implemented in MATLAB^{TM} [123]. The simulator is split into separate parts with one routine defining the receiver performance range, a test routine for each of the test scenarios defined in the standardization document, a main routine, and finally a routine for presenting the results. It is not possible to make all tests exactly match the 7dB requirement but a close-to optimum specification arrangement is produced using the proposed method. After optimizations the overall receiver specifications listed in Table 2.4 result.

2.5 Summary

A number of different receiver architectures is presented and the characteristics from an IC implementation point of view is presented. Despite its inherent short-comings, a direct-downconversion receiver architecture is used to implement a receiver for a W-CDMA system. The specific target system is UTRA-FDD with the overall goal being a multi-mode GSM/UTRA-FDD solution. The DC-offset issue is evaluated and worst-case requirements to a cancellation scheme are derived based on a DC-offset model. Based on link-simulations the potential of using a simple highpass filter approach is evaluated and found useful. The effect of such a filter on WCDMA signal performance is analyzed and found to be within 0.2dB while offering 80dB attenuation of a worst-case DC-offset component.

In continuation of this a simple approach to receiver planning is presented. As the method considers all interferring components simultaneously, the designer can utilize advantages of the applied technology and thereby minimize the effect of impairments. Compared to equivalent results obtained using traditional calculations and manual distribution of distortion effects, the proposed method leads to relaxed block specifications.

Table 2.4: *Resulting DCR block specifications after optimization. The DPX, LNA, and BPF blocks are commercially available components.*

Specification	**DPX** [124]	**LNA** [125]	**BPF** [126]	**CNV**	**BFA**
Voltage gain, max. AGC [dB]	-2.3	11	-1.5	16	60
Gain margin [dB]	±0	±1.5	±0.5	±2	±2
AGC range [dB]	0	15	0	0	60
Input noise [nV/$\sqrt{\text{Hz}}$]	0.37	0.31	0.34	≤1.95	≤10
Input impedance [Ω]	50	50	50	50	≥2k
Output impedance [Ω]	50	50	50	≤300	≤300
Rel. att. at baseband (<5MHz) [dB]	10	40	40	40	0†
Rel. att. of 1st adj. ch. (5MHz) [dB]	0	0	0	0	≥16.2‡
Rel. att. of 2nd adj. ch. (10MHz) [dB]	0	0	0	0	≥40‡
Rel. att. of 3rd adj. ch. (15MHz) [dB]	0	0	0	0	≥57
Rel. att. of 4th adj. ch. (20MHz) [dB]	0	0	0	0	≥57.5
Rel. att. at 15MHz offset [dB]	1.5	0	1	≥0	≥57
Rel. att. at 60MHz offset [dB]	10	0	5	≥0	≥57
Rel. att. at 67MHz offset [dB]	18	0	10	≥0	≥57
Rel. att. at 85MHz offset [dB]	22	0	7	≥0	≥60.5
Rel. att. at 135MHz offset (TX) [dB]	55	0	30	≥0	≥60.5
Maximum input [dBV_{rms}]	20.0	n.a.	17.0	-27.9	-9.9
iCP1 [dBV_{rms}]	n.a.	-12.0	n.a.	≥-25	≥-9
iIP2 at 15MHz offset [dBV_{rms}]	∞	∞	∞	≥6.7	≥45.1
iIP2 at TX spurious [dBV_{rms}]	∞	∞	∞	≥6.7	≥45.1
iIP3 at 10MHz/20MHz offset [dBV_{rms}]	∞	-4.0	∞	≥-17.7	≥1.2
iIP3 at 67MHz/135MHz offset [dBV_{rms}]	∞	-4.0	∞	≥-17.7	≥1.2

† A 10kHz HPF with order ≥2 will provide effective attenuation of non-linear products (≥6dB).

‡ An additional 18dB is achieved in digital filter after ADC (3 extra bits).

Part III

CMOS Circuit and Device Design

UTRA-FDD Mixer Design and Inductor Crosstalk Issues

"The silicon wafer also contributes eddy current losses and if it is at all possible one avoids the use of inductors".

D.J. Hamilton

DC-offset, low frequency noise, and intermodulation distortion components falling at low frequency are the main limiting factors for the direct-downconversion receiver architecture. In that respect the mixer plays a key role in defining the overall success of the receiver. On top of this circuit-related issue a number of technology related device coupling mechanisms exists. For a successful receiver design both levels are important. This part considers the design of a CMOS mixer intended for the direct-downconversion UTRA-FDD receiver. A classical approach to improving isolation is to use guard-rings. It is evaluated to what extent the use of guard-rings limits inductor performance. Following this, the extent of inductor-related coupling is evaluated and the benefit of having guard-ring structures is evaluated in comparison to distance between inductors.

3.1 Mixer Design for a UTRA-FDD Direct-Downconversion Receiver

In all receiver designs, low noise performance and high linearity are major design goals. When a design manages to meet both requirement's a very good signal handling capability results. This allows for reception of weak wanted signals with a minimum of distortion despite interfering signals such as blockers and image signals. Traditionally, third order intermodulation has been the preferred measure for receiver linearity. But for systems operating with varying-envelope modulated signal, such as W-CDMA, even-order distortion is also important. When specifying mixer performance it is therefore important to include both second and third-order distortion.

Based on the receiver analysis presented in Part 2 a CMOS direct-downconversion mixer for UTRA-FDD is designed. To meet the requirements in Table 2.4 the mixer implementation illustrated in Figure 3.17 is chosen. The mixer is based on a modified Gilbert cell where both the I and Q channel share the same input transconductance stage.

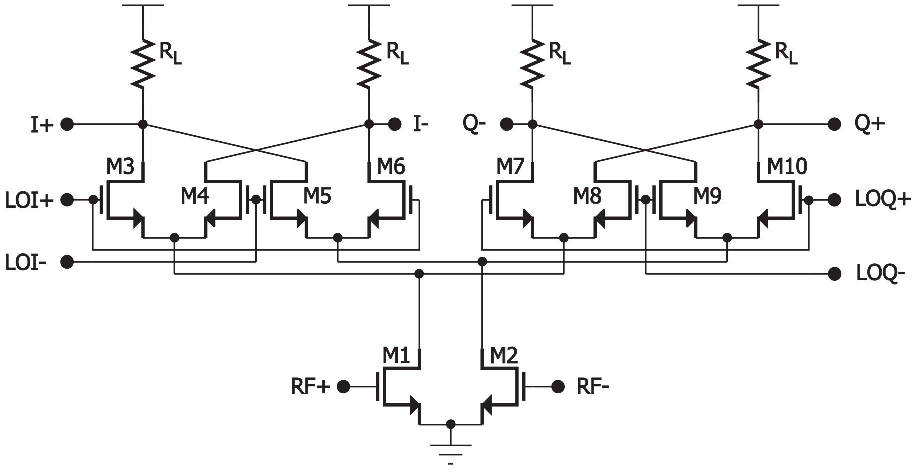

Figure 3.17: *Quadrature mixer topology based on a modified Gilbert cell.*

The balanced Gilbert cell type mixer is chosen for its robustness and its good attenuation properties related especially to even-order distortion. To minimize leakage from LO-to-IF a double-balanced topology is selected. Minimizing the LO leakage component is particularly important in a direct-conversion receiver where a high-power leakage signal easily could cause saturation of the subsequent baseband blocks as well as intermodulation distortion.

3.1-1 Switching Core

Instead of running two separate mixers in parallel, the switching cores of the quadrature mixers share a differential transconductance input stage. This constellation means that the input stage is shared between I and Q branches and it can therefore not contribute to quadrature imbalance. There is, however, a disadvantage to this approach since the mixer becomes sensitive towards LO imbalance and transistor mismatch. As Figure 3.18 illustrates the sensitivity is most significant for square-wave LO signals where transistors M3 and M6 conduct current simultaneously with transistors M7 and M10 for part of the LO cycle. In case of an amplitude imbalance in the LO signal, transistors M3 and M7 are going to steal current from each other. The same is the case for transistors M6 and M10.

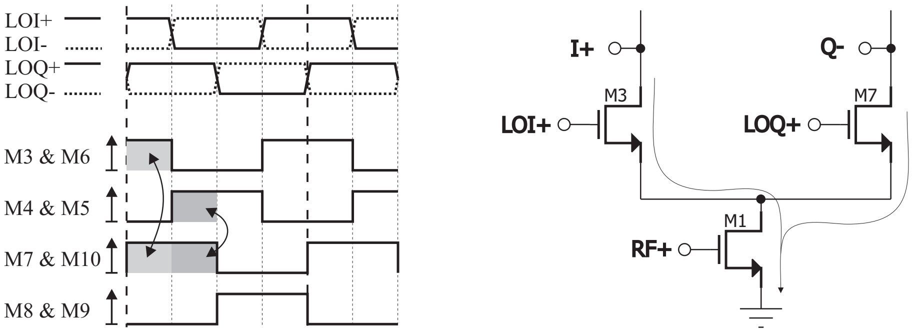

Figure 3.18: Illustration of switching currents (left) for a square-wave LO signal. The schematic (right) is simplified and shows only half of the active branches.

The significance of an amplitude imbalance in the LO signal is much less for a sinusoidal LO signal. In this case the transistors only share current for a fraction of the LO cycle which reduces the effect of the imbalance. Using sinusoidal LO signals also provides for a noise advantage over the traditional approach where two separate mixers are used to form the quadrature output. As Figure 3.19 illustrates only one output branch is conducting at any time when the mixer is driven by large sinusoidal signals. In this case the majority of the noise originates from the input stage and since this stage is shared, the noise contributions to the I and Q branches are correlated with a resulting 3dB noise figure improvement over the traditional approach.

3.1-2 Input Stage

To feed the input stage an on-chip balun is used. A balanced input signal may easily be obtained using an off-chip balun or a SAW filter with a balanced output. However, to evaluate the performance of an on-chip balun and to pertain flexibility the on-chip approach is chosen in

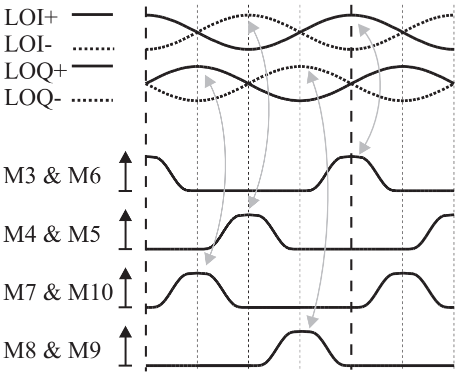

Figure 3.19: *Illustration of switching currents for a sinusoidal LO signal.*

spite of this. The implemented balun is formed by placing two octagonal inductor with two windings each in an intertwined and symmetric layout as shown in Figure 3.20.

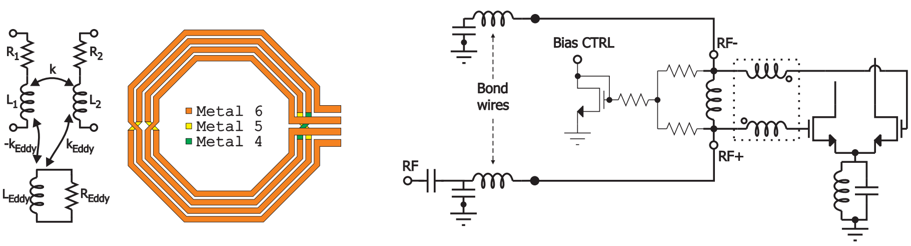

Figure 3.20: *Simulation model and layout for the on-chip balun (left) and an illustration of the input scheme for the mixer (right).*

A number of simulations is conducted on the layout using Agilent's ADS/Momentum to establish an accurate lumped component model for the balun. Based on simulations the coupling coefficient, k, is found to be approximately 0.7 and the Q factor is found to be approximately five. From these results it is clear that the poor coupling and the low Q of the balun could compromise the mixer performance. To compensate for this a third inductor is included to form a tapped impedance transformator where the balun inductors are connected in series with the gates of the input stage.

3.1-3 Measurement Results

The final mixer is wire-bonded to a PCB for testing. During gain, noise, and IP2 measurements a differential-to-single-ended instrumentation amplifier is used to provide a single-ended output from the mixer. The amplifier is needed to evaluate even-order distortion performance but it is not necessary for odd-order distortion measurements. To ensure that IP3 measurements are not affected by the amplifiers, these are therefore omitted for that particular measurement. To provide the balanced quadrature LO signal a design based on three resistive equal-power dividers and microstrip delay lines is used.

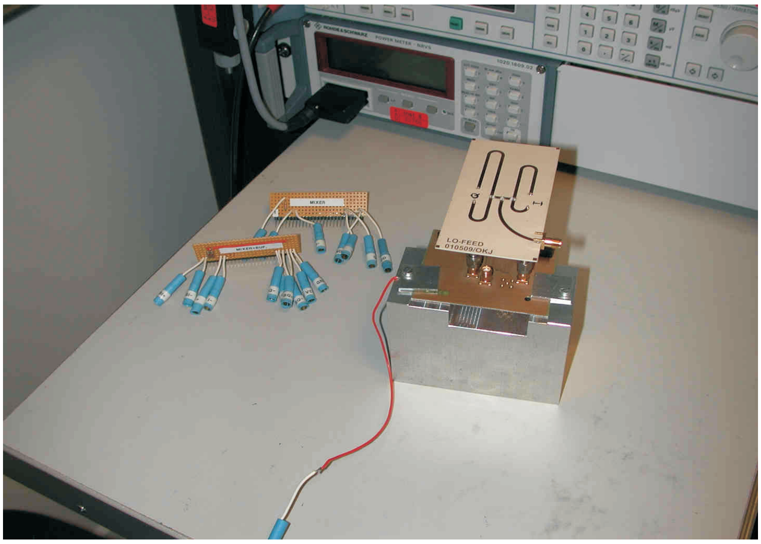

Figure 3.21: *Photo of the measurement set-up showing the LO feed circuit on top of the mixer PCB.*

The LO feed circuit, illustrated in Figure 3.21, provides for a simple generation of the required four-phase LO signal. However, the LO feed is found to be very sensitive and consequently the signal balance is reduced. When measured, the LO feed is found to display a gain imbalance of approximately 0.7dB. This imbalance adds directly to any mixer imbalance and all measurements where I and Q channel performance is compared show a significant imbalance. As an example the voltage gain presented in Figure 3.22 shows a measured imbalance of 1 – 1.2dB between I and Q branches with the highest gain in the I branch.

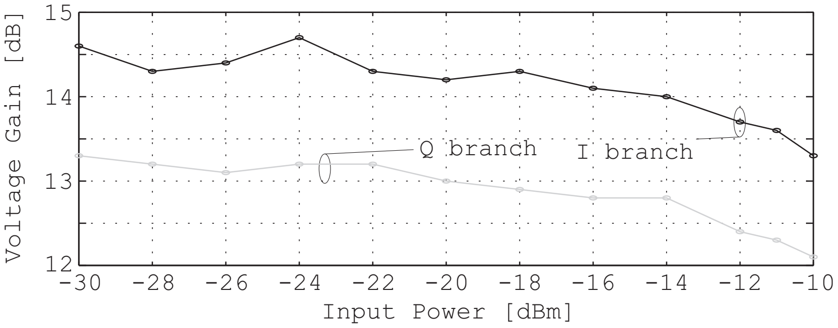

Figure 3.22: *Measured conversion gain versus input power level.*

With the LOI and LOQ signals interchanged the measured mixer imbalance drops to approximately 0.7dB with the Q-branch displaying the highest gain. By comparison, interchanging the LO signals is found to result in an improvement of 0.3 – 0.5dB. Depending on the orientation of the LO feed the overall gain imbalance is found to 1.7 – 1.9dB. Consequently, the majority of the measured gain imbalance may be attributed to the poor balance of the LO feed circuitry. Assuming a first-order relationship the overall mixer gain imbalance is found to 0.3 – 0.5dB.

The imbalance of the LO feed is also reflected in both noise and linearity measurements. The simulated IP2 values listed in Table 3.5 are based on imbalance performance of the LO feed circuit as well as mismatch measurements on the resistive loads. The mean value of the four loads is found to be 226.6Ω which is around 9% less than intended. The minimum and the maximum resistor-values deviate by 0.8% and 1% from the mean value respectively. No transistor mismatch has been included which partly explains the discrepancy between measured and simulated IP2 performance.

Table 3.5: *Input-related performance specifications and measured results for the direct-downconversion mixer. The voltage gain is given at a -26dBm input power level.*

Parameter	**Unit**	**Req.**	**Sim.**	**Meas. (I/Q)**
Voltage Gain	dB	16	16.3	14.4/13.2
NF [10kHz-2MHz]	dB	< 7.6	7.6	7.4/8.5
1dB CP	dBm	> -12	-10	-11/-10
IP2 (15MHz offset)	dBm	–	33	31/28
IP2 (135MHz offset)	dBm	>17	38	26/2
IP3 (10/20MHz offset)	dBm	–	-1.3	-0.8/-1.4
IP3 (67/135MHz offset)	dBm	> -4.7	-0.8	-2.7/-3.1
Input match $\|S_{11}\|$	dB	<-10	<-10	<-10.9
$\|Z_{out}\|$ (Single ended)	Ω	< 300	250	226

In general, the measured results are in good agreement with both requirements and simulations. However, the gain and especially the gain imbalance are found to differ from simulations. Since the mixer topology is sensitive towards amplitude imbalance in the LO signal it is necessary to have an accurate LO feed. Through an improved LO feed it is expected that the gain imbalance may be significantly reduced. With the gain imbalance solved the measurements still display a voltage gain that is 2.5dB less than predicted through simulations. Part of the deviation may be attributed to the absolute error in the load resistors. The noise figure is also slightly higher than simulated. The difference is, however, very small and it is therefore safe to assume that this is due to the reduced voltage gain. Overall, the mixer represents state-of-the-art performance especially for noise and linearity.

3.2 Circuit Isolation and Inductor Design Trade-off

By using a double-balanced mixer topology, port isolation is as good as circuit design techniques allow. Provided that sufficient matching performance is obtained in the circuit the unwanted signal components are ideally canceled. However, leakage is not limited to circuit characteristics only. Leakage also depends on the actual implementation with coupling mechanisms typically being related to substrate carried noise, capacitive coupling, and bond-wire coupling [115]. For silicon technologies coupling through the lossy substrate is an important part of the overall design challenge. However, coupling is not limited to substrate effects and therefore three types of coupling need to be considered; magnetic (inductive), substrate (resistive and capacitive), and coupling via ground current return paths.

3.2-1 Inductor Performance and Guard-Rings

A structure such as the planar spiral inductor gives rise to both magnetic coupling and substrate related coupling. To limit the coupling to and from inductors a guard-ring is generally used to restrict the extension of the fields, as Figure 3.23 illustrates. Having a surrounding guard-ring close to the inductor structure improves the isolation properties but it also degrades the performance by adding capacitive coupling and by restricting the magnetic field. This is illustrated in Figures 3.23a and 3.23c respectively. If instead the guard-ring is placed at some distance to the inductor it affects performance to a lesser extent, as Figures 3.23b and 3.23d illustrate. Often, to present customers with good device performance, fairly large guard-ring distances are used by the IC vendors. Not only does this optimize component performance it also consumes extra die area. Whereas the former is desirable the added area is a significant drawback.

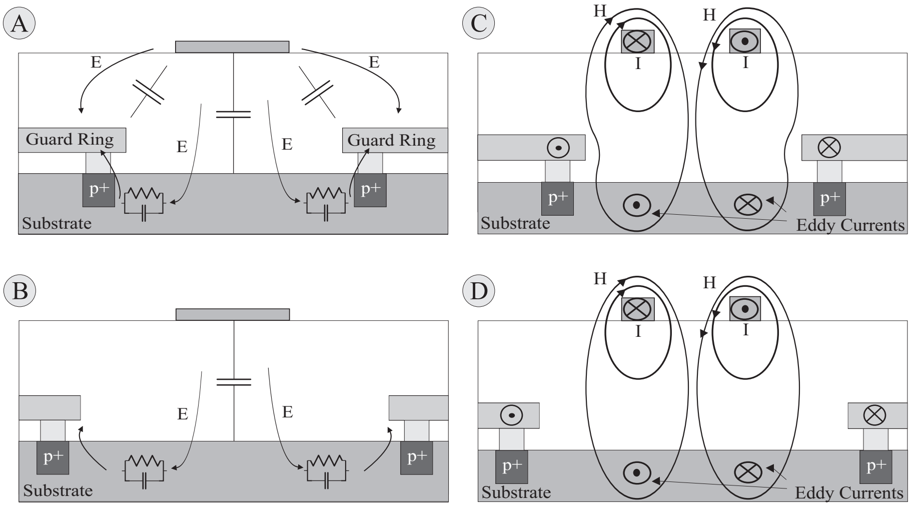

Figure 3.23: *Illustration of electrical and magnetic fields induced by inductors. a) Electrical field for a close guard-ring, b) electrical field for a distant guard-ring, c) magnetic field for a close guard-ring, and d) magnetic field for a distant guard-ring*

To analyze the significance of the distance between inductor and guard-ring the two test structures in Figure 3.24 are designed. The two inductor structures are identical and the only difference is the distance between the outermost winding and the guard-ring. In one case the distance is approximately 10μm while the distance is set to 32μm for the other structure.

To support measurements and to promote an understanding of the general coupling effects in the test structures, a 2.5D simulation model is formed using Agilent Momentum. With some limitations in geometry, this simulator is able to simulate 3D structures. A significant limitation

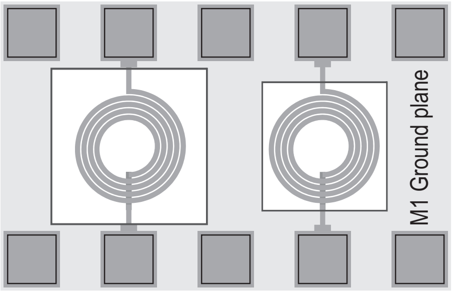

Figure 3.24: *Experimental set-up for measuring and simulating inductor performance as function of the guard-ring distance.*

is that inclusion of a high number of layers results in a very long simulation time. Furthermore, to limit simulation time metal layers of finite thickness must be approximated by sheets of zero thickness. To accommodate this the simulations are based on the substrate definition given in Figure 3.25.

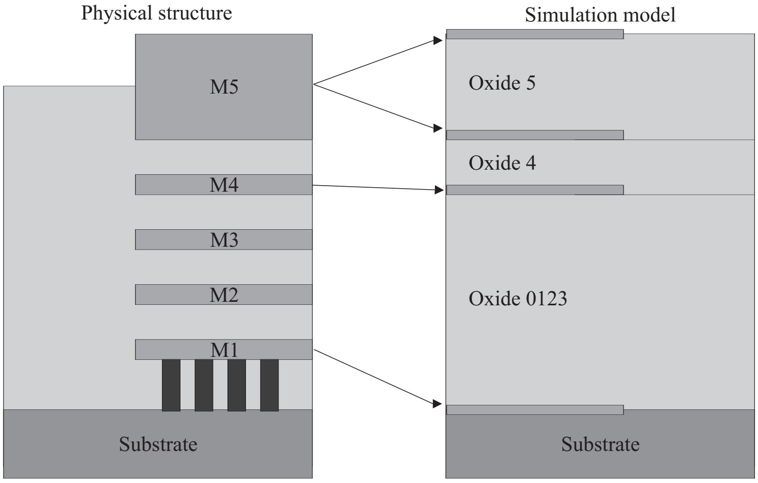

Figure 3.25: *The physical metal layer structure and the simplified structure use during Momentum simulations.*

To make simulations more accurate metal 5 is represented by two sheets of metal in the simulation set-up. The two sheets each have twice the sheet resistance of the metal 5 layer and are subsequently connected in parallel by vias. For metal 4 only a single sheet is assumed to be sufficiently accurate. Metal 1 is used for the guard-ring and it is connected to the substrate by a vast number of contacts. A detailed modeling of these would result in unacceptable simulation times and instead a single sheet is placed directly on top of the semi-conducting substrate. This approach models the main properties of the guard ring; i) a low resistance contact to the substrate is provided for both the physical structure and the model, and ii) a short-circuited ring is present in both cases.

The structures are measured using 2-port S-parameters and the results are subsequently de-embedded to remove effects native to the test fixture. Using a π-type equivalent values for inductance, series resistance, and also Q-factor are calculated. These results are illustrated in Figure 3.26 together with the corresponding simulated values.

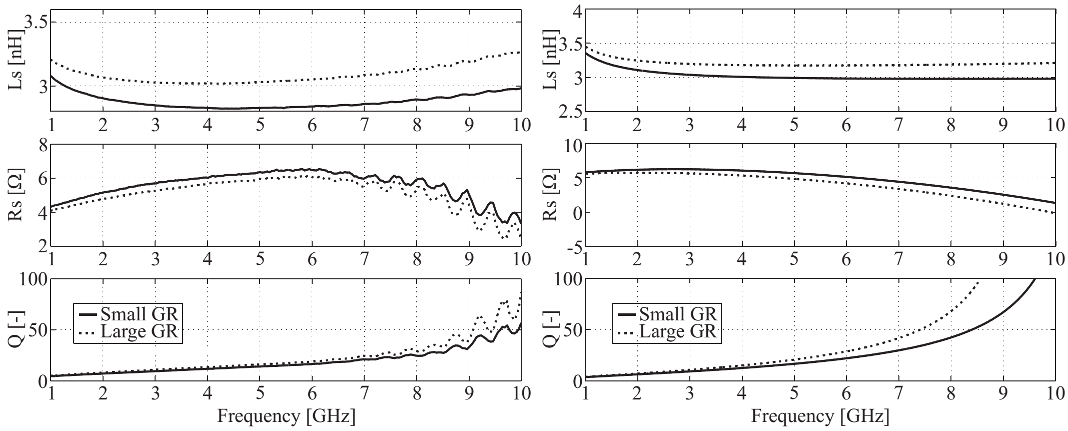

Figure 3.26: *Measured (left) and simulated (right) inductor performance for two different guard-ring distances.*

Simulation results are found to be in reasonable agreement with measurements. Most noticeable is the different shapes of the inductance curves. The simulated values seem to remain constant for increasing frequency while the measured inductance values are found to increase with frequency. This may be explained by the limitations of the simulation model. In the model the series capacitance is significantly underestimated due to zero thickness of metal layers. The measured results include a significant fringing capacitance between the windings.

From Figure 3.26 the guard-ring is found to have a significant impact on inductor performance and as expected the inductance value decreases as the guard-ring is moved closer to the inductor. The results from measurements and simulations are summarized in Table 3.6 for a frequency of 2GHz. From these numbers it is found that approximately 6% reduction in inductance value results from the reduced guard-ring distance. The equivalent reduction in measured Q factor is found to be 16%. A 6% reduction in inductance is not a severe problem, however, a 16% reduction of the Q factor is a significant degradation especially since Q factors are generally low for CMOS inductors. When measurements and simulations are compared a deviation around 6 – 13% is found. This indicates that the Momentum simulations are fairly accurate.

Table 3.6: *Inductor parameters for different guard-ring distances.*

	L_s [nH] @ 2GHz			Q [–] @ 2GHz		
	Meas.	**Sim.**	**Dev.**	**Meas.**	**Sim.**	**Dev.**
Small GR	2.9	3.1	6.4%	7.2	6.4	10.8%
Large GR	3.1	3.3	5.7%	8.5	7.4	13.0%
GR effect	5.8%	5.1%		16.0%	13.8%	

3.2-2 Inductor Crosstalk

Considering that inductor Q factors already represent a bottleneck for RF-CMOS design any degradation must be prevented. Degradations as those listed in Table 3.6 are unacceptable. For performance reasons it is therefore mandatory that a sufficiently large distance is kept between inductor and guard-ring. For cost reasons the distance needs to be kept at a minimum in order to reduce the die area. Such considerations clearly form a trade-off in the design of on-chip inductors. It is therefore interesting to determine whether a guard-ring is required in the first place. To do this the isolation properties between two inductors need to be evaluated as function of both distance and use of guard-ring. To do this the experimental set-up illustrated in Figure 3.27 is used. The set-up consists of two almost identical inductor structures based on a squared structure where metal layer 5 (M5) is used to form the coil and M4 is used for the under-pass. For the transmitter inductor (TX), 4.25 turns are used while all receiving inductors (RX1 - RX4) are using 4.5 turns. The inductors are placed in two set-ups, one where all RX inductors use guard-rings and one where no guard-rings are used. Each test fixture has a M1 ground-ring surrounding the devices to provide good grounding. Further, when measured from center to center, the distance between the TX and RX structures are 190, 490, 790, and 1090μm respectively.

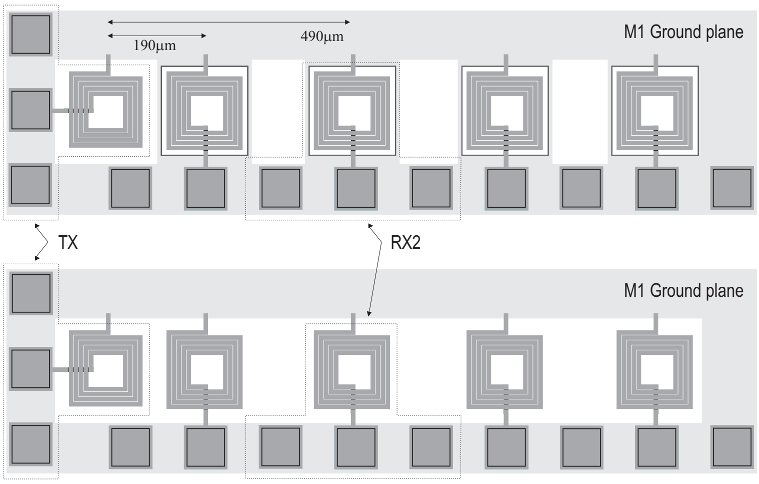

Figure 3.27: *Experimental set-up for measuring and simulating inductor isolation when using guard-rings (top) for RX structures and when not using guard-rings (bottom).*

Again a set of EM-simulations is conducted to support the measurements. For the isolation simulations the same substrate set-up as illustrated in Figure 3.25 is used. The resulting simulations and measurements for structures with and without guard-rings are presented in Figure 3.28. All measurements are illustrated using solid lines while the corresponding 2.5D simulations are presented using dashed lines.

For both types of structures the simulations are found to match measurements very accurately for most of the frequency range. At low frequencies (<2GHz) relatively large deviations are seen for structures RX2 - RX4 when guard-rings are used. For these structures the isolation level

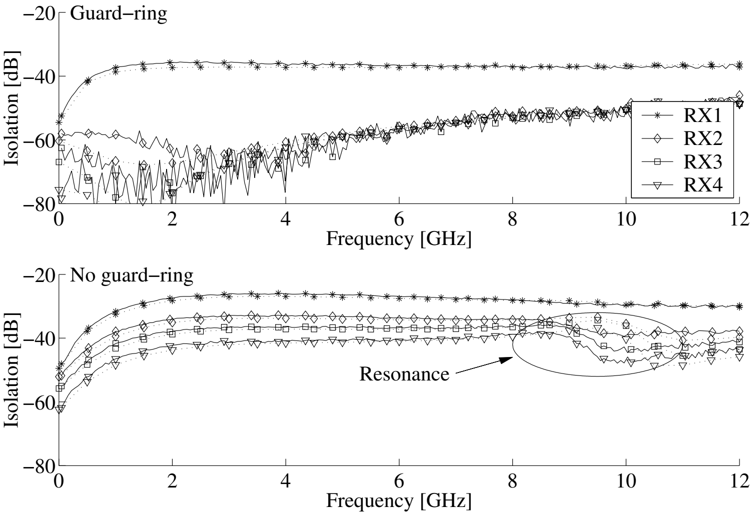

Figure 3.28: Measured (solid) and simulated (dotted) isolation performance for structures with (top) and without (bottom) guard-rings.

is around -60 to -80dB which makes measurement a non-trivial task. At approximately 9GHz a sudden drop in isolation is seen for structures RX2 - RX4 when no guard-rings are used. The explanation for the unexpected drop is found in the unused floating inductor structures. When left floating, the inductor is loaded by the pad capacitance. This forms a resonance circuit with a resonance frequency of approximately 9GHz. This effect is also found in the simulation results where the phenomenon is shifted slightly up in frequency in comparison to measurements.

The added isolation provided by the guard-ring is found to be as high as 40dB at around 2GHz. Considering the structures without guard-rings distance is found to have only a minor effect on the isolation performance. Here an improvement of around 6 - 7dB is the result of moving from RX1 to RX2. For RX3 and RX4 the improvement is around 10dB and 15dB respectively. This performance appears to be independent of frequency as the only change may be attributed to the resonating unused inductors. Based on further analysis the results shown in Figure 3.28 are found to ignore an important effect resulting from inductive coupling. It can be shown that a significant part of the coupling results from coupling between TX inductor and the test fixture. Due to the structure of the test fixture the metal ground shield acts as a ground-ring surrounding all the inductor structures. The current induced in the ground-ring subsequently couples to the RX inductor, hence the overall coupling is significantly increased. This has been validated through simulations as well as measurements. To enable the latter, samples were subject to laser cutting to prevent the ground-ring current path. The aim here is to evaluate the effect of having a ground-ring surrounding the entire test structure as is the case with M1 in Figure 3.27. Having good grounding is normally used in RF circuits and measurement set-ups. However, for coupling measurements the layout of the ground plane turns out to be very important. The result of the laser cutting operation is illustrated in Figure 3.29 where the cut marks are clearly visible.

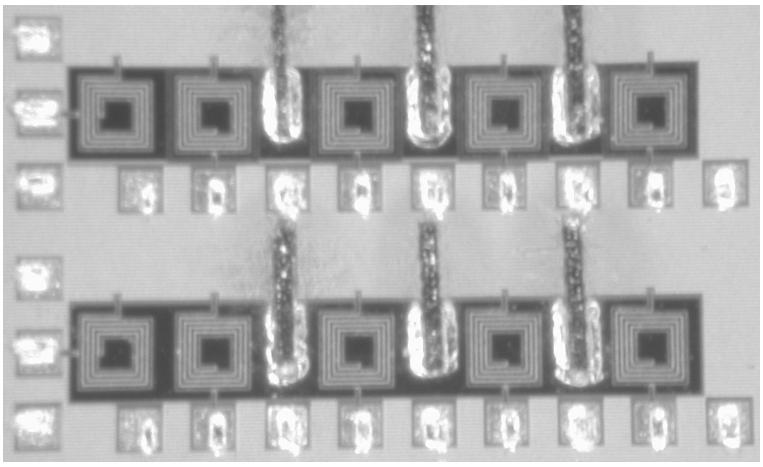

Figure 3.29: *Chip photo of experimental set-up after laser cutting of the fixture ground-ring.*

Results from isolation measurement based on structures exposed to laser cutting are shown in Figure 3.30. When comparing the results in Figure 3.30 with the results presented in Figure 3.28 it is clearly seen that the ground-ring is responsible for a significant percentage of the combined coupling. For RX1 the difference is hardly noticeable whether a guard-ring is used or not. For the remaining structures the change is significant, especially for structures that are not using guard-rings. Here as much as 15 to 25dB of additional coupling results, depending on distance and frequency.

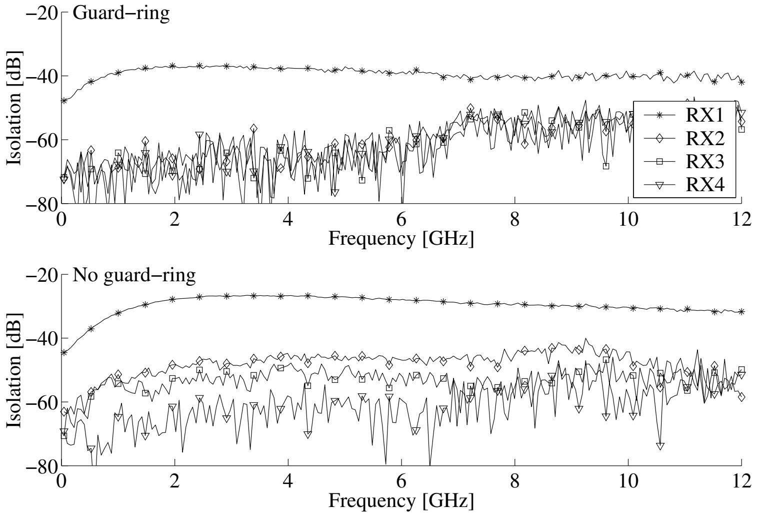

Figure 3.30: *Measured isolation performance for structures with (top) and without (bottom) guard-rings where the test fixture ground-ring is cut.*

Since the ground-ring affects structures with and without guard-rings very differently this is also going to be reflected when evaluating the effect of using a guard-ring. For the structures exposed to laser cutting the improvement in isolation as function of distance and use of guard-ring is plotted in Figure 3.31. Based on the results in Figure 3.31 the isolation performance as function of distance is found to have changed significantly. The guard-ring structures are found to provide equal performance independent of distance. A peak isolation of around 30dB is found for frequencies up to 4GHz. For structures without guard-rings an improvement of around 15 - 20dB is the result of moving from RX1 to RX2. For RX3 and RX4 the improvement is around 25dB and 30 - 40dB respectively. This is a significantly different result than what may be derived from Figure 3.28. The result from having simple guard-rings is seen from the bottom graph of Figure 3.31. For RX1 the improvement is fairly constant over frequency with a peak improvement of around 11dB at 7GHz. For RX2 and RX3 the improvement is found to be around 15 - 20dB up to 6GHz. As the frequency is increased the gain drops down to approximately 10dB for RX2 while RX3 appears to gain almost nothing from having a guard-ring. For RX4 the guard-ring is found to have almost no effect on the isolation performance. From these results it is clear that the test fixture ground-ring contributes significantly to the coupling, especially for structures without guard-rings. As a result of this the guard-ring appears to have a significantly higher effect on isolation when the ground-ring is left intact during measurements. Depending on frequency and distance the effect of the ground-ring may be as high as 20dB.

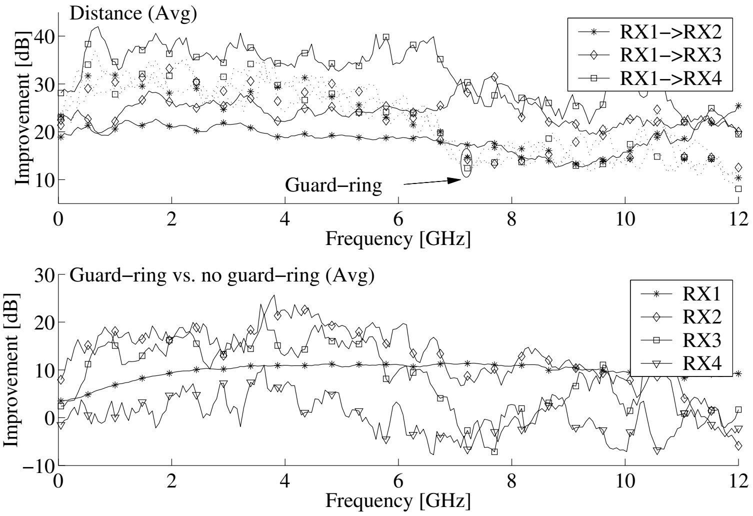

Figure 3.31: *Measured improvement in isolation as a function of distance (top) and use of guard-rings (bottom) where the test fixture ground-ring is cut. For the distance plot guard-ring structures use dotted lines.*

To include crosstalk effects in the design of RFIC circuits it is important to have an accurate model that may be used in circuit simulations. To evaluate the crosstalk between two planar inductor structures the simple substrate model shown in Figure 3.32 is often used. In this model the coupling is assumed to result from only substrate carried effects. Part of the inductor current couples to the substrate via C_{ox} where it appears as a surface current. This surface current eventually couples partly to another inductor. To model the level of coupling an RC path ($R_c||C_c$) is included as Figure 3.32 shows.

This model is found to be insufficient and to overcome this a more accurate description of the

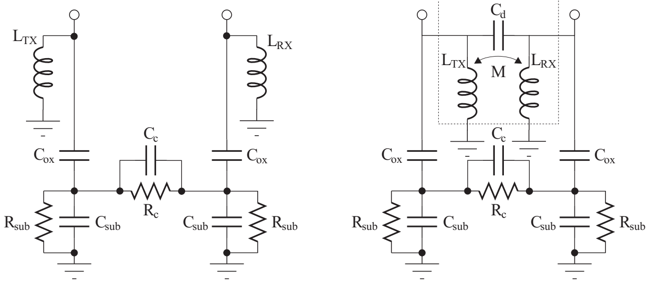

Figure 3.32: *Lumped element equivalent circuits describing the crosstalk between two devices; simple model (left) and extended model (right).*

crosstalk is needed. To accomplish this a capacitor (C_d) and two mutual coupled inductors (L_1 and L_2) are added to include additionally two sources of crosstalk. The resulting and more accurate model is shown in Figure 3.32.

The model parameters are fitted to the measured s-parameters for the structures exposed to laser cutting. The resulting performance of the developed model is shown in Figures 3.33 and 3.34 together with measurement for both structures with and without the use of guard-rings. From these results the model is seen to fit measured data very nicely which speaks in favor of the extended model.

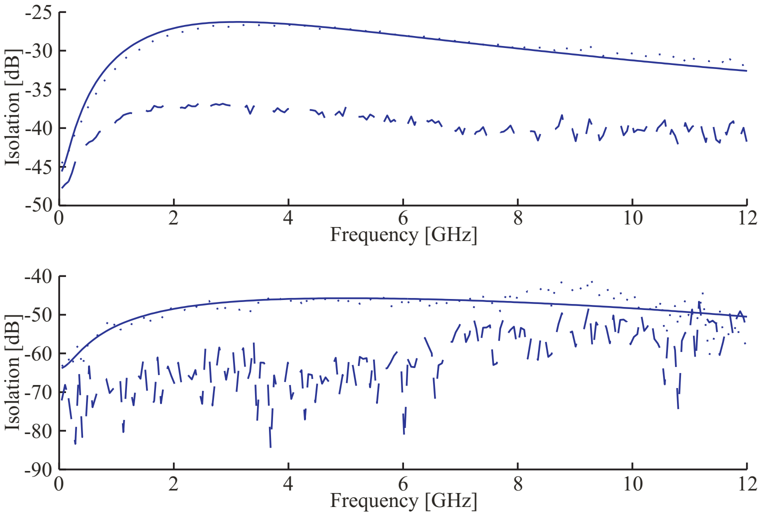

Figure 3.33: *Isolation performance for RX1 (top) and RX2 (bottom). Results are for structures without guard-ring (dotted), with guard-ring (dashed), and prediction based on lumped component model (solid).*

3.3 Summary

Based on a set of mixer requirements a quadrature direct-downconversion mixer for a UTRA/FDD receiver is designed and implemented. Overall the measured results are in good

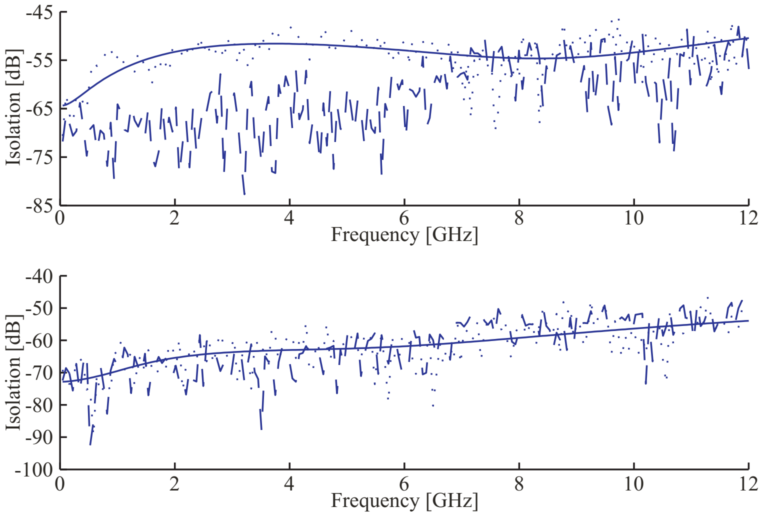

Figure 3.34: *Isolation performance for RX3 (top) and RX4 (bottom). Results are for structures without guard-ring (dotted), with guard-ring (dashed), and prediction based on lumped component model (solid).*

accordance with simulations. Only for the gain and especially the imbalance a significant difference is observed. The mixer is sensitive towards imbalance in the LO voltage levels and it is therefore necessary to have an accurate LO feed. With a well-balanced LO feed it is expected that I and Q gain mismatch is reduced significantly.

To minimize signal leakage, guard-ring structures are generally used in inductor designs. While guard-rings improve isolation they also form a trade-off between device area and performance. To analyze this trade-off the effect of having guard-rings in different distances to the device perimeter is evaluated. It is found that a decrease of the guard-ring distance results in a reduction of inductance value as well as an increase of series resistance. Both these factors combine to reduce the Q value of the device. In the presented case, a decrease of 35% in die area results in a Q value reduction of approximately 16% up to 2GHz.

To determine whether the use of guard-rings is justified a number of isolation measurements is conducted using structures with and without guard-rings. Further, the impact of guard-rings is evaluated at different distances between inductors. Different coupling effects for CMOS on-chip co-planar spiral inductors are presented. Based on simulations and measurements the test fixture is shown to have a significant impact on coupling measurements. Taking the test fixture into account, an extended lumped element model is developed and found to fit very well with measurements. Further, simple guard-rings are shown to improve isolation between closely spaced adjacent inductors by approximately 10-15dB. At larger distances the gain of having a guard-ring reduces and is eventually found to be zero at a distance of 1000μm. For closely spaced devices a doubling of distance is found to provide an additional 20dB attenuation of crosstalk.

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Papers

Evaluation of CMOS Front-End Receiver Architectures for GSM Handset Applications

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IEEE International Symposium on Communication Systems and Digital Signal Processing (CSDSP)
Sheffield Hallam University, Sheffield, England, pp. 164 – 167, April 1998.

Evaluation of CMOS Front-End Receiver Architectures for GSM Handset Applications *

Jan H. Mikkelsen

Abstract

This paper analyses two front-end receiver architectures intended for GSM900 use; (i) A direct-conversion receiver, and (ii) a low-IF receiver using a poly-phase filter. The aim is to determine the circuit performance required for GSM operation and to compare this to current state-of-the-art CMOS performance. The analysis shows that direct-conversion receivers fail to meet specifications when based on of-the-shelf CMOS circuits. The main reason being noisy baseband stages and lack of RF gain. When based on equivalent CMOS performance the low-IF receiver presents a promising solution to fully integrated CMOS receivers for GSM.

1 Introduction

The demand for ever more efficient communication system implementations increases constantly. The ultimate research goal is represented by a single-chip transceiver concept where no off-chip components are present. The analog front-end here imposes problems. To solve this, effort is required in all levels of integrated design; component modeling, circuit implementation, and system level design. Already, the push towards fully integrated radio receivers has lead to new developments in circuit design and architectures [9]. Especially IF digitization has been the aim of much attention. The benefits of pushing the analog/digital interface towards the antenna are evident; simplification of analog design, reduction of power consumption, higher degree of integration, and reduced cost [2]. Often, however, realizing integrated telecommunication system requires integrated circuit implementations of key blocks yet not available.

This paper analyses two front-end receiver architectures for GSM; (i) A direct-conversion receiver, and (ii) a low-IF receiver using poly-phase filtering. The aim is to determine the performance required for the different receiver blocks and compare the results for the two architectures. The block performance required by the architectures are also compared to actual performance from state-of-the-art CMOS implementations. The obtainable receiver performance is evaluated trough simulations and compared to GSM-specifications [4].

2 Basic GSM900 System Requirements

In complying with the GSM specifications basic radio performance requirements such as noise figure (NF), third order input referred intercept-point (${}_iIP_3$), local oscillator (LO) phase noise, and dynamic range must be known. The measures listed in Table 1 are found using co-channel interference requirements.

NF	${}_iIP_3$	LO Phase noise	DR	Img. Rej.
< 10 dB	> -19.5dBm	-141dBc/Hz@3MHz	92dB	65dB

Table 1: Basic GSM900 front-end requirements as derived using co-channel requirements.

The receiver must also handle large blocking signals while receiving a wanted signal at -98 dBm. Here the maximum requirements are -23 dBm and 0 dBm for in-band and out-of-band interferers, respectively. This input scenario places significant requirements on the filtering and dynamic range performance of the receiver, hence, the wide spread use of the traditional super-heterodyne receiver architecture. This well known architecture is based on the concept of repeatedly amplification, frequency down-conversion, and filtering. This approach is not implementable in CMOS – due to high demands on analog filters – and hence other alternatives must be considered. The LO phase noise requirement of Table 1 is not pursued further in this paper.

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[*] Paper published in Proc. of IEEE First International Symposium on Communication Systems & Digital Signal Processing (CSDSP), Sheffield Hallam University, Sheffield, England, pp. 164-167, April 1998.

3 Direct-Conversion Receiver Architecture

The direct-conversion receiver in Figure 1 converts the RF signal directly to baseband in one single step. This approach reduces the use of high frequency signal-processing as most amplification and filtering take place at low frequencies. The conceptual direct-conversion architecture thus presents a power efficient approach to receiver design.

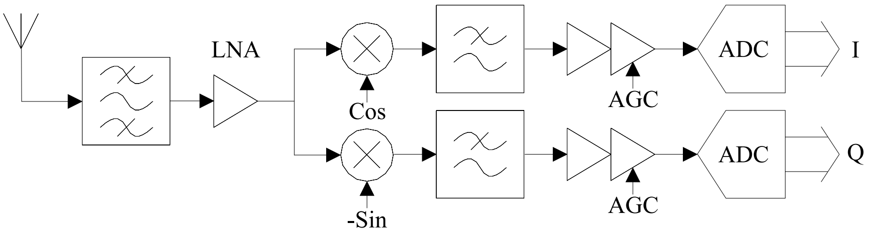

Figure 1: Direct-conversion receiver architecture.

It is of particular concern in a direct-conversion receiver to meet sensitivity requirements as only a moderate gain is located at RF. Very low noise operation is called for in all RF circuits including the mixer. Also, generally, a large LNA gain is required to overcome the inherently larger mixer noise. On the other hand, too large a gain may cause the mixer to overload. In both cases the receiver dynamic range is compromised. Typical CMOS parameters for circuit blocks suited for a 900MHz direct-conversion receiver are illustrated in Table 2.

Zero-IF	RF-filter	LNA [5]	Mixer [5]	Filter [1]	BB-Amp.	TOTAL
Gain [dB]	-3.2	15.6	8.8	24	60	95.2
NF [dB]	3.2	2.8	9.7	33	30	16
${}_iIP_3$ [dBm]	∞	-3.2	-4.1	30	30	-15.5

Table 2: Typical CMOS performance measures for a 900MHz direct-conversion receiver.

Table 2 results in a receiver with an overall noise figure of 16dB and an ${}_iIP_3$ of -15.5dBm. Hence, the receiver fails to meet the sensitivity requirement. This is a direct result of moderate RF gain and noisy baseband filter. The filter alone adds 11.8dB to the overall noise figure with the current RF gain.. As such the mixer noise is not the sensitivity bottleneck in direct-conversion receivers. When based on of-the-shelf CMOS performance direct-conversion receivers provide for noise factors in the range of 16dB to 21dB and ${}_iIP_3$'s of -16dBm to -10dBm . The LNA gain must be raised to combat the low sensitivity. Here more than 33dB LNA gain is required to meet sensitivity requirements only now compromising receiver ${}_iIP_3$. Calculations indicate this to be a general problem in CMOS direct-conversion. For the down-converting mixer not to represent the bottle-neck in terms of receiver linearity, its ${}_iIP_3$ should be at least a factor better than that of the preceding LNA [7]. For reasons of dynamic range the LNA must provide for a 1dB compression point better than -15dBm corresponding to a ${}_iIP_3$ of approximately -3dBm. This implies a mixer ${}_iIP_3$ better than 9dBm, hence, the mixer in Table 2 needs to be replaced by a mixer topology having a more linear RF-to-IF transfer function. Generally, highly linear mixers, such as sub-sampling mixers and R_{on} modulating mixers, display poor noise performance [7]. In a traditional receiver this would set LNA gain specifications. However, due to its high noise contribution the baseband filter sets LNA gain specifications in a direct-conversion receiver. Moving channel selection filtering to baseband reduces RF filtering requirements at the expense of increased RF amplification. Relaxing the baseband filtering reduces the noise contribution but it also increases the dynamic range requirement of the ADC. Already, the 5'th order baseband filter in Table 2 requires 30dB ($\approx$5bit) extra dynamic range performance of the ADC in order to meet adjacent channel requirements. Besides, the single most important reason to the limited use of direct-conversion in commercial available products is DC-offset. Direct-conversion receivers suffer from both LO-leakage and DC-offset resulting in both static and dynamic DC-offset contributions. The mean value of the DC-offset at the CMOS mixer output is as high as 3mV [7]. This represents a severe design problem for GSM where signal information is located at DC and low frequencies.

4 Low-IF Poly-Phase Filter Receiver Architecture

The low-IF receiver in Figure 2 converts the received RF signal to a low intermediate frequency whereby the 1/f noise problem is mitigated. The low-IF receiver architecture reintroduces the concept of image-rejection. This is of significant concern for low-IF where no image-rejection takes place at RF. However, by allowing for the down-conversion take place in quadrature – as for the direct-conversion receiver – the image-rejection may be postponed until after the down-conversion.

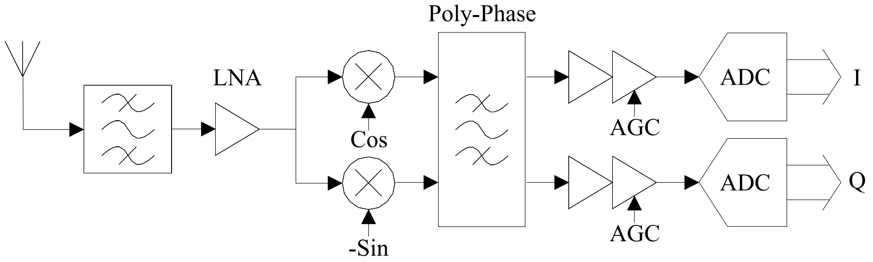

Figure 2: Low-IF poly-phase filter receiver architecture.

Quadrature down-conversion generally provides for 20 - 40dB's of image-discrimination [6]. 1° phase imbalance results in -35dB discrimination. For the quadrature down-converter alone to meet with the specified 65dB image-rejection an unachievable phase match of 0.03° or better is required. Also, with an image-signal power level 56dB above that of the desired 9bit extra ADC resolution is required to handle image-signal dynamics. Additional image-rejection must be implemented prior to digitization to reduce ADC requirements. This may be implemented using an asymmetric poly-phase filter with passband from positive (+90°) to positive frequencies and stopband from negative (-90°) to negative frequencies. Also, poly-phase filters reduce the effect of phase and gain imbalance in the quadrature down-converter. Typical CMOS parameters for circuit blocks suited for a 900MHz low-IF receiver using a 250kHz IF are illustrated in Table 3.

Low-IF	RF-filter	LNA [5]	Mixer [5]	IF-Filter [3]	BB-Amp.	TOTAL
Gain [dB]	-3.2	15.6	8.8	18.8	60	97
NF [dB]	3.2	2.8	9.7	25^*	30	10
$_iIP_3$ [dBm]	∞	-3.2	-4.1	1^*	30	-19

Table 3: Typical CMOS performance measures for a 900MHz low-IF receiver. Values indicated by $*$ are not actual reported measures but performance limits that must be complied with for the receiver to comply with NF and $_iIP_3$ specifications.

Migration from zero-IF to a low-IF of just 250kHz alone provides for at least the required 8dB noise factor reduction. In fact, crude extrapolations from equivalent order zero-IF filter noise figures estimate a noise figure of approximately 18dB. Based on this approximation receiver noise figures around 8dB are achievable using of-the-shelf CMOS designs. Meeting receiver linearity requirements is readily accomplished using current CMOS performance.

5 Results and Discussion

To compare the obtainable receiver performances a number of simulations are carried out. This also gives indication of the receiver architectures potentials in relation to GSM. Based on adjusted circuit specifications the results listed in Table 4 are obtained. Limitations of the simple hard-decision data-detector affect FER and RBER Class Ib measures. These are hence not ideal for evaluating front-end performance alone, however, they allow the results to be related to GSM requirements. RBER Class II provides a better measure of front-end performance. The simulations show that the low-IF performs significantly better than the direct-conversion receiver. This difference causes the direct-converter to fail GSM sensitivity test specifications on RBER Class II bit errors while the low-IF receiver passes. One explanation for this is the better overall receiver noise figure achievable using low-IF. Also, low-IF displays better selectivity towards adjacent channels than direct-conversion, especially when I/Q imbalance is included.

Test	Architecture	FER [%]	RBER Class Ib [%]	RBER Class II [%]
Sensitivity	Zero-IF	0.18	0.17	3.08
	Low-IF	0.04	0.02	1.50
Sensitivity*	Zero-IF	0.12	0.18	3.18
	Low-IF	0.02	0.02	1.62
Adj. Channel	Zero-IF	0.22	0.20	1.68
	Low-IF	0.00	0.00	0.38
Adj. Channel*	Zero-IF	0.44	0.23	2.00
	Low-IF	0.00	0.00	0.40

Table 4: Simulation results based on hard decision detection and static channel profiles. Simulations marked with * include down-converter phase and gain imbalance of 1° and 1dB, respectively.

6 Conclusion

These initial investigations indicate that an all CMOS receiver solution for GSM900 is indeed realistic. Of the two architectures analyzed the low-IF is the most promising. Large RF gain is required for the CMOS direct-conversion receiver to comply with sensitivity requirements. Meeting such LNA gain requirements is very difficult as low noise and high linearity must be preserved. LNA gain requirements rather than DC-offset limits the use of CMOS direct-conversion. This results as the dynamics of CMOS DC-offset resemble that of equivalent bipolar designs where the problem has been solved [8]. Still, LNA gain requirements compromise the inherent low-power potential of the direct-conversion receiver. Low-IF represent a low-power solution as less RF gain is required. Also, low-IF receivers meet basis GSM requirements when based on current CMOS designs. Complete integration of receiver blocks is of course not trivial, however, the use of poly-phase filters present low-IF as a realistic solution to an all CMOS integrated GSM900 receiver. Increasing the accuracy of simulation models is part of the future work on analyzing the potential of low-IF receiver architectures.

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CMOS Technology Adjusts to RF Applications

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CMOS Technology Adjusts To RF Applications

Continuing progress in processing techniques is facilitating the application of CMOS well into the 2-GHz operating range.

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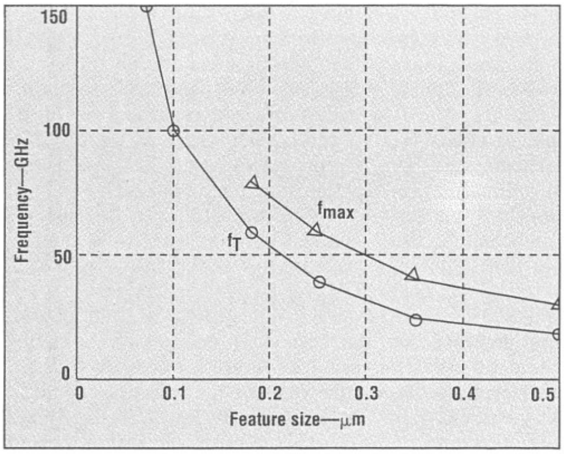
RECENT advances in complementary-metal-oxide-semiconductor (CMOS) technology are expected to make it a viable option for RF designs into the 2-GHz range. This may make CMOS a strong contender for implementing transceivers in the International Telecommunications Union's (ITU's) proposed IMT-2000 global wireless system. Among the advantages promised by CMOS realization of RF circuits are low fabrication costs and easier integration with digital circuitry.

As Europe is finalizing its move to the IMT-2000 radio-access standard, it is clear that future mobile terminals will have much greater complexity than current second-generation terminals.[1] The significant increase in complexity is due primarily to much higher data rates, the need for multimode and multiband operation, as well as the availability of more-versatile terminal software to support multimedia applications. The software-radio concept is suggested as a basis for these new terminals in order to avoid extensive use of parallel hardware and to enhance flexibility. The main idea behind the software radio is that radio parameters are downloaded to the terminal from the wireless network. In a manner transparent to the user, the terminal adapts to local radio characteristics such as modulation as well as source coding. Hence, the software-radio architecture is capable of meeting the demands for terminal versatility required in a global communications system.



Measured FET f_T and f_{max} values are shown as functions of feature size. Since conflicting values have been reported for feature sizes below 0.18 μm, these results are not included.

This approach, however, requires a change in the design of the wireless terminals that are currently in use. For IMT-

Achievable RF performance for passive devices in CMOS technology

Component	Value	Accuracy	Performance
Resistors			
Polysilicon	5 to 10 Ω/square	30 to 40 percent	Good linearity
Well (n or p)	1 to 10 Ω/square	50 to 80 percent	Large parasitics and voltage coefficient
Inductors			
Bondwire	1 to 5 nH/mm	1 to 100 percent	Q ~ 60 at 2 GHz
Spiral	1 to 10 nH	5 to 10 percent	Q ~ 3 to 6 at 2 GHz
Enhanced spiral	1 to 100 nH	3 to 5 percent	Q ~ 7 to 9 at 2 GHz
Capacitors			
Fractal	1 to 2 fF/μm^2	2 percent	Q ~ 60 at 2 GHz
MOS	1 to 5 fF/μm^2	15 percent	Q ~ 15 at 2 GHz
MIM	50 to 200 aF/μm^2	20 percent	Q ~ 30 at 2 GHz

2000 to be attractive to operators as well as end users, terminals must be lightweight, small, and inexpensive. In addition, they must provide extensive standby and operating times. Hence, integrated-circuit (IC) technology is the key to enabling a viable development toward IMT-2000.

Another aspect to consider is that the software radio leads to greater use of digital circuitry in order to enhance flexibility. Considerable attention has recently been given to the use of silicon processes in order to enable a fully integrated solution that supports digital and analog high-frequency circuitry. Recognizing that IMT-2000 will not exceed operating frequencies of slightly more than 2 GHz, a full-silicon solution should be plausible. Many silicon processes have evolved, but it is generally believed that CMOS will provide the best solution if its current limitations are solved.[2]

TECHNOLOGY TRENDS

Recent achievements in semiconductor technology make the RF capability of CMOS technology more evident than ever. If CMOS technology can adjust to RF needs, it has the potential of dominating digital and RF analog design. The enormous market potential for a system such as IMT-2000 provides a good reason for CMOS plants to make the necessary adjustments. Furthermore, as digital microprocessors cross the 1-GHz boundary, digital circuitry now requires technology enhancements which were considered exotic analog features a few years ago.

To specify the special needs for high-frequency operation, the RF performance of semiconductor processes is typically measured with respect to the active devices [i.e., the field-effect transistors (FETs)]. This method is used despite the fact that passive devices in CMOS also constitute some fundamental problems for high-frequency operation. In RF terms, the primary performance parameters are the unity-current-gain frequency (f_T) and the maximum oscillation frequency (f_{max}). As a conservative rule of thumb, each of these parameters should be at least 10 times greater than the maximum system frequency in order to ensure sufficient gain. For RF designs in the 2-GHz range, f_T and f_{max} values above 20 GHz are therefore required.

In digital ICs, critical parameters such as speed, power consumption, and yield are directly improved by downscaling. However, RF IC design also requires good performance in terms of gain, noise, linearity, and power efficiency. These parameters are not necessarily improved as the minimum feature size is reduced.

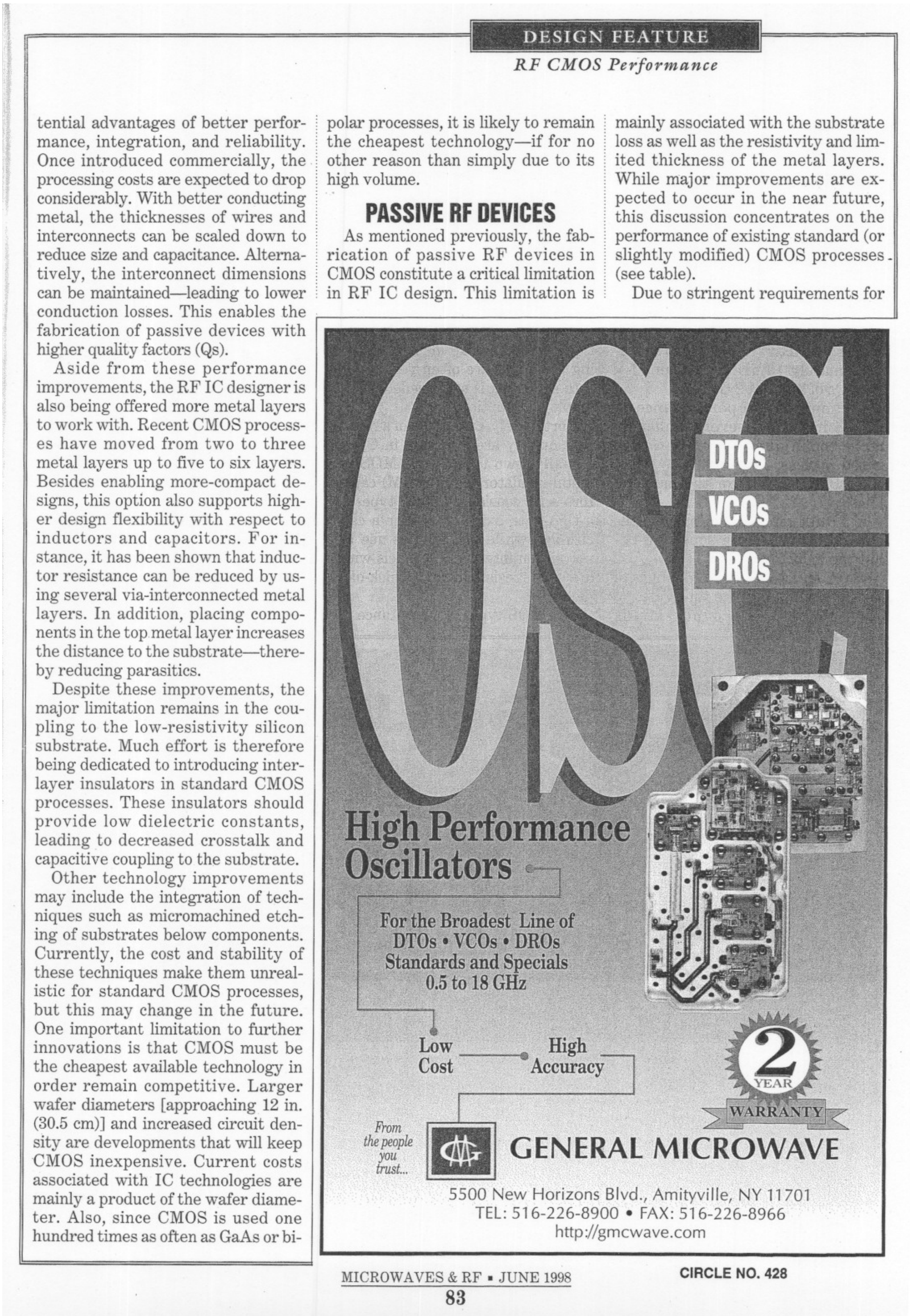
The major achievement in CMOS process technology has been the decrease of the minimum feature size into the deep-submicron area (now approaching 0.1-μm feature size). In fact, the Semiconductor Industries Association (SIA), which periodically makes forecasts regarding the future of the IC industry, has started defining processes in terms of nanometers rather than micrometers.[3]

This downscaling into the deep-submicron range leads to f_T and f_{max} values well above the required 20 GHz for 2-GHz applications.

As demonstrated by a plot of measured device f_T and f_{max} versus feature size (see figure), processes with feature sizes below 0.25 μm should be able to operate in the 2-GHz range. This has already been verified through a large number of published designs. Other factors (such as power performance) are also greatly improved by the continuous scaling. In fact, the reduction in analog-to-digital (ADC) power consumption is likely to enable high-resolution wideband sampling at megahertz frequencies—an important step toward implementing a highly integrated solution for IMT-2000.

Although device f_T and f_{max} now approach sufficient values, factors such as interconnect resistivity, process tolerances, and substrate losses are other major concerns. However, this situation may improve since major semiconductor companies such as IBM Corp. (Armonk, NY), Motorola, Inc. (Phoenix, AZ), and Texas Instruments (Dallas, TX) have started to replace aluminum with low-resistivity copper in metal interconnects. While these process improvements have been developed to address digital design concerns, they may also have a significant impact on RF performance. Compared to aluminum, copper is a better electrical conductor due to its 40-to-45-percent lower resistivity. Furthermore, the resistance of copper to electromigration is superior to that of aluminum alloys. The latter performance feature is expected to result in more-reliable ICs. Last but not least, copper is less expensive than aluminum.

The key to enabling copper interconnects has been a new processing step which prevents copper from reacting chemically with the silicon material. This technique is currently rather expensive but offers the po-



tential advantages of better performance, integration, and reliability. Once introduced commercially, the processing costs are expected to drop considerably. With better conducting metal, the thicknesses of wires and interconnects can be scaled down to reduce size and capacitance. Alternatively, the interconnect dimensions can be maintained—leading to lower conduction losses. This enables the fabrication of passive devices with higher quality factors (Qs).

Aside from these performance improvements, the RF IC designer is also being offered more metal layers to work with. Recent CMOS processes have moved from two to three metal layers up to five to six layers. Besides enabling more-compact designs, this option also supports higher design flexibility with respect to inductors and capacitors. For instance, it has been shown that inductor resistance can be reduced by using several via-interconnected metal layers. In addition, placing components in the top metal layer increases the distance to the substrate—thereby reducing parasitics.

Despite these improvements, the major limitation remains in the coupling to the low-resistivity silicon substrate. Much effort is therefore being dedicated to introducing interlayer insulators in standard CMOS processes. These insulators should provide low dielectric constants, leading to decreased crosstalk and capacitive coupling to the substrate.

Other technology improvements may include the integration of techniques such as micromachined etching of substrates below components. Currently, the cost and stability of these techniques make them unrealistic for standard CMOS processes, but this may change in the future. One important limitation to further innovations is that CMOS must be the cheapest available technology in order remain competitive. Larger wafer diameters [approaching 12 in. (30.5 cm)] and increased circuit density are developments that will keep CMOS inexpensive. Current costs associated with IC technologies are mainly a product of the wafer diameter. Also, since CMOS is used one hundred times as often as GaAs or bipolar processes, it is likely to remain the cheapest technology—if for no other reason than simply due to its high volume.

PASSIVE RF DEVICES

As mentioned previously, the fabrication of passive RF devices in CMOS constitute a critical limitation in RF IC design. This limitation is mainly associated with the substrate loss as well as the resistivity and limited thickness of the metal layers. While major improvements are expected to occur in the near future, this discussion concentrates on the performance of existing standard (or slightly modified) CMOS processes (see table).

Due to stringent requirements for

OSC
DTOs
VCOs
DROs
High Performance Oscillators
For the Broadest Line of
DTOs • VCOs • DROs
Standards and Specials
0.5 to 18 GHz
Low Cost
High Accuracy
2 YEAR WARRANTY
From the people you trust...
GENERAL MICROWAVE
5500 New Horizons Blvd., Amityville, NY 11701
TEL: 516-226-8900 • FAX: 516-226-8966
http://gmcwave.com
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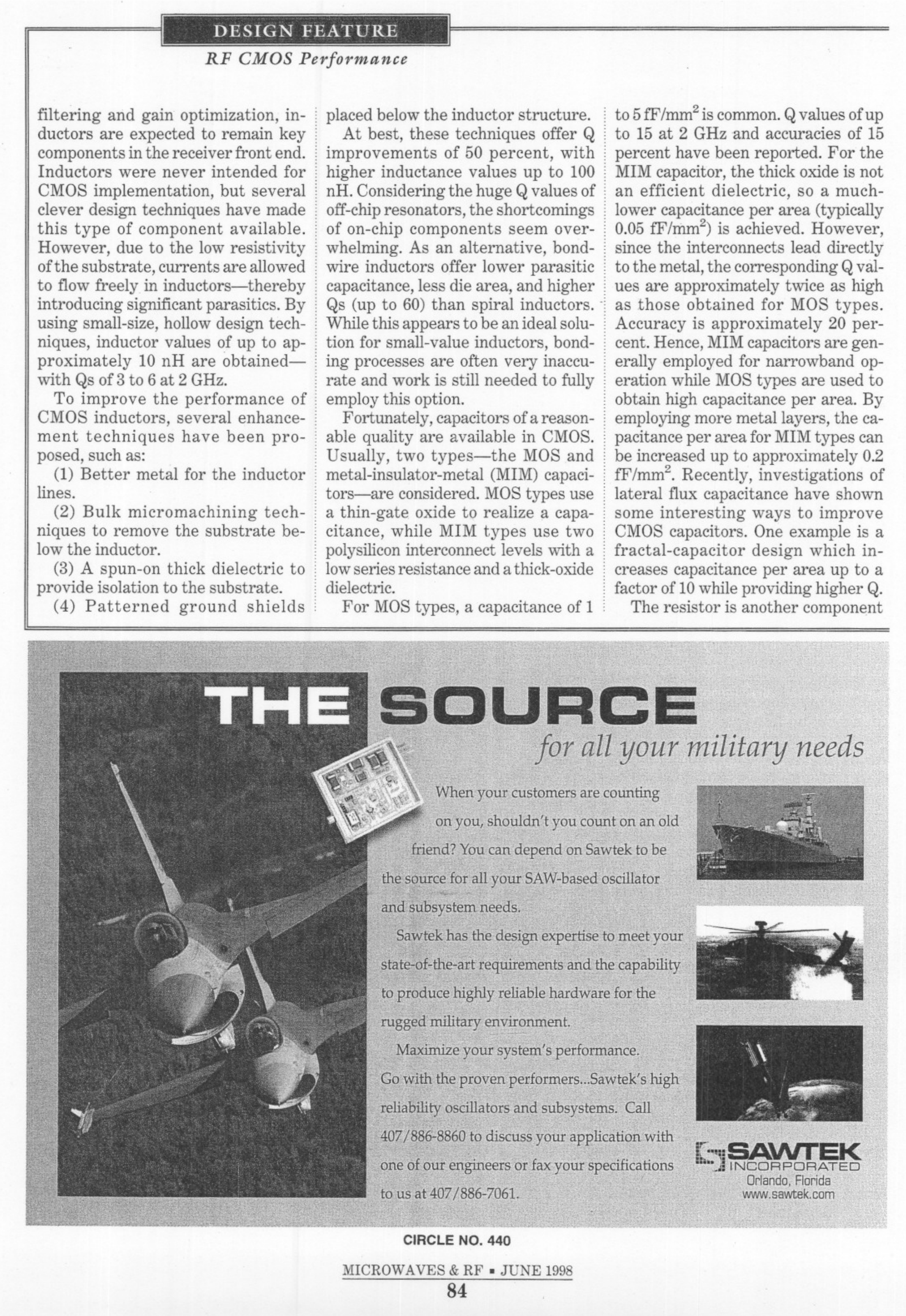

filtering and gain optimization, inductors are expected to remain key components in the receiver front end. Inductors were never intended for CMOS implementation, but several clever design techniques have made this type of component available. However, due to the low resistivity of the substrate, currents are allowed to flow freely in inductors—thereby introducing significant parasitics. By using small-size, hollow design techniques, inductor values of up to approximately 10 nH are obtained—with Qs of 3 to 6 at 2 GHz.

To improve the performance of CMOS inductors, several enhancement techniques have been proposed, such as:

(1) Better metal for the inductor lines.

(2) Bulk micromachining techniques to remove the substrate below the inductor.

(3) A spun-on thick dielectric to provide isolation to the substrate.

(4) Patterned ground shields placed below the inductor structure.

At best, these techniques offer Q improvements of 50 percent, with higher inductance values up to 100 nH. Considering the huge Q values of off-chip resonators, the shortcomings of on-chip components seem overwhelming. As an alternative, bondwire inductors offer lower parasitic capacitance, less die area, and higher Qs (up to 60) than spiral inductors. While this appears to be an ideal solution for small-value inductors, bonding processes are often very inaccurate and work is still needed to fully employ this option.

Fortunately, capacitors of a reasonable quality are available in CMOS. Usually, two types—the MOS and metal-insulator-metal (MIM) capacitors—are considered. MOS types use a thin-gate oxide to realize a capacitance, while MIM types use two polysilicon interconnect levels with a low series resistance and a thick-oxide dielectric.

For MOS types, a capacitance of 1 to 5 fF/mm^2 is common. Q values of up to 15 at 2 GHz and accuracies of 15 percent have been reported. For the MIM capacitor, the thick oxide is not an efficient dielectric, so a much-lower capacitance per area (typically 0.05 fF/mm^2) is achieved. However, since the interconnects lead directly to the metal, the corresponding Q values are approximately twice as high as those obtained for MOS types. Accuracy is approximately 20 percent. Hence, MIM capacitors are generally employed for narrowband operation while MOS types are used to obtain high capacitance per area. By employing more metal layers, the capacitance per area for MIM types can be increased up to approximately 0.2 fF/mm^2. Recently, investigations of lateral flux capacitance have shown some interesting ways to improve CMOS capacitors. One example is a fractal-capacitor design which increases capacitance per area up to a factor of 10 while providing higher Q.

The resistor is another component

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found in most RF circuits. Common applications include biasing and stabilization. High-precision resistors (such as nichrome/sichrome resistors, which provide accuracies down to 1 percent) are not readily fabricated without adding costly steps to the process. A standard option is the use of polysilicon-type resistors, which offer an accuracy of approximately 30 to 40 percent. Due to the low resistivity of approximately 5 to 10 Ω/square, only small-value resistors are realistic. However, since the polysilicon resistor is readily available and is quite linear with respect to the applied voltage, it has been used widely in RF CMOS designs.

To obtain higher-value resistors, wells can be employed as an option. However, since large parasitics limit the operational frequency range, this resistor type is only useful for noncritical applications. The resistance tolerance can be up to 80 percent, and there is also a large voltage coefficient.

ACTIVE RF DEVICES

Reactive and resistive components can also be implemented using active configurations based on FETs. In general, this solution is best avoided due to high power consumption, noise, and intermodulation distortion (IMD), as well as limited dynamic range. However, for specific applications requiring better filtering performance and tunability, active solutions may be the only option. Active solutions are also widely used for biasing purposes. Nevertheless, in the analog parts of a transceiver, the FET is used mostly for amplification or mixing purposes.

While increases in f_T continue with downscaling, a similar increase in f_{max} has recently been questioned.[4] For sub-0.1-μm processes, the FET gate resistance, output resistance, and overlay capacitance (gate-drain and drain-bulk) seem to limit f_{max} to values well below f_T. Although FET design techniques can be employed to alleviate this problem, further investigation is needed to ensure mutual dependence between f_T and f_{max}. The f_{max} value represents an important parameter since it indicates the maximum speed of a transistor in a practical configuration.

Another important concern is the reduction of gate resistance and, consequently, gate noise. Although interconnects are of relatively good quality, FET gates are made out of silicided polysilicon, which exhibits high resistivity. One way to reduce the resistance is to lay out a multifingered device by placing a large number of small FETs in parallel. By connecting the gate fingers to both sides of the device, the gate resistance, gate-source capacitance, and gate-drain capacitance are altered. In this process, low gate resistance must be traded off for high parasitic capacitance. The choice of an optimum gate-finger arrangement with respect to f_T and f_{max} still warrants study. However, this design approach seems to be the most realistic solution, until other enhancements (such as aluminum T gates with noise performance comparable to that of GaAs FETs) are fully evaluated.

Given the improvements seen in f_T and f_{max} values, the major RF limitations of MOSFETs are:

(1) Low transconductance for a particular current (g_m/I_D).

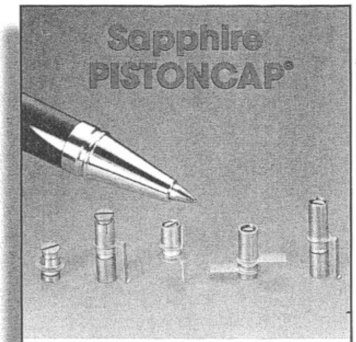
(2) The aforementioned gate noise.

(3) 1/f (flicker) noise.

The lack of gain makes it difficult to design power-efficient circuits, and the 1/f-noise issue is important when designing low-intermediate-frequency (IF) transceivers and local oscillators (LOs). Furthermore, the MOSFET acts like a delay line, and the inherent phase shift may degrade stability at high frequencies if proper measures are not taken. The input of the MOSFET is mainly capacitive and is therefore hard to match to 50 Ω. However, for internal nodes with unconstrained impedance levels, the almost lossless input of the FET can relax certain matching concerns.

CAD TOOLS

More-sophisticated computer-aided-design/engineering (CAD/CAE) packages have evolved in response to the increased interest in RF ICs. Companies that used to concentrate on low-frequency ICs are now addressing RF design. This development toward complete integrated-design tools is aptly demonstrated by



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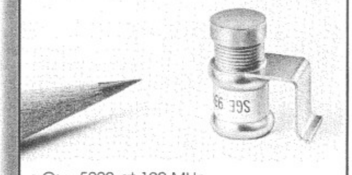
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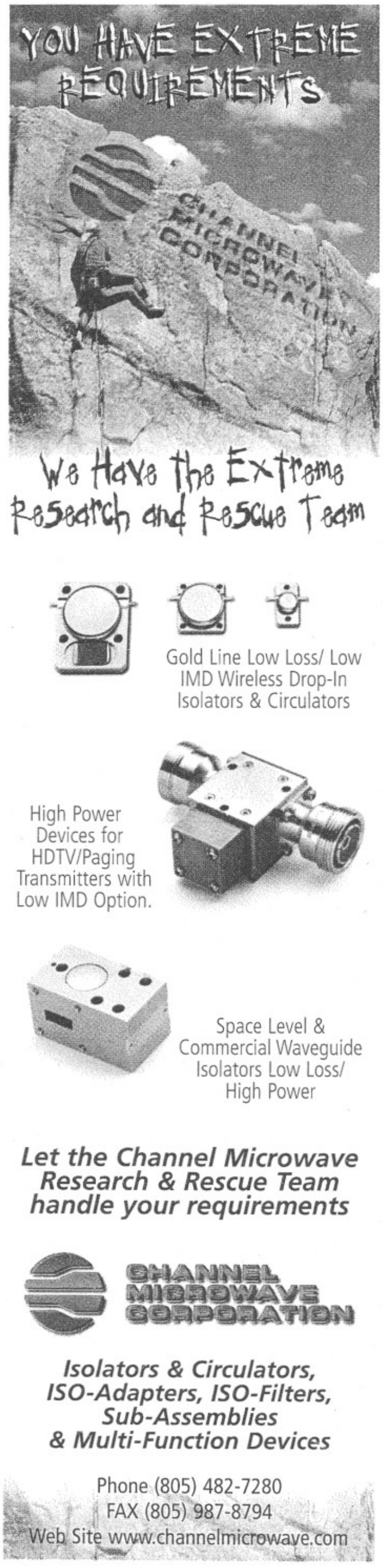
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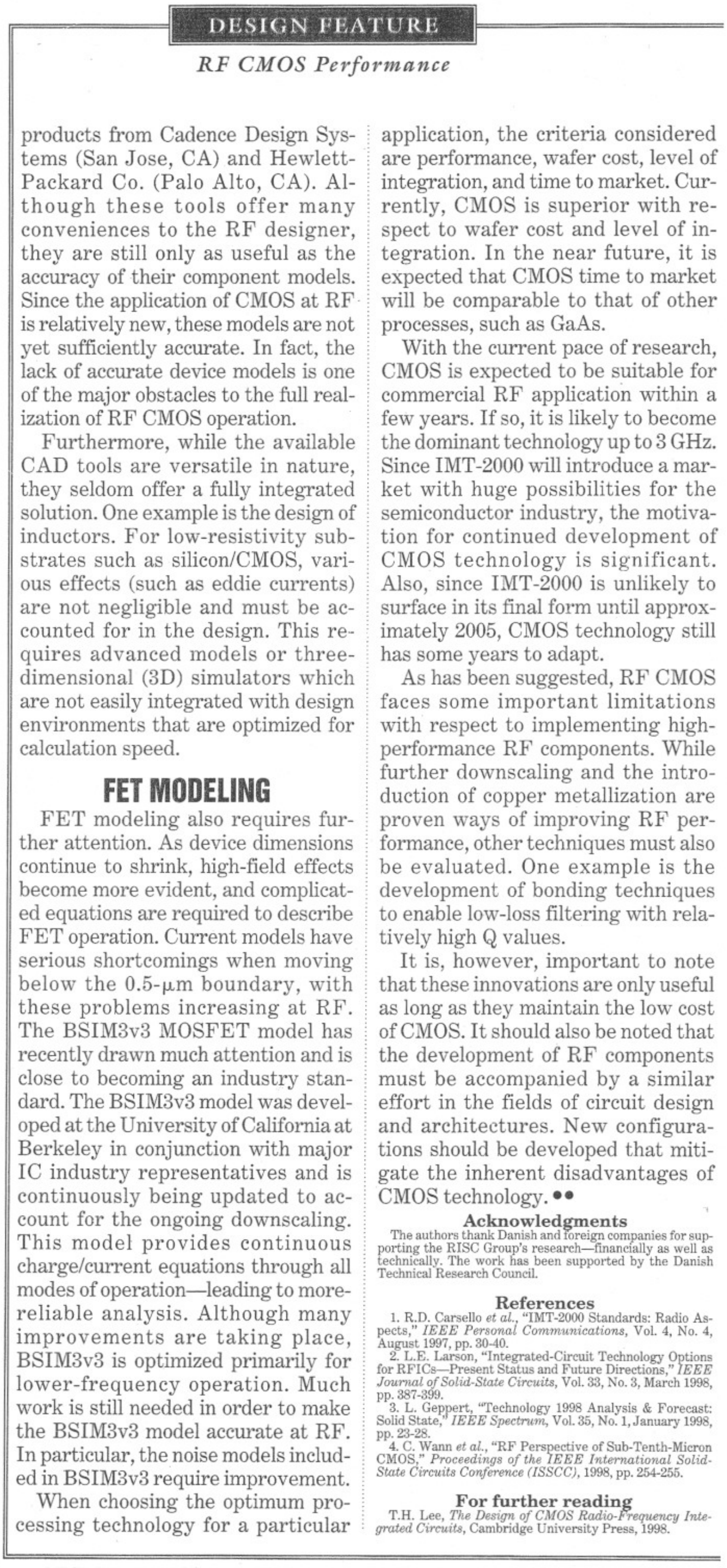

DESIGN FEATURE

RF CMOS Performance

products from Cadence Design Systems (San Jose, CA) and Hewlett-Packard Co. (Palo Alto, CA). Although these tools offer many conveniences to the RF designer, they are still only as useful as the accuracy of their component models. Since the application of CMOS at RF is relatively new, these models are not yet sufficiently accurate. In fact, the lack of accurate device models is one of the major obstacles to the full realization of RF CMOS operation.

Furthermore, while the available CAD tools are versatile in nature, they seldom offer a fully integrated solution. One example is the design of inductors. For low-resistivity substrates such as silicon/CMOS, various effects (such as eddie currents) are not negligible and must be accounted for in the design. This requires advanced models or three-dimensional (3D) simulators which are not easily integrated with design environments that are optimized for calculation speed.

FET MODELING

FET modeling also requires further attention. As device dimensions continue to shrink, high-field effects become more evident, and complicated equations are required to describe FET operation. Current models have serious shortcomings when moving below the 0.5-μm boundary, with these problems increasing at RF. The BSIM3v3 MOSFET model has recently drawn much attention and is close to becoming an industry standard. The BSIM3v3 model was developed at the University of California at Berkeley in conjunction with major IC industry representatives and is continuously being updated to account for the ongoing downscaling. This model provides continuous charge/current equations through all modes of operation—leading to more-reliable analysis. Although many improvements are taking place, BSIM3v3 is optimized primarily for lower-frequency operation. Much work is still needed in order to make the BSIM3v3 model accurate at RF. In particular, the noise models included in BSIM3v3 require improvement.

When choosing the optimum processing technology for a particular application, the criteria considered are performance, wafer cost, level of integration, and time to market. Currently, CMOS is superior with respect to wafer cost and level of integration. In the near future, it is expected that CMOS time to market will be comparable to that of other processes, such as GaAs.

With the current pace of research, CMOS is expected to be suitable for commercial RF application within a few years. If so, it is likely to become the dominant technology up to 3 GHz. Since IMT-2000 will introduce a market with huge possibilities for the semiconductor industry, the motivation for continued development of CMOS technology is significant. Also, since IMT-2000 is unlikely to surface in its final form until approximately 2005, CMOS technology still has some years to adapt.

As has been suggested, RF CMOS faces some important limitations with respect to implementing high-performance RF components. While further downscaling and the introduction of copper metallization are proven ways of improving RF performance, other techniques must also be evaluated. One example is the development of bonding techniques to enable low-loss filtering with relatively high Q values.

It is, however, important to note that these innovations are only useful as long as they maintain the low cost of CMOS. It should also be noted that the development of RF components must be accompanied by a similar effort in the fields of circuit design and architectures. New configurations should be developed that mitigate the inherent disadvantages of CMOS technology. ●●

Acknowledgments

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RF CMOS Circuits Target IMT-2000 Applications

J.H. Mikkelsen, T.E. Kolding, and T. Larsen

Microwaves and RF, vol. 37, pp. 99 – 107, July 1998.

DESIGN FEATURE
RF CMOS Circuits

RF CMOS Circuits Target IMT-2000 Applications

The potential advantages of RF CMOS designs are creating interest in applications at the 2-GHz range.

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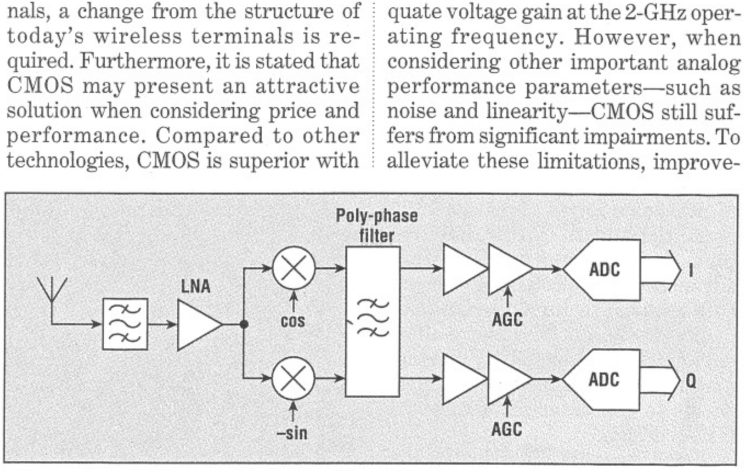
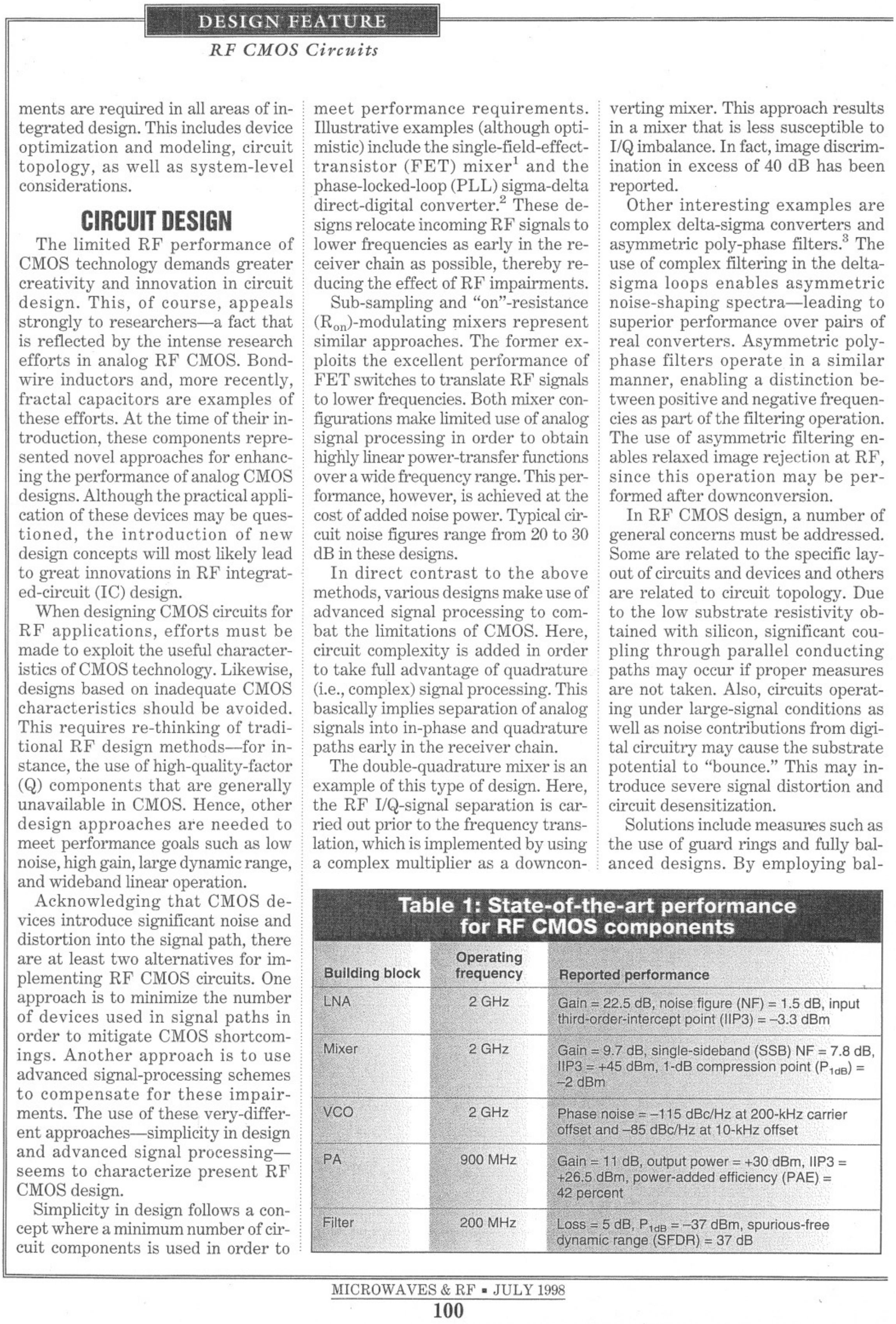
WITH the continuing development of complementary-metal-oxide-semiconductor (CMOS) components and processing techniques, this technology is expected to become suitable for RF application within a few years. Advances with respect to improved devices, circuit topologies, and system-level architecture make CMOS a strong contender for implementing transceivers for the IMT-2000 global wireless system being proposed by the International Telecommunications Union (ITU).

In a previous article (see *Microwaves & RF*, June 1998, p. 79), it was noted that future mobile terminals will have much higher overall complexity than current second-generation terminals. This is needed in order to comply with future needs for multimode and multiband operation, as well as terminal software to support multimedia applications. With the software-radio concept being suggested as a basis for these new terminals, a change from the structure of today's wireless terminals is required. Furthermore, it is stated that CMOS may present an attractive solution when considering price and performance. Compared to other technologies, CMOS is superior with respect to wafer cost, level of integration, and yield. The remaining issue is whether the RF performance of CMOS technology will be adequate for commercial operation in the 2-GHz range, as required for IMT-2000.

As a result of continuous downscaling, device unity-current-gain frequency (f_T) and maximum oscillation frequency (f_{max}) for 0.25-µm processes exceed 40 GHz. Hence, RF CMOS technology already provides adequate voltage gain at the 2-GHz operating frequency. However, when considering other important analog performance parameters—such as noise and linearity—CMOS still suffers from significant impairments. To alleviate these limitations, improve-



This receiver design employs a low-IF architecture based on asymmetric polyphase filtering.



ments are required in all areas of integrated design. This includes device optimization and modeling, circuit topology, as well as system-level considerations.

CIRCUIT DESIGN

The limited RF performance of CMOS technology demands greater creativity and innovation in circuit design. This, of course, appeals strongly to researchers—a fact that is reflected by the intense research efforts in analog RF CMOS. Bondwire inductors and, more recently, fractal capacitors are examples of these efforts. At the time of their introduction, these components represented novel approaches for enhancing the performance of analog CMOS designs. Although the practical application of these devices may be questioned, the introduction of new design concepts will most likely lead to great innovations in RF integrated-circuit (IC) design.

When designing CMOS circuits for RF applications, efforts must be made to exploit the useful characteristics of CMOS technology. Likewise, designs based on inadequate CMOS characteristics should be avoided. This requires re-thinking of traditional RF design methods—for instance, the use of high-quality-factor (Q) components that are generally unavailable in CMOS. Hence, other design approaches are needed to meet performance goals such as low noise, high gain, large dynamic range, and wideband linear operation.

Acknowledging that CMOS devices introduce significant noise and distortion into the signal path, there are at least two alternatives for implementing RF CMOS circuits. One approach is to minimize the number of devices used in signal paths in order to mitigate CMOS shortcomings. Another approach is to use advanced signal-processing schemes to compensate for these impairments. The use of these very-different approaches—simplicity in design and advanced signal processing—seems to characterize present RF CMOS design.

Simplicity in design follows a concept where a minimum number of circuit components is used in order to meet performance requirements. Illustrative examples (although optimistic) include the single-field-effect-transistor (FET) mixer[1] and the phase-locked-loop (PLL) sigma-delta direct-digital converter.[2] These designs relocate incoming RF signals to lower frequencies as early in the receiver chain as possible, thereby reducing the effect of RF impairments.

Sub-sampling and "on"-resistance (R_{on})-modulating mixers represent similar approaches. The former exploits the excellent performance of FET switches to translate RF signals to lower frequencies. Both mixer configurations make limited use of analog signal processing in order to obtain highly linear power-transfer functions over a wide frequency range. This performance, however, is achieved at the cost of added noise power. Typical circuit noise figures range from 20 to 30 dB in these designs.

In direct contrast to the above methods, various designs make use of advanced signal processing to combat the limitations of CMOS. Here, circuit complexity is added in order to take full advantage of quadrature (i.e., complex) signal processing. This basically implies separation of analog signals into in-phase and quadrature paths early in the receiver chain.

The double-quadrature mixer is an example of this type of design. Here, the RF I/Q-signal separation is carried out prior to the frequency translation, which is implemented by using a complex multiplier as a downconverting mixer. This approach results in a mixer that is less susceptible to I/Q imbalance. In fact, image discrimination in excess of 40 dB has been reported.

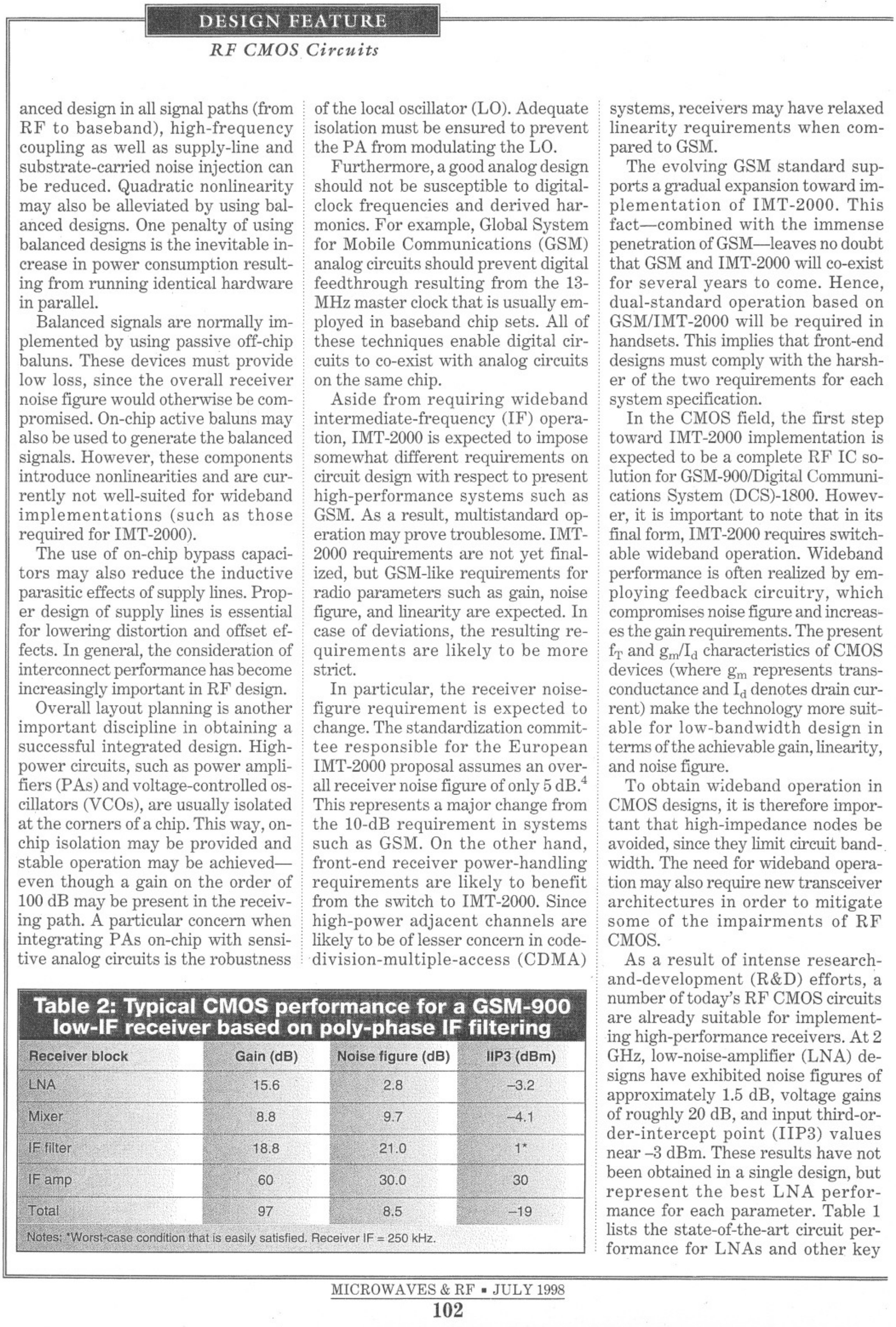
Other interesting examples are complex delta-sigma converters and asymmetric poly-phase filters.[3] The use of complex filtering in the delta-sigma loops enables asymmetric noise-shaping spectra—leading to superior performance over pairs of real converters. Asymmetric polyphase filters operate in a similar manner, enabling a distinction between positive and negative frequencies as part of the filtering operation. The use of asymmetric filtering enables relaxed image rejection at RF, since this operation may be performed after downconversion.

In RF CMOS design, a number of general concerns must be addressed. Some are related to the specific layout of circuits and devices and others are related to circuit topology. Due to the low substrate resistivity obtained with silicon, significant coupling through parallel conducting paths may occur if proper measures are not taken. Also, circuits operating under large-signal conditions as well as noise contributions from digital circuitry may cause the substrate potential to "bounce." This may introduce severe signal distortion and circuit desensitization.

Solutions include measures such as the use of guard rings and fully balanced designs. By employing bal-

Table 1: State-of-the-art performance for RF CMOS components

Building block	Operating frequency	Reported performance
LNA	2 GHz	Gain = 22.5 dB, noise figure (NF) = 1.5 dB, input third-order-intercept point (IIP3) = –3.3 dBm
Mixer	2 GHz	Gain = 9.7 dB, single-sideband (SSB) NF = 7.8 dB, IIP3 = +45 dBm, 1-dB compression point (P_{1dB}) = –2 dBm
VCO	2 GHz	Phase noise = –115 dBc/Hz at 200-kHz carrier offset and –85 dBc/Hz at 10-kHz offset
PA	900 MHz	Gain = 11 dB, output power = +30 dBm, IIP3 = +26.5 dBm, power-added efficiency (PAE) = 42 percent
Filter	200 MHz	Loss = 5 dB, P_{1dB} = –37 dBm, spurious-free dynamic range (SFDR) = 37 dB



anced design in all signal paths (from RF to baseband), high-frequency coupling as well as supply-line and substrate-carried noise injection can be reduced. Quadratic nonlinearity may also be alleviated by using balanced designs. One penalty of using balanced designs is the inevitable increase in power consumption resulting from running identical hardware in parallel.

Balanced signals are normally implemented by using passive off-chip baluns. These devices must provide low loss, since the overall receiver noise figure would otherwise be compromised. On-chip active baluns may also be used to generate the balanced signals. However, these components introduce nonlinearities and are currently not well-suited for wideband implementations (such as those required for IMT-2000).

The use of on-chip bypass capacitors may also reduce the inductive parasitic effects of supply lines. Proper design of supply lines is essential for lowering distortion and offset effects. In general, the consideration of interconnect performance has become increasingly important in RF design.

Overall layout planning is another important discipline in obtaining a successful integrated design. High-power circuits, such as power amplifiers (PAs) and voltage-controlled oscillators (VCOs), are usually isolated at the corners of a chip. This way, on-chip isolation may be provided and stable operation may be achieved—even though a gain on the order of 100 dB may be present in the receiving path. A particular concern when integrating PAs on-chip with sensitive analog circuits is the robustness of the local oscillator (LO). Adequate isolation must be ensured to prevent the PA from modulating the LO.

Furthermore, a good analog design should not be susceptible to digital-clock frequencies and derived harmonics. For example, Global System for Mobile Communications (GSM) analog circuits should prevent digital feedthrough resulting from the 13-MHz master clock that is usually employed in baseband chip sets. All of these techniques enable digital circuits to co-exist with analog circuits on the same chip.

Aside from requiring wideband intermediate-frequency (IF) operation, IMT-2000 is expected to impose somewhat different requirements on circuit design with respect to present high-performance systems such as GSM. As a result, multistandard operation may prove troublesome. IMT-2000 requirements are not yet finalized, but GSM-like requirements for radio parameters such as gain, noise figure, and linearity are expected. In case of deviations, the resulting requirements are likely to be more strict.

In particular, the receiver noise-figure requirement is expected to change. The standardization committee responsible for the European IMT-2000 proposal assumes an overall receiver noise figure of only 5 dB.[4] This represents a major change from the 10-dB requirement in systems such as GSM. On the other hand, front-end receiver power-handling requirements are likely to benefit from the switch to IMT-2000. Since high-power adjacent channels are likely to be of lesser concern in code-division-multiple-access (CDMA) systems, receivers may have relaxed linearity requirements when compared to GSM.

Table 2: Typical CMOS performance for a GSM-900 low-IF receiver based on poly-phase IF filtering

Receiver block	Gain (dB)	Noise figure (dB)	IIP3 (dBm)
LNA	15.6	2.8	–3.2
Mixer	8.8	9.7	–4.1
IF filter	18.8	21.0	1*
IF amp	60	30.0	30
Total	97	8.5	–19

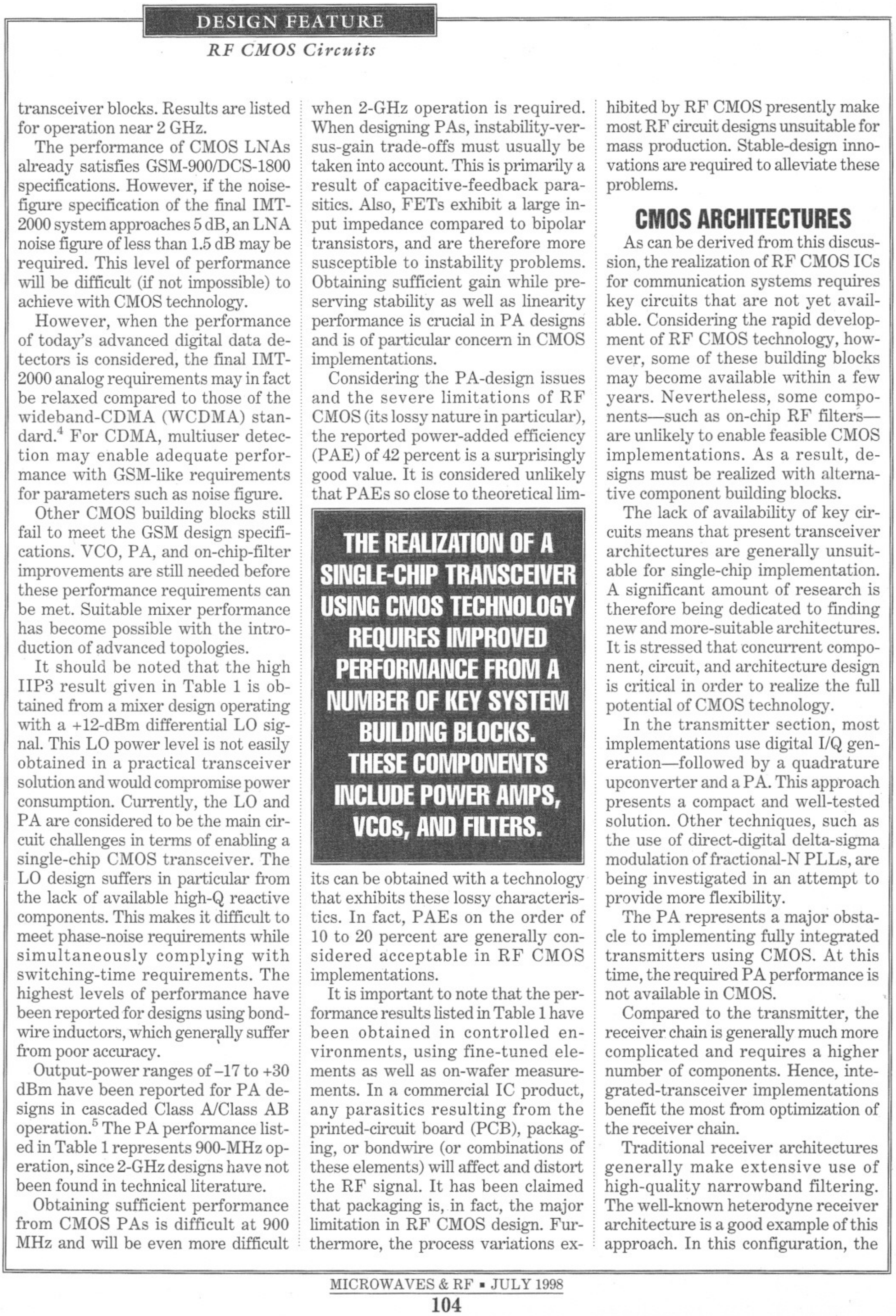
Notes: *Worst-case condition that is easily satisfied. Receiver IF = 250 kHz.

The evolving GSM standard supports a gradual expansion toward implementation of IMT-2000. This fact—combined with the immense penetration of GSM—leaves no doubt that GSM and IMT-2000 will co-exist for several years to come. Hence, dual-standard operation based on GSM/IMT-2000 will be required in handsets. This implies that front-end designs must comply with the harsher of the two requirements for each system specification.

In the CMOS field, the first step toward IMT-2000 implementation is expected to be a complete RF IC solution for GSM-900/Digital Communications System (DCS)-1800. However, it is important to note that in its final form, IMT-2000 requires switchable wideband operation. Wideband performance is often realized by employing feedback circuitry, which compromises noise figure and increases the gain requirements. The present f_T and g_m/I_d characteristics of CMOS devices (where g_m represents transconductance and I_d denotes drain current) make the technology more suitable for low-bandwidth design in terms of the achievable gain, linearity, and noise figure.

To obtain wideband operation in CMOS designs, it is therefore important that high-impedance nodes be avoided, since they limit circuit bandwidth. The need for wideband operation may also require new transceiver architectures in order to mitigate some of the impairments of RF CMOS.

As a result of intense research-and-development (R&D) efforts, a number of today's RF CMOS circuits are already suitable for implementing high-performance receivers. At 2 GHz, low-noise-amplifier (LNA) designs have exhibited noise figures of approximately 1.5 dB, voltage gains of roughly 20 dB, and input third-order-intercept point (IIP3) values near –3 dBm. These results have not been obtained in a single design, but represent the best LNA performance for each parameter. Table 1 lists the state-of-the-art circuit performance for LNAs and other key



transceiver blocks. Results are listed for operation near 2 GHz.

The performance of CMOS LNAs already satisfies GSM-900/DCS-1800 specifications. However, if the noise-figure specification of the final IMT-2000 system approaches 5 dB, an LNA noise figure of less than 1.5 dB may be required. This level of performance will be difficult (if not impossible) to achieve with CMOS technology.

However, when the performance of today's advanced digital data detectors is considered, the final IMT-2000 analog requirements may in fact be relaxed compared to those of the wideband-CDMA (WCDMA) standard.[4] For CDMA, multiuser detection may enable adequate performance with GSM-like requirements for parameters such as noise figure.

Other CMOS building blocks still fail to meet the GSM design specifications. VCO, PA, and on-chip-filter improvements are still needed before these performance requirements can be met. Suitable mixer performance has become possible with the introduction of advanced topologies.

It should be noted that the high IIP3 result given in Table 1 is obtained from a mixer design operating with a +12-dBm differential LO signal. This LO power level is not easily obtained in a practical transceiver solution and would compromise power consumption. Currently, the LO and PA are considered to be the main circuit challenges in terms of enabling a single-chip CMOS transceiver. The LO design suffers in particular from the lack of available high-Q reactive components. This makes it difficult to meet phase-noise requirements while simultaneously complying with switching-time requirements. The highest levels of performance have been reported for designs using bondwire inductors, which generally suffer from poor accuracy.

Output-power ranges of –17 to +30 dBm have been reported for PA designs in cascaded Class A/Class AB operation.[5] The PA performance listed in Table 1 represents 900-MHz operation, since 2-GHz designs have not been found in technical literature.

Obtaining sufficient performance from CMOS PAs is difficult at 900 MHz and will be even more difficult when 2-GHz operation is required. When designing PAs, instability-versus-gain trade-offs must usually be taken into account. This is primarily a result of capacitive-feedback parasitics. Also, FETs exhibit a large input impedance compared to bipolar transistors, and are therefore more susceptible to instability problems. Obtaining sufficient gain while preserving stability as well as linearity performance is crucial in PA designs and is of particular concern in CMOS implementations.

Considering the PA-design issues and the severe limitations of RF CMOS (its lossy nature in particular), the reported power-added efficiency (PAE) of 42 percent is a surprisingly good value. It is considered unlikely that PAEs so close to theoretical limits can be obtained with a technology that exhibits these lossy characteristics. In fact, PAEs on the order of 10 to 20 percent are generally considered acceptable in RF CMOS implementations.

THE REALIZATION OF A SINGLE-CHIP TRANSCEIVER USING CMOS TECHNOLOGY REQUIRES IMPROVED PERFORMANCE FROM A NUMBER OF KEY SYSTEM BUILDING BLOCKS. THESE COMPONENTS INCLUDE POWER AMPS, VCOs, AND FILTERS.

It is important to note that the performance results listed in Table 1 have been obtained in controlled environments, using fine-tuned elements as well as on-wafer measurements. In a commercial IC product, any parasitics resulting from the printed-circuit board (PCB), packaging, or bondwire (or combinations of these elements) will affect and distort the RF signal. It has been claimed that packaging is, in fact, the major limitation in RF CMOS design. Furthermore, the process variations exhibited by RF CMOS presently make most RF circuit designs unsuitable for mass production. Stable-design innovations are required to alleviate these problems.

CMOS ARCHITECTURES

As can be derived from this discussion, the realization of RF CMOS ICs for communication systems requires key circuits that are not yet available. Considering the rapid development of RF CMOS technology, however, some of these building blocks may become available within a few years. Nevertheless, some components—such as on-chip RF filters—are unlikely to enable feasible CMOS implementations. As a result, designs must be realized with alternative component building blocks.

The lack of availability of key circuits means that present transceiver architectures are generally unsuitable for single-chip implementation. A significant amount of research is therefore being dedicated to finding new and more-suitable architectures. It is stressed that concurrent component, circuit, and architecture design is critical in order to realize the full potential of CMOS technology.

In the transmitter section, most implementations use digital I/Q generation—followed by a quadrature upconverter and a PA. This approach presents a compact and well-tested solution. Other techniques, such as the use of direct-digital delta-sigma modulation of fractional-N PLLs, are being investigated in an attempt to provide more flexibility.

The PA represents a major obstacle to implementing fully integrated transmitters using CMOS. At this time, the required PA performance is not available in CMOS.

Compared to the transmitter, the receiver chain is generally much more complicated and requires a higher number of components. Hence, integrated-transceiver implementations benefit the most from optimization of the receiver chain.

Traditional receiver architectures generally make extensive use of high-quality narrowband filtering. The well-known heterodyne receiver architecture is a good example of this approach. In this configuration, the incoming signal experiences repeated amplification, filtering, and downconversion. Often, two or more IFs are used in this process. This approach provides excellent selectivity and signal-handling capabilities. However, due to the large amount of filtering required, the heterodyne structure is not suitable for CMOS implementation and the corresponding low-Q components. More importantly, the heterodyne receiver architecture does not provide the flexibility required for IMT-2000.

From a technology point of view, it is expected that future radio systems will display intelligent performance based on adaptive schemes, as represented by the software-radio concept. In particular, adaptability in terms of spectrum usage is required (this applies to bandwidth as well as band selection). These requirements are mandatory for implementing receivers for IMT-2000 terminals, since these systems must operate at variable bandwidths.

The European IMT-2000 proposal specifies operation using 4-, 8-, or 16-MHz bandwidths. The need to cover bandwidths as wide as 16 MHz represents a major change from the relatively narrowband cellular systems in use today (≈ 200 kHz for GSM).

In addition, it is expected that future radio systems will exploit digital-signal-processor (DSP) performance to the fullest through the use of more-advanced signal-processing schemes. Receivers based largely on digital circuitry enable greater operating flexibility than their analog counterparts.

The desire to exploit this characteristic in front-end designs has resulted in considerable interest in IF-sampling architectures. IF sampling is desirable since it enables digital I/Q separation, all-digital channel-select filtering, and digital demodulation. However, the real benefit of IF sampling is yet to be realized since only single-channel IF sampling has been implemented in handsets. Hence, only flexibility in terms of facilitating different modulation schemes is provided. This must change if IF sampling is to be used for IMT-2000 receivers, since this system requires digitization of wideband IF signals.

The required IF bandwidth and the choice of IF involve a number of trade-offs. While a high IF reduces image-signal concerns, it also implies increased power consumption due to a higher sampling frequency. Moving to a high IF generally reduces the amount of analog filtering in the front end—resulting in increased dynamic-range requirements for the analog-to-digital converters (ADCs). This calls for high-precision converters operating at high sample rates. Not only does this add to the overall power consumption, but it may also cause sluggishness in the receiver operation since multibit converters may require calibration on power-up. In fact, the need to apply ADCs directly at IF is questionable when considering that baseband 4-b ADCs appear to provide sufficient resolution in CDMA systems.

GREATER USE OF DIGITAL SIGNAL PROCESSING WILL BE ESSENTIAL IN ORDER TO ACHIEVE THE OPERATING FLEXIBILITY REQUIRED FOR IMT-2000 SYSTEMS. FOR INSTANCE, THESE SYSTEMS MUST PROVIDE VARIABLE BANDWIDTHS OF UP TO 16 MHz.

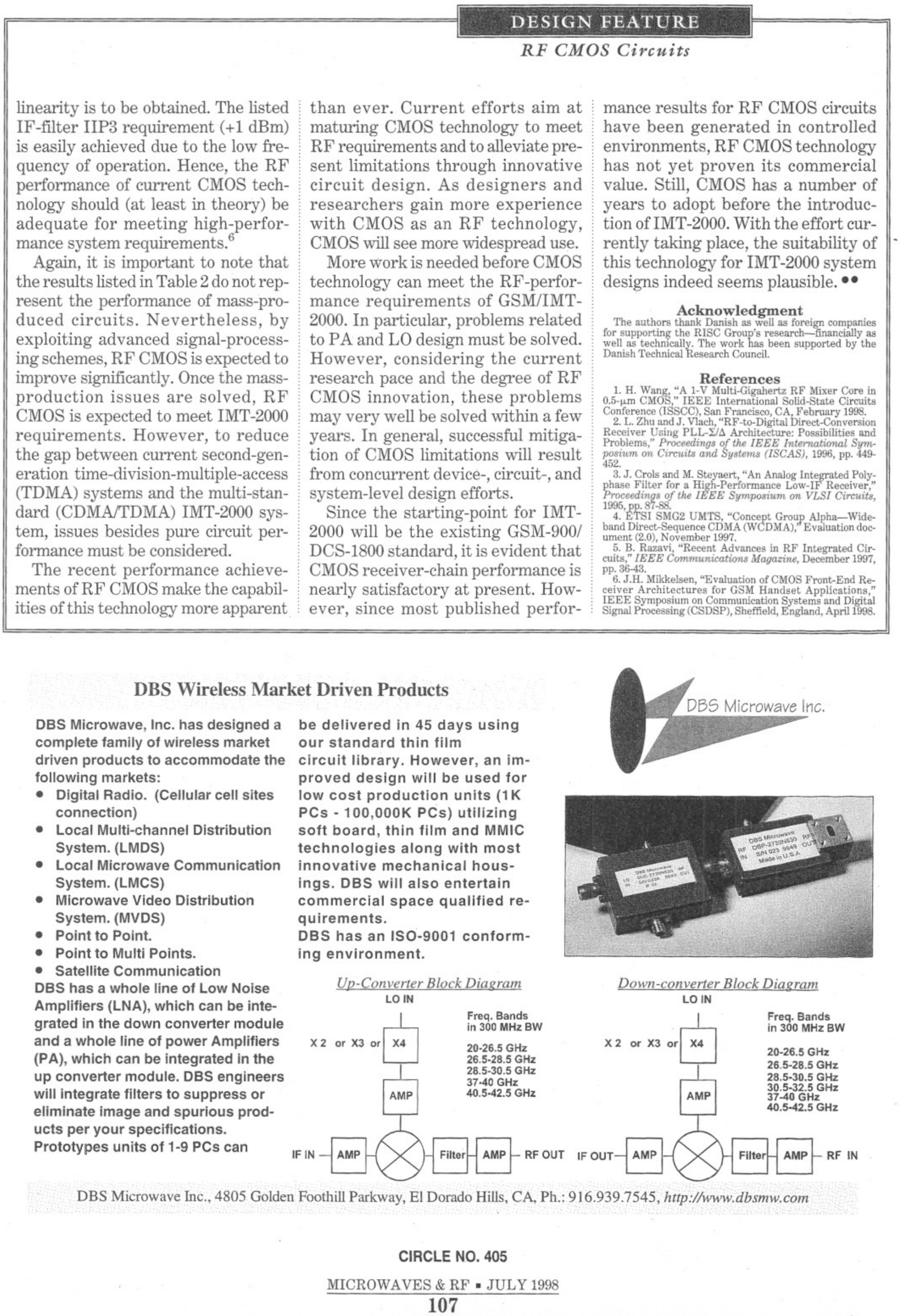
Regardless of the choice of architecture, some type of RF signal processing is required to convert the incoming analog RF signal to a form that can be processed digitally. In conjunction with the software-radio concept, direct-RF sampling is being pursued. However, this approach is not considered realistic due to power-consumption concerns alone. Currently available high-frequency ADCs consume up to 250-mW power to provide 12-b resolution at sample rates in the 20-MHz range. Obtaining high resolution at RF will presently result in power consumption on the order of several watts.

Aiming at a single-chip transceiver solution, the direct-conversion (zero-IF) receiver may initially appear to be the ideal architecture in terms of simplicity—the main benefit being the elimination of the image-signal problem. Since the signal generates its own image-signal I/Q matching, requirements are very relaxed and are easily satisfied. However, while the zero-IF receiver is a theoretically superior solution, it suffers from a number of practical problems—such as LO leakage, DC offset, and noise.

Recently, the low-IF receiver has attracted intense attention since this architecture has the potential of mitigating a number of the problems experienced by the zero-IF receiver. While the low-IF approach had previously been neglected due to the image-signal problem, advances in analog and digital signal processing have resulted in a number of proposed methods for reducing the image signal. These include the aforementioned double-quadrature mixer and poly-phase filter (see figure). Adaptive-calibration schemes for correcting the I/Q imbalance have also been suggested as a way to improve image rejection. The availability of these techniques makes the low-IF receiver a very-strong contender for implementing the receiver parts of a fully integrated, high-performance CMOS transceiver.

Compared to the zero-IF architecture, 1/f noise is less of a concern in a low-IF receiver. The amount of RF gain required to meet sensitivity requirements is relaxed accordingly. While an RF gain of at least 30 dB is needed in a zero-IF architecture, only 15 to 20 dB is required in a low-IF design. Based on the performance of available receiver blocks (Table 2), the low-IF receiver is capable of meeting GSM-900 radio requirements. These results are based on an IF of 250 kHz.

The values listed in Table 2 represent actual performance parameters for CMOS devices—with the exception of the poly-phase IF filter. In that case, the noise figure is extrapolated from an equivalent-order low-pass-filter design. The IIP3 result represents a maximum value that must be satisfied if sufficient receiver



linearity is to be obtained. The listed IF-filter IIP3 requirement (+1 dBm) is easily achieved due to the low frequency of operation. Hence, the RF performance of current CMOS technology should (at least in theory) be adequate for meeting high-performance system requirements.[6]

Again, it is important to note that the results listed in Table 2 do not represent the performance of mass-produced circuits. Nevertheless, by exploiting advanced signal-processing schemes, RF CMOS is expected to improve significantly. Once the mass-production issues are solved, RF CMOS is expected to meet IMT-2000 requirements. However, to reduce the gap between current second-generation time-division-multiple-access (TDMA) systems and the multi-standard (CDMA/TDMA) IMT-2000 system, issues besides pure circuit performance must be considered.

The recent performance achievements of RF CMOS make the capabilities of this technology more apparent than ever. Current efforts aim at maturing CMOS technology to meet RF requirements and to alleviate present limitations through innovative circuit design. As designers and researchers gain more experience with CMOS as an RF technology, CMOS will see more widespread use.

More work is needed before CMOS technology can meet the RF-performance requirements of GSM/IMT-2000. In particular, problems related to PA and LO design must be solved. However, considering the current research pace and the degree of RF CMOS innovation, these problems may very well be solved within a few years. In general, successful mitigation of CMOS limitations will result from concurrent device-, circuit-, and system-level design efforts.

Since the starting-point for IMT-2000 will be the existing GSM-900/DCS-1800 standard, it is evident that CMOS receiver-chain performance is nearly satisfactory at present. However, since most published performance results for RF CMOS circuits have been generated in controlled environments, RF CMOS technology has not yet proven its commercial value. Still, CMOS has a number of years to adopt before the introduction of IMT-2000. With the effort currently taking place, the suitability of this technology for IMT-2000 system designs indeed seems plausible. ●●

Acknowledgment

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CIRCLE NO. 405

CMOS Low-Noise Asymmetric Poly-Phase Filter for GSM Low-IF Radio Receivers

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European Conference on Circuit Theory and Design (ECCTD)
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CMOS Low-Noise Asymmetrical Poly-Phase Filter for GSM Low-IF Radio Receivers

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Abstract

Recent investigations of RF CMOS technologies puts increased focus on front-end architectures. In this paper the combined use of a low-IF receiver architecture and an asymmetric poly-phase filter is pursued. Previously, the importance of low-noise operation in low frequency circuits has been mostly overlooked in RF front-end design. This work considers the design and implementation of asymmetric poly-phase filters with emphasis on low-noise. Three different approaches are taken; (i) Active-RC, (ii) Gm-C, and (iii) a differential current-adder circuit. The main purpose is to demonstrate IF stages capable of meeting requirements for high performance narrow band systems, such as GSM.

1 Introduction

Within the last decade CMOS has seen a renewed interest in terms of analog integrated circuit design. From being mostly a low and medium frequency technology, CMOS is now also targeting high frequency RF applications [4]. In the design of such RF products, front-ends represent key components. Today off-chip filters are used extensively to meet selectivity requirements. Rearranging the receiver concept on a system level has potential for great cost reductions as the majority of the off-chip filters may be omitted. Further cost reductions are possible if CMOS can replace the more complex and more expensive technologies, such as BiCMOS and GaAs.

Table 1: Example of receiver chain requirements for a GSM hand portable.

Parameter	Rx	LNA	Mixer	AGC
Gain [dB]	-3	0/15	8	10/80
NF [dB]	3	2	10	14
iIP_3 [dBm]	N/A	-3	-4	4

Recently, the low-IF receiver has attracted a lot of attention as this receiver architecture has the potential of mitigating a number of the problems associated with the pragmatic direct-conversion receiver [3]. While the low-IF approach mainly is questioned due to the reintroduced image-signal problem, advances in analog and digital signal processing have resulted in a number of proposed methods for reducing the image signal [2, 1]. Based on todays reported CMOS performance, equivalent to that listed in Table 1, low-IF receivers present promising solutions for fully integrated CMOS GSM receivers.

This paper pursues the use of asymmetric poly-phase filtering as a mean to reduce image-signal interference. The main purpose is to analyze IF building blocks capable of implementing poly-phase filter responses in order to evaluate the potential of the low-IF receiver architecture for high performance narrow band systems, such as GSM.

2 Poly-Phase Filtering

Using GSM900 as a reference system it is found that the image-rejection requirement may be relaxed significantly by choosing a sufficiently low IF. Assuming an IF of 200kHz, as illustrated in Figure 1, the image-rejection requirement results from an adjacent-channel rejection test and is accordingly relaxed to approximately 50dB.

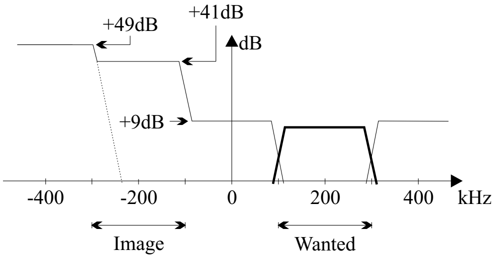

Figure 1: Frequency domain scenario resulting from a down-conversion to a 200kHz IF.

Besides providing for the required degree of image-rejection the IF stage must also be capable of delivering approximately 60dB controllable gain, a noise figure less than 14dB, and an IIP3 better than 4dBm for the low-IF receiver to comply with GSM specifications.

For the poly-phase filter structure to be able to distinguish between wanted signals and image

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signals, both In-phase (I) and Quadrature-phase (Q) components of incoming signals are utilized as shown in Figure 2.

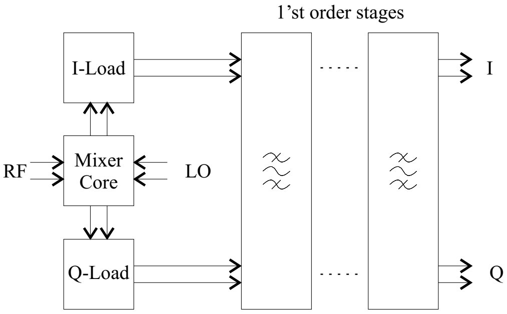

Figure 2: Combination of Low-IF and poly-phase filtering.

As a result the filter requires a complex signal interface to the preceding mixer as Figure 2 illustrates. Since only first order responses may be implemented at one time, a number of cascaded poly-phase sections is required to achieve higher-order filter responses. Each of these cascade stages can be described by

$$\left[\begin{array}{c} I_o(j\omega) \\ \\ Q_o(j\omega) \end{array}\right] = \left[\begin{array}{cc} H_I & -H_Q \\ \\ H_Q & H_I \end{array}\right] \left[\begin{array}{c} I_{in}(j\omega) \\ \\ Q_{in}(j\omega) \end{array}\right],$$

with H_I and H_Q given as

$$\begin{aligned} H_I(j\omega) &= \frac{H(j\omega)}{1+k^2H^2(j\omega)} \\ H_Q(j\omega) &= \frac{kH^2(j\omega)}{1+k^2H^2(j\omega)} \end{aligned}$$

Under the assumption that $H(j\omega)$ is a first order lowpass filter and that k equals ω_c/ω_0, with ω_c representing the center frequency of the resulting poly-phase filter response and ω_0 the bandwidth, the following result for the complex first order poly-phase response is obtained

$$H_{PP}(j\omega) = H(j(\omega - \omega_c))$$

From this it is clear that a single poly-phase filter stage implements a frequency shifted replica of a first order lowpass response. More over, the required filter order and hence the number of cascaded first order stages is a trade-off between image-rejection and desired channel select filtering. As a reasonable trade off between filter order, IF frequency, group delay, and ADC requirements a 5'th order Butterworth filter having a ω_c of $2\pi \cdot 250kHz$ and a ω_0 of $2\pi \cdot 150kHz$ is designed for. The following implementations all realize a complex pole located at 100kHz+j·250kHz.

3 Filter Implementations

In this paper three first order asymmetric poly-phase filter stages, all implemented in CMOS, are presented. One filter stage is based on an Active-RC while the remaining two are based on the current-mode principles. The implementations aim to compare the noise performance of the different structures rather than optimize for linearity and dynamic range in each stage. Hence, less than optimum linearity performance is accepted.

3.1 Active-RC

Active-RC implementations generally provide for good dynamic range performance. Also, as the performance of the active-RC implementation depends on the matching of passive, rather than active components, good robustness towards process variations generally results. A possible active-RC implementation is illustrated in Figure 3.

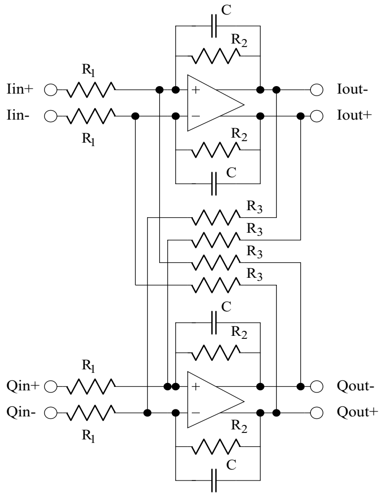

Figure 3: Active-RC implementation for a first order poly-phase stage. $R_1 = R_2 = 53\text{k}\Omega$, $R_3 = 31.8\text{k}\Omega$, and $C = 20\text{pF}$.

The center frequency, ω_c, and filter section Q-value for the show poly-phase structure are given as $R_3/(2R_2)$ and $1/(R_2C)$, respectively. With modern CMOS technologies as much as 40% variation on the Q-value is potential while ω_c is relatively robust as resistor variations are likely to be correlated. A disadvantage of this approach, however, is that low noise is not inherent as seen from the different noise and signal transfer functions

$$V^2_{n,out} = \left(\frac{R_2}{R_1}\right)^2 \cdot e^2_n + R^2_2 \cdot i^2_n$$

$$V_{s,out} = -\frac{R_2}{R_1} \cdot V_{s,in}$$

Hence, a significant amplification of intrinsic OPAMP noise may result. To minimize this noise contribution small R_2 values are required which inflicts at least two limitations, namely; (i) for minimization of noise only low to moderate signal gains may be implemented and (ii) simultaneous low noise and low frequency operation requires the use of very large capacitor values. The use of resistors directly in the signal path adds further noise to the signal. Also, the use of signal coupling capacitors often severely limit performance due to bottom plate capacitances. The parasitic capacitance formed by the bottom plate and the substrate beneath it contributes significantly to the overall capacitance. Here 10 - 30% or more of the main capacitance may result from the parasitic bottom plate [3]. Active-RC implementations are also generally rather space consuming, especially if AGC operation is to be incorporated, and they display relatively high power consumption levels. Further, being a voltage-mode structure the active-RC implementation has inherent wideband limitations.

3.2 G$_m$-C

In contrast to active-RC implementations, current-mode circuits use currents as the active signal carrier. This results in increased signal-bandwidths, potential improved linearity and increased dynamic range. Depending on the design structure both the transconductor and the capacitors may be grounded which greatly improves circuit sensitivity towards bottom plate capacitances. The potential for improved accuracy through grounding comes at the expense of increased capacitance. Another benefit of using currents as signal carriers is that low-voltage operation is inherent to the design. A disadvantage of the schematic presented show in Figure 4 is the dependency on the accuracy of transconductance values.

As the center frequency is given as G_{m2}/C tuning is required. Further, as the bandwidth of the applied structure depends on matching of G_m values the design is sensitive towards transistor matching unless measures are taken. To mitigate part of this problem an enhanced transconductor is designed to provide for a robust center frequency. With a scaled current mirror the differential input stage may be reused whereby accuracy is improved. Having G_m values determining both gain and cut-off frequency makes it possible to implement both AGC processing as well as multi-standard functionalities in the filter.

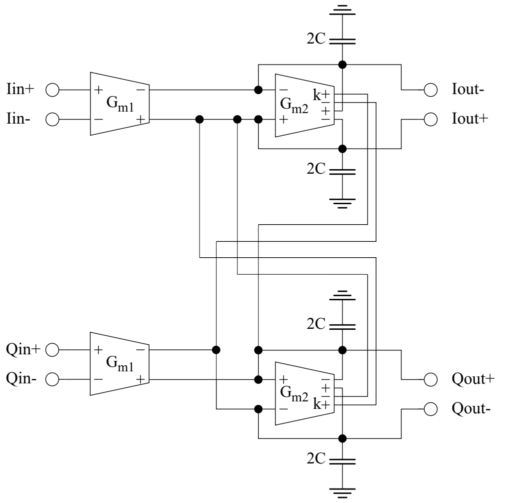

Figure 4: Enhanced G_m-C based implementation. $G_{m1} = G_{m2} = 18.85\mu$S and C = 20pF.

3.3 Differential Current-Adding

This paper suggests a new approach to poly-phase filter implementation based on current addition using a minimum number of transistors. This is realized trough cross coupling of differential amplifiers. Low-noise is here the aim rather than good robustness towards process variations. This structure aims to mitigate the traditional high frequency limitations of OPAMP and OTA based designs.

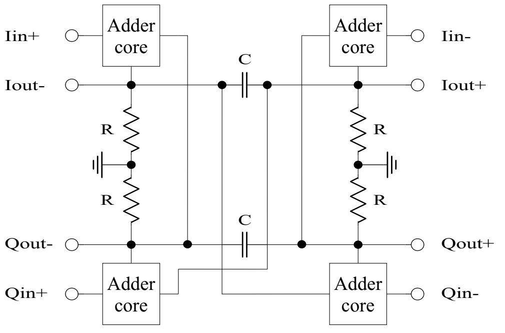

Figure 5: Current-adding first order stage implementation. R = 26.5kΩ and C = 20pF.

As the performance of the circuit depends largely on the matching of transistors which is also is displayed from linearity measures. However, the structure uses only a minimum of capacitances and the cut-off frequency is again determined by matching of passive components. The center frequency is still based on transistor matching as Figure 6 illustrates.

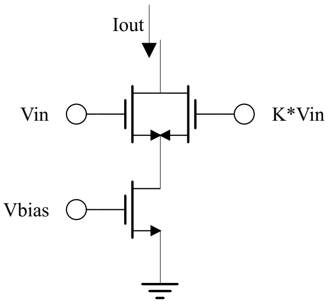

Figure 6: The core circuit of the current-adder implementation.

4 Results

All realizations are based on a standard 0.5 micron CMOS process providing three metal layers and double-poly technology. As expected the best noise performance is provided by the current-adder circuit. The noise voltages level plotted in Figure 7 are not normalized and serve only for a comparison.

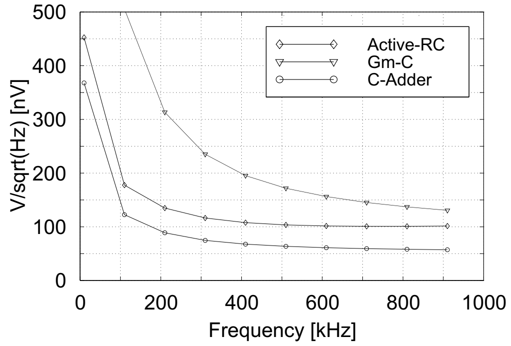

Figure 7: Input referred noise voltages.

From Figures 8 and 9 it is seen that the Gm-C design displays the poorest linearity performace of the realized circuits.

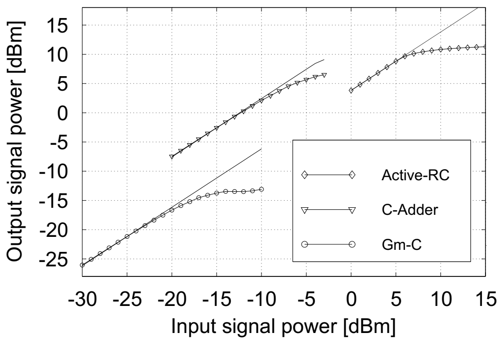

Figure 8: Compression points.

While the enhanced OTA structure improves the center frequency stability significantly it requires further optimization before it may be used in high performance filter designs.

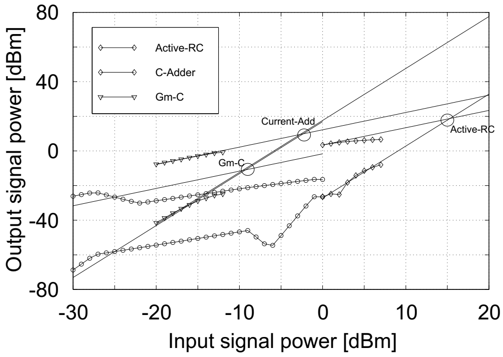

Figure 9: IP3 measures.

Further, the current-adder structure is seen to outperform the OTA based structure and it displays the best noise performance. The proposed structure is indeed a potential structure for implementing low-noise poly-phase filters. Further simulations and measurements are needed to further characterize the structures and to provide further verification of performance.

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Feasibility Study of DC Offset Filtering for UTRA-FDD/WCDMA Direct-Conversion Receiver

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Feasibility Study of DC Offset Filtering for UTRA-FDD/WCDMA Direct-Conversion Receiver*

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Abstract

This paper presents a feasibility study of DC offset filtering for direct-conversion UTRA-FDD/WCDMA receivers. Spectral characteristics and properties of continuous transmission facilitate the use of simple high-pass filtering and this method is evaluated in the paper. Design equations for DC offset power to down-converted signal power ratio are presented and the impact on bit error rate of high-pass filtering WCDMA signals is evaluated by UTRA-FDD system simulations.

1 INTRODUCTION

AS standardization work for third generation mobile communications (UMTS/UTRA-FDD) approaches its final stages, it is clear that WCDMA becomes one of the major supported schemes. Low terminal form factor and power consumption as well as extended functionality and bandwidth, call for higher levels of integration than present in current mobile terminals. To reach a proper tradeoff between performance and cost, silicon technologies, and preferably CMOS technologies, should be used. Due to various issues related to filtering and isolation requirements, the implementation of the RF frontend constitutes one of the major challenges. One potential frontend architecture which lends itself towards complete integration is the direct-conversion architecture. However, due to issues of (i) inherent DC offset, (ii) dynamic range requirements, (iii) I/Q gain and phase imbalance, (iv) LO leakage to antenna, (v) second order distortion, and (vi) susceptibility to flicker noise, the success with this architecture in cellular TDMA systems has been very limited. Fortunately, with the shift to WCDMA some of these issues may be relaxed. In this paper the problem of DC offset filtering with an analog *high-pass filter* (HPF) in the receive path is addressed. First, a detailed description of DC offset problems leads to a simple analysis of implementation tradeoffs. Next, *bit error rate* (BER) simulations are performed with a developed UTRA-FDD simulation platform and conclusions are drawn.

2 THE DC OFFSET PROBLEM

The causes to DC offset are numerous but can be characterized as being either *largely time-invariant* or *time-variant*. Largely time-invariant effects are caused by process mismatch and drift of analog circuitry that vary slowly versus temperature, aging, and current gain setting.

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Time-variant errors are caused mainly by parasitic LO signal coupling to mixer RF port (I''_{lo} in Fig. 1), LNA input-port ($I'_{lo}/2$ in Fig. 1), and antenna ($\alpha I'_{lo}/2$ in Fig. 1). The attenuation factor α describes (i) antenna impedance mismatch and (ii) the fraction of leakage at LNA input port which is radiated from the antenna and then subsequently reflected back from nearby moving objects to the receiver. The LO leakage depends on the actual implementation and is typically due to substrate, capacitive, and bond-wire coupling [1]. Any leakage between LO and RF ports of the mixer causes self-mixing which produces an undesired DC component. The instantaneous amount of self-mixing depends on antenna movement and AGC setting. As the latter is usually switchable, it is assumed that the DC offset frequency variation (although a humorous concept!) is dominated by receiver movements and, hence, the associated Doppler shift [2]. To consider a worst-case scenario, it is assumed that the maximum frequency content of all time-variant offset errors is determined by the maximum Doppler shift $f_{dob} = v_{max}/\lambda$.

The major concern is that DC offsets can easily reach values that are large enough to saturate stages following the mixer. For sufficient performance, the total DC offset power should be around 20dB lower than the total down-converted signal power [3]. Although circuit design techniques can be applied to reduce the DC offset [4], it is believed that additional compensation is needed. Several DC offset compensation techniques have been suggested [1, 5] but most of these techniques put rather steep requirements on hardware performance when operating at a bandwidth of 5MHz. Hence, in this paper only the simplest method is evaluated: DC offset filtering with analog HPF as illustrated in Fig. 1. It is assumed that the desired channel has been perfectly received/filtered at the LNA input. The DEMOD block contains an analog low-pass filter and limiting amplifier which precede ADC, de-spreader, and DSP.

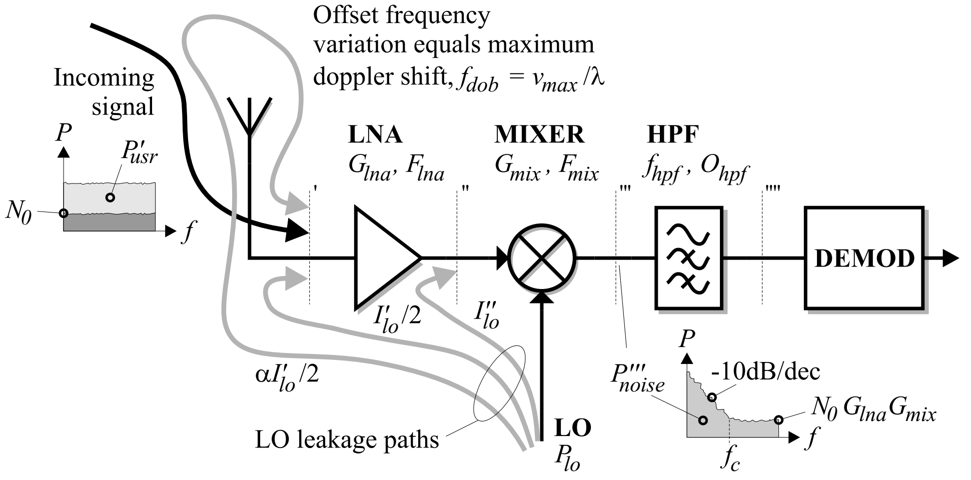

FIGURE 1: *Illustration of the DC offset problem in direct-conversion receiver.*

Unfortunately, DC offset filtering is associated with a number of important problems. Mainly, the low-frequency content of typical M-ary data is significantly distorted unless the HPF corner frequency, f_{hpf}, is less than about 0.1% of the data rate [1]. The requirement for a large time-constant leads to (i) slow response time and large group delay, (ii) requirement for large capacitor and resistor values infeasible in silicon technology, and (iii) possible data loss with wrong initial conditions [1, 6]. However, for continuously transmitted and received WCDMA noise-like signals, a more realistic tradeoff between distortion and response time is facilitated. Hence, the use of HPF compensation becomes more attractive. Possibly, it can be combined with an adaptive scheme to give a better overall implementation tradeoff.

3 A DC OFFSET MODEL

In order to arrive at an expression for the down-converted DC offset, some simplifications are in order. Phase changes for coupling mechanisms are neglected so that a worst-case scenario is considered. Further, perfect isolation between transmitter and receiver is assumed so that LO leakage to transmit path can be neglected. Nonlinearities and spectral imperfections of the LO signal are not considered either. As mentioned previously, an important quality factor is the ratio of DC offset power to down-converted signal power, η'''_{dsr}. By adopting the notation of Fig. 1 and neglecting the minor contribution from largely time-invariant errors,

$$\eta'''_{dsr} = \frac{P'''_{dco}}{P'''_{usr}} = \frac{P_{lo}I'_{lo}(1+\alpha)G_{lna}/2 + P_{lo}I''_{lo}}{P'_{usr}G_{lna}} \qquad (1)$$

at the reference plane before the HPF. Insertion of typical values in Eq. (1), reveals that η'''_{dsr} can be as large as 60-80dB at the specified sensitivity level [7]. This indicates the need for DC offset compensation. Note that the static part of the DC offset is removed effectively by the HPF. However, the dynamic portion of the mechanisms gives a moving self-mixing contribution at low frequencies. The highest offset frequency experienced is limited by a maximum Doppler shift around 1kHz ($v_{max} \simeq$ 250km/h). The worst-case scenario is shown in Fig. 2a where the full dynamic offset power, $\alpha I'_{lo}P_{lo}G_{lna}G_{mix}/2$, is shown at the the maximum Dobbler shift frequency. The ratio of time-variant offset power to signal power, η'''_{ddsr} is given by

$$\eta'''_{ddsr} = \frac{\alpha I'_{lo}}{2}\frac{P_{lo}}{P'_{usr}}, \qquad (2)$$

which can be on the order of 40-60dB in practice. Hence, an HPF filter attenuation, A_{hpf}, at 1kHz of 60-80dB is required in order to reach the target value of -20dB [3, 7]. From the design curves in Fig. 2b it is seen that such an attenuation can be obtained only with filter orders of 4, or higher, if a maximum corner frequency of 10kHz is required. This is a rather steep filtering requirement.

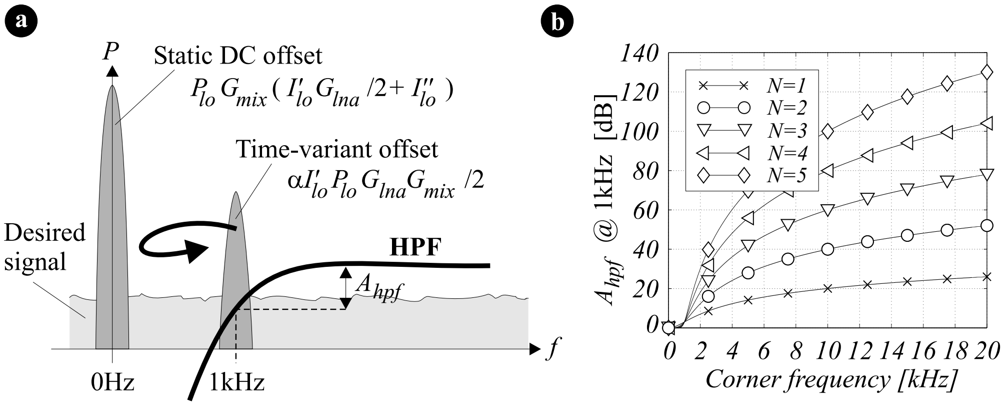

FIGURE 2: *Illustration of (a) static and dynamic offset with HPF characteristic and (b) HPF attenuation at 1kHz for various Butterworth filter orders (N) and configuration.*

The above analysis is exclusively minded for the prevention of saturation problems in stages after the mixer. Hereby, minimum filtering requirements for the HPF can be fixed so that the dynamic DC offset is reduced to adequate levels. However, the analysis does not include the signal degradation which is inherent to the filtering process. This issue is addressed in terms of user BER in the following.

4 UTRA-FDD/WCDMA SIMULATIONS

Based on the current UTRA-FDD/WCDMA proposal [7], a simulation platform is developed. The slot format for speech services as well as the baseband part of the downlink transmitter are illustrated in Figs. 3a and 3b. The incoming data stream consists of a sequence of identical slots which are constructed of four pilot symbols, one power control symbol, and 15 data symbols which are QPSK modulated [7]. This signal is modulated with a channelization code and a complex spreading code before it is pulse shaped with $p(t)$. The pulse shaping filter is a root raised cosine filter with a roll-off factor equal to 0.22, but to simplify simulations it is implemented as a Nyquist filter (roll-off factor equal to zero). In the current study, the spreading factor is fixed at 128 and the chip-rate is assumed to equal 4.096Mcps. It should be noted that the processing gain setting significantly affects the results. The used setup corresponds to the parameter settings for speech traffic.

In order to investigate the performance degradation associated with the use of HPF compensation in UTRA-FDD, a number of Monte-Carlo simulations have been conducted. The receiver setup is depicted in Fig. 3b. The transmitted signal is filtered through a simple radio channel, which is assumed to be either flat Rayleigh fading or constant unity (AWGN). Rayleigh fading is simulated according to Jakes' model [8] assuming 32 scatterers and a mobile speed of 50km/h. The succeeding noise source consists of (i) white Gaussian noise and (ii) an undesired signal component at 1kHz to represent the time-variant offset error in Fig. 2a. The Gaussian noise power is adjusted to the desired ratio of bit energy to noise spectral density (E_b/N_0). The 1kHz-component is set 60dB above the level of the desired signal. Subsequently, the signal with noise is filtered through an HPF with corner frequency f_{hpf} and order O_{hpf}. Butterworth characteristics are used to minimize ripple and group delay. The filtered signal is then demodulated by a standard *semi-coherent RAKE receiver* (SCRR). The channel state information is obtained by averaging two consecutive pilot-blocks; each block consisting of 4 pilot symbols. This enhances the SNR on the channel estimate. Based on the estimated data symbols from the RAKE receiver, the uncoded BER is computed. For both the flat fading and the AWGN channels, 240,000 bits are simulated. This gives accurate results for BER>10^{-3}.

The first set of simulations shown in Fig. 3c is based on the AWGN channel and without the time-variant offset. Hence, the results show the signal degradation caused by the HPF alone. The HPF-induced degradation in E_b/N_0 at two BER reference values is seen to increase with corner frequency and filter order as expected. Hence, for the HPF to provide the full DC offset suppression, it seems as if a choice of $O_{hpf} = 4$ and $f_{hpf} = 10$kHz gives the smallest distortion. If one can live with 0.3dB E_b/N_0-degradation, the combination of $O_{hpf} = 3$ and $f_{hpf} = 20$kHz is a possible way to reduce group delay. Note that as the corner frequency exceeds 20kHz, the signal degradation starts accelerating for the AWGN channel.

The second set of simulations include both types of channels and the time-variant offset at 60dB above the reference signal level. Without including the HPF, the time-variant offset completely corrupts the reception quality (BER=50%). From the AWGN results plotted in Fig. 3d it is noted that for $O_{hpf} \geq 3$, the HPF is able to effectively remove the 1kHz offset component. Again, the E_b/N_0 degradation is more noticeable at $f_{hpf} = 20$kHz. It is interesting to note that when the Rayleigh fading channel is included, the E_b/N_0 degradation levels remain approximately unchanged. At BER=10% which is close to actual operating point, the degradation for the 4th order 10kHz HPF is less than 0.2dB. Again 2nd order implementations are not capable of removing the time-variant offset. As the two channel types represent the worst and best conditions, it is expected that the actual degradation is bounded by the results given in Fig. 3.

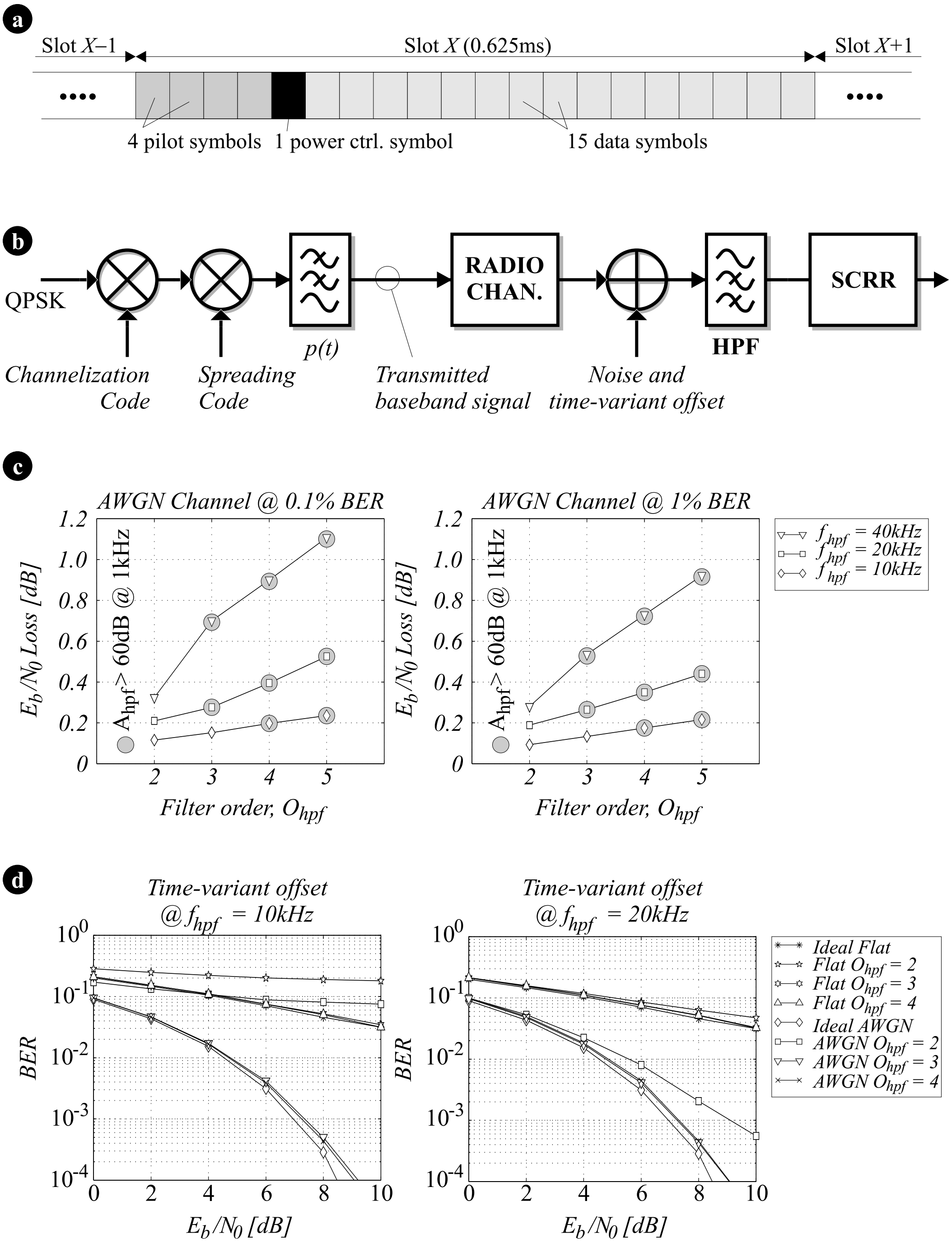

FIGURE 3: *Illustration of (a) slot configuration, (b) baseband transmitter and receiver configuration, and (c)-(d) simulation results for various HPF and system configurations.*

For a spreading factor of 4 the 2nd and 3rd order 10kHz HPF fail while a 4th order filter sees a relative E_b/N_0 loss of 0.2dB for BER=10%. However, a change in frame structure adds pilot bits to improve the channel estimate and an overall E_b/N_0 gain of 0.5dB results. It follows that a filter order around three or four as well as a corner frequency around 10kHz are proper choices. The 4th order 10kHz HPF displays a group delay ripple of 46μs over the 10-5,000kHz signal band. The delay distortion may be reduced by adopting a smaller filter order. However, this calls for additional compensation to meet required suppression levels. Further, the tested filter implementations give a negligible increase in power control loop delay for frequencies a few kHz above the corner frequency. Hence, the insertion of an HPF in the receiver chain should have only limited impact on power control performance.

5 CONCLUSIONS

In this paper, the feasibility of DC offset filtering for a UTRA-FDD/WCDMA direct-conversion receiver has been investigated for an absolute worst-case scenario. A simple DC offset analysis reveals that the HPF should at least provide 60dB of attenuation at the maximum Doppler shift. Further, uncoded BER simulations reveal that 0.2-0.3dB of E_b/N_0-degradation is to be expected from inserting a 10kHz HPF in the receive path. As 10kHz corresponds to 0.24% of the chip-rate it appears that WCDMA spectral characteristics facilitate the use of HPF compensation. Simulations show that 2nd order filters fail to meet total suppression requirements. Further, for spreading factors of 4 it is found that 4th order filters are required to meet requirements. However, combined with an adaptive compensation technique, the use of lower order filters may prove to be an interesting alternative. As such, HPF compensation appears to be a viable solution for highly integrated WCDMA direct-conversion receivers.

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RF Receiver Requirements for 3G WCDMA Mobile Equipment

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TECHNICAL FEATURE

RF RECEIVER REQUIREMENTS FOR 3G W-CDMA MOBILE EQUIPMENT

The first standardization phase for upcoming third-generation (3G) wireless communications is coming to an end. As is typical for standardization work, sufficient analog performance has been assumed and predominant emphasis has been placed on modulation and coding. However, recent revisions to the standardization document for the European wideband CDMA (W-CDMA) proposal,[1] known as UTRA/FDD, enable a prediction of required performance for the RF front end. Such requirements are important when preparing commercial products for the new market. In this article, receiver requirements for the mobile unit are derived in terms recognizable by the RF designer.

For RF designers who are experienced with 2G TDMA/FDMA wireless systems, the introduction of W-CDMA requires some change of mind. First, rather than being separated in frequency or time, users are now separated by orthogonal codes. As the use of codes implies a spectral spreading, the treatment of overall signal-to-noise ratio requires considerations that are different from those required for TDMA systems. Second, a single radio channel behaves more like band-limited noise than a single sinusoid. Statistical terms like peak-to-average power ratio are therefore necessary to reflect this new constellation of signals.

TABLE I

UTRA/FDD W-CDMA SYSTEM CHARACTERISTICS

Parameter	*Specification*
Uplink frequency band (Tx) (MHz)	1920 to 1980
Downlink frequency band (Rx) (MHz)	2110 to 2170
Tx-to-Rx frequency separation (MHz)	134.8 to 245.2
Nominal channel spacing (MHz)	5
Chip rate (Mcps)	3.84

General characteristics of the UTRA/FDD system are listed in ***Table 1***.[1] The nominal frequency spacing between adjacent channels is 5 MHz and the signal bandwidth is 3.84 MHz (corresponding to the chip rate). The downlink employs quadrature phase-shift keying (QPSK) modulation. Root-raised-cosine filtering is applied to shape the spectrum. Using orthogonal spreading and gold-code scrambling, several CDMA channels are multiplexed onto the same frequency channel.[2] Hence, the received signal consists of many simultaneously transmitted channels that use the same carrier frequency. As a result, large amplitude variations occur over time. The uplink is similar but uses a more complicated hybrid-QPSK modulation scheme. Although a combination of code allocation and complex scrambling is used to minimize the number of

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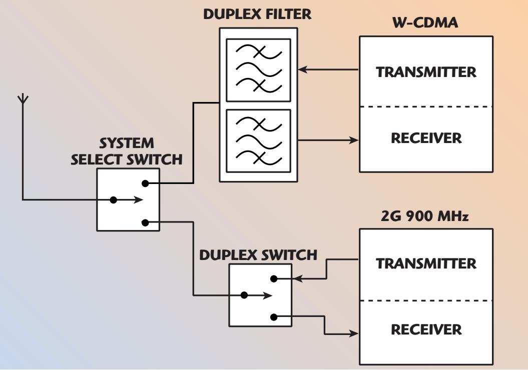


▲ *Fig. 1 Example of a duplex arrangement of a mobile receiver unit including 3G W-CDMA and 2G TDMA systems.*

signal nulls,[2] the envelope of the transmitted signal continues to display large amplitude variations. These variations place high linearity requirements on the power amplifier, which is believed to be a major RF design challenge.

Until the new 3G system delivers the coverage and services offered by the well-established 2G systems, multimode terminals with both 2G and 3G capabilities are required. Such a transceiver system configured for two wireless systems is shown in ***Figure 1***. In the transceiver system, a system select switch is used for selection between a 2G 900 MHz system (E-GSM) and a 3G W-CDMA system. The 2G system applies time division duplex (TDD) as well as frequency division duplex (FDD), and a duplex switch is used to select transmit or receive modes. Since the considered W-CDMA system only applies FDD and thus employs simultaneous transmission and reception, a duplex filter is required to provide isolation between the transmitter and the receiver. The continuous presence of the high power transmitter signal causes problems with spurious leakage from the transmit band located at a 134.8 to 245.2 MHz offset. Unless sufficient selectivity is available between the Tx and Rx bands, this spurious transmitter signal will cause severe dynamic range and intermodulation problems in the receiver chain.

From the previous comments, it should be clear that a high performance duplex circuit with good Tx-Rx isolation is needed. Based on data for switches and ceramic duplex filters available commercially today, an estimate of duplex circuit performance is listed in ***Table 2***. The 4 dB loss in the receive path has severe implications for the overall noise figure, however, since a small physical size is mandatory, it appears inevitable. The power level of the transmitter leakage signal at the receiver input is determined by taking the transmitter power class, adding the specified tolerance (+1/–3 or +2/–2 dB), adding the transmit path loss (2.5 dB) and subtracting the expected duplex filter isolation. The result is between –23.5 and –34.5 dBm and, since it is still being debated which maximum power levels will apply to hand-held units, a spurious transmitter level around –30 dBm is expected to be typical. The receiver must be able to handle this signal without significant performance degradation.

In the next section, the test cases specified in the standardization document[1] are studied in detail and issues of noise, second-order distortion, third-order intermodulation, selectivity and oscillator phase noise are treated. From this treatment, performance requirements for the W-CDMA receiver are derived. Note that all derived expressions assume insertion in decibel/decibel relative to 1 mW (dB/dBm) numbers and that signal powers are specified over a channel bandwidth (3.84 MHz) as in the UTRA/FDD standard.[1] A complete list of symbols and conventions used in this paper can be found in the sidebar on the following page. (Receiver requirements are only approximate since they do not relate to a specific receiver architecture.) Given a detailed architecture, more accurate requirements can be derived by studying the test cases specified by the standard.[1] However, for the purpose of assessing challenges faced by RF designers of 3G wireless equipment, the treatment is adequate. This article concludes with a direct-conversion receiver example, which illustrates a possible implementation that complies with derived requirements.

TABLE II

ANTICIPATED PERFORMANCE FOR W-CDMA DUPLEX ARRANGEMENT

Duplexer Parameter	*Anticipated Performance*
Duplex filter Tx loss (dB)	< 1.5
Duplex filter Rx loss (dB)	< 3.0
Loss of system select switch and antenna feed (dB)	< 1.0
Combined Tx loss (dB)	< 2.5
Combined Rx loss (dB)	2.0 to 4.0
Duplex filter Tx-Rx isolation in Tx band (dB)	> 60
Transmitter power classes (hand-held and fixed-mounted units) (dBm)	33/27/24/21
Typical transmitter leakage signal at receiver input (dBm)	–30

TEST CASES

The UTRA/FDD standard[1] describes a number of test scenarios in which the user bit rate is fixed at 12.2 kbps and the bit error rate (BER) must be below 10^{-3}. The desired downlink channel signal includes two or more orthogonal CDMA channels, which comprise the dedicated physical channel (DPCH) carrying the user data, a synchronization channel and, in some cases, other users' data channels. The standard specifies total power levels within the channel bandwidth and the relative level of the DPCH. For simplicity, the desired channel power is specified as the DPCH channel power throughout this article.

In the baseband receiver, the despreading process concentrates the desired signal energy in a bandwidth that corresponds to the channel symbol rate. Since noise and interference are uncorrelated with the despreading code, noise is not concentrated in a smaller bandwidth. Further, signal decoding results in a coding gain, and the total resulting improvement in signal-to-noise ratio is defined as the user data processing gain given by[3]

$$\begin{aligned} G_P &= 10\log_{10}\left(\frac{3.84\,\text{Mcps}}{12.2\,\text{kbps}}\right) \\ &= 25\,\text{dB} \end{aligned}$$

Note that this notation differs from the standard CDMA processing gain definition, which relates correlation time to chip time.[6] However, the chosen definition facilitates a more general comparison of different systems. The required minimum E_b/N_t for a BER of 10^{-3} is determined from simulations to be 5.2 dB.[3] The term E_b/N_t is used here instead of the traditional notation E_b/N_0 since most tests include interference in addition to noise. It is also suggested that an implementation margin be added to account for various baseband imperfections.[3] The required effective E_b/N_t is then expressed as

$$\left(\frac{E_b}{N_t}\right)_{eff} \approx 7\,dB$$

which complies with the chosen definition of processing gain.

NOISE FIGURE

The noise figure (NF) of the UTRA receiver is calculated from the standard's reference sensitivity test. The desired channel power is $P_{R,DPHC} = -117$ dBm. Using the previously determined $(E_b/N_t)_{eff}$ requirement and including the user data processing gain, the maximum allowable noise power within the channel bandwidth is calculated to be

$$\begin{aligned}P_N\left(acceptable\right)\\ &= P_{R,DPHC} - \left(\frac{E_b}{N_t}\right)_{eff} + G_p\\ &= -117\,dBm - 7\,dB + 25\,dB\\ &= -99\,dBm\end{aligned}$$

When the NF of the receiver and the bandwidth (BW) are known, the actual noise power is determined using

$$\begin{aligned}P_N\left(actual\right) &= NF + 10\log_{10}\\ &\quad\left(k \bullet T_0 \bullet BW\right)\\ &= NF - 138\,dBW\\ &= NF - 108\,dBm\end{aligned}$$

where

k = Boltzmann's constant
T_0 = standard noise temperature

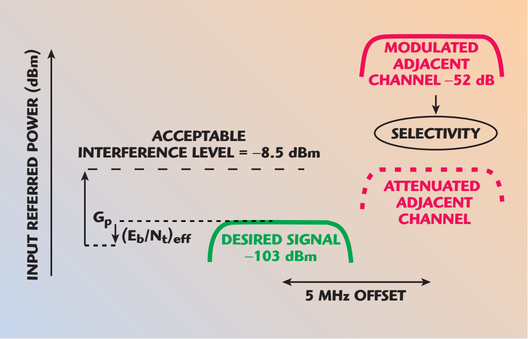
Since the actual noise power must be lower than or equal to the acceptable noise power, the NF requirement is

$$\begin{aligned}NF &\le P_N\left(acceptable\right) + 108\,dBm\\ &= -99\,dBm + 108\,dBm\\ &= 9\,dB\end{aligned}$$

This NF requirement is for the entire receiver. Subtracting the loss of 4 dB in the duplex circuit, the NF requirement for the rest of the receiver is 5 dB. This level appears to be within reach for low cost integrated receivers. It should be noted that the NF must be met in the presence of the transmitter leakage signal.

ADJACENT-CHANNEL SELECTIVITY

Adjacent-channel selectivity is defined as the relative attenuation of the adjacent-channel power. Selectivity includes filtering at the IF, analog baseband and digital baseband, and the frequency sensitivity of the demodulator. A test setting requirement for the first adjacent-channel selectivity is shown in


INPUT REFERRED POWER (dBm)
MODULATED ADJACENT CHANNEL –52 dB
SELECTIVITY
ACCEPTABLE INTERFERENCE LEVEL = –8.5 dBm
ATTENUATED ADJACENT CHANNEL
G_p
$(E_b/N_t)_{eff}$
DESIRED SIGNAL –103 dBm
5 MHz OFFSET

▲ *Fig. 2 Test for adjacent-channel selectivity.*

Figure 2. In this test, the desired signal power is $P_{R,DPHC} = -103$ dBm. Since this level is 14 dB above the sensitivity limit, noise is of minor importance. The first adjacent channel has a power of $P_{AC1} = -52$ dBm centered around a 5 MHz offset.

Treating the adjacent-channel signal as noise, the required first adjacent-channel selectivity can be derived. The acceptable interference level, P_I, is determined in the same

NOTATION, SYMBOLS AND ABBREVIATIONS USED IN THIS ARTICLE

Note that all power levels and intercept points are given in decibels relative to 1 mW (dBm), power levels of modulated signals are measured within a channel bandwidth (3.84 MHz) and all gain loss values are given in decibels (dB).

BER:	bit error rate
BW:	channel bandwidth (3.84 MHz)
DPCH:	dedicated physical channel
E_b/N_t**:**	ratio of average bit energy to noise and interference power spectral density
$(E_b/N_t)_{eff}$**:**	effective E_b/N_t including an implementation margin
G_p**:**	user data processing gain
IIP_2**:**	second-order intercept point referred to the input
IIP_3**:**	third-order intercept point referred to the input
k:	Boltzmann's constant of 1.38×10^{-23} J/K
NF:	noise figure
P_{AC1}**:**	power of the first adjacent channel
P_{BLOCK}**:**	power of blocker signal
P_{BLeak}**:**	power of blocking signal leaking to the demodulator
P_I**:**	power of intermodulation product
P_{I3}**:**	power of third-order intermodulation products
P_{INT}**:**	interfering signal power
P_N**:**	noise power
P_{N+1}**:**	noise and interference power
$P_{R,DPCH}$**:**	received DPCH channel power
P_{TxLeak}**:**	power of transmitter leakage signal
P_{2DIS}**:**	power of second-order distortion products
$P_{2DISeff}$**:**	effective power of second-order distortion products (after removal of DC and components above the signal bandwidth)
T_0**:**	standard noise temperature of 290 K

manner as was used during the NF calculation:

$$\begin{aligned} P_I &= P_{R,DPCH} - \left(\frac{E_b}{N_t}\right)_{eff} + G_P \\ &= -103\,dBm - 7\,dB + 25\,dB \\ &= -85\,dBm \end{aligned}$$

and the adjacent-channel selectivity requirement at 5 MHz is

$$\begin{aligned} &\text{Selectivity}(5\,MHz) \\ &\quad \geq P_{AC1} - P_I \\ &\quad = -52\,dBm - 85\,dBm \\ &\quad = 33\,dB \end{aligned}$$

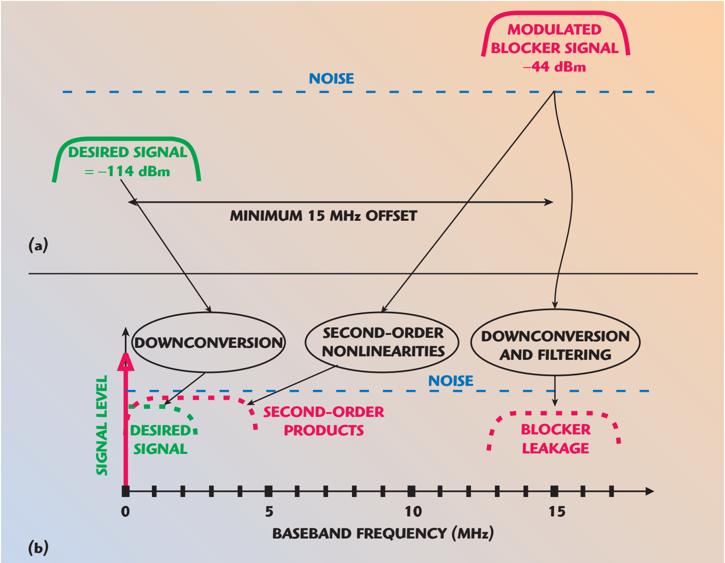
SECOND-ORDER INTERCEPT POINTS

Low even-order distortion, especially second-order distortion, is crucial to the receiver's performance because of the presence of strong modulated signals with time-varying envelopes. When a second-order nonlinearity is exposed to such a signal, a spurious baseband signal proportional to the squared envelope is generated at baseband, which disturbs the reception of the desired signal. Two such groups of disturbing signals are present: unwanted channels in the receive band (downlink) and the transmitter leakage signal. (The problem of unwanted channels in the receive band is addressed in the in-band blocker test.^{1})

The spectral shape of these signals is the same as for the wanted signal (root-raised-cosine) but the spectral shape of the second-order product is different, as shown in ***Figure 3***. A significant DC component is present and the spectrum is broader than the desired baseband signal. Typically, the DC component represents 50 percent of the power while 50 percent of the remaining power lies above the desired signal bandwidth. Consequently, a combination of highpass and lowpass filtering can improve E_b/N_t by approximately 6 dB. Highpass filtering of the W-CDMA signal can be accomplished with negligible degradation of performance due to the large-signal bandwidth.^{4} However, the actual improvement in E_b/N_t depends on the present signal configuration and is different for uplink and downlink signals. According to simulations, the possible suppression of the spurious second-order product ranges from 4 to 13 dB.

IIP_2 is determined by the in-band blocker test. The desired signal has a power of $P_{R,DPCH} = -114$ dBm. The modulated blocker has a power of $P_{BLOCK} = -44$ dBm and is offset in frequency by a minimum of 15 MHz. In this scenario, the demodulator experiences three sources of interference: noise with power P_N, highpass and lowpass filtered second-order products of the blocker signal with power $P_{2DISeff}$ and blocker leakage around 15 MHz at baseband with power P_{BLeak}. Since the power of the desired signal in this test is 3 dB higher than for the sensitivity test, it is assumed that noise constitutes 50 percent of the total disturbing power. For simplicity, the remaining power is divided equally (25 percent 6 dB) between the second-order products and the blocker leakage. The acceptable noise plus interference level measured at the antenna input is expressed as

$$\begin{aligned} P_{N+I} &= P_{R,DPCH} - \left(\frac{E_b}{N_t}\right)_{eff} + G_P \\ &= -114\,dBm - 7\,dB + 25\,dB \\ &= -96\,dBm \end{aligned}$$



▲ *Fig. 3 In-band modulated blocker test; (a) RF spectrum with desired signal and offset modulated blocker, and (b) baseband spectrum with desired and disturbing signals.*

and the acceptable levels are

$$\begin{aligned} P_N &= P_{N+I} - 3\,dB \\ &= -99\,dBm \end{aligned}$$

and

$$\begin{aligned} P_{BLeak} &= P_{2DISeff} \\ &= P_{N+I} - 6\,dB \\ &= -102\,dBm \end{aligned}$$

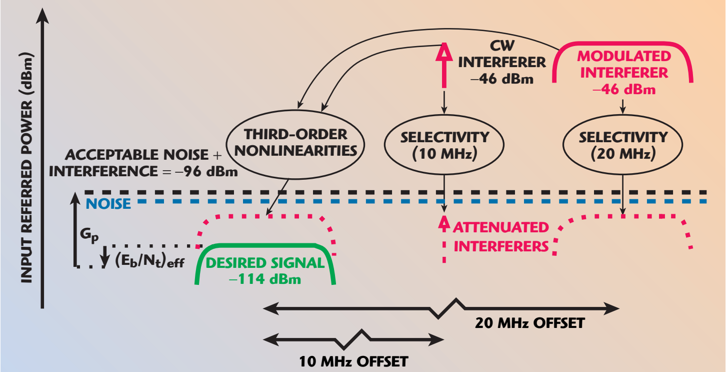
Note that $P_{2DISeff}$ is the effective level of second-order distortion that can be tolerated. However, as a 6 dB improvement due to baseband filtering is assumed, an additional 6 dB of second-order distortion actually can be accepted. Hence, in the calculation of the required IIP_2, the value of $P_{2DISeff}$ is corrected to $P_{2DIS} = P_{2DISeff} + 6$ dB. Consequently, the requirement to the second-order input intercept point is obtained using

$$\begin{aligned} &IIP_2(15\,MHz) \\ &\quad \geq 2P_{BLOCK} - P_{2DIS} \\ &\quad = 2(-44)\,dBm - (-102 + 6)\,dBm \\ &\quad = 8\,dBm \end{aligned}$$

The necessary selectivity for a channel at 15 MHz offset is found to be

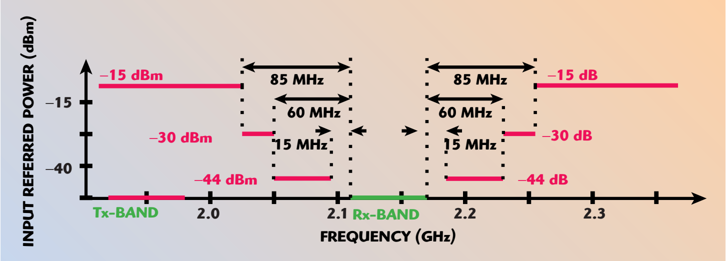
$$\begin{aligned} &\text{Selectivity}(15\,MHz) \\ &\quad \geq P_{BLOCK} - P_{BLeak} \\ &\quad = -44\,dBm - (-102)\,dBm \\ &\quad = 58\,dBm \end{aligned}$$

In the specification document, an additional blocker test is specified with


INPUT REFERRED POWER (dBm)
CW INTERFERER –46 dBm
MODULATED INTERFERER –46 dBm
THIRD-ORDER NONLINEARITIES
SELECTIVITY (10 MHz)
SELECTIVITY (20 MHz)
ACCEPTABLE NOISE + INTERFERENCE = –96 dBm
NOISE
G_P
$(E_b/N_t)_{eff}$
DESIRED SIGNAL –114 dBm
ATTENUATED INTERFERERS
20 MHz OFFSET
10 MHz OFFSET

▲ *Fig. 4 Intermodulation test.*

▼ *Fig. 5 Out-of-band CW blocker test.*


INPUT REFERRED POWER (dBm)
–15 dBm
–15
–30 dBm
–40
–44 dBm
85 MHz
60 MHz
15 MHz
85 MHz
60 MHz
15 MHz
–15 dB
–30 dB
–44 dB
Tx-BAND
2.0
2.1
Rx-BAND
2.2
2.3
FREQUENCY (GHz)

a blocker power of –56 dBm and a 10 to 15 MHz frequency offset. Corresponding to previous calculations, the IIP_2 requirement is derived using

$$\begin{aligned}
&IIP_2(10\,MHz)\\
&\quad \geq 2P_{BLOCK} - P_{2DIS}\\
&\quad = 2(-56)\,dBm - (-102+6)\,dBm\\
&\quad = -16\,dBm
\end{aligned}$$

Finally, the required out-of-band IP_2 is determined by the transmitter leakage level at the receiver input. The disturbance mechanisms are the same as those shown previously but the blocker signal is replaced by the transmitter leakage signal. Since the duplex distance is a minimum 134.8 MHz, the direct transmitter leakage through the receiver to the demodulator is insignificant.

Since the transmitter signal is always present, the second-order products should be sufficiently suppressed (for example, 10 dB below the noise level). A rough estimate of IIP_2 is then determined using

$$\begin{aligned}
IIP_2(Tx) &\geq 2P_{TxLeak} - (P_N + 6\,dB\\
&\quad -10\,dB)\\
&= 2(-30)\,dBm -\\
&\quad (-99-4+6-10)\,dBm\\
&= 47\,dBm
\end{aligned}$$

The noise level has been corrected for the 4 dB duplexer loss, thus $IIP_2(Tx)$ refers to the circuit after the duplexer. Again, a 6 dB improvement due to highpass and lowpass filtering has been assumed.

THIRD-ORDER INTERCEPT POINTS

The third-order intercept point of the UTRA receiver is determined using the intermodulation test described in the UTRA standard. The intermodulation test scenario is shown in ***Figure 4***. The desired signal is at $P_{R,DPCH}$ = –114 dBm, 3 dB above the minimum sensitivity. Two interfering signals are offset 10 and 20 MHz from the desired signal. The first interferer is a CW signal at P_{INT} = –46 dBm; the second interferer is a modulated signal with a power of P_{INT} = –46 dBm. As the desired signal is close to the minimum sensitivity level, both noise and interference must be taken into account. Assuming that the third-order intermodulation product of the two interferers may be treated as noise, the maximum level of noise and interference is found to be

$$\begin{aligned}
P_{N+I} &= P_{R,DPCH} - \left(\frac{E_b}{N_t}\right)_{eff} + G_P\\
&= -114\,dBm - 7\,dB + 25\,dB\\
&= -96\,dBm
\end{aligned}$$

where P_{N+I} is referred to the antenna input.

In this test case, several interfering products are created, thus the allowable noise and interference power (P_{N+I}) must be distributed. The assumed power distribution is: noise, 50 percent of power (–3 dB); intermodulation, 15 percent of power (–8 dB); CW interferer's blocking effect, 15 percent of power (–8 dB); modulated interferer's blocking effect, 15 percent of power (–8 dB); and oscillator noise, five percent of power (–13 dB). Second-order distortion products are neglected. The power level corresponding to each of the interfering or blocking products is then P_{N+I} – 8 dB = –104 dBm. This power level, along with the relationship between intermodulation power level and input intercept point, gives the minimum receiver IIP_3:

$$\begin{aligned}
&IIP_3(10/20\,MHz)\\
&\quad \geq P_{INT} + \frac{1}{2}\left(P_{INT} - (P_{N+I} - 8\,dB)\right)\\
&\quad = -46\,dBm + \frac{1}{2}\left(-46 - (-104)\right)dBm\\
&\quad = -17\,dBm
\end{aligned}$$

In addition, the test results in two selectivity requirements are

$$\begin{aligned}
&Selectivity(10\,MHz, CW)\\
&\qquad \geq P_{INT} - (P_{N+I} - 8\,dB)\\
&\qquad = -46\,dBm - (-104)\,dBm\\
&\qquad = 58\,dB
\end{aligned}$$

and

$$\begin{aligned}
&Selectivity(20\,MHz)\\
&\qquad \geq P_{INT} - (P_{N+I} - 8\,dB)\\
&\qquad = -46\,dBm - (-104)\,dBm\\
&\qquad = 58\,dB
\end{aligned}$$

The out-of-band CW blocker test, shown in ***Figure 5***, indirectly sets an IP_3 requirement for the receiver. If a CW blocker is present at some frequency distance (for example, 67.4

MHz) from the receive band and the transmitter leakage signal is located at the double frequency distance (134.8 MHz), then a third-order intermodulation product is created at the receive frequency in the same way as the intermodulation test described previously.

The level of the CW blocker and the attenuation in the duplex filter depend on the frequency band. For typical duplex filters, the CW blocker level after the duplex filter is below –45 dBm. For calculation of the $\mathrm{IIP_3}$, the transmitter leakage signal of –30 dBm and the CW blocker of –45 dBm are replaced with two signals of equal level such that

$$\begin{aligned} P_{INT} &= \frac{1}{3}\left(-30\,\mathrm{dBm}\right)+\frac{2}{3}\left(-45\,\mathrm{dBm}\right) \\ &= -40\,\mathrm{dBm} \end{aligned}$$

since the interferer closest to the desired signal has the highest weight in third-order intermodulation. Because of the large frequency offset, blocking effects are negligible and the allowable interference level is $P_{N+I} - 3$ dB since noise contributes 50 percent of the power. Correcting this level with the duplexer loss of 4 dB, an $\mathrm{IIP_3}$ is found to be

$$\begin{aligned} &\mathrm{IIP_3}\left(67.4\,/\,134.8\,\mathrm{MHz}\right) \\ &\quad\geq P_{INT}+\frac{1}{2}\Big(P_{INT}-\big(P_{N+I}- \\ &\qquad 3\,\mathrm{dB}-4\,\mathrm{dB}\big)\Big) \\ &\quad= -40\,\mathrm{dBm}+\frac{1}{2}\Big(-40\,\mathrm{dBm}- \\ &\qquad \big(-96\,\mathrm{dBm}-3\,\mathrm{dB}-4\,\mathrm{dB}\big)\Big) \\ &\quad\approx -8\,\mathrm{dBm} \end{aligned}$$

This number is for the receiver part after the duplexer and is highly dependent on the actual duplexer characteristics.

IMAGE REJECTION

The required image rejection also can be determined from the out-of-band blocker test. If the image frequency is distanced at more than 85 MHz from the receive band, the necessary rejection is

$$\begin{aligned} &\text{Image rejection } (> 85\ \mathrm{MHz}) \\ &\quad\geq P_{BLOCK}-\left(P_{N+I}-3\,\mathrm{dB}\right) \\ &\qquad -15\,\mathrm{dBm}-\left(-96\,\mathrm{dBm}-3\,\mathrm{dB}\right) \\ &\quad= 84\,\mathrm{dB} \end{aligned}$$

In the calculation it has been noted that noise constitutes 50 percent of the disturbing power P_{N+I}.

OSCILLATOR PHASE NOISE

The presence of blocking signals sets requirements for the LO noise sidebands. The worst-case scenario is probably set by the intermodulation test where a –46 dBm CW blocker is present at a 10 MHz offset. Allowing five percent of the disturbing power in this test to come from the oscillator noise, the LO noise power must be below P_{N+I} – 13 dB = –109 dBm. This level corresponds to –63 dBc measured over a 3.84 MHz bandwidth when taken relative to the CW-blocker carrier. This number can be transferred to the LO since it represents a cross-modulation phenomenon. The spectral shape of the LO noise sidebands is unknown, however, taking the case of a flat spectrum seems reasonable because of the large frequency offset. With this assumption, the –63 dBc over 3.84 MHz corresponds to a power spectral density of –129 dBc/Hz. This specification must be met for an offset from the LO carrier of more than 10 MHz – BW/2 ≈ 8 MHz.

REQUIREMENT SUMMARY

A summary of receiver requirements for the entire receiver and the part of the receiver that follows the duplex circuits is listed in ***Table 3***.

RECEIVER EXAMPLE

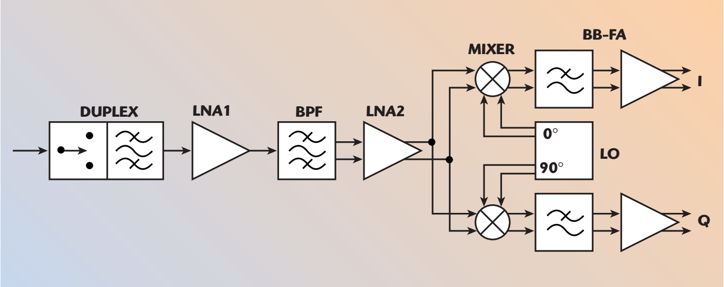
Because of its high noise and selectivity performance, the heterodyne receiver architecture has been the preferred architecture for the 2G market. However, as issues of power consumption, cost and size become more critical than ever, other architecture candidates are being explored. Recently, homodyne (or direct-conversion) receivers have emerged for the GSM market and many consider this architecture the proper choice for 3G systems. A particular nicety is the fact that the large signal bandwidth makes W-CDMA systems less susceptible to the 1/f noise and DC off-set problems inherent in homodyne receivers.

An example of an UTRA/FDD direct-conversion receiver is shown in ***Figure 6***. An interstage bandpass filter is used to provide sufficient attenuation of the transmitter leakage signal. Sufficient selectivity with low insertion loss is possible with commercial ceramic or surface

TABLE III

SUMMARY OF REQUIREMENTS

Requirement	Entire Receiver	After Duplex
Noise figure (dB)	≤ 9	≤ 5
In-band selectivity (dB)		
first adjacent channel (5 MHz)	≥ 33	≥ 33
CW interferer (10 MHz)	≥ 58	≥ 58
third adjacent channel (15 MHz)	≥ 58	≥ 58
modulation blocker (> 15 MHz)	≥ 58	≥ 58
Intercept points (dBm)		
$\mathrm{IIP_2}$ (10 MHz)	≥ –16	≥ –18
$\mathrm{IIP_2}$ (15 MHz)	≥ 8	≥ 6
$\mathrm{IIP_2}$ (Tx)		≥ 47
$\mathrm{IIP_3}$ (10/20 MHz)	≥ –17	≥ –19
$\mathrm{IIP_3}$ (67.4/134.8 MHz)		≥ –8
Image rejection (> 85 MHz) (dB)	≥ 84	n/a
Oscillator noise sidebands at > 8 MHz offset (dBc/Hz)	≤ –129	



▲ *Fig. 6 Direct-conversion receiver including filter.*

TABLE IV

BLOCK SPECIFICATIONS FOR A DIRECT-CONVERSION RECEIVER

Block	Duplexer	LNA1	BPF	LNA2	Mixer	BB-FA	Combined	Required
Gain in Rx band (dB)	–3 ±1	15 ±1	–2 ±1	8 ±1	10 ±1			
Rx/Tx selectivity (dB)	≥ 60	≥ 0	≥ 21	≥ 0	≥ 0	≥ 0		
Noise figure (dB)	≤ 4	≤ 2.5	≤ 3	≤ 3	≤ 15	≤ 25	≤ 8.8	≤ 9
IIP_2 (15 MHz) (dBm)					≥ 37	≥ 47	≥ 8.5	≥ 8
IIP_2 (Tx) (dBm)					≥ 37	≥ 47	≥ 48.5	≥ 47
IIP_3 (67.4/134.8 MHz) (dBm)		≥ –3					≥ –3	≥ –8
IIP_3 (10/20 MHz) (dBm)		≥ –3		≥ 3	≥ 10	≥ 20	≥ –16.8	≥ –17

Note: The numbers for IIP_2 (Tx) and IIP_3 (67/135 MHz) are for the receiver part after the duplexer. Other numbers are combined values for the entire receiver, including duplex filter and system select switch.

acoustic wave (SAW) filters. The filter may have a single-ended or balanced output, however, the second low noise amplifier (LNA) stage should have a balanced output to facilitate good even-order distortion performance of the mixers.

Overall block requirements are listed in ***Table 4***. Due to the interstage bandpass filter, the overall out-of-band IIP_3 performance is dominated by the first LNA and this block must comply with the overall requirement of –8 dBm. Note that the IIP_3 has been set slightly higher at –3 dBm to relieve the performance requirement to the mixer and BB-FA blocks. For the direct-conversion receiver, the mixer and baseband unit are critical components for the overall linearity and noise while most gain is placed with the baseband unit. IIP_2 and IIP_3 requirements to the mixer and baseband units are difficult but certainly realistic. With respect to noise, the baseband unit constitutes a major challenge if low cost technologies such as CMOS are to be used. However, recent work has shown much progress in this area.[5] In the example, 1 dB of gain tolerance of the first receiver blocks is assumed. A higher tolerance makes it difficult to meet any worst-case specification.

Most of the Tx signal suppression is obtained in the duplex and interstage bandpass filters. The interstage bandpass filter also attenuates out-of-band blockers but, since the filter characteristics are typically less steep in the upper stop band, only limited selectivity toward these disturbing signals can be assumed. Hence, the BB-FA unit must implement most of the required selectivity derived in this article. In-band disturbances can be suppressed only at baseband. In this sense, one of the most fundamental decisions is the distribution of filtering requirements between analog and digital hardware. With the high chip rate employed in 3G W-CDMA systems, constraints of low power limit the available analog-to-digital converter (ADC) resolution.

Assuming a sampling frequency of 15.36 MHz (corresponding to four samples per chip), it is not possible to use digital filtering with the third adjacent channel and the first modulated blocker (> 15 MHz) due to aliasing. Hence, these interferers must be suppressed in analog hardware prior to sampling. With the first and second adjacent channels each additional bit enables 6 dB of digital selectivity. Preliminary analyses[7] indicate that four to five bits are required as minimum ADC resolution (no digital selectivity), and 8 to 10 dB bits immediately appears to be a necessary choice. This selectivity may be combined with a fourth-order Butterworth analog filter (2.5 MHz cutoff frequency) to achieve the listed selectivity requirements.

Issues other than those considered here are critical to the implementation of the direct-conversion receiver. Such issues include DC offsets, in-phase and quadrature gain/phase imbalance problems, LO-to-antenna leakage and susceptibility to 1/f noise. Baseband highpass filtering should be combined with adaptive correction for sufficient performance of this architecture.[4]

CONCLUSION

Detailed specifications for a W-CDMA receiver were derived from the tests presented in the standardization documents. It was shown that a direct-conversion receiver architecture with reasonable block requirements is capable of meeting derived specifications. The problems caused by the continuous presence of the transmitter leakage signal emphasize the need for a high performance duplex filter. There are still implementation challenges left for RF designers, but the specifications seem reasonable enough to facilitate the design of the low power, low cost, hand-held multimedia products that the world is awaiting.

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RF Requirements for UTRA/FDD Tranceivers

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RF Requirements for UTRA/FDD Transceivers*

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Abstract

Unified RF requirements are derived for an UTRA/FDD compliant mobile transceiver. Consideration of system issues, multi-mode operation, and interfacing concerns leads to detailed receiver and transmitter calculations based on existing UMTS specifications. Finally, compliant and design-compatible transceiver requirements are derived.

1. Introduction

The UTRA/FDD mobile standard provides an improved platform for personal communications including voice, data, and multimedia services compared to current 2G systems. In order for UTRA/FDD to retain a competitive advantage, high-performance and low-cost *user equipment* (UE) must be made available to the general public. In this work, unified UTRA/FDD UE transceiver requirements are derived on block level, based on previous work for the receiver branch [2] and ongoing work for the transmitter branch [4].

2. Duplex Aspects

As UTRA/FDD is based on *frequency division duplex* (FDD), the required isolation between *transmitter* (Tx) and *receiver* (Rx) can only be provided by means of a duplex filter. The performance of the duplex filter is very important for the transceiver requirements and since the available physical size is limited, several design compromises apply:

- A low insertion loss in the Tx-band is difficult to combine with a high Tx-Rx isolation in the Rx-band.
- A low insertion loss in the Rx-band is difficult to combine with a high Tx-Rx isolation in the Tx-band.

The transmitter-induced noise level at the receiver input (Rx-band) is determined by the transmitter noise level and the duplexer isolation. A level of -111 dBm/3.84 MHz is shown in later sections to give an acceptable degradation of receiver sensitivity. To reduce insertion loss at Tx, the duplex filter should only attenuate noise generated by the *power amplifier* (PA) itself, while noise generated before the PA is filtered inside the Tx-chain. Assuming (i) a class 3 transmitter with a maximum output power of 24 dBm and (ii) a Tx-insertion loss of 2 dB, duplexer isolation of 37 dB is needed. Also, it need to be considered that a Tx-leakage signal may disturb the Rx-band because of receiver nonlinearities. With 50 dB of Tx-Rx isolation, the leakage level from a class 3 transmitter becomes -24 dBm which is realistic in combination with a 3 dB Rx-insertion loss. The assumed duplexer performance data is summarized in Table 1.

Parameter	Requirement
Tx-Ant attenuation (Tx-band) [dB]	< 2
Rx-Ant attenuation (Rx-band) [dB]	< 3
Tx-Rx isolation (Rx-band) [dB]	> 37
Tx-Rx isolation (Tx-band) [dB]	> 50

Table 1: Duplex filter requirements.

3. Receiver

To ensure that the receiver has adequate performance it must meet requirements for a number of tests defined in the UTRA/FDD standard [1]. For each of these tests, a BER of 10^{-3} must be achieved at a user bit rate of 12.2 kbps. To meet this, a $(E_b/N_t)_{eff}$ of 5.2 dB is needed [7]. A margin of 0.8 dB is suggested [7] to cover for baseband implementation imperfections. It is therefore decided to use 6 dB as the target value for $(E_b/N_t)_{eff}$. It is assumed that any disturbing signals, such as distortion products, may be treated as noise. This allows thermal noise and any distortion products to be combined in a single *power spectral density* (PSD), N_t. It is further assumed that any signal that is not on the desired channel is removed by filtering in the digital baseband part. In order not to overload the ADCs, such signals are attenuated to the power level of the desired signal before sampling takes place. Several disturbance mechanisms are active so a disturbance power budget must be chosen. Further, it should be noted that all Rx calculations relate to the Rx chain following the switch/duplexer arrangement, unless otherwise specified. This implies that power levels specified in the standard are adjusted for the loss in the duplexer. As an example, during sensitivity testing, a wanted signal of -117 dBm is specified. This value is adjusted to -120 dBm during calculations to take the estimated duplexer loss of 3 dB into account.

3.1. Noise Figure

The sensitivity requirement is specified for a data channel (DPCH) signal power, S_i. Based on the required $(E_b/N_t)_{eff}$ the acceptable noise and distortion power in a channel bandwidth, P_{acc}, is calculated as

$$\begin{aligned} P_{acc} &= S_i - (E_b/N_t)_{eff} + 10 \cdot \log(PG) \\ &= -120 - 6 + 25 = -101 \text{ dBm}, \end{aligned} \quad (1)$$

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where the processing gain, PG, is given as chip rate over bit rate. The chip and bit rates equals 3.84 Ms/s and 12.2 kbps, respectively. The actual bit rate that should be used is 15 kbps as this is the bit rate prior to the encoding. However, some degree of coding gain is expected and for that matter 12.2 kbps is used. The Tx-leakage signal with varying envelope results in distortion products located at baseband due to even-order nonlinearities in the receiver. As a result, P_{acc} consists of Rx-noise, $P_{Rx,N}$, Tx-noise, $P_{Tx,N}$, and distortion products due to Tx-leakage and Rx-nonlinearities. In the special case where the Tx-signal is turned off, $P_{Rx,N} = P_{acc}$ resulting in a Rx noise figure of 7 dB. To make room for any Tx-signal noise and distortion effects, the Rx noise figure must be reduced. As a compromise, a 1 dB reduction ($P_{Rx,N} = P_{acc}$ - 1 dB) is accepted. Allowing the remaining noise and disturbance power to be shared equally between $P_{Tx,N}$ and $P_{Tx,D}$, they must display disturbance powers less than -111 dBm/3.84 MHz. This disturbance budget leads to the power levels illustrated in Figure 1.

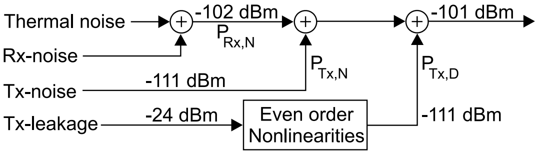

Figure 1: Illustration of the noise and disturbance power distribution.

In other tests, the Tx-power is reduced to 20 dBm for a power class 3 transmitter. This only gives a minor reduction in Tx-noise and is therefore neglected in the following calculations.

3.2. Second-Order Intercept Point

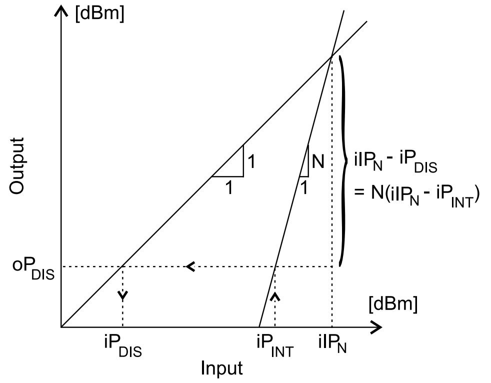

Figure 2: Geometrical interpretation of intercept point.

The presence of strong modulated signals with varying envelope is critical in baseband circuits since some even-order distortion products end up at baseband. To establish requirements to receiver linearity, the illustration on Figure 2 is useful. Figure 2 shows how to find the input-referred nonlinear response for an Nth order system with a given intercept point. Based on the relations given in Figure 2, the required Nth order intercept point is given as

$$iIP_N = \frac{N}{N-1}\cdot iP_{INT} - \frac{1}{N-1}\cdot iP_{DIS} \qquad \text{[dBm]}, \quad (2)$$

where N is the order of the nonlinearity, iP_{INT} the input-referred power of the interferer, and iP_{DIS} the acceptable distortion level referred to the input. To use Eq. (2), the specific test scenario must be considered. During the in-band modulated blocker test, the wanted signal is at -114 dBm, which is 3 dB above the sensitivity limit. This results in a P_{acc} of -98 dBm. Referred to the output of the duplexer, the blocking levels are at -59 dBm, at an offset of ±10 MHz, or at -47 dBm, at an offset of ±15 MHz. The test scenario is shown in Figure 3. A disturbance budget allowing for 50% (-3 dB) receiver noise and Tx-disturbance and for 50% (-3 dB) noise from the second-order product is chosen. Based on Eq. (1) and the disturbance budget, both the maximum allowed noise power and second-order disturbance is -101 dBm. A significant part of the power of the second-order products is at baseband. However, high-pass filtering can be used to reduce this without significant signal degradation [5]. Further, as the spectra of the second-order distortion products are wider than the wanted signal spectrum, low-pass filtering also gives an improvement. In all, the combined reduction of second-order products is estimated to 6 dB. Using this, the second-order intercept point caused by the blocker at ±10 MHz is found from Eq. (2) as

$$iIP_2 = 2\cdot(-59) - (-101+6) = -23 \text{ dBm} \qquad (3)$$

Using the same calculations the intercept point caused by the blocker at ±15 MHz is found to 1 dBm.

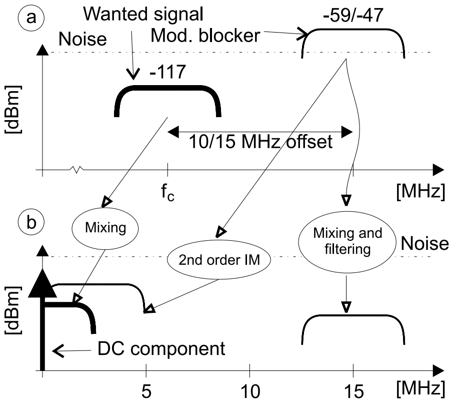

Figure 3: In-band modulated blocker test. (a) RF spectrum with wanted signal an offset modulated blocker. (b) Baseband spectrum with desired and disturbing signals.

During the sensivity test, the Tx-leakage signal acts as a modulated blocker. Second-order distortion is therefore a severe problem. The required second-order intercept point is found to

$$iIP_2 = 2\cdot(26-50) - (-111+6) = 57 \text{ dBm}, \qquad (4)$$

where 50 dB of Tx-Rx isolation is included. While this appears to be a very hard target value, it is by no means unrealistic. One approach could be to make use of a RF filter after the first LNA stage.

3.3. Third-Order Intercept Points

The in-band third-order intercept point is determined from the intermodulation test. The wanted signal is 3 dB above the sensitivity limit, corresponding to -117 dBm while the interfering signal scenario consists of a CW-signal at an offset of ±10 MHz and a modulated signal at an offset of ±20 MHz. Both interfering signals are at a power level of -49 dBm as Figure 4 shows.

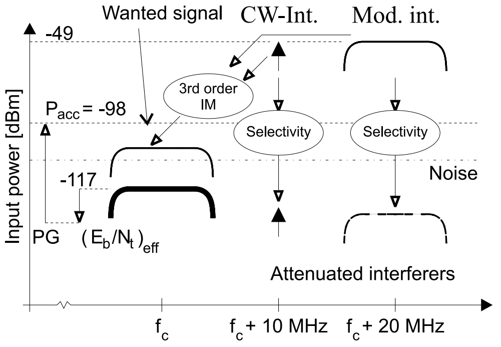

Figure 4: Intermodulation test.

A noise budget is set up as follows: Noise power: 50% (-3 dB), third-order IM-product: 50% (-3 dB). Combined, the disturbances must not exceed -98 dBm. Based on this disturbance budget, it is possible to calculate the required third-order intercept point from Eq. (2)

$$iIP_3 = \frac{3}{2} \cdot (-49) - \frac{1}{2} \cdot (-101) = -23 \text{ dBm} \qquad (5)$$

Because of Tx-leakage, the blocking tests described in [2] also sets demands to iIP_3. The out-of-band blocking test specifies that a CW-blocker is present with a level of -44/-30/-15 dBm at minimum distances from the Rx-band of 15/60/85 MHz, respectively, while the Tx output power is 20 dBm. Blockers at offsets of 85 MHz may generate intermodulation products. In this test the third-order IM-products is allowed generate 50 % of the interfering power. If the frequency of the CW-blocker is *above* that of Tx-leakage signal and the duplex filter offers 27 dB attenuation at offsets of 85 MHz from the Rx-band, the required iIP_3 is found by [2]

$$iIP_3 = \frac{1}{2} \cdot (-28 + 2 \cdot (-42)) - \frac{1}{2} \cdot (-101) = -5.5 \text{ dBm} \quad (6)$$

The requirement to iIP_3 is more harsh if the frequency of the CW-blocker is *below* that of the Tx-leakage signal. It is assumed that Eq. (6) still applies in this case. To obtain an iIP_3 of -5 dBm, 40 dB attenuation of the CW-blocker is required in the duplex filter.

3.4. In-band Selectivity

The selectivity demands are made from the philosophy that disturbing signals should be attenuated to the level of the desired signal in order not to overload the ADCs. A special test is set up for the selectivity for the first adjacent channel located at an offset of ±5 MHz. Here, all signals are well above the noise level and no other disturbance mechanisms are active. The resulting selectivity requirement at ±5 MHz offset is 33 dB [2]. Selectivity here includes any kind of filtering and frequency sensitivity of the demodulator. Several tests use interfering signals at offsets of ±10 MHz. The harshest requirement to selectivity is made by the third-order IM test in which an interferer at -49 dBm is feed to the receiver. The requirement here is 49 dB attenuation. For the remaining Rx-band the blocking test makes a requirement of 51 dB attenuation. 85 MHz below the Rx-band the blocking test makes a requirement of 56 dB attenuation. Finally the sensitivity test makes a requirement of 77 dB attenuation in the Tx-band.

4. Transmitter

Transmitter requirements for the direct up-conversion architecture, illustrated in Figure 5, are derived from the transmitter tests prescribed in the UTRA/FDD standard [1].

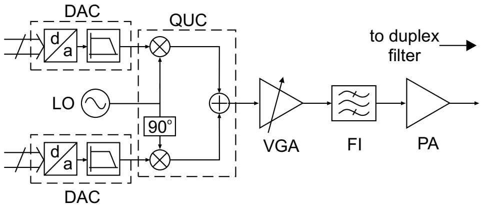

Figure 5: Block diagram of transmitter.

4.1. Input/Output Signals

The input signals are delivered by two DACs, each assumed to deliver an RMS power of -13 dBm. Each DAC is assumed to deliver a signal with the PSD illustrated in Figure 6.

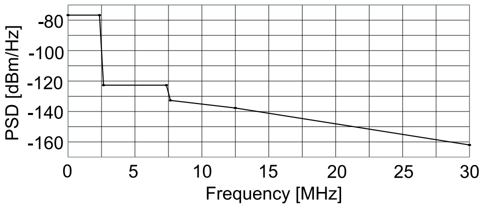

Figure 6: Power spectral density of the DAC.

The assumed PSD is such that no additional filtering of the DAC output is required. In the overall *RMS error vector magnitude* (EVM) budget for the transmitter, the DACs are allowed to contribute with 8 % due to filtering and I/Q imbalance. The output signal specification is based on the noise requirements presented in [1] and on the requirement to noise in the UTRA/FDD Rx-band, taking the duplex filter attenuation into account. The input and output signals for the Tx front-end are specified in Table 2. Three bands have been identified as critical for the spurious emission tests. These bands are band 1 = [1805 MHz – 1880 MHz], band 2 = [1893.5 MHz – 1919.6 MHz], and band 3 = [2110 MHz – 2170 MHz].

4.2. Spurious Requirements

Apart from the input signal spurious power, sources of undesired power are noise generated in the transmitter circuits and phase noise in the LO signal. The output noise is thus a sum of power contributions of each of these factors. In bands 1 to 3, the LO phase noise spectrum is assumed to be flat, meaning that the output signal SNR owing to LO phase noise corresponds directly to the phase noise specified at the LO output. The output phase noise power in the bandwidth *B*, $P_{OPH\,B}$, is found for a

Parameter	**DAC**	**Output**
Power [dBm]	-13	26
EVM [%]	8	17.2
ACLR [dB]		
$f_c \pm$ 5 MHz	-43	-33
$f_c \pm$ 10 MHz	-53	-43
Spurious		
Band 1 [dBm/100 kHz]	-116	-69
Band 2 [dBm/300 kHz]	-79	-39
Band 3 [dBm/3.84 MHz]	-	-74

Table 2: Requirements to DAC and output signals.

output signal of P_{OS} by Eq. (7).

$$P_{OPH\,B} = \mathcal{L}_{LO} + 10 \cdot \log(B) + P_{OS} \qquad \text{[dBm/B]} \qquad (7)$$

Apart from the desired signal, the transmitter also amplifies DAC noise and phase noise introduced by the LO. It is assumed that the gain of the transmitter blocks is constant at frequencies up to ± 30 MHz from the Tx-band. Furthermore, PAs are notorious for making image mixing. Image mixing happens when the second harmonic of desired signal mixes noise that is offset $+f$ from the carrier to an offset of $-f$. Conversion gains in the range of 0 dB have been encountered in state-of-the-art PAs. This means that the power at both the positive and the negative offsets will appear in the same band. For the DACs this means that the sidebands indicated in Figure 6 are amplified with two times the in-band transmitter gain. In the most critical scenarios, noise at 12.5 MHz appears in band 2, while noise at 30 MHz appears in band 1. Assuming the noise performance of the DACs is given, the margin to the output noise power specified in Table 2 is used to specify white noise and LO phase noise. Circuit noise power requirements for bands 1 to 3 are listed in Table 3.

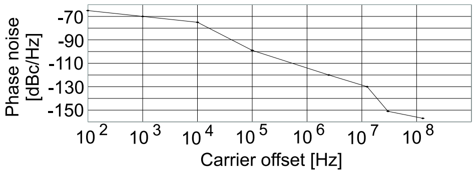

Figure 7: Tx LO phase noise requirement.

Figure 7 describes the phase noise of the LO used in the transmitter. For bands 1 and 2 phase noise power is specified at offsets of ± 30 MHz and ± 12.5 MHz. For band 3, the shortest distance from the carrier is 130 MHz. The LO phase noise is thus specified at an offset of ± 30 MHz.

4.3. Adjacent Channel Leakage Ratio (ACLR)

The ACLR test specified in [1] sets requirements to intermodulation products, phase noise, and noise in the DACs. With T_{OIMD} being the equivalent temperature of the intermodulation noise at the output, the equivalent noise temperature for adjacent channels is found from

$$T_{OT} = T_{OIMD} + T_{OPH} + T_{ODAC} \qquad \text{[k]} \qquad (8)$$

From state-of-the-art devices it is found that especially third-order intermodulation is critical. Assuming that ACLR is due to third-order intermodulation only, an oIP_3 of 37.6 dBm is needed to obtain the ACLR required at ± 5 MHz [8]. Assume instead that DACs and LO are used that features the performance shown in Figure 6 and 7 respectively at frequencies and frequency offsets of ± 2.5 MHz. Then using Eq. (8) and [8] an oIP_3 of 37.7 dBm is found to provide the required ACLR. DACs and LOs with the indicated performance can thus be used at the cost of only 0.1 dB increase of the required oIP_3. ACLR has been observed to depend on the *output single tone 1 dB compression point* (CP_O) instead of the corresponding oIP_3, when PAs are operated near their CP_O. The transmitter simulated in [8] features a CP_O that is 10.6 dB below the corresponding oIP_3 [3]. The required CP_O is therefore 27.1 dBm.

4.4. Error Vector Magnitude

EVM of the output signal of the transmitter is a result of many factors that cause signal degradation. The total EVM (EVM_T) caused by N uncorrelated factors is found by

$$\text{EVM}_T = \sqrt{\sum_{n=1}^{N} \text{EVM}_n^2} \qquad [\,\%] \qquad (9)$$

Which factors that contribute to EVM depend on the transmitter architecture. For a direct up-conversion transmitter, significant contributing factors are: DACs, in-band ripple, I and Q imbalance, phase noise, third-order intermodulation and LO leakage. The contributions from the DAC and the third-order intermodulation are already given. When amplifiers that meets the ALCR requirement are used, EVM in the range of 3 % have been observed. In the following the remaining contributors are specified so that a total of 17.2 % EVM is obtained at the output signal. In-band ripple is specified for the desired channel only. It includes in-band magnitude ripple compared to the RMS magnitude, and RMS phase ripple compared to the linearized in-band phase that causes minimum RMS error. Amplitude ripple of 0.4 dB results in an EVM of 4.7 % [6], while phase ripple of 4 deg. results in an EVM 7 % [6]. EVM is measured in time slots with a duration of 667 μs [1]. LO phase noise at offsets of less than one tenth of the frequency of the time slots is not detected by the receiver as phase error. The lower limit for the specification of LO phase noise is therefore 150 Hz. Figure 7 defines the phase noise of the LO used for the transmitter. The average in-band phase noise of this LO is 4 deg. The EVM caused be an RMS phase noise of 4 deg. is approximately 7 % [4]. An I/Q amplitude imbalance of 1.4 dB generates an EVM of 8.0 % [4], while a phase offset between the I and the Q signal of 5 deg. generates and EVM of 4.4 % [4]. A general expression that depends on LO leakage is *LO to signal ratio* (LSR). LSR is defined as the ratio between the average power of the LO signal, measured at the output of the *quadrature up converter* (QUC), and the average power of the desired signal, measured at the same place. LSR can be transferred directly to the output of the transmitter, which makes it suitable for specification of LSR induced EVM, EVM_{LO}, found by

$$\text{EVM}_{LO} = \sqrt{\text{LSR}} \cdot 100 \qquad [\,\%] \qquad (10)$$

Eq. (10) defines LSR as a ratio. For specification purposes the required LSR is presented in dB. An LSR of -27 dB is found to generate an EVM of 4.5 %. When a gain budget exists for the transmitter, a specification of LO-leakage can be made. The UTRA/FDD standard does not allow adjustments of DC offsets during EVM measurements. If this is allowed, LSR will have no effect on EVM.

5. Block Requirements for a Direct Up/Down Conversion Transceiver

The Rx and Tx requirements are summarized in Table 3.

Rx parameter	**Requirement**
Noise figure [dB]	≤ 6
In-Band selectivity [dB]	
1st adj. (5 MHz)	≥ 33
2nd adj. (10 MHz)	≥ 49
Remaining Rx-band	≥ 51
2025 – 1980 MHz	≥ 56
Tx-band	≥ 77
Intercept points [dBm]	
iIP_2 (10 MHz)	≥ -23
iIP_2 (15 MHz)	≥ 1
iIP_2 (Tx)	≥ 57
iIP_3 (10/20 MHz)	≥ -23
iIP_3 (Tx)	≥ -5.5
iIP_3 (1730 – 1830 MHz)	≥ -5
Tx parameter	**Requirement**
Circuit noise [dBm/Hz]	
Band 1	≤ -124
Band 2	≤ -107
Band 3	≤ -140
1 dB compression points [dBm]	
CP_O	≥ 27.1
IQ imbalance	
Amplitude [dB]	≤ 1.4
Phase [deg]	≤ 5
In-band ripple	
Amplitude [dB]	≤ 0.4
Phase [deg]	≤ 4
LSR [dB]	-27

Table 3: Summary of transceiver requirements.

5.1. Receiver Block Requirements

In the recent years, direct-conversion receivers have emerged for GSM applications and many consider this architecture the proper choice for 3G systems. A particular nice feature is the fact that the large bandwidth makes W-CDMA systems less sensitive towards $1/f$ noise and DC offset problems inherent to homodyne receivers. An example of an UTRA/FDD direct-conversion receiver is shown in Figure 8.

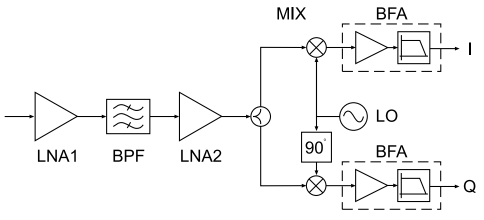

Figure 8: Direct-conversion receiver.

An interstage *bandpass filter* (BPF) is used to provide attenuation of the Tx-leakage signal. To meet the requirements, the BPF must attenuate the Tx-band and the band stretching from 1730 MHz to 1830 MHz at least 30 dB. Considering linearity, iIP_2 and iIP_3 is assumed to be of constant value for carrier offsets up to ±380 MHz. iIP_2 is only critical for the *mixer* (MIX) and *subsequent base band blocks* (BFA). In spite of the extra filtering, the harshest demand to iIP_2 is made by the Tx-leakage signal. It is therefore not sufficient to specify iIP_2 for MIX and BFA from the requirements to iIP_2 in the Rx-band. MIX and BFA are specified so they generate an equal amount of noise power due to iIP_2. Tx-leakage also sets the harshest demand to iIP_3. However, in this case BPF lowers demands to the subsequent blocks, making only *Low noise amplifier number 1* (LNA1) critical to the Tx-leakage signal. The block requirements are listed in Table 4.

Block	**LNA1**	**BPF**	**LNA2**	**MIX**	**BFA**
Gain [dB]	15	-3	9	10	–
NF [dB]	4	3	4	16	31
iIP_2 [dBm]	–	–	–	27	37
iIP_3 [dBm]	-4	–	-6	0	10

Table 4: Receiver block requirements.

Some tolerances must be specified for all block gains to accommodate different variations. These tolerances require an additional margin to be put on the performance parameters listed in Table 4. Based on these block requirements, it is clear that meeting the test specifications listed in the UTRA/FDD standard is by no means unrealistic. Being able to operate LNA1 at a noise figure of 4 dB makes the design of this block less critical. In terms of linearity, the continuous presence of the Tx-signal sets the most stringent requirements to the receiver. This problem becomes less severe when an interstage bandpass filter is used.

5.2. Transmitter Block Requirements

The effect of LO phase noise on spurious and EVM depends on how gain and noise figure budgets are set up for the transmitter presented in Figure 5. The gain budget represents a compromise between noise figure and CP_O. Noise contributions in bands 1 to 3 are calculated using cascaded noise figures. When calculating the resulting output noise, image mixing in the PA, described in Subsection 4.2, has to be taken into account. A one to one conversion of the noise at the image band has been observed on a state-of-the-art PA running at the desired power level. It is therefore assumed that image mixing in the PA can be taken into account by doubling the effective noise-band-width. Table 5 lists the in-band gain, noise figure and CP_O performance required from each individual block.

Block	**QUC**	**VGA**	**FI**	**PA**
Gain [dB]	0	13	-2	25
NF [dB]	10	4	2	5
CP_O [dBm]	3.9	15.4	30	27.7

Table 5: Transmitter block requirements.

Figure 9 presents budgets for signal power, cascaded CP_O and noise in the critical bands. The large signal gain of the PA at band 1 and band 2 are expected to be the same as the in-band gain i.e. 25 dB. At band 3, a gain of 23 dB and a NF of 7 dB is assumed.

As was the case for the receiver, the Tx blocks has to be designed with some margin on NF and CP_O to take into account

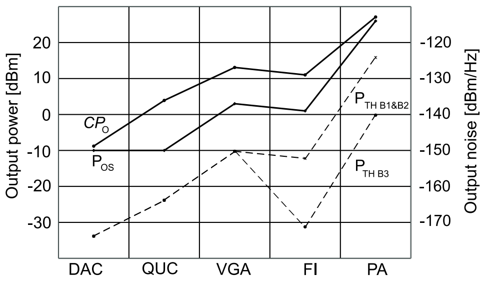

Figure 9: Budgets for signal power [dBm], cascaded noise power at band 1 and 2 $P_{THB1\&B2}$ and band 3 P_{THB3} [dBm/Hz], and CP_O [dBm].

gain variations. It is found that 21 dB attenuation is needed in band 3. When the transmitter is operated at its highest channel, the UTRA/FDD Rx-band is offset 130 MHz from the carrier. However, the image is only offset 70 MHz from the lower edge of the Tx-band. Therefore the *filter* FI must provide 21 dB of attenuation ± 70 MHz from the Tx-band. The need for FI arose from the philosophy that the duplex filter should only attenuate as much power as was generated in the PA. If the duplex filter was to attenuate all the noise power generated by the transmitter in the Rx-band, the duplex filter would be required to attenuate the Rx-band by 49 dB. Assuming that the LO drives each mixer in the QUC with -6 dBm, a requirement for LO-leakage in QUC can now be made from the gain budget illustrated in Figure 9. Here the output signal power of QUC is -7 dBm and in Table 3 LSR is specified to -27 dB. The requirement to LO-leakage is thus -28 dB. A decrease in signal output power of the QUC or an increase in LO drive power, results in more harsh requirements to LO-leakage. Generally, the requirements relating to EVM does not seem critical for state-of-the-art devices. However, the requirement to output noise in band 1 sets harsh demands to the QUC. FI can not do any significant attenuation here, since the image may be in the Tx-band. The only way to allow for a significant increase in the QUC noise figure, is by attenuating band 1 in the duplex filter. If for example 8 dB attenuation was available here, the noise figure of the QUC could be as high as 20 dB. Obtaining such noise figures should not be a problem.

6. Conclusion

In this paper, UE transceiver requirements have been derived from the UTRA/FDD standard. Requirements found in recent specifications have been mapped into block requirements suitable for design. Based on the derived Rx requirements only, plausible block requirements result from using the direct-conversion architecture. It is important to notice that having the Tx-signal running at all times results in the harshest requirement to the Rx linearity. Tx specifications have been translated to overall requirements for a direct up-conversion transmitter. These have been translated to block requirements. It was found that because Rx and Tx is running at the same time, a bandpass filter is required in front of the PA if the specified duplex filter is used. It should be noted that requirements presented in this document are based directly on specifications. In practice, some margin need be included to take into account fabrication tolerances and other uncertainties. Also, it is worth noting that UTRA/FDD to a wide extent is an interference limited system where any additional performance surplus on the UE receiver side will lead to increased system capacity. Hence, network providers will prefer “good” UEs to increase their profit and thus UE manufacturers may wish to exceed specifications significantly in order to gain market shares.

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Accurate Computer-Assisted Planning of Integrated Radio Receivers

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Accurate Computer-Assisted Planning of Integrated Radio Receivers*

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Abstract

In this paper, we propose a general methodology for accurate, yet manageable, planning of integrated low-cost receivers. The approach considers interstage selectivity and baseband performance and is applicable to systems containing on-chip/off-chip block interfaces including non-50Ω transitions. A UTRA/FDD receiver design is used to illustrate the capability of the methodology.

1 INTRODUCTION

As silicon processes are applied to high-performance RF integrated circuit design, technology impairments become increasingly important. Traditionally, the use of high performance discrete and integrated solutions has allowed designers to consider non-ideal effects separately while obtaining full receiver compliance with specifications. However, for low-cost integrated low-IF/zero-IF receivers where baseband circuits seriously degrade overall performance, technology limitations call for a non-trivial tradeoff among gain-distribution, noise, nonlinearities, and selectivity. Hence, receiver planning must consider interstage selectivity and baseband performance in order to reach a balanced tradeoff between power consumption, form factor, and cost. In this paper, a computer-assisted methodology for simple, yet accurate, receiver planning is proposed. A CMOS-based UTRA/FDD RF/baseband receiver is used as a case study to exemplify the approach. The focus is on selectivity in conjunction with gain, noise, and linearity since other block requirements can be derived directly from the specifications.

2 OVERALL METHODOLOGY

A common approach to simplify receiver planning is to employ a full or partial separation of different distortion mechanisms. For instance, noise performance is usually assessed assuming that interferers, blockers, and intermodulation distortion are negligible. In cases where a clear separation of effects is not applicable, each effect is commonly allowed a certain degradation threshold. However, low-cost silicon technologies applied for today's RF and baseband circuitry, offer only limited design surplus which means that over-specification of the receiver becomes very critical. By considering all interferring components simultaneously, the designer can utilize advantages and minimize the effect of impairments of the applied technology. This philosophy forms the basis of our methodology illustrated in Fig. 1. To simultaneously consider various effects and include issues of relevance to modern receiver architectures, it is necessary to employ more accurate analytical tools. Suitable theory has recently been presented in the literature [1], and is briefly reviewed in Section 3.

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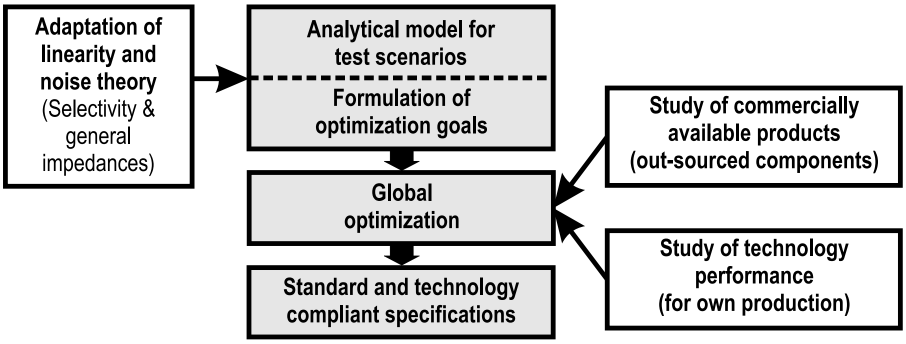

Adaptation of linearity and noise theory (Selectivity & general impedances)
Analytical model for test scenarios
Formulation of optimization goals
Global optimization
Standard and technology compliant specifications
Study of commercially available products (out-sourced components)
Study of technology performance (for own production)

FIGURE 1: *Work-flow of computer-assisted receiver planning.*

Accordingly, a computer model is built for each of the test-scenarios to which compliance must be guaranteed. Once, the test-scenarios have been mapped into measurable goals, specific optimization values can be defined. Such values are not always directly available from specifications since they are often defined after demodulation and channel de-coding. Hence, link simulations and a baseband implementation margin need be considered. Next, performance measures for each of the blocks contained in the receiver architecture are then adjusted using a numeric optimization procedure. To reach a realistic outcome, it is important that optimization ranges are set to take into account the capabilities of the employed technology for each building block. This process often involves a scanning of literature and data sheets as well as good old-fashioned design experience. As a final result, the optimization leads to technology-compliant as well as standard-compliant block performance requirements.

3 THEORY OF RECEIVER PLANNING

To consider different distortion mechanisms simultaneously, absolute signal levels of desired response, noise, intermodulation products, and interferers/blockers are preferable over standard cascade measures (e.g. noise figure). For wireless radio design, the optimization procedure can be based on an effective *signal-interference ratio* (SIR) defined at the input of the demodulator just before the *analog-digital converter* (ADC). The SIR is calculated as

$$\mathrm{SIR} \simeq \frac{|A_{usr}|^2}{n_{out}^2 \Delta f + \sum_r |A_r|^2}, \tag{1}$$

where A_{usr} is the RMS amplitude of the desired signal before the demodulator, n_{out} is the effective noise amplitude, Δf is the baseband signal bandwidth, and the summation term denotes the contribution of all other distortion mechanisms, including *multiple access interference* (MAI), intermodulation distortion, adjacent channels, etc. All amplitude powers are added in-phase assuming no correlation regardless of the frequency location within the Δf band. Note that since baseband circuitry of low-IF/zero-IF architectures contribute heavily to the overall receiver performance, an extended version of traditional microwave theory that incorporates general selectivity is needed [1]. This theory is based on voltage domain calculations. The loaded voltage gain for block k is denoted by $G_k(f)$, where f is the frequency. The gain functions denote the full frequency dependence and, hence, selectivity is considered. To be able to consider frequency translating devices, each block k is denoted by its input-referred passband frequency f_k. Hence, for a baseband circuit k (input to output), $f_k = 0$Hz. This way, interferers and other intermodulation products may be treated by their absolute offset to the passband frequency which enables a simplified notation and computer-assisted analysis. Given these assumptions, the total noise output from a cascade of K stages is

$$n_{out} = \sqrt{\sum_{k=1}^{K} n_k^2 \left(\frac{r_{i,k}}{r_{i,k}+r_{o,k-1}} \right)^2 \cdot \prod_{r=k}^{K} \alpha_r G_r^2(f_r)}, \qquad (2)$$

where n_r is the equivalent mean square noise voltage density (referred to zero source impedance) for block r, $r_{i,k}$ and $r_{o,k}$ are the input and output resistance for block k respectively, and α_r is a factor denoting the type of frequency translation in block r [1].

The 2nd order distortion that originates from an interferer placed at a frequency δf away from the passband frequency may be calculated as [1]

$$A_{o,2} = A_i^2 \left(\prod_{k=1}^{K} G_k(f_k) \right) \sum_{k=1}^{K} \frac{1}{\mathrm{iIP2}_k} \left(\prod_{r=1}^{k-1} \frac{G_r^2(f_r+\delta f)}{G_r(f_r)} \right) \left(\prod_{r=k+1}^{K} \frac{G_r(f_{im})}{G_r(f_r)} \right), \qquad (3)$$

where $\mathrm{iIP2}_k$ is the measured 2nd order input intercept point for block k, and f_{im} represents the absolute output frequency at which the distortion arrives (usually a low-frequency contribution). A similar expression exists for the intermodulation distortion created at the output by two interferers located at δf and $2\delta f$ (with amplitudes A_1 and A_2 respectively) [1]

$$A_{o,3} = A_1^2 A_2 \left(\prod_{k=1}^{K} \right) \sum_{k=1}^{K} \frac{1}{\mathrm{iIP3}_k^2} \prod_{r=1}^{k-1} \frac{G_r^2(f_r+\delta f) G_r(f_r+2\delta f)}{G_r(f_r)}, \qquad (4)$$

where $\mathrm{iIP3}_k$ is the 3rd order input intercept point for block k. The loop-form of these equations is directly compatible with most programming languages, e.g. MATLAB$^{\mathrm{TM}}$.

4 CASE STUDY: UTRA/FDD RECEIVER PLANNING

With a theory for simple, yet accurate, system evaluations established, optimization goals and test conditions must be determined. Once these are known, an optimization is conducted to ensure an overall performance that meets requirements. In this case study the target is a zero-IF UTRA/FDD receiver based primarily on CMOS technology. The important disturbance effects must be considered and the system model defined.

4-1 Receiver Structure

Based on initial studies the receiver structure and the interface definitions illustrated in Fig. 2 are chosen. The first stage is a *duplexer* (DPX) including a multi-mode selection switch. Despite the intention of a fully integrated CMOS receiver, initial evaluations show that with the available CMOS RF filter performance, an off-chip *bandpass filter* (BPF) following the LNA is needed. Following the BPF there is a quadrature down-converter (CNV) with an active phase splitter as input, and two parallel *baseband filter and amplifier* (BFA) paths. The BFA includes a servo-type feedback loop to compensate for DC-offset generated in both the CNV and the BFA. Further, the core part of the receiver interacts with the duplex filter on the RF side and with dual ADC's on the low-frequency output side.

4-2 System Model

The model must encompass all simultaneous active effects that contribute to the overall performance degradation. An important issue for UTRA receiver specification is the continuous

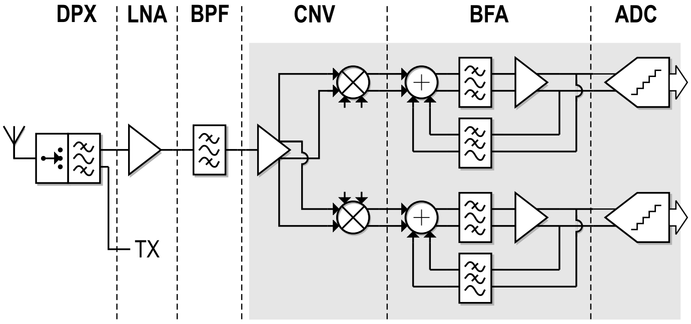


FIGURE 2: *System diagram of the UTRA/FDD receiver. Shaded blocks are intended for CMOS implementation.*

presence of the transmitter signal. As it leaks to the receiver part it generates IMD together with blockers, direct 2nd order distortion, and direct distortion. The required isolation between TX and RX can only be provided by means of a duplex filter. Based on duplex filters available in stock, a TX-to-RX isolation of 50dB in combination with an insertion loss of 3dB is realistic.

Another interference component of particular concern for the zero-IF receiver is the low-frequency 2nd order product. This component is generated by adjacent channels and intermodulation disturbances. Fortunately, it has been shown that DC-offset filtering up to 1kHz – 20kHz can also suppress 2nd order distortion by approximately 6dB with a resulting SIR degradation of around 0.2dB – 0.5dB [2, 3].

As in most modern transceivers a performance trade-off is found in the ADC interface. By exchanging resolution and sample-rate for increased power consumption, analog filtering requirements may be relaxed. Previously published results indicate that 4 – 5 bits used in the ADC is sufficient to prevent quantization noise to be significant [4]. Consideration state-of-the-art ADC performance an additional 3 bits appear realistic which enables 18dB of digital filtering for both the 1st and 2nd adjacent channels.

4-3 Test Scenarios

Common to all the test scenarios presented in [5] is that the receiver is required to operate at a BER of less than 10^{-3}. In order to simplify the optimization by discluding baseband processing, it is desirable to map this BER value to a corresponding SIR at the input of the ADC. It has been determined from system simulations that the BER requirement is met for a SIR of 6dB – 6.2dB after processing gain while including some implementation margin [4]. Including a 0.5dB degradation expected from the DC-offset filtering the resulting requirement is 6.7dB. Hence, the overall design target to the demodulator is chosen to

$$\mathrm{SIR} = \left(\frac{E_b}{N_t}\right) \simeq \frac{\mathrm{PG}\cdot|A_{usr}|^2}{n_{out}^2\Delta f + |A_{blck}|^2 + |A_{adjc}|^2 + |A_{2,\mathrm{BFA}}|^2 + |A_{3,\mathrm{BFA}}|^2 + |A_{\mathrm{mai}}|^2} \geq 7\mathrm{dB}, \qquad (5)$$

where PG is the processing gain (25dB), A_{blck} is the RMS amplitude of all blockers/interferers (including spurious TX), A_{adjc} is the RMS amplitude of adjacent channels, $A_{2,\mathrm{BFA}}$ and $A_{3,\mathrm{BFA}}$ are the RMS amplitudes of all 2nd and 3rd order products, and A_{mai} is the MAI from all other code channels.

The different test scenarios described in the standardization document may be boiled down to the three major distortion groupings illustrated in Table 1. This table indicates which interference and distortion mechanisms are present during the tests. In Table 1 the IMD1 test refers to the two-tone intermodulation test specified in [5] while IMD2 refers to blocking tests where a blocker and the TX-signal interact to form intermodulation products.

TABLE 1: *Indication of effects included in the various simulation tests. Here, a '+' indicates that the effect is active while a '-' indicates that it has been omitted.*

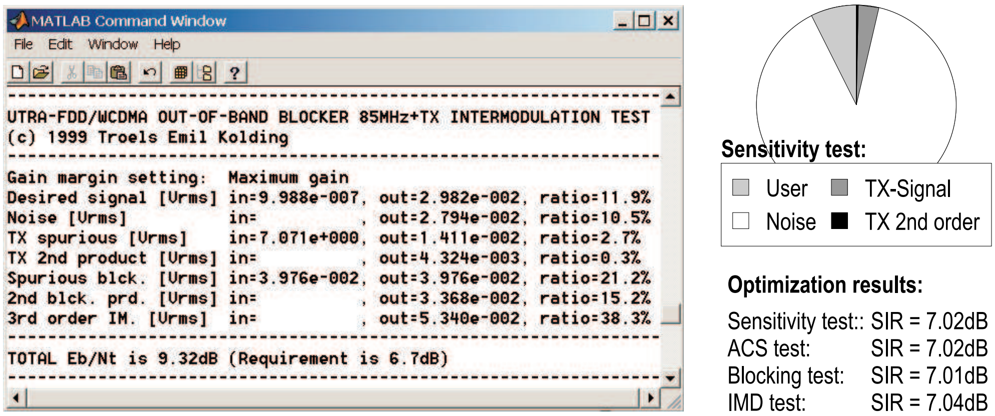
Test	**Desired**	**Direct Distortion**					**2nd Order**			**3rd Order**	
	User	Noise	MAI	Blk1	Blk2	Tx	Blk1	Blk2	Tx	Blk1/Blk2	Blk1/Tx
Sensitivity	+	+	+	–	–	+	–	–	+	–	–
ACS	+	+	+	+	–	+	+	–	+	–	–
Blocking	+	+	+	+	–	+	+	–	+	–	–
IMD1	+	+	+	+	+	+	+	+	+	+	–
IMD2	+	+	+	+	–	+	+	–	+	–	+

4-4 Optimization and Parameter Tuning

During the optimization a number of parameters are swept to search the performance space for a optimum combination of receiver block performance. Block parameters open for optimization include gain, selectivity, and linearity. All combinations of gain and gain margin are used as noise and linearity are weighted randomly which prevents the identification of a worst-case setup. Realistic ranges for available block performances are determined using public literature and own design experience.

4-5 Output Results

The entire scheme is implemented in MATLAB^{TM}. The simulator is split into separate parts with one routine defining the receiver performance range, a test routine for each of the test scenarios defined in the standardization document, a main routine, and finally a routine for presenting the results. The output of the simulator is displayed in Fig. 3 together with the overall SIR resulting from the different tests. Included in Fig. 3 is also a diagram to illustrate the distribution of interferring powers. It is not possible to make all tests exactly match the 7dB requirement but a close-to optimum specification arrangement is produced using the method as Fig. 3 illustrate. The resulting block specifications are listed in Table 2.



```
--------------------------------------------------------------
UTRA-FDD/WCDMA OUT-OF-BAND BLOCKER 85MHz+TX INTERMODULATION TEST
(c) 1999 Troels Emil Kolding
--------------------------------------------------------------
Gain margin setting:  Maximum gain
Desired signal [Vrms] in=9.988e-007, out=2.982e-002, ratio=11.9%
Noise [Vrms]          in=          , out=2.794e-002, ratio=10.5%
TX spurious [Vrms]    in=7.071e+000, out=1.411e-002, ratio=2.7%
TX 2nd product [Vrms] in=          , out=4.324e-003, ratio=0.3%
Spurious blck. [Vrms] in=3.976e-002, out=3.976e-002, ratio=21.2%
2nd blck. prd. [Vrms] in=          , out=3.368e-002, ratio=15.2%
3rd order IM. [Vrms]  in=          , out=5.340e-002, ratio=38.3%
--------------------------------------------------------------
TOTAL Eb/Nt is 9.32dB (Requirement is 6.7dB)
--------------------------------------------------------------
```

Optimization results:

Sensitivity test::	SIR = 7.02dB
ACS test:	SIR = 7.02dB
Blocking test:	SIR = 7.01dB
IMD test:	SIR = 7.04dB

FIGURE 3: *Optimization output, example of power distribution, and optimization results.*

TABLE 2: *Optimized block specifications.*

Specification	**DPX**	**LNA**	**BPF**	**CNV**	**BFA**
Voltage gain, max. AGC [dB]	-3	11	-1.5	16	60
Gain margin [dB]	±0	±1.5	±0.5	±2	±2
Input noise [nV/$\sqrt{\text{Hz}}$]	0.37	0.31	0.34	≤2.0	≤11.2
Input impedance [Ω]	50	50	50	50	≥2k
Output impedance [Ω]	50	50	50	≤300	≤300
Rel. att. at baseband (<5MHz) [dB]	10	40	40	40	0
Rel. att. of 1st adj. ch. (5MHz) [dB]	0	0	0	0	≥15.2
Rel. att. of 2nd adj. ch. (10MHz) [dB]	0	0	0	0	≥35.8
Rel. att. of 3rd adj. ch. (15MHz) [dB]	0	0	0	0	≥57
Rel. att. of 4th adj. ch. (20MHz) [dB]	0	0	0	0	≥57.5
Rel. att. at 15MHz offset [dB]	1.5	0	1	≥0	≥57
Rel. att. at 60MHz offset [dB]	10	0	5	≥0	≥57
Rel. att. at 67MHz offset [dB]	18	0	10	≥0	≥57
Rel. att. at 85MHz offset [dB]	22	0	7	≥0	≥60.5
Rel. att. at 135MHz offset (TX) [dB]	55	0	30	≥0	≥60.5
iIP2 at 15MHz offset [dBV$_{\text{rms}}$]	∞	∞	∞	≥6.7	≥45.1
iIP2 at TX spurious [dBV$_{\text{rms}}$]	∞	∞	∞	≥6.7	≥45.1
iIP3 at 10MHz/20MHz offset [dBV$_{\text{rms}}$]	∞	-4.0	∞	≥-17.7	≥1.2
iIP3 at 67MHz/135MHz offset [dBV$_{\text{rms}}$]	∞	-4.0	∞	≥-17.7	≥1.2

5 CONCLUSIONS

A simple, yet accurate, approach to receiver planning is presented. As the method considers all interferring components simultaneously, the designer can utilize advantages and minimize the effect of impairments of the applied technology. This philosophy forms the basis of the methodology which has been illustrated using a UTRA/FDD test case. Compared to the results presented in [3] the proposed method produce block specifications allowing for slightly increased input noise levels and relaxed baseband filtering.

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UTRA/FDD RF Tranceiver Requirements

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UTRA/FDD RF Transceiver Requirements

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Abstract. Unified RF requirements are derived for an UMTS Terrestrial Radio Access/Frequency Division Duplex (UTRA/FDD) compliant mobile transceiver. A set of transceiver requirements are proposed with consideration to system issues including duplex aspects. From these design-compatible requirements are proposed for each functional block in the transceiver.

Keywords: RF transceiver, UTRA/FDD, transceiver requirements, direct up/down conversion, receiver, transmitter.

1. Introduction

The UTRA/FDD mobile standard provides an improved platform for personal communications including voice, data, and multimedia services compared to current 2G systems. For UTRA/FDD to retain a competitive advantage, high-performance, low-cost *user equipment* (UE) must be made available to the general public. This paper proposes a set of specifications for functional blocks used in direct up/down conversion transceivers, corresponding to the UTRA/FDD interface specifications [1]. This paper is an update of previous work for the receiver branch [2] and ongoing work for the transmitter branch [3].

2. Duplex Aspects

As UTRA/FDD is based on *frequency division duplex* (FDD), the required isolation between *transmitter* (Tx) and *receiver* (Rx) is only practically obtainable using a duplex filter. The transmitter-induced noise level at the receiver input is determined by the transmitter noise level and the duplexer isolation. A level of –111 dBm measured in a single UMTS channel bandwidth (3.84 MHz) is shown in later sections to give an acceptable degradation of receiver sensitivity. To reduce the insertion loss at Tx, the duplex filter should only attenuate noise generated by the *power amplifier* (PA) itself, while noise generated before the PA should be filtered inside the Tx-chain. Measurements on a state-of-the-art PA indicate that –74 dBm of noise can be expected on an Rx channel. Also, it needs to be considered that a Tx-leakage signal may cause disturbance in the Rx-band because of receiver non-linearities. The proposed duplexer performance requirements are summarized in Table 1.

Table 1. Duplex filter requirements [4].

Parameter	Requirement [dB]
Tx-Ant attenuation (Tx-band)	<2
Rx-Ant attenuation (Rx-band)	<3
Tx-Rx isolation (Rx-band)	>37
Tx-Rx isolation (Tx-band)	>50

3. Receiver

To ensure that the receiver has adequate performance it must meet requirements for a number of tests defined in the UTRA/FDD standard [1]. For each of these tests, a BER of 10^{-3} must be achieved at a user bit rate of 12.2 kbps and a chip rate of 3.84 Mc/s. To meet this, an $(E_b/N_t)_{eff}$ of 6 dB is needed, including a 0.8 dB implementation margin [7]. The down-link signal is protected by a unique scrambling code, which gives it noise-like qualities. The same is true for the modulated test signals and the up-link signal. Any disturbing signals, including distortion products, are therefore treated as white noise. It should be noted that all Rx calculations relate to the Rx chain following the duplex filter, unless otherwise specified.

3.1. NOISE FIGURE (NF)

The sensitivity requirement is specified for a dedicated physical channel (DPCH) signal power, S_i. Based on the given required $(E_b/N_t)_{eff}$, the acceptable noise and distortion power in a channel bandwidth, P_{acc}, is calculated as

$$\begin{aligned} P_{acc} &= S_i - (E_b/N_t)_{eff} + 10 \cdot \log(PG) \\ &= -120 - 6 + 25 = -101 \text{ [dBm]}, \end{aligned} \tag{1}$$

where PG is the processing gain (the ratio of chip rate to bit rate) and P_{acc} consists of Rx-noise ($P_{Rx,N}$), Tx-noise in the Rx band ($P_{Tx,N}$) and distortion products due to Tx-leakage combined with Rx non-linearities ($P_{Tx,D}$). If the Tx-signal is turned off, $P_{acc} = P_{Rx,N}$ resulting in an Rx noise figure of 7 dB. To make room for any Tx-signal noise and distortion effects, the Rx noise figure must be reduced accordingly. If a 1 dB reduction in $P_{Rx,N}$ is accepted and the remaining noise and disturbance power is distributed equally between $P_{Tx,N}$ and $P_{Tx,D}$, the acceptable level of each is –111 dBm/3.84 MHz or less. This disturbance budget is illustrated in Figure 1. The maximum noise figure is then reduced to 6 dB. The Tx-leakage power level in Figure 1 is the power level of the Tx-signal at the Rx-output of the duplexer, i.e. the 26 dBm Tx output power attenuated by 50 dB.

3.2. INTERMODULATION

In [4], the power budgets for the different test scenarios from the UTRA/FDD specification are described. The different test scenarios are listed in Table 2 along with the resulting n-th order, two tone intercept point, iIP_n. Note that in many of the test cases, several disturbance mechanisms are active at the same time, reducing the acceptable disturbance power level for intermodulation. In Table 2, f_c represents the carrier frequency. Although the Tx leakage signal results in a very high overall iIP_2, the frequency offset of the Tx means that requirements to

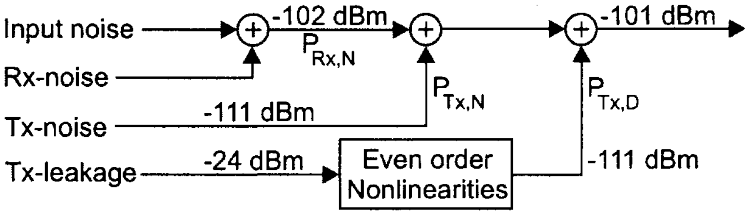

Figure 1. Illustration of the noise and disturbance power distribution.

Table 2. Required iIP_n based on different test scenarios.

Test	iIP_2 [dBm]	iIP_3 [dBm]
In-band modulated blocker test		
$f_c \pm 10$ MHz	≥ -23	–
$f_c \pm 15$ MHz	$\geq +1$	–
Tx leakage	$\geq +57$	–
Intermodulation test	–	≥ -23
Out-of-band blocker		
1670–2025 MHz	–	≥ -5

the blocks where iIP_2 is critical may be relaxed using RF interstage filtering. The Tx leakage signal, together with the out-of-band blocker also sets a harsh requirement to iIP_3 (–5 dBm). The requirement to iIP_3 is based on the assumption that blocking signals are attenuated by at least 40 dB in the duplex filter [4]. In a transceiver that supports variable transmit to receive frequency separation, this iIP_3 must be maintained from 1670 MHz to 2025 MHz.

3.3. IN-BAND SELECTIVITY

The selectivity requirements are defined so all unwanted signals and the desired signal appear with equal power at the ADC. The resulting requirements are derived in [4], based on the tests defined for intermodulation, in-band and out-of-band blocking, and Tx-leakage. These requirements are summarized in Table 4.

4. Transmitter

Transmitter requirements for the direct up-conversion architecture are derived from the transmitter tests described in [1]. The requirements apply to the Tx chain, not including the duplex filter.

4.1. INPUT/OUTPUT SIGNALS

The modulated signal is delivered to the transmitter as I and Q signals, that meet the signal quality requirements in Table 3. The output signal specification is based on [1] and on the requirement to noise in the UTRA/FDD Rx-band. These specifications, including the effect of duplex filter attenuation, are also listed in Table 3. The average power of the LO is assumed to be –6 dBm, and the limits for LO phase noise are proposed in Figure 2.

Table 3. Requirements to I/Q and output signals.

Parameter	I/Q signals	Output
Power [dBm]	–13	26
EVM [%]	≤ 8	≤ 17.2
ACLR [dB]		
$f_c \pm 5$ MHz	≥ 43	≥ 33
$f_c \pm 10$ MHz	≥ 53	≥ 43
Spurious		
Band 1 (1805 MHz–1880 MHz) [dBm/100 kHz]	≤ –116	≤ –69
Band 2 (1893.5 MHz–1919.6 MHz) [dBm/300 kHz]	≤ –79	≤ –39
Band 3 (2110 MHz–2170 MHz) [dBm/3.84 MHz]	–	≤ –74

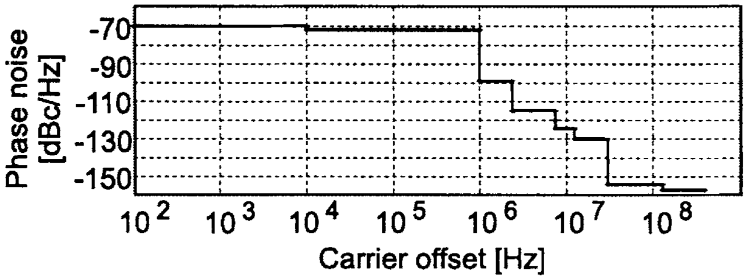

Figure 2. Limits for Tx LO phase noise.

4.2. SPURIOUS REQUIREMENTS

Noise emissions are critical for the spurious emission test in [1] and noise in the UTRA/FDD Rx band. Three critical sources of noise power are found. These are the transmitter circuits, the LO and the I and Q signals. It is assumed that the LO phase noise spectrum is flat in bands 1 to 3, meaning that the SNR at the LO carrier is maintained at the output signal. It is further assumed that noise power at offsets up to ±30 MHz from the Tx-band is amplified with the inband gain. Third order intermodulation between the Tx signal and input noise has been observed on PAs. This has the effect that input noise at $f_c - f$ is converted to $f_c + f$. Measurements on a state-of-the-art PA have indicated a conversion gain of the same magnitude as the gain at $f_c + f$. This means that the LO and input signals contribute at both $f_c - f$ and $f_c + f$. The resulting noise requirements for the transmitter circuits are listed in Table 4.

4.3. ADJACENT CHANNEL LEAKAGE RATIO (ACLR)

ACLR may be generated from intermodulation in the transmitter, phase noise, and noise in the I and Q signals. Phase noise and noise in the I and Q signals is chosen so that ACLR generated by the transmitter must be 1 dB above the overall Tx requirements. The ACLR requirements to the transmitter are listed in Table 4. It is likely that the PA is allowed to generate most of the ACLR in the transmitter in order to improve power efficiency. If the PA is allowed to generate, say, 33.5 dB of ACLR at $f_c \pm 5$ MHz, the requirements to ACLR, generated by the I and Q signals and phase noise, must be increased by 3 dB. Investigations of intermodulation

Table 4. Summary of transceiver requirements.

Rx parameters		Tx parameters	
Noise figure [dB]	≤ 6	Output noise [dBm/Hz]	
Selectivity [4] [dB]		Band 1	≤ -124
1st adj. ch. ($f_c \pm 5$ MHz)	≥ 33	Band 2	≤ -107
2nd adj. ch. ($f_c \pm 10$ MHz)	≥ 49	Band 3	≤ -140
Remaining Rx-band	≥ 51	ACLR [dB]	
1980–2025 MHz	≥ 56	$f_c \pm 5$ MHz	≥ 34
Tx-band	≥ 77	$f_c \pm 10$ MHz	≥ 44
Intercept points [dBm]		IQ imbalance [3]	
iIP_2 ($f_c \pm 10$ MHz)	≥ -23	Amplitude [dB]	≤ 1.4
iIP_2 ($f_c \pm 15$ MHz)	≥ 1	Phase [deg]	≤ 5
iIP_2 (Tx-band)	≥ 57	Average offset [5]	
iIP_3 ($f_c \pm$ (10–20) MHz)	≥ -23	Amplitude [dB]	≤ 0.4
iIP_3 (1670–2025 MHz)	≥ -5	Phase response [deg]	≤ 4
		LSR [4] [dB]	≤ -27

in PAs have shown that the most suitable way to describe ACLR performance of such devices on a general level, is simply to specify ACLR [3]. Therefore, in this work, only the ACLR is specified.

4.4. ERROR VECTOR MAGNITUDE (EVM)

EVM is generated by many different circuit imperfections, depending on which transmitter architecture is used. For a direct up-conversion transmitter, the significant factors are: Input signal, inband phase response and amplitude ripple, I- and Q-imbalance, phase noise, intermodulation and LO leakage. The relation between EVM and offset from the average gain, as well as the relation between EVM and the difference between the actual phase response and the ideal phase response are described in [5]. The effects of I- and Q-imbalance, inband phase noise and intermodulation are described in [3], which also explains how to combine uncorrelated contributors of EVM. In [4], LO leakage is described by the *LO to Signal Ratio* (LSR). No adjustments of DC-offsets is allowed during EVM measurements. If this is allowed, LSR will have no effect on EVM. The total amount of average EVM generated by the transmitter must not exceed 17.2% rms. This leads to the requirements proposed in Table 4.

5. Block Requirements for a Direct Up/Down Conversion Transceiver

The Rx and Tx requirements are summarized in Table 4.

5.1. RECEIVER BLOCK REQUIREMENTS

In recent years, direct-conversion receivers have emerged for GSM applications and many consider this architecture the proper choice for 3G systems. A particularly nice feature of W-CDMA is the fact that the large bandwidth makes W-CDMA systems less sensitive towards

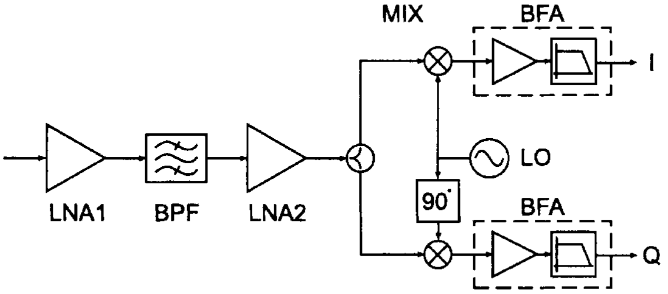

Figure 3. Direct-conversion receiver.

$1/f$ noise and DC offset problems inherent to direct-conversion receivers. An example of a UTRA/FDD direct-conversion receiver is shown in Figure 3. An interstage *bandpass filter* (BPF) is used to provide attenuation of the Tx-leakage signal. The amount of attenuation required from this filter depends on the difference in requirements to in-band and out-of-band linearity. The goal is to attenuate the Tx-signal such that requirements to iIP_2 and iIP_3 for the subsequent RF blocks are the same for both the Rx band and out-of-band. Assuming that the BPF has an insertion loss of 3 dB, the required attenuation must be at least 31 dB from 1670 MHz to 2025 MHz. The proposed block requirements are listed in Table 5. The gain budget represents a compromise between NF and iIP_n and as such several budgets could be made resulting in different sets of NF and iIP_n. Requirements to NF are found using Friis's cascade formulae while requirements to iIP_3 are found using the cascade formulae described in [6]. The BPF is assumed to be passive and thus without significance when concerning linearity. Second order non-linearity is only critical for blocks operating at baseband and is therefore only specified for the *mixer* (MIX) and the *baseband filter and amplifier* (BFA). In this configuration, Tx-leakage only sets the requirements to *Low noise amplifier number 1* (LNA1). Requirements to iIP_2 represent compromises between how much distortion power the MIX and the BFA are allowed to generate. The budget in Table V allows MIX to generate most of the distortion power. At high frequency offsets, this means that seemingly harsh requirements are made to BFA. However, since the requirements to iIP_2 are based on interfering signals at 7 times the BFA cut-off frequency, this is not considered to be a critical design parameter. Some tolerances must be specified for all block gains to accommodate different variations. These tolerances require an additional margin to be put on the performance parameters in Table 5. Based on these block requirements, it is clear that meeting the test specifications listed in the UTRA/FDD standard is by no means unrealistic. Being able to operate LNA1 at a noise figure of 4 dB makes the design of this block less critical. In terms of linearity, the continuous presence of the Tx-signal sets the most stringent requirements to the receiver. This problem becomes less severe when an interstage bandpass filter is used.

Table 5. Receiver block requirements.

Block	LNA1	BPF	LNA2	MIX	BFA
Gain [dB]	15	–3	9	10	–
NF [dB]	≤ 4	≤ 3	≤ 4	≤ 16	≤ 31
Intercept points [dBm]					
iIP_2 ($f_c \pm 10$ MHz)	–	–	–	≥ 1	≥ 11
iIP_2 ($f_c \pm 15$ MHz)	–	–	–	≥ 23	≥ 39
iIP_2 (Tx)	–	–	–	≥ 23	≥ 39
iIP_3 ($f_c \pm$ (10–20) MHz)	≥ -4	–	≥ -6	≥ 0	≥ 10
iIP_3 (1670–2025 MHz)	≥ -4	–	≥ -6	≥ 0	≥ 10

Table 6. Transmitter block requirement.

Block	QUC	VGA	FI	PA
Gain [dB]	0	13	–2	25
NF [dB]	≤ 10	≤ 4	≤ 2	≤ 5
ACLR [dB]				
$f_c \pm 5$ MHz	≥ 43	≥ 45	–	≥ 35
$f_c \pm 10$ MHz	≥ 53	≥ 55	–	≥ 45

5.2. TRANSMITTER BLOCK REQUIREMENTS

The direct up-conversion transmitter architecture is illustrated in Figure 4. When calculating the output noise, intermodulation in the PA must be considered. It is assumed that the conversion gain is equal to the actual gain and that this can be taken into account by doubling the effective noise bandwidth. A set of block requirements to in-band gain, NF and ACLR is proposed in Table 6. Noise and gain are assumed constant for all frequencies under observation, except for the PA, where a gain of 23 dB and a NF of 7 dB are assumed for band 3 and the image of this band. NF is specified so the overall requirement to noise in band 1 is met. To meet the more harsh requirement to noise in band 3, the *filter* (FI) must attenuate this band and the image with 21 dB. When the transmitter is operated at the highest frequency, the

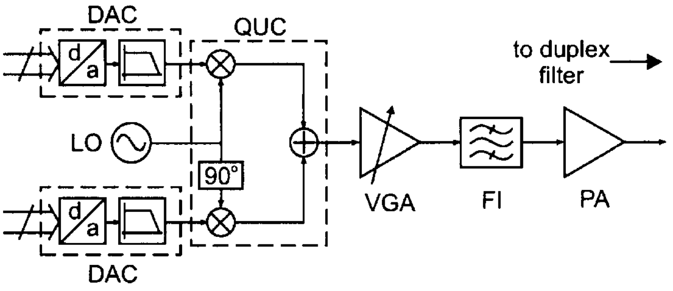

Figure 4. Direct up-conversion transmitter.

image may be offset 70 MHz from the lower edge of the Tx-band. Therefore, FI must provide 21 dB of attenuation at ± 70 MHz offsets from the Tx-band. To omit FI the duplex filter must provide 49 dB of Tx-Rx isolation in the Rx band. The total ALCR generated by n circuits, $ACLR_T$, can be found from the ACLR of each circuit, $ACLR_{m|m=1,2,\ldots,n}$, using Equation (2), where all ACLR are represented in numbers.

$$ACLR_T = \frac{1}{\sum_{m=1}^{n} ACLR_m^{-1}}. \tag{2}$$

As was the case for the receiver, tolerances on block requirements must be specified in order to accommodate different variations. The proposed gain budget means that the average output power of the *quadrature up-converter* (QUC) is –7 dBm. The proposed LO power is –6 dBm. To obtain the proposed LSR the LO-leakage must thus be –28 dB or less. If the LO power is increased, requirement to LO-leakages becomes more harsh. The requirement to output noise in band 1 sets harsh requirements to noise in the QUC. Image mixing in the PA prevents FI from removing this noise, because the image is inside the Tx-band. The only way to allow for an increase in the QUC noise figure, is to attenuate band 1 in the duplex filter.

6. Conclusion

In this paper, a set of UE transceiver requirements have been derived from the UTRA/FDD standard. Plausible block requirements for a direct-conversion receiver are proposed. FDD operatio means that Rx and Tx may be active simultaneously. This results in a harsh requirement to Rx linearity. Tx specifictions are translated to block requirements for a direct up-conversion transmitter. FDD operation means that an RF band-pass filter is required in the Tx chain to reduce Tx-noise in the Rx band. It should be noted that requirements proposed in this document are based directly on specifications. In practice, some margin must be included to take into account fabrication tolerances and other uncertainties. Also, it is worth noting that UTRA/FDD is an interference limited system to a wide extent, where any additional performance surplus on the UE will lead to increased system capacity. Hence, network providers may prefer UEs with better performance. UE manufacturers may therefore wish to exceed specifications to gain market shares.

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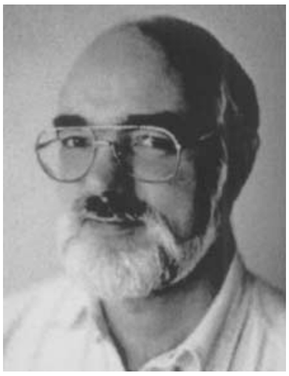

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An UTRA/FDD Direct-Downconversion Mixer in 0.25mu CMOS

J. Bøjer, M.B. Gentsch, O.K. Jensen, J.H. Mikkelsen, K.A. Pedersen, and S. Lindfors
vspace0.5cm *IEEE NORCHIP Conference*
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An UTRA/FDD Direct-Downconversion Mixer in 0.25μm CMOS*

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Abstract

In this paper, the design of a 2GHz direct-downconversion mixer for a UTRA/FDD receiver is presented. The mixer is implemented using a standard low-cost 0.25µm, single-poly, six-metal CMOS process. A four-port on-chip balun is used to generate a balanced RF input signal. In-house optimized device models are used for both active and passive components to achieve a voltage conversion gain of 15dB, an iIP_2 *of 23dBm, an* iIP_3 *of -1dBm, a noise figure of 8dB. The circuit provides I and Q signal path outputs while drawing 6mA from a 2.5V supply.*

1 INTRODUCTION

In all receiver designs, low noise and capability of handing interfering signals, such as blockers and image frequencies, is a major concern. The scenario for the 3G systems [1] has changed compared with the 2G systems. The W-CDMA signals have varying envelope, making even order distortion problems more severe. The use of simultaneous transmission and reception (FDD) causes disturbance of the receiver from the transmitted signal appearing as a high level blocker at an offset of 134.8 MHz to 245.2 MHz, even though a good duplex filter is used [2]. The Tx-leakage combined with a single external blocking signal also sets requirements to 3rd order intercept points.

Studies of receiver structures based on system level simulations reveal that an interstage bandpass filter is required to meet radio specifications while still preserving realistic requirements for the remaining CMOS blocks. Due to its flexibility and low cost a direct-conversion receiver (DCR) approach is chosen, despite its well known problems. Unlike narrow-band systems, W-CDMA is fairly robust towards DC offsets in the I and Q path as low frequency content can be rejected by high pass filters[3]. The resulting interface definitions for the chosen direct down-conversion receiver are illustrated in Figure 1.

The first stage is a *duplexer* (DPX) with RX bandpass characteristics. It is followed by an LNA driving the interstage filter (BPF) that further rejects the TX signal to an acceptable level. Following the BPF there is a quadrature down-converter (CNV) with a passive balun at the input, and finally two parallel *baseband filter and amplifier* (BFA) paths that provides the channel selectivity. The BFA includes a servo-type feedback loop to compensate for DC-offset generated in both the CNV and the BFA [4].

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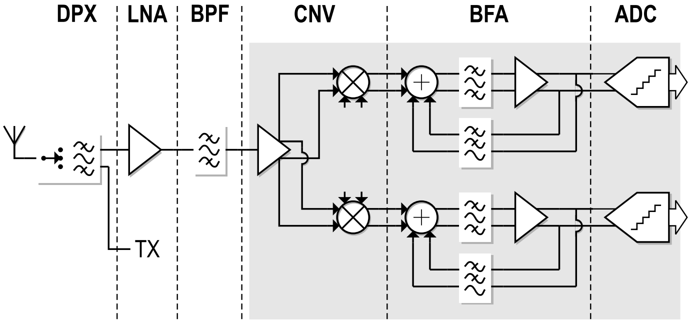


FIGURE 1: *System diagram of the UTRA/FDD direct-downconversion receiver. Shaded blocks are intended for CMOS implementation.*

A receiver analysis taking into account technology limitations, gain distribution, noise, nonlinearities and selectivity leads to the mixer requirements listed in Table 1 [5].

2 MIXER DESIGN

The mixer topology[6] is a modification of the well known Gilbert cell mixer and it is shown in Figure 2. A balanced structure is desirable since it helps to minimize substrate current injection, package-to-board ground bounce and it offers good attenuation of the even order distortion. Moreover, the transconductance and switching devices required in the Gilbert cell lines well up with CMOS IC technology strong points.

As Figure 2 shows, the Gilbert cell has been modified to accomodate the quadrature signal requirement of the DCR. Instead of running two separate mixers in parallel the quadrature capability is attained using a shared differential transconductance stage as input to the I and Q channel switching cores. While this has no effect on power consumption it implies that only switching core mismatch add to imbalance. The reason for this is illustrated in Figure 3 where it is shown that during one quarter period of the LO cycle the current is shared between the two positive terminals for I and Q signals. During the subsequent quarter period the I path current is handed over from the positive to the negative terminal while the positive Q terminal still carries its half of the current.

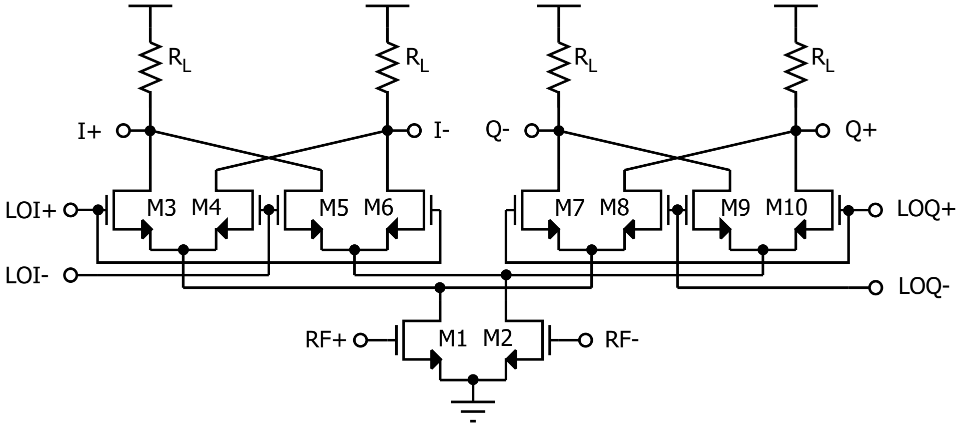


FIGURE 2: *Direct-downconversion I/Q mixer topology*

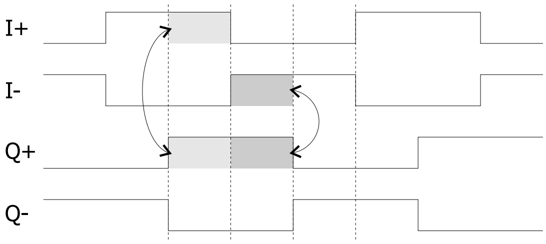


FIGURE 3: *LO switching scheme results in current sharing between I and Q paths.*

2-1 Switching transistors

The mixers have been designed in an approach starting with the output and switching stage. A quiescent current of 6mA was chosen for the mixer based on the output power requirement.

In Gilbert cell mixer the switch transistors contribute only little noise assuming instantaneous switching. This is because they are presented by a high source impedance from the input stage which effectively prevents the channel noise current from flowing to the output. In the case of a combined quadrature mixer, the switch transistors see the low source impedance of the current switch transistors in the other quadrature branch. This provides the channel noise of the switch transistors with a coupling path to the output and consequently they will add to the noise figure even in an instantaneously switching case.

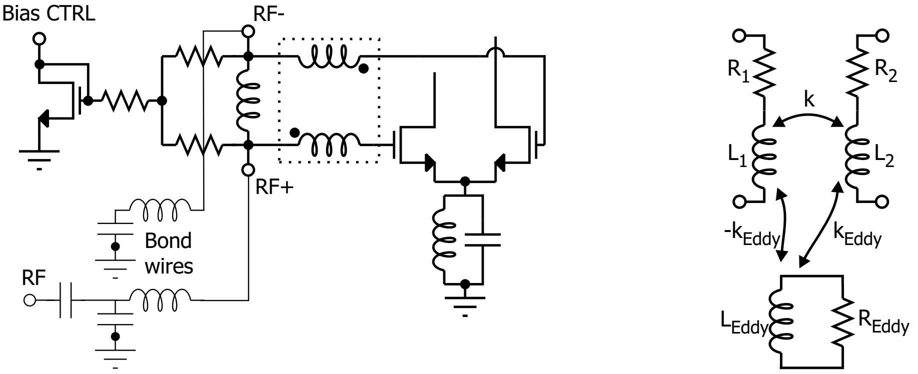
In [7] it is shown that the combined quadrature mixer has a noise advantage compared to two Gilbert cell mixers which partly offsets the relatively higher noise contribution from the current switches. Furthermore, the noise contribution from the switches is in fact reduced when the switching is not instantaneous. For example when the LOI+ input goes high M3 will pull the drain of M1 up and close M4, thus preventing it from contributing noise. However, when LOI+ is high both LOQ+ and LOQ- are close to zero crossing and the switch transistors M7 and M8 are also turned off, for a period of time, effectively preventing any of the switch transistors M3-M4, M7-M8 from contributing noise.

The size of the switching transistors were optimized with Agilent ADS for low noise figure and a gate width of 100μm with a 1.42V_{PP} differential LO amplitude was selected.

2-2 Input transconductance stage

The g_m stage transistor size has been determined by simulating the stage for noise figure, gain and compression as a simple amplifier stage. A load impedance equivalent to the switch has been used. Differential source degeneration inductance has been avoided.

In a direct conversion receiver it is important that the mixer provides some common mode rejection. This is necessary for obtaining a good balance for the differential current signal entering the switching stages. Usually, a differential pair is biased with a current source to fix the common-mode current and thus reject common-mode signals present at the differential pair input. However, the current source requires some voltage headroom which is undesirable at a low supply voltage. Alternatively, an LC resonator may be used [8][9]. It was found from simulation that this topology provides a common-mode rejection comparable with the current source approach while having the advantage of not consuming DC voltage headroom.



(a) (b)

FIGURE 4: *a) Illustration of the input scheme used in the mixer implementation. b) The on-chip transformer simulation model. (Capacitive couplings not shown.)*

2-3 Input balun network

One requirement of the mixer is that it is capable of being driven by a single 50ohm source. A significant part of the attention has been put on designing an input structure that is able to deliver a well balanced AC signal to the mixer switching stage despite being driven by a single-ended source. This is particularly important for minimizing the even order distortion. An on-chip balun has been designed for this purpose. Being a passive structure, the balun does not produce any distortion and has a lower noise figure than an active balun would have.

The balun is made using an octagonal on-chip coil with 2 separate windings (2 turns each) with a symmetric layout. An EM- simulation is made using Agilent ADS/Momentum. The model shown in Figure 4b is used in the circuit simulations. The model includes inductive and capacitive coupling between the windings, lossy capacitive substrate coupling, resistive series losses and Eddy-current loss. The model parameters are adjusted to fit the EM-simulation results.

Due to the poor coupling factor of 0.7 and Q in the balun a different configuration from that reported in [10] was chosen where the coupling inductors are connected in series to the input gates (Fig. 4a). The coupling inductors are connected to a third inductor making up a tapped coil impedance transformator. The transformator is brought into resonance by the gate capacitance and external capacitors. The two inputs to the network are brought out so the mixer can be driven both in a balanced manner as well as single ended by adding an external shunt capacitor. The circuit topology allows for further integration of the external capacitors. The balun is able to only partially reject the input common-mode component due to single-ended excitation. However, the quadrature mixer input stage provides further common-mode rejection yielding a sufficient balance prior to the switching core.

3 MEASUREMENT RESULTS

The mixer die was directly bonded to a PCB for testing. The local oscillator phasing was generated with microstrip delay lines. For gain, noise and IP2 measurements a TI THS4031 derived differential to single ended measurement amplifier was used. Noise figures and iIP_3 have been measured with an R&S FSIQ26 spectrum analyzer. Gain and P_{1dB} have been measured with an oscilloscope. Measurement amplifiers were omitted for the iIP_3 measurement.The phase splitting network generated, at the time of measurements, an offset between LOI and LOQ of up to 0.7 dB. This has generated a discrepency between I and Q gain in the measurements. It has been verified that the DUT is indeed symmetric by interchanging the inputs for LOI and LOQ.

The measurement results and simulation results are listed in Table 1. The difference between I and Q gain can be seen. This is also influencing the noise figure as the signal is attenuated or amplified relative to output related noise. With a well balanced LO feed it is expected that I and Q gain will be in balance. There is a difference between the simulated iIP_2 and the measured, allthough the results meet the specifications with margin. Monte Carlo simulations with device mismatches have been performed without showing this extent of degradation. The root cause of this discrepancy has not been found. The LO balance may be one reason.

The input match (S_{11}) can be seen in Figure 6. The input has a match better than -10 dB for a frequency range from 1.5GHz to 2.3GHz.

All measurement results comply well with the requirements. The gain, noise figure and compression results do also align reasonably well with the simulations.

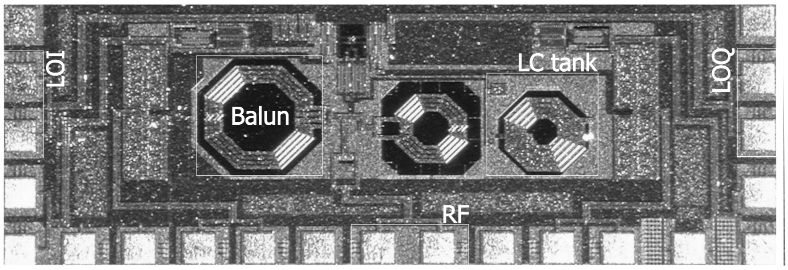


FIGURE 5: *Chip photo showing the direct-downconversion mixer occupying 1.9x0.7mm.*

TABLE 1: *Performance specifications and measured results for the direct-downconversion mixer.*

Parameter	Requirements	Simulations	Measurements
Voltage Conversion Gain (I/Q)	16dB	16.3dB	15 dB (15.9/13.9) (13.9/15.9)
Noise figure [10kHz-2MHz] (I/Q)	< 7.6 dB	7.6 dB	8 dB (7.4/8.5)
Input 1 dB Compression Point I/Q	> -12dBm	-10 dBm	-11/-10dBm
2^{nd} Order Input Intercept Point I/Q	>+19.7dBm	+54 dBm	+26.3/+22.7dBm
3^{rd} Order Input Intercept Point I/Q	> -4.7dBm	-2.2 dBm	-0.9/-1.4 dBm
Input match S_{11}	<-10dB	<-10dB	<-10.9dB
Output Impedance (Single ended)	< 300Ω	250Ω	226 Ω

4 CONCLUSIONS

Based on a simple, yet accurate, approach to receiver planning a set of radio requirements have been derived for a direct-downconversion mixer for a UTRA/FDD receiver. Using a modified Gilbert cell mixer a quadrature-output direct-downconversion mixer has been designed and implemented. The mixer input matching network functions as a balun and enables the mixer to be driven with a single-ended source. The measured results are in good agreement with the simulations. The mixer meets the derived requirements except for the gain and the noise figure which are very close to the specification.

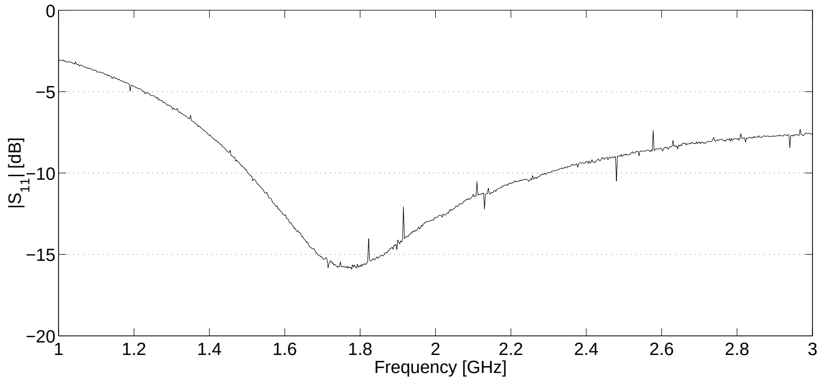


FIGURE 6: *Input match at the RF port.*

5 ACKNOWLEDGMENT

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Evaluation and Modeling of Guard Ring Related Device Performance Degradation

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vspace0.5cm *IEEE NORCHIP Conference*
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Evaluation and Modeling of Guard Ring Related Device Performance Degradation[*]

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Abstract

In this paper, the effect of different guard ring distances is presented for both inductor and capacitor designs. Test devices are fabricated in a $0.25\mu m$ CMOS process and subsequently measured and simulated for this purpose. The results help quantify the performance degradation compared to required component area. A simplified simulation model for one of the structures is presented to support measurement results.

1. Introduction

Passive components, such as inductors and capacitors, are extensively used in a variety of RF applications [1]. Due to the cost reducing potential of integrated circuit design many of these applications aim at RF-IC solutions. Compared to discrete solutions, passive IC components have inferior performance and for that matter, analysis and optimizations of these components represent important tasks for integrated circuit design. With time-to-market being an important business parameter, the accuracy of IC vendor supplied models is an important competition parameter as well as the actual component performance.

One way to improve performance for inductor structures is to maximize the electromagnetic energy stored in the structure while, at the same time, minimizing the energy dissipation [2]. However, to restrict the extension of the fields and thereby limit coupling to other circuits a guard ring is needed. Having a guard ring closely surrounding the inductor structure improves on the isolation properties but it is also expected to degrade inductor performance thereby presenting a trade-off in device design. Often, to present customers with good device performance vendors use fairly large distances between device perimeter and guard ring. For the designer this also has the drawback of consuming extra die area.

The aim of this paper is to quantify the variations in device performance parameters for different guard ring distances. This is done for both inductor and capacitor structures. In both cases the structures are implemented using a 0.25μm, 5 metal layer, CMOS technology.

To understand the effect of the guard ring it is helpful to consider the coupling effects as they appeared in a conductor [3]. The two effects illustrated in Figure 1 are results of the magnetic field and the electrical field. Any AC current in a conductor gives rise to a magnetic field whereby current is induced into the substrate beneath the conductor and any neighboring metal layers. The electric field is generated by voltage difference between conductor and substrate and it goes through the oxide layer and into the substrate. This introduces parasitic capacitance between metal layers and substrate and it also results in resistive losses due to electric fields into the conductive substrate.

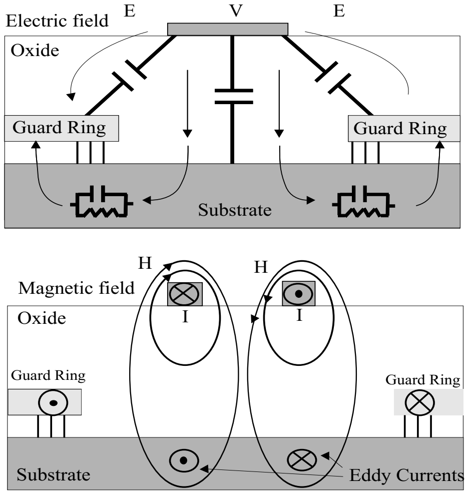

Figure 1: Electric and electromagnetic fields induced by a conductor.

The guard ring is used to connect the substrate below the device to a ground reference to obtain isolation to other circuits. The guard ring is basically a short-circuited winding and because of magnetic coupling it carries a substantial current. Moving the guard ring closer to the device perimeter limits the extension of the magnetic field which results in a reduced inductance value. Further, a tightly placed guard ring reduces the direct capacitive coupling from device to substrate but it also slightly increase the capacitive coupling from device to the grounded guard ring. Finally, the increased coupling from device to guard ring also increases induced current and therefore also an excess loss for inductors.

In this paper, structures with different distances to their guard rings are presented. A simplified model for inductance simulation is explained and measurements and simulations on the devices are presented.

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[0] * Paper published in Proc. of 21th IEEE NORCHIP Conference, (Riga, Latvia), pages 228-231, November 2003

2. Layout Considerations

In order to test the effects of a reduction in guard ring size, two structures are designed; S1 and S2. Structure S1 contains two inductors where guard rings have been placed at distances of approximately 10μm and 32μm from the device perimeter. Structure S2 contains two capacitors with different distances to their respective guard rings. One capacitor uses a tight guard ring where the substrate contacts are placed at only 2μm from the perimeter of the device. The other capacitor makes use of a distance of approximately 32μm. The actual layout of the two structures are illustrated in Figure 2 and Figure 3.

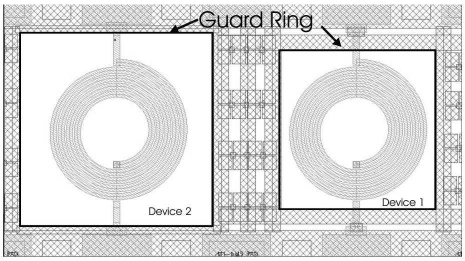

Figure 2: Layout of structure S1 showing two inductors.

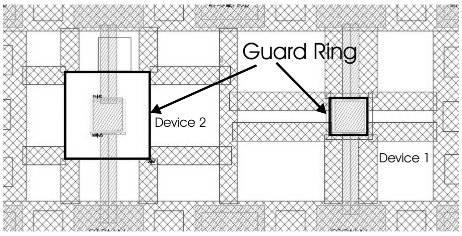

Figure 3: Layout of structure S2 showing two capacitors.

3. Simulations

To support measurements and to help understand these the "2.5D" EM-Simulator Agilent ADS/Momentum is used. This simulator is able to simulate 3D structures with some limitations in geometry.

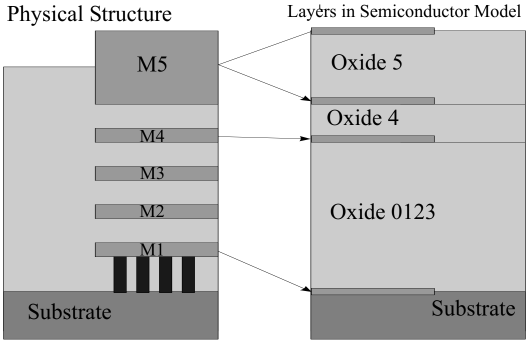

Figure 4: Physical metal layer structure and the simplified structure used in inductor simulations.

A significant limitation is that inclusion of a high number of layers gives a very long simulation time. Also, to limit simulation time metal layers of finite thickness must to be approximated by sheets of zero thickness. The physical structure and the structure used in simulations are shown in Figure 4. In the case of the inductor structures, metal 5 is used for the inductor spiral while metal 4 is used for the under-pass. In simulations metal 5 is represented by two sheets to make to simulations more accurate. The two sheets each have twice the sheet resistance of the metal 5 layer and are subsequently connected in parallel by vias. For metal 4 only a single sheet is assumed to be sufficiently accurate during simulations. Metal 1 is used for the guard ring and this is connected to the substrate by a vast number of contacts. A detailed modeling of these would be result in unacceptable simulation times and instead a single sheet is placed directly on top of the semi-conducting substrate. This approach models the main properties of the guard ring; i) a low resistance contact to the substrate is provided for both the physical structure and the model, and ii) a short-circuited ring is present i both cases. The guard ring is positioned slightly lower in the modeling than in the physical structure, but since the displacement is small compared to the distance between windings and guard ring this effect is expected to be insignificant. Again, to further reduce the computation time the substrate is modeled by an infinitely thick layer. Since the substrate thickness is considerably larger than the inductor diameter this approach is considered sufficiently accurate.

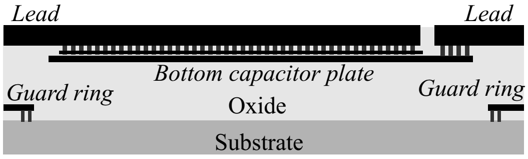

Figure 5: Physical metal layer structure used in the capacitor design.

For the capacitance structures (see Figure 5) the effect of changes in guard ring distance is expected to have significantly less effect on device performance. However, any reduction in the guard ring distance may decrease the bottom plate stray capacitance to the substrate, but at the same time the coupling from the bottom plate to the guard ring may increase. The same aspects are expected to be valid for the stray capacitance resulting from connecting leads. Overall, the total stray capacitance is expected to increase slightly for a reduction in guard ring distance. For the used CMOS process, the distance between the top and bottom plates of the capacitor is significantly smaller than the distance from bottom plate to guard ring and to substrate. As a result it is expected that the stray capacitance from the bottom plate to the substrate amounts to only around 1% of the wanted series capacitance. Adding the stray capacitance of the test structure leads increase this percentage. With the majority of the electrical fields being trapped between the two plates of the capacitor the primary capacitance should therefore not be affected. Since measurements support this the capacitor structures have not been simulated.

4. Measurements

The implemented structures are evaluated using 2-port s-parameter measurements based on an ISS-based calibration. The obtained data is subsequently de-embedded to remove any effect from the probing pads and measurement structure [4]. To illustrate the results y-parameters are used as they provide for a convenient translation to the pi-type equivalent circuit (see Figure 6) used for the component modeling.

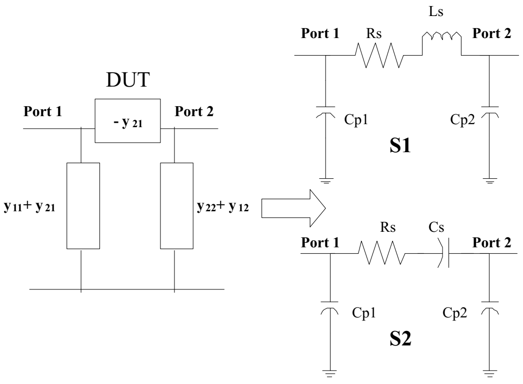

Figure 6: Model for components extraction.

Translation from y-parameters to the device model parameters illustrated in Figure 6 is done according to the following equations

$$L_s = \frac{1}{\Im\left(\frac{1}{y_{12}}\right) \cdot \omega} \quad \wedge \quad R_s = \Re\left(\frac{-1}{y_{22}}\right) \tag{1}$$

$$C_s = \frac{-\Im\left(\frac{1}{y_{12}}\right)}{\omega} \tag{2}$$

For the Q-factor the calculations are according to the following equations

$$Q_L = \frac{\omega \cdot L_s}{R_s} \quad \wedge \quad Q_C = \frac{1}{R_s \cdot C_s \cdot \omega} \tag{3}$$

Five different dies are measured in order to reduce random errors. For inductors, averaged measurement results as well as simulation results are shown in Figure 7 and Figure 8. For capacitors the measurement results are shown in Figure 9.

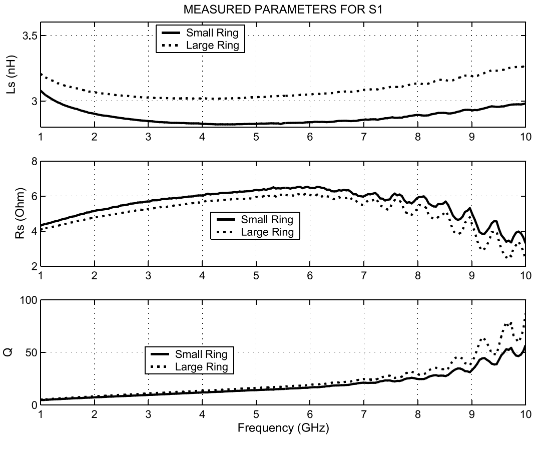

Figure 7: Measured parameters for both inductor devices on structure S1.

From Figure 7 the guard ring distance is found to have substantial impact. As expected, the inductance value decreases when the size of the guard ring is reduced. Reducing the size of the guard ring increases the effect on the magnetic field of the inductor. This tighter coupling between inductor and guard ring also introduce more loss. Both these effects combine to degrade the Q-factor of the inductor.

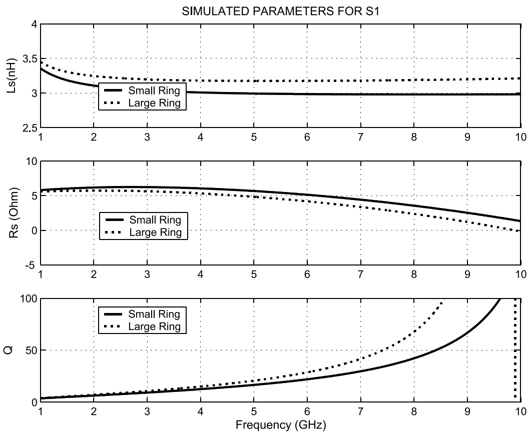

Figure 8: Simulated parameters for both inductor devices on structure S1.

The simulation results shown in Figure 8 support the measurements and also follow the same tendencies as the measurements. It should be noted that the value and curve shape for the results, measured as well as simulated, depend on representation. In both Figure 7 and Figure 8 the series resistance approach zero at high frequency while Q-values appear to increase. When represented as a 1-port device the exact same structure shows an increase in series resistance for higher frequencies. Also, when analyzed as a 1-port the Q-factor is found to have a maximum of 10 at 5GHz for the large guard ring distance and for the reduced distance the maximum value is approximately 9 at 5.5GHz. The explanation for this phenomenon is not quite clear but it is expected to be partly due to transmission line effects.

To summarize the results, Table 1 and Table 2 show the measured and simulated values obtained for the inductor structures at 2GHz and 5GHz. Also, the tables indicate the deviation between measured and simulated values. The net area within the small guard ring is approximately 65% of the net area within the large guard ring. While this change is relatively small the results clearly show that the Q-factor for inductors decreases with a tight guard ring. The results can be used as help for selecting the proper compromise between the overall size and the Q-value for a given application.

Table 1: Parameters for inductors at 2GHz.

S1	L_s (nH)			Q		
	Meas.	**Sim.**	**Dev.**	**Meas.**	**Sim.**	**Dev.**
Small GR	2.9	3.1	6.4%	7.2	6.4	10.8%
Large GR	3.1	3.3	5.7%	8.5	7.4	13.0%
GR effect	5.8%	5.1%		16.0%	13.8%	

When capacitors are regarded, the difference in port-to-port capacitance at low frequencies is so small, that it is impossible to measure. Also, as Figure 9 shows the series resistance values are very similar and also very small for both devices.

Table 2: Parameters for inductors at 5GHz.

S1	L_s (nH)			Q		
	Meas.	**Sim.**	**Dev.**	**Meas.**	**Sim.**	**Dev.**
Small GR	2.8	3.0	6.6%	14.4	15.9	9.3%
Large GR	3.0	3.2	3.1%	17.1	22.1	22.3%
GR effect	8.1%	4.7%		15.8%	27.9%	

The difference is in fact smaller than the variations in probing contact resistance.

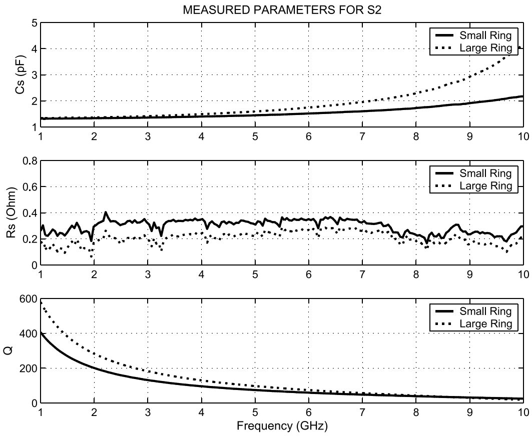

Figure 9: Measured parameters for capacitors on structure S2.

Q-values are found to decrease as the guard ring is moved closer. While this is not in accordance with expectations it must be noted that measuring high Q-values is always very difficult due to the high sensitivity towards for instance contact resistance variations.

The frequency dependent increase in capacitance indicate that the applied pi-equivalent is insufficient for representing the measurements. To see if the stray capacitances may affect measurements, C_{p1} and C_{p2} are calculated using the following equations

$$C_{p1} = \frac{\Im\left(y_{11} + y_{12}\right)}{\omega} \quad \wedge \quad C_{p2} = \frac{\Im\left(y_{22} + y_{12}\right)}{\omega} \tag{4}$$

When plotted as done in Figure 10 C_{p1} and C_{p2} are found to be in the order of 10fF to 25fF. This is almost one hundred times smaller than series capacitance of the device so the effect of stray capacitances is negligible.

The C_s deviation at high frequencies may instead be explained by a difference in lead inductance in the two capacitor structures. The models used for capacitors and inductors are very simple and it turns out that is too simple to describe the capacitor case here. In this case, to explain the increase in capacitance value at high frequencies it is necessary to consider the series inductance of the test structure.

The inductance of the device leads and ground leads becomes increasingly important when the distance between the guard ring and the component is higher. This can be the reason why the capacitance presents a lower resonant frequency. For frequencies up to around 5GHz the inductive effect is negligible and the results summarized in Table 3 apply. The net area within the small guard ring is approximately 18% of the net area within the large guard ring. Despite this significant change in guard ring area the effect on the final capacitance value is negligible. In this case the use of a large guard ring distance is not justified. A capacitor may therefore be designed without wasting a large area for the guard ring.

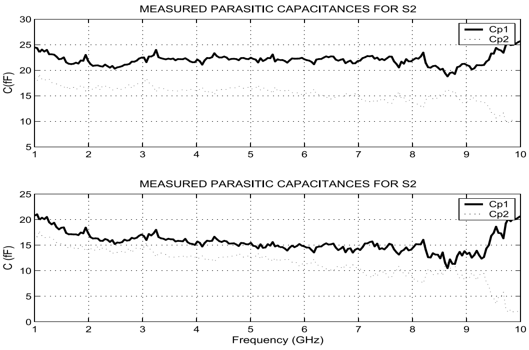

Figure 10: Measured parasitic capacitance versus frequency for both capacitor devices of S2 structure. Top: Large GR and bottom: small GR.

Table 3: Parameters for capacitors at 2GHz and 5GHz.

S2	@2GHz		@5GHz	
	C_s (pF)	Q	C_s (pF)	Q
Small GR	1.3	200	1.5	74
Large GR	1.4	283	1.6	96
GR effect	1.4%	30%	9.3%	23%

5. Conclusion

The effect of having guard rings in different distances to device perimeter has been presented for inductor and capacitor structures. For inductances, a decrease of the guard ring distance results in a reduction of inductance value as well as an increase of series resistance. Both these factors combine to reduce the Q-value of the device. In the presented case, a decrease of 35% in die area results in a Q-value reduction of approximately 16% up to 5GHz. This effect is even more pronounced at higher frequencies.

For capacitances, the use of a small guard ring does not give any noticeable degradation compared to a larger ring as stray capacitances are small in both cases. At higher frequencies the lower inductance associated with the small guard ring is beneficial.

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An UTRA/FDD Direct-Downconversion Mixer in 0.25mu CMOS

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An UTRA/FDD Direct-Downconversion Mixer in 0.25 μm CMOS

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Abstract. In this paper the design of a 2 GHz direct-downconversion mixer for a UTRA/FDD receiver is presented. The mixer is implemented using a standard low-cost 0.25 μm, single-poly, six-metal CMOS process. An on-chip passive balun is used to generate a balanced RF input signal. In-house optimized device models are used for both active and passive components to achieve a voltage conversion gain of 12.8 dB, an iIP_2 of 25 dBm, an iIP_3 of -3.1 dBm, and a noise figure of 8 dB. The circuit provides I and Q signal path outputs while drawing 6 mA from a 2.5 V supply.

Key Words: UTRA, CMOS, mixer, balun, direct-downconversion

1. Introduction

In all receiver designs low noise and capability of handling interfering signals, such as blockers and image frequencies, are of major concern. The scenario for the 3G systems has changed compared with the 2G systems [1]. The W-CDMA signals have varying envelope, making even-order distortion problems more severe. The use of FDD (simultaneous transmission and reception) causes disturbance of the receiver as the transmitted signal appears as a high level blocker at the RX input. Even though a good duplex filter is used, the TX signal appears as an interferer at an offset of 134.8 MHz to 245.2 MHz, [2]. The TX leakage combined with a single external blocking signal also set requirements to third-order intercept points. Studies of receiver structures based on system level simulations reveal that an interstage bandpass filter is required to meet radio specifications while still preserving realistic requirements for the remaining CMOS blocks [2]. Due to its flexibility and low cost a direct-conversion receiver (DCR) approach is chosen. Because of its wideband nature, W-CDMA is fairly robust towards DC offsets in the I and Q paths. As a result undesired low frequency signal content can be attenuated by highpass structures [3]. This makes the DCR a viable receiver structure for this application. The resulting interface definitions for the chosen direct down-conversion receiver are illustrated in Fig. 1.

In the overall receiver set-up a provision for multimode operation is made by inserting a mode-selection switch just after the antenna. The second stage in the UTRA part of the receiver is a *duplexer* (DPX) with RX bandpass characteristics. It is followed by an LNA driving the interstage filter (BPF) that further rejects the TX signal to an acceptable level. Following the BPF there is a quadrature down-converter (CNV) with a passive balun at the input and finally two parallel *baseband filter and amplifier* (BFA) paths that provide the channel selectivity. The BFA implements a fifth order Butterworth filter response and provides up to 85 dB of voltage gain with an AGC range of 60 dB. Also, the BFA includes a servo-type feedback loop to compensate for DC-offset generated in both the CNV and the BFA [4].

A receiver analysis [5] where technology limitations, gain distribution, noise, non-linearities, and selectivity are taken into account leads to the mixer requirements listed in Table 1. Several of the test cases may cause second-order non-linearities to distort the wanted signal. One example is the sensitivity test where second-order distortion products resulting from the TX leakage signal adds to the received signal. This causes the wanted weak signal to be degraded.

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[*] Corresponding author.

Table 1. Input-related performance requirements for the direct-downconversion mixer. Note that the iIP2 requirement is translated into a two-tone specification [5].

Gain	NF	$CP_{1\,dB}$	$iIP_{2,tt}$	iIP_3	$\lvert S_{11}\rvert$	$\lvert Z_0\rvert$
16 dB	<7.6 dB	>−12 dBm	>+17 dBm	>−4.7 dBm	<−10 dB	<300Ω

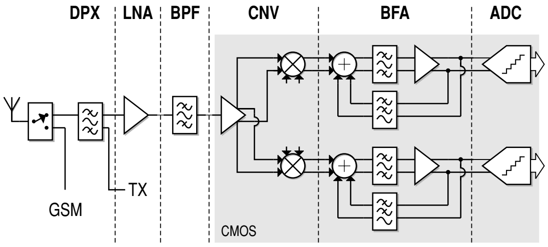

Fig. 1. System diagram of the UTRA/FDD direct-downconversion receiver. Shaded blocks are intended for CMOS implementation.

The TX leakage signal also affects the third-order non-linearity requirement of the receiver as the TX leakage causes a 67 MHz-offset blocker test to form an intermodulation test. With several tests overlapping only worst-case requirements are listed in Table 1.

2. Mixer Design

The selected mixer topology, shown in Fig. 2, is a modification of the well-known Gilbert cell mixer. The balanced structure of the Gilbert cell is desirable since it is robust and it offers good attenuation of even-order distortion components. Also, the transconductance and switching devices required in Gilbert cell mixer structures line up well with strong points of CMOS IC technology. Further, the mixer is implemented using a double-balanced structure in order to provide good LO-to-IF isolation which is particularly important in a DCR. If not attenuated the LO leakage easily dominates the mixer output voltage headroom and thereby compromises the mixer performance. To attenuate the LO signal resonant loads are often used. In a DCR this is not possible and hence the importance of LO-to-IF isolation in the mixer. To minimize the effect of LO-to-IF leakage capacitors are placed in parallel with the mixer load resistors to provide for some lowpass filtering.

As Fig. 2 shows the Gilbert cell has been modified to accommodate the quadrature signal requirement of the DCR. Instead of running two separate mixers in parallel, the quadrature capability is attained using a shared differential transconductance stage as input to the *I* and *Q* channel switching cores [6]. With this structure the transconductance stage is common to the *I* and *Q* branches, and therefore it cannot contribute to mixer imbalance. This construction has no effect on power consumption as the two branches are needed anyway. On the other hand, the structure has an increased sensitivity towards LO signal imbalance than two separate mixers. With a square-wave LO signal the transconductor current is shared between the *I* and the *Q* branch transistors as illustrated in Fig. 3. In this case transistors M3 and M6 conduct current simultaneously with transistors M7 and M10 for part of the LO cycle. If there is an amplitude imbalance in the LO signal, this is going to be reflected in the sharing

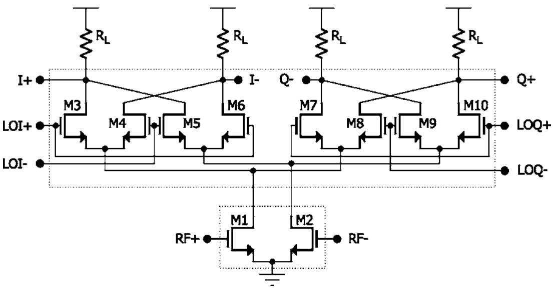

Fig. 2. Direct-downconversion I/Q mixer topology [6].

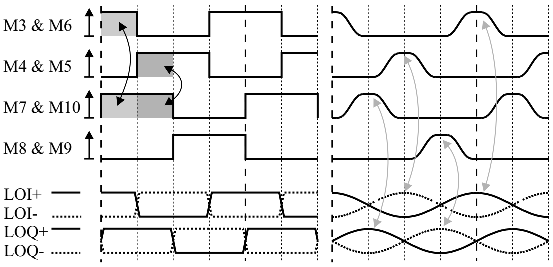

Fig. 3. Illustration of the switch transistor current with square (left) and sinusoidal (right) LO-voltages.

of the current. In this case, transistors M3 and M7 (as well as M6 and M10) are going to steal current from one another. With a sinusoidal LO signal the mixer is much less sensitive towards imbalance in the LO signals. During such LO signal conditions the transconductor current is only shared for a small part of the LO period. As a result the sensitivity towards LO amplitude mismatch is reduced. Considering this dependency on LO conditions and the penalty for using square-wave signals, the latter is not feasible. As is shown in the following section there is another advantage of having a sinusoidal LO signal.

2.1. Switching Transistors

During instantaneous square-wave switching operation conditions both mixer configurations provide for the same gain [7]. During such ideal switching conditions the noise from the core of the Gilbert mixer is negligible. This is not the case for the quadrature mixer where pairs of transistors are conducting current at any given time as Fig. 3 shows. As a result there is a low-impedance path for the switch transistor noise current to reach the output. Further, the noise from either pair of mixer core transistors is injected onto both I and Q branch outputs.

When driven by large sinusoidal LO signals neither of the two mixer configurations exhibits any significant mixer core noise. Here, the majority of the mixer noise originates from the transconductor. However, unlike in the conventional Gilbert cell $I/2$-modulators, the input transconductor noise contribution to the I- and 2-outputs is correlated. Consequently, in each branch the transconductor contributes noise only to one side band and there is a 3 dB noise advantage [7].

To minimize mixer noise figure the size of the switching transistors is optimized and a gate width of 100 μm is selected. Further, it is found that a differential LO amplitude of 1.42 V_{PP} provides for good performance.

2.2. Input Transconductance Stage

The transistor size used in the transconductance stage is determined through simulations. Here, the transconductor is modeled as a simple amplifier and subsequently optimized for noise figure, transconductance, and compression. During optimizations a load impedance equivalent to that of the switch is used. Differential source degeneration inductances are avoided as the resulting gain may be reduced.

In a DCR it is important that the input stage of the mixer provides some common-mode rejection. This is necessary for obtaining a good balance for the differential current signal entering the switching stages. Usually a differential pair is biased with a current source to fix the common-mode current and thus reject common-mode signals present at the differential input. However, the current source requires some voltage headroom which is undesirable when operating at low supply voltages. Alternatively an LC resonator may be used [8, 9] . It is found from simulation that this topology provides a common-mode rejection comparable to that of the current source approach while having the advantage of not consuming DC voltage headroom. On the downside, an LC resonator takes up considerably more die area and it also has an effect on mixer linearity due to the frequency dependent source loading of the transconductance stage. A differential pair with grounded source terminals ideally produces only second-order distortion (common-mode) while a pair based on a current source ideally results in only third-order distortion. Assuming perfect matching in switch-cores and mixer loads, the second-order distortion in the mixer therefore translates into a CMRR requirement for the following stages. As perfect matching is not possible, some second-order distortion is going to appear as differential-mode distortion as well. Which approach to choose therefore involves a trade-off between even and odd order non-linearity. The LC approach forms such a linearity trade-off in the sense that the resulting performance is somewhere in between that attainable with the grounded pair or the current source approach.

2.3. Input Balun Network

Although the interface between the BPF and the CNV is illustrated as being single-ended in Fig. 1, this need not be the case. A balanced solution may easily be obtained using an off-chip balun or a SAW BPF with a balanced output. To maintain the freedom of using either a balanced or a single-ended BPF, it is chosen to implement an on-chip balun.

It is important that the input stage is able to deliver a well-balanced AC signal to the mixer switching stage despite being driven by a single-ended source. This is particularly important for the isolation performance of the mixer. In the design of the input structure, illustrated

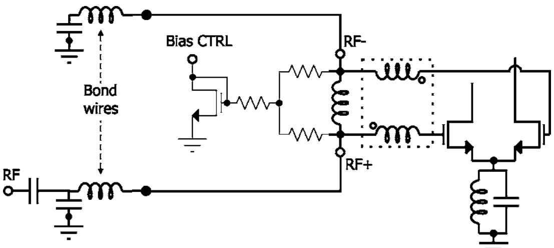

Fig. 4. Illustration of the input scheme used in the mixer implementation.

in Fig. 4, it is therefore important to ensure good balance.

An on-chip balun is designed as part of the input matching network. Being a passive structure, the balun does not produce any distortion and has a lower noise figure than that of an equivalent active balun. The balun is implemented using an octagonal on-chip coil with two separate windings (two turns each) with a symmetric layout as illustrated in Fig. 5. EM simulations are conducted using Agilent ADS/Momentum to provide an accurate simulation model. The final model, also shown in Fig. 5, is used through all the circuit simulations. The model includes inductive and capacitive coupling between the windings, lossy capacitive substrate coupling, resistive series losses, and Eddy-current loss. The model parameters are adjusted to fit the EM simulation results.

Due to a poor coupling factor in the balun (approximately 0.7) and a low Q value (app. five), a different configuration from that reported in [10] is chosen. Here, the coupling inductors are connected in series to the input gates (see Fig. 4). The coupling inductors are connected to a third inductor making up a tapped coil impedance transformer. Transformer resonance is ensured by the gate capacitance and through additional external capacitors. Both of the two inputs to the network are made available. This allows for the mixer to be tested using either balanced or single-ended signals. In the single-ended configuration an external shunt capacitor is added to the inverting input terminal. The circuit topology allows for further integration of the external capacitors. The balun is able to only partially reject the input common-mode component due to single-ended excitation. However, the quadrature mixer input stage provides further common-mode rejection yielding a sufficient balance prior to the switching core.

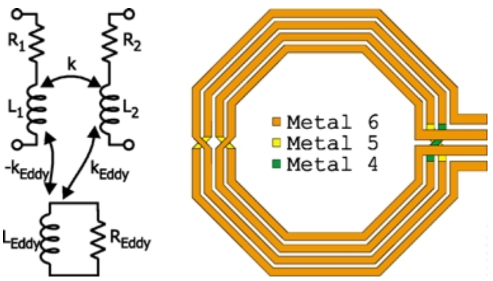

Fig. 5. The on-chip transformer simulation model (capacitive couplings not shown) and the corresponding layout.

3. Measurement Results

The final mixer circuit (see Fig. 6) is bonded directly to a PCB for testing. The phasing of the LO is generated using microstrip delay lines. For gain, noise, and IP2 measurements a TI THS4031 based differential-to-single-ended instrumentation amplifier is used. For noise figure and IP2/IP3 measurements an R&S FSIQ26 spectrum analyzer is used. Gain and 1dB compression point are measured with an oscilloscope. To ensure that the instrumentation amplifiers do not affect linearity, these are omitted from the IP3 measurement.

As a first measurement the match of the input balun is evaluated. The result, shown in Fig. 7, illustrates that

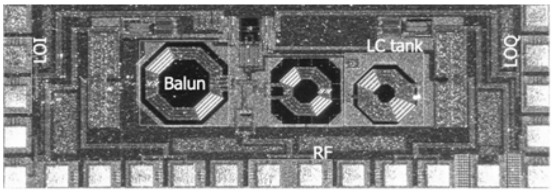

Fig. 6. Chip photo showing the direct-downconversion mixer. Including pads the design occupies 1.3 mm^2 (1.9 mm × 0.7 mm).

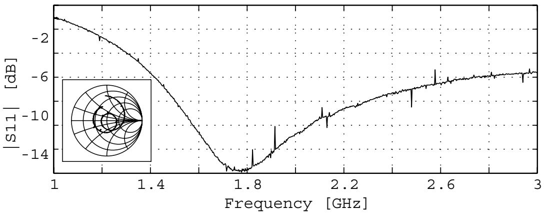

Fig. 7. Input match at the RF port. Inset picture shows the Smith chart plot of the input match.

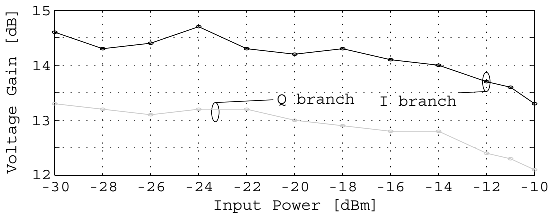

Fig. 8. Mixer conversion gain as a function of the input power level.

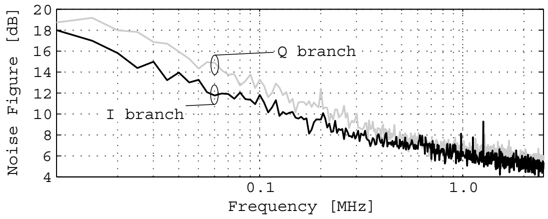

Fig. 9. I and Q channel noise measured with sinusoidal LO signals.

the match is better than -10 dB for a frequency range from 1.5 GHz to 2.3 GHz.

Conversion gain measurements (see Fig. 8) reveal a discrepancy between I and Q gain in the order of 1.0 dB. In this set-up the discrepancy remains at a constant 1 dB over the entire input power range tested. With the LO signals switched the situation is almost the same. However, here the Q branch displays the higher gain. When measured on its own the LO feed network is found to generate a gain offset between LOI and LOQ of approximately 0.7 dB—with the I-path displaying the larger gain. This offset adds directly to the discrepancy between I and Q gain in all the measurements. To evaluate the balance of the mixer the inputs for LOI and LOQ are interchanged and the resulting offset is found to be app. 0.7 dB which give an improvement of 0.3 dB. Depending on the orientation of the LO feed network, the overall change in gain offset is 1.7 dB. Consequently, the majority of the measured imbalance is caused by the poor symmetry of the LO feed. Assuming a first-order relationship, 0.3 dB of the total imbalance may be attributed to mixer imbalance.

The effect of the LO feed imbalance is also reflected in the noise measurements. As a result of the higher gain in the I branch the lowest noise power is also measured for this branch. As Fig. 9 shows, the difference is most distinct at lower frequencies where a difference of up to 3 dB is observed. At higher frequencies the difference becomes less significant. For the linearity measurements the same trend is observed as I and Q branches also perform differently here. During linearity measurements (see Fig. 10) the iIP2 is found to 26 dBm and 25 dBm for the I and Q paths respectively. For iIP3 the resulting I and Q path performance is -2.7 dBm and -3.1 dBm respectively. These linearity measurements all reflect test cases involving the TX, as they represent the worst-case scenarios.

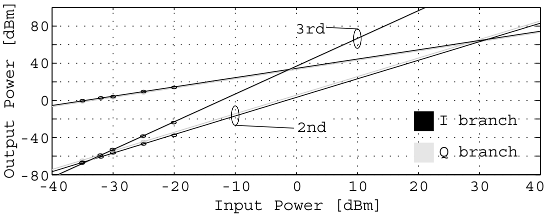

Fig. 10. Second and third-order input intercept point measurements for the mixer.

Table 2. Input-related performance specifications and measured results for the direct-downconversion mixer.

Parameter	Req.	Sim.	Meas.
Voltage gain (I/Q)	16 dB	16.3 dB	13.8 dB (14.4/13.2)
NF [10 kHz-2 MHz] (I/Q)	<7.6 dB	7.6 dB	8 dB (7.4/8.5)
1 dB CP I/Q	>-12 dBm	-10 dBm	$-11/-10$ dBm
IP2 (15 MHz offset) I/Q	–	33 dBm	31/28 dBm
IP2 (135 MHz offset) I/Q	>17 dBm	38 dBm	26/25 dBm
IP3 (10/20 MHz offset) I/Q	–	-1.3 dBm	$-0.8/-1.4$ dBm
IP3 (67/135 MHz offset) I/Q	>-4.7 dBm	-0.8 dBm	$-2.7/-3.1$ dBm
Input match $\|S_{11}\|$	<-10 dB	<-10 dB	<-10.9 dB
$\|Z_{\text{out}}\|$ (Single ended)	<300Ω	250Ω	226Ω

For completion both iIP2 and iIP3 performance are measured for some of the additional test cases. These numbers are included in Table 2 where the final simulation and measurement results are summarized. Here, the difference between I and Q gain can easily be seen to affect all measurements.

The simulated iIP2 values listed in Table 2 are based on measured mixer load resistor values as well as measured imbalance in the LO feed network. Transistor mismatch is not included in simulations since no reliable statistical information is available. For ease of measurement the iIP2 is measured with RF signals at 1 MHz and 1.3 MHz offsets from the LO.

4. Conclusions

Using a modified Gilbert cell mixer, a quadrature direct-downconversion mixer for a UTRA/FDD receiver has been designed and implemented. The mixer input matching network functions as a balun and enables the mixer to be driven with a single-ended source. In general, the measured results are in good accordance with simulations. Only the gain and especially the imbalance are found to differ from predictions. To properly evaluate the quadrature mixer it is absolutely necessary to have an accurate LO feed. With a well-balanced LO feed it is expected that I and Q gain mismatch is reduced significantly. Even with the LO imbalance corrected, an app. 2.5 dB gain deviation from simulations remains. Part of this error arises from the absolute error in load resistors whereas the extraction of layout parasitics also appears to be too optimistic. Apart from the conversion gain all measurement results comply well with the requirements.

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Measurement and Modeling of Coupling Effects of CMOS On-Chip Co-Planar Inductors

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Measurement and Modeling of Coupling Effects of CMOS On-Chip Co-Planar Inductors

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Abstract— **The coupling effects between two adjacent co-planar spiral inductors are characterized for two cases, one where no guard structure is used and one where simple guard-rings are used. In addition, the effect of guard-rings is evaluated at different distances (190μm to 1090μm) between inductors. Measuring low levels of crosstalk is difficult and in this context the effect of the test fixture itself is evaluated. Return current paths are here found to have significant influence on low frequency results. In addition, based on laser cutting of test fixtures, a surrounding ground-ring is found to increase the crosstalk level. With the effect of ground-ring coupling removed, the use of simple guard-rings is shown to improve isolation by approximately 10-15dB for closely spaced adjacent inductors. At larger distances the gain from having a guard-ring reduces and eventually reduces to zero at a distance of 1000μm. For closely spaced devices a doubling of distance is found to provide an additional 20dB attenuation of crosstalk. An extended model including mutual inductive coupling and direct capacitive coupling is shown to provide accurate fit.**

I. INTRODUCTION

Passive components are extensively used in a variety of RF applications. In particular the inductor plays an important role in tuning of narrow band amplifiers and to balance out unwanted capacitive parasitics. For silicon technologies coupling through the lossy substrate is an important part of the overall design challenge. However, coupling is not limited to substrate effects and therefore three types of coupling need to be considered; magnetic (inductive) coupling, substrate (capacitive and resistive) coupling, and coupling via ground current return paths. To limit the coupling between circuits a guard-ring is often used. By restricting the extension of the magnetic fields this generally improves isolation but it also degrades inductor performance thereby presenting a trade-off in device design. The objective of this work is to evaluate the isolation properties between two co-planar spiral inductors as a function of both distance and use of guard-ring.

II. EXPERIMENTAL SET-UP

The experimental set-up shown in Fig. 1 consists of two almost identical inductor structures implemented using a 0.25μm, 5-metal layer CMOS technology. Both inductors are based on a squared structure where metal layer 5 (M5) is used to form the coil and M4 is used for the underpass. For the transmitter inductor (TX), 4.25 turns are used while all receiving inductors (RX1 - RX4) are using 4.5 turns. The inductors are placed in two set-ups, one where all RX inductors use guard-rings and one where no guard-rings are used. Each test fixture has a M1 ground-ring surrounding the devices to provide good grounding. Further, when measured from center to center, the distance between the TX and RX structures are 190, 490, 790, and 1090μm respectively.

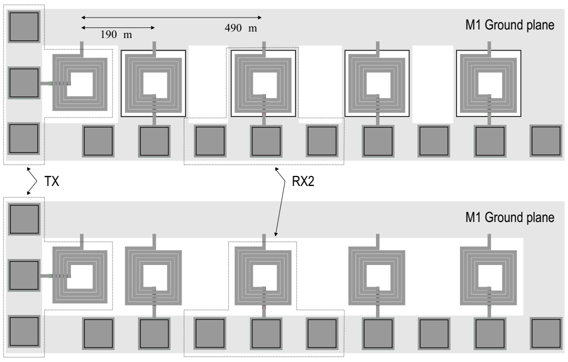

Fig. 1. Experimental set-up for measuring and simulating inductor isolation when using guard-rings (top) for RX structures and when not using guard-rings (bottom).

The s-parameters are measured using Cascade Microtech GSG probes and an HP8510C network analyzer. The structures are characterized by measuring 4 sets of 2-port s-parameters. During measurements an RF signal is fed to port 1 and the coupling is then measured by sensing on ports 2 to 5. After a frequency sweep from 45MHz to 12GHz, the sensing port is shifted to another RX device and the measurement is repeated. While the 2-port measurements are completed, the remaining ports are left floating. Measurements are subsequently de-embedded to remove effects from test structures [1].

III. SIMULATION SET-UP

To support measurements and to promote an understanding of the general coupling effects in the test structures, a 2.5D simulation model is formed using Agilent Momentum. With some limitations in geometry, this simulator is able to simulate 3D structures. A significant limitation is that inclusion of a high number of layers results in a very long simulation time. Furthermore, to limit simulation time metal layers of finite thickness must be approximated by sheets of zero thickness. To accomodate this the simulations are based on the substrate definition given in Fig. 2.

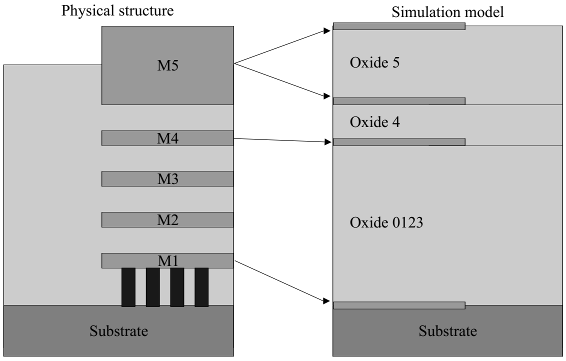

Fig. 2. Physical metal layer structure and the simplified structure use during Momentum simulations.

IV. MEASUREMENT AND SIMULATION RESULTS

The resulting measurements for structures with and without guard-rings are presented in Fig. 3. All measurements presented in Fig. 3 are illustrated using solid lines while the corresponding 2.5D simulations are presented using dashed lines.

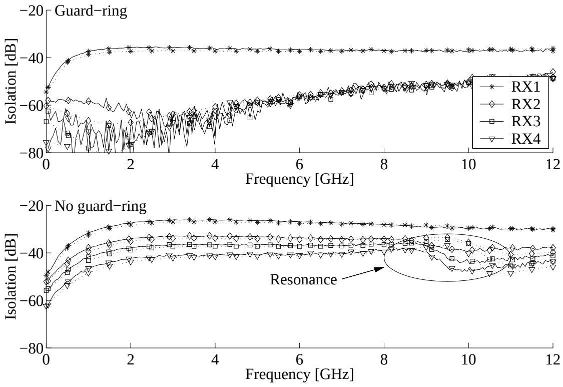

Fig. 3. Measured (solid) and simulated (dotted) isolation performance for structures with (top) and without (bottom) guard-rings.

For the structures using guard-rings the simulations are found to match measurements very accurately for most of the frequency range. At low frequencies (<2GHz) relatively large deviations are seen for structures RX2 - RX4. For these structures the isolation level is around -60 to -80dB which makes measurement a non-trivial task. Based on this a reduced accuracy is expected at high isolation levels. For structures without guard-rings the simulations are found to be equally accurate. Compared to measurements the simulations are found to be accurate to within 1.5dB. This applies for frequencies up to approximately 9GHz where a sudden drop in isolation is seen for structures RX2 - RX4. The explanation for the unexpected drop is found in the unused floating inductor structures. When left floating, the inductor is loaded by the pad capacitance. This forms a resonance circuit with a resonance frequency of approximately 9GHz. This effect is also found in the simulation results but the phenomenon is shifted up in frequency by approximately 1.6GHz in comparison to measurements. When comparing the measurements presented in Fig. 3 the use of simple guard-ring structures is found to provide for a significant improvement in isolation. Another result of having guard-rings is that the influence of the floating inductors is almost mitigated. Apart from the frequency range with very high isolation the simulations fit very well compared to measurements. To evaluate the actual effect of having a guard-ring and to evaluate the effect of distance the results from Fig. 3 are processed further. To evaluate the effect of distance the difference between the isolation measurements are plotted. By taking the difference between the RX1 and RX2 measurements in Fig. 3 the effect of moving RX1 further away from the TX inductor is found. Likewise, to evaluate the effect of having a guard-ring an RX measurement using guard-rings is compared to an equivalent one where no guard-ring is used. All these results are presented in Fig. 4.

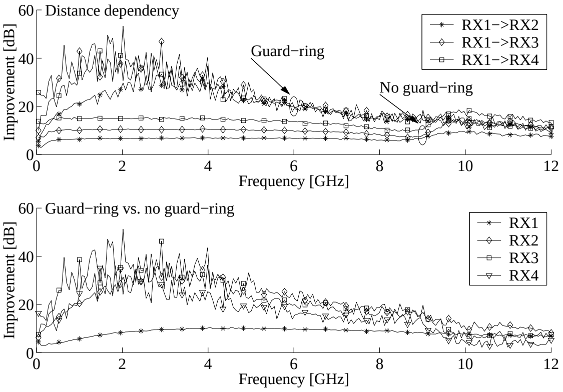

Fig. 4. Measured improvement in isolation as a function of distance (top) and use of guard-rings (bottom).

For structures with guard-rings the effect of increasing the distance between TX and RX structures from 190μm to 490μm (RX1->RX2) is an isolation improvement better than 10dB for the entire frequency range. The improvement is found to have a peak value of around 30dB for frequencies from 2 - 4GHz. As the distance increases the benefit of distance is seen to have an effect at low frequencies only. At around 2GHz the additional 300μm involved in the RX3 measurement (RX1->RX3) is seen to provide an additional 5 - 10dB in isolation. Moving to RX4 (RX1->RX4) only a minor increase in isolation compared to RX3 is observed. The effect of distance is seen to reduce significantly for frequencies higher than 4GHz. From 4 - 12GHz the performance for RX2 - RX4 are seen to be almost identical. The same trend is not observed for structures without guard-rings. Here an improvement of around 6 - 7dB is the result of moving from RX1 to RX2. For RX3 and RX4 the improvement is around 10dB and 15dB respectively. This performance appears to be independent of frequency as the only change may be attributed to the resonating unused inductors. The increase in isolation as a result of having simple guard-rings is clearly seen from the bottom graph of Fig. 4. For RX1 the improvement is fairly constant over frequency with a peak improvement of around 10dB at 4GHz. For RX2 - RX4 the improvement is found to be around 35dB at 3GHz. As the frequency is increased the gain drops down to approximately 7dB. At this point distance is found to have almost no effect on the isolation improvement resulting from the guard-ring.

V. EFFECT OF TEST-FIXTURE LAYOUT

Based on further analysis the results shown in Fig. 3 and Fig. 4 ignore an important effect resulting from inductive coupling. It can be shown that a significant part of the coupling results from coupling between TX inductor and ground-ring. The current induced in the ground-ring subsequently couples to the RX inductor, hence the overall coupling is significantly increased. This has been validated through simulations as well as measurements. To enable the latter, samples were subject to laser cutting to prevent the ground-ring current path. The aim here is to evaluate the effect of having a ground-ring surrounding the entire test structure as is the case with M1 in Fig. 1. Having good grounding is normally used in RF circuits and measurement set-ups [2]. However, for coupling measurements the layout of the ground plane turns out to be very important. The result of the laser cutting operation is illustrated in Fig. 5 where the cut marks are clearly visible.

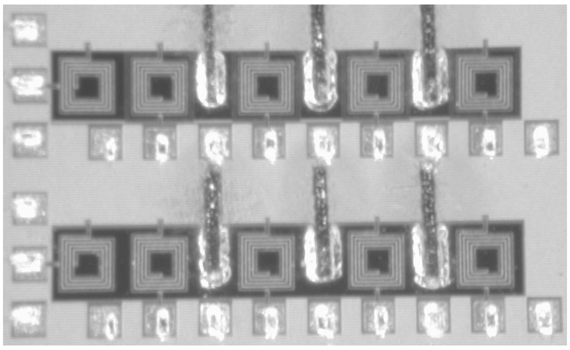

Fig. 5. Chip photo of experimental set-up after laser cutting of the fixture ground-ring.

Measurement results based on structures exposed to laser cutting are shown in Fig. 6 and Fig. 7. When comparing the results in Fig. 6 with the results presented in Fig. 3 it becomes clear that the ground-ring is responsible for a significant percentage of the coupling. For RX1 the difference is hardly noticable whether a guard-ring is used or not. For the remaining structures the change is significant, especially for structures that are not using guard-rings. Here as much as 15 to 25dB of additional coupling results, depending on distance and frequency.

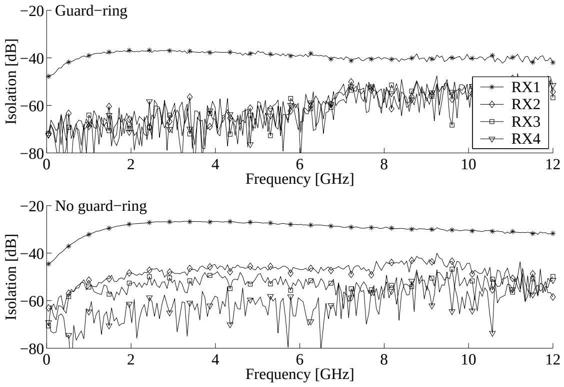

Fig. 6. Measured isolation performance for structures with (top) and without (bottom) guard-rings where the test fixture ground-ring is cut.

Since the ground-ring affects structures with and without guard-rings very differently this is also going to be reflected when evaluating the effect of using a guard-ring. The increase in isolation for the structures exposed to laser cutting is plotted in Fig. 7. Due to the low coupling levels and the resulting fluctuations in the measurements, the results in Fig. 7 have been averaged by taking the mean value for five adjacent frequency points.

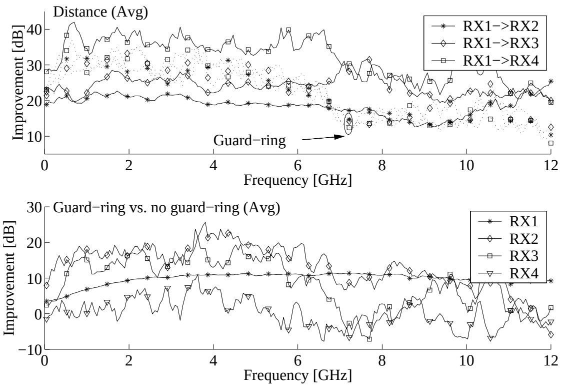

Fig. 7. Measured improvement in isolation as a function of distance (top) and use of guard-rings (bottom) where the test fixture ground-ring is cut. For the distance plot guard-ring structures use dotted lines.

Considering Fig. 4 the results indicate that the effect of a guard-ring depends on distance for frequencies up to 4GHz. At higher frequencies, distance has no significant effect on the performance of the guard-ring. From 9GHz and higher, the performance of the guard-ring drops to provide only the same performance as added distance offers. Further, it is evident that the use of guard-rings generally offer better isolation than may be obtained from having inductors placed at a greater distance. Based on the results in Fig. 7 this proves not to be the case when the ground-ring has been cut. Here the isolation performance as function of distance is found to have changed significantly. The guard-ring structures are found to provide equal performance independant of distance. A peak isolation of around 30dB is found for frequencies up to 4GHz. For structures without guard-rings an improvement of around 15 - 20dB is the result of moving from RX1 to RX2. For RX3 and RX4 the improvement is around 25dB and 30 - 40dB respectively. This is a significantly different result than for Fig. 4. The result from having simple guard-rings is seen from the bottom graph of Fig. 7. For RX1 the improvement is fairly constant over frequency with a peak improvement of around 11dB at 7GHz. For RX2 and RX3 the improvement is found to be around 15 - 20dB up to 6GHz. As the frequency is increased the gain drops down to approximately 10dB for RX2 while RX3 appears to gain almost nothing from having a guard-ring. For RX4 the guard-ring is found to have almost no effect on the isolation performance. From these results it is clear that the test fixture ground-ring contributes significantly to the coupling, especially for structures without guard-rings. As a result of this the guard-ring appears to have a significantly higher effect on isolation when the ground-ring is left intact during measurements. Depending on frequency and distance the effect of the ground-ring may be as high as 20dB.

VI. LUMPED ELEMENT COUPLING MODEL

Most often a simple model is applied to describe the crosstalk between planar inductors. To model all three proposed coupling effects the simple RC model is found to be insufficient as mutual inductive coupling is very important. The lumped element model adobted in this work is shown in Fig. 8.

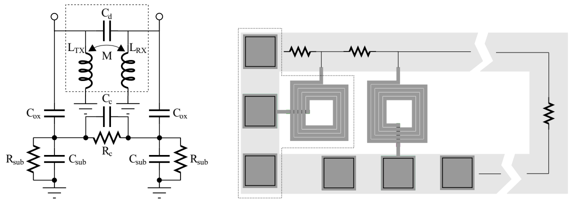

Fig. 8. Adobted lumped element coupling model (left) and essential test fixture resistances (right).

As shown previously the test fixture may have a significant impact on the results and an accurate de-embedding is therefore mandatory. To ensure that only direct coupling is included the model fit is based on the structures exposed to laser cutting. To enable a complete de-embedding procedure for this experimental set-up, 16 different structures are required. This would be very costly and the parasitics are therefore estimated manually and subsequently added to the model. Resistive parasitics in the test fixture are normally not critical since, ideally, no current flow is present in the fixture itself. Since the TX and RX inductors in this case have (in part) a common ground return path via the lossy ground-ring a cross-coupling contribution extending down to DC is formed. The current induced in the ring increases the problem due to both resistance and inductance of the ring. In this particular case three important resistive parasitics may easily be identified as shown in Fig. 8 (right). When looking at the isolation measurements in a log-scale the low frequency performance is seen to depend on these since only a few ohms drastically affect results. In Fig. 9 the optimized lumped element model is compared to measurements for the RX1 structure without guard-ring. Two sets of simulations are illustrated; one where fixture resistances have been included and one set where these parasitics have been ignored.

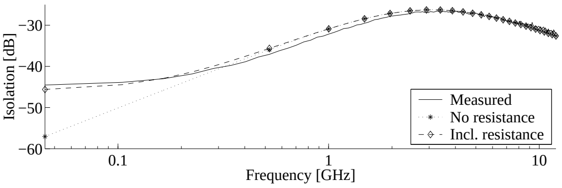

Fig. 9. Effect of test fixture resistances. The data is for RX1 without use of guard-rings.

The only difference between the two simulations in Fig. 9 is that fixture resistances of 150mΩ to 300mΩ have been included on one while they have been set equal to an ideal zero Ohms in the other.

VII. CONCLUSION

The test fixture ground-ring usually used in RF measurements is found to add to the coupling whereby the effect of a guard-ring appears to be as much as 20dB higher than it actually is. For frequencies up to 6GHz an increase in distance from 190μm to 490μm provides 30dB additional isolation for structures using guard-rings. Increasing the distance further seems to have no effect. For structures without guard-rings around 20dB additional isolation is gained by an increase in distance from 190μm to 490μm. Increasing the distance from 190μm to 1090μm is found to provide up to 35dB in additional isolation. Any practical RF design has a more or less dense ground plane covering the majority of the circuit area. Simulations using the model in Fig. 2 show that the coupling may be as low as -90dB up to 12GHz when a solid ground plane is used. Hence, for applications where inductors are not closely spaced and a ground plane seperates these, the guard-ring is not needed and a more optimum tradeoff in inductor design in terms of Q-factor may be used.

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Crosstalk Coupling Effects of CMOS Co-Planar Spiral Inductors

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Abstract— **The coupling effects between two adjacent co-planar spiral inductors are characterized in two cases, one where no guard structure is used and one where simple guard-rings are used. In addition, the effect of guard-rings is evaluated at different distances (190μm to 1090μm) between inductors. The model traditionally used to predict this crosstalk is found to be insufficient and an extended model including mutual inductive coupling and direct capacitive coupling is shown to provide accurate fit. Measuring low levels of crosstalk is difficult and in this context the effect of the test fixture itself is evaluated. Return current paths are here found to have significant influence on low frequency results. Also, based on laser cutting of test fixtures, a surrounding ground-ring is found to increase the crosstalk level. The use of simple guard-rings is shown to improve isolation by approximately 10-15dB for closely spaced adjacent inductors. At larger distances the gain from having a guard-ring reduces and eventually reduces to zero at a distance of 1000μm. For closely spaced devices a doubling of distance is found to provide an additional 20dB attenuation of crosstalk.**

I. INTRODUCTION

Passive components, such as inductors and capacitors, are extensively used in a variety of RF applications [1]. Due to the cost-reducing potential of integrated circuit design many of these applications aim at RF-IC solutions. Compared to discrete solutions, passive IC components have inferior performance and for that matter, analysis and optimizations of these components represent important tasks for integrated circuit design. Due to the dense nature of modern IC designs, circuits and components are placed very close to each other hereby providing a potential source for crosstalk. For silicon technologies the significant coupling through the lossy substrate is an important part of the overall design challenge. To limit the coupling between circuits a guard-ring is often used. Having a guard-ring closely surrounding the inductor structure improves isolation properties by restricting part of the surface carried coupling current [2]. On the other hand, the guard-ring is also expected to degrade inductor performance thereby presenting a trade-off in device design [3]. The aim of this paper is to evaluate and model the isolation properties between two co-planar spiral inductors as a function of distance both with and without the use of guard-rings. When characterizing crosstalk, very low signal powers need to be accurately measured. In these cases the test fixture becomes an important part of the measurement and therefore this paper also deals with measurement issues to ensure that correct measurements are obtained.

II. MODELING OF INDUCTOR COUPLING

When designing RFIC circuits a number of parasitic effects need to be taken into account. One way to do this is to conduct 3D simulations and extract the required information from the results. This is a useful approach for simple structures but for complicated circuits this is not an efficient solution. To provide for simple and fast simulation approaches it is therefore necessary to develop crosstalk models that may be used in circuit simulations. To evaluate the crosstalk between two planar inductor structures the simple substrate model shown in Figure 1 is often used. In this model the coupling is assumed to result from only substrate carried effects. Part of the inductor current couples to the substrate via C_{ox} where it appears as a surface current. This surface current eventually couples partly to another inductor. To model the level of coupling an RC path ($R_c||C_c$) is included as Figure 1 shows.

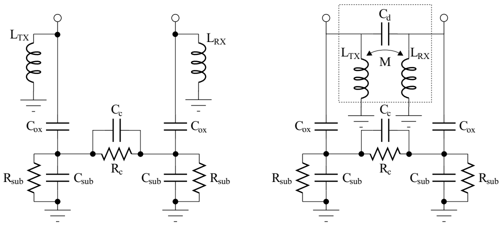

Fig. 1. Lumped element equivalent circuits desribing the crosstalk between two devices; Simple model (left) and extended model (right).

This model is found to be insufficient and to overcome this a more accurate description of the crosstalk is needed. To accomplish this four types of coupling effects need consideration; i) substrate coupling (capacitive and resistive), ii) magnetic (inductive) coupling, iii) direct capacitice coupling, and iv) coupling effects resulting from ground current return paths. The simple model already provides an equivalent for the substrate coupling. By adding a capacitor (C_d) and mutual coupled inductors (L_1 and L_2) to this simple model additionally two sources of crosstalk are included and the more accurate model shown in Figure 1 results. The effect from ground current paths is more difficult to predict and therefore it has been left out of model.

III. EXPERIMENTAL SET-UP

The inductor structures are implemented using a 0.25μm, 5-metal layer CMOS technology. The thickness of metal layers 1-4 and 5 is 6kA and 20kA respectively. Two almost identical inductors form the basis for the coupling measurements. Both inductors are based on a squared spiral structure where metal layer 5 (M5) is used to form the coil and M4 is used for the underpass. For the transmitter inductor (TX) 4.25 turns are used while all receiving inductors (RX1-RX4) are using 4.5 turns. The inductors are placed in two set-ups, one where each RX inductor uses a guard-ring and another set-up where no guard-rings are used. The guard-rings are implemented as simple loops of substrate contacts connected to ground (M1). Both of the set-ups are shown in Figure 2.

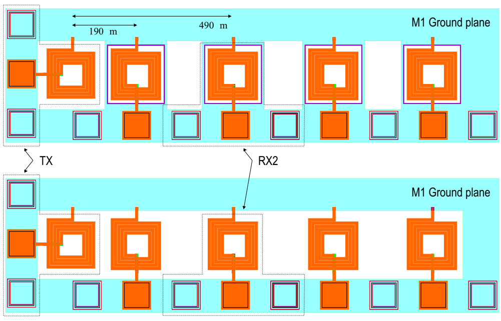

Fig. 2. Experimental set-up for measuring and simulating inductor isolation when using guard-rings (top) for RX structures and when not using guard-rings (bottom).

All inductors are placed in a single-ended configuration with the TX inductor defined as port 1 while the RX inductors are defined as ports 2 to 5. When measured from center to center, the distance between the TX and RX structures are 190, 490, 790, and 1090μm respectively. The s-parameters are measured using Cascade Microtech GSG probes and an HP8510C network analyzer. The structures are characterized by measuring 4 sets of 2-port s-parameters. During measurements an RF signal is fed to port 1 and the coupling is then measured by sensing on ports 2 to 5. After a frequency sweep from 45MHz to 12GHz, the sensing port is shifted to another RX device and the measurement is then repeated. While the 2-port measurements are done, the remaining ports are left floating. The raw s-parameters are subsequently de-embedded to remove effects from the actual test structures [4].

A. Simulation Set-Up

To promote an understanding of the general coupling effects the 2.5D EM-simulator Agilent ADS/Momentum is used. With some limitations in geometry, this simulator is able to simulate 3D structures. The physical structure and the structure used during simulations are illustrated in Figure 3.

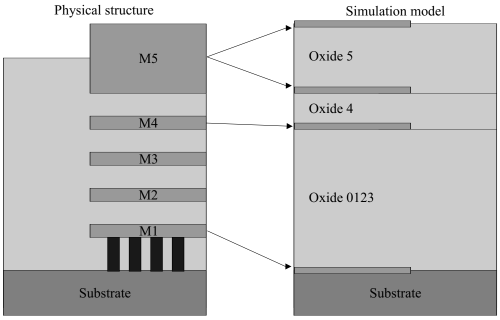

Fig. 3. Physical metal layer structure and the simplified structure used during simulations.

In the simulation model M5 is represented by two sheets of metal to improve simulation accuracy. The two sheets each have twice the resistance of the actual metal 5 and are subsequently connected in parallel by vias. For metal 4 a single sheet is assumed to be sufficient. Metal 1 is used as guard-ring in the physical structures and this layer is connected to the substrate by a vast number of contacts. A detailed modeling of this would result in unacceptable simulation time and a single sheet is therefore placed directly on top of the substrate. By doing so the guard-ring is positioned slightly lower in the modeling than in the physical structure but since the displacement is small compared to the distance between windings and guard-ring, this effect is expected to be insignificant. The output of the simulation is a 5-port s-parameter matrix. This matrix is subsequently reduced to 4 sets of 2-port s-parameters by loading the unused ports with a 60fF capacitance to ground. This corresponds to the capacitive load of the used probe pads.

B. Evaluation of Test Fixture Effects

Providing for a good signal ground is normally essential for RF circuits and RF measurement set-ups. It is especially important for device characterization purposes as it provides for well-defined parasitics whereby the de-embedding is simplified [5]. This approach is generally accepted and is used for many characterization purposes including crosstalk evaluation [6]. When analyzed coupling measurements are found to represent a special case. A careful ground layout is here even more important and the actual test fixture is therefore analyzed further. Looking at Figure 2 the basic test fixture may be viewed as consisting of three inductors; the transmit inductor, the receive inductor, and a single turn inductor surrounding both the TX and the RX inductor. Using this approach it is assumed that the measured crosstalk may consist of two components; the direct device-to-device coupling and a parasitic coupling component resulting from the ground ring. To estimate the effect of the ground ring a number of Momentum simulations are carried out to produce the results presented in Figure 4.
For this particular example the surrounding ground-ring is seen to increase coupling by more than 20dB depending on the distance between the inductors. The effect is most significant

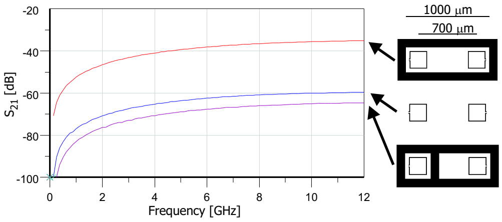

Fig. 4. Simulations of test fixture ground-ring using a simplified substrate structure.

at larger distances as the direct coupling here is reduced. In this case the TX coil leaks to the ground-ring, which in turn induces a current in the RX coil whereby the total coupling is increased. This clearly demonstrates that coupling measurements are very sensitive to the test fixture layout. To mitigate this false coupling from the measurements a few chip samples were subject to laser cutting to break the ground ring. A chip photo of the chip after being laser cut is shown in Figure 5.

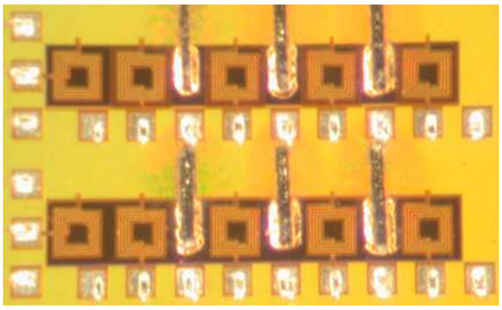

Fig. 5. Chip photo of experimental set-up after laser cutting of the test fixture ground ring.

IV. RESULTS

To evaluate the effects of both distance, the use of a guard-ring, and the ground ring, all combinations of TX-RX inductors are measured. The resulting measurements based on the structures from Figure 2 are presented in Figure 6. For all the structures simulations are found to provide an accurate fit to measurements. Overall simulations are within 1.5dB of measurements. Around 8.6GHz a sudden drop in isolation is seen. The drop is visible in all the measurements but it is most significant for structures RX2-RX4.

The explanation for the unexpected drop is found in the unused floating inductor structures. When left floating, the inductor is loaded by the pad capacitance. This forms a resonance circuit with a resonance frequency of approximately 9GHz. With a small upwards shift in frequency this effect is also found in the simulation results. When looking at the structures using the simple guard-ring, a significant improvement in isolation is found. Another result of having guard-rings is that the influence of the floating inductors is almost mitigated. At frequencies less than 2GHz the coupled power is very low for structures using guard-rings. In this case measurement uncertainty begins to influence measurements and the simulations are also seen to provide a less accurate fit in this range. The measurements based on the structures from Figure 5 are presented in Figure 7.

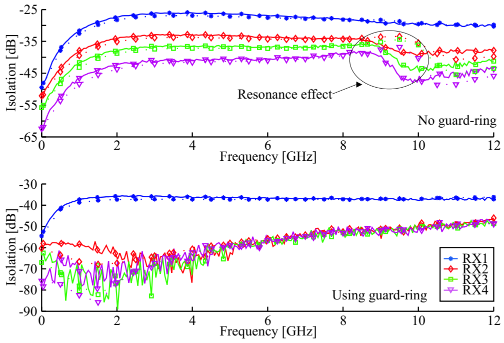

Fig. 6. Measured (solid) and simulated (dashed) isolation performance for structures with (bottom) and without (top) guard-rings. Results are based on a solid ground ring.

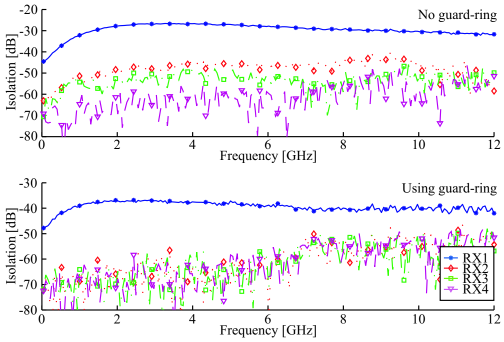

Fig. 7. Measured isolation performance for structures with (bottom) and without (top) guard-rings. Results are based on a cut ground ring.

Comparing the results presented in Figures 6 and 7 clearly reveal the effect of the surrounding ground ring. The difference between the two situations is presented in Figure 8.

From Figure 8 the surrounding ground ring is found to have only a minor effect on the isolation performance for the structures using guard-rings. When the structures without guard-ring are considered, the ring is found to have a significant impact on the resulting crosstalk measurement. The difference is seen to be as high as 20dB with 10dB to 15dB being an average for frequencies up to approximately 8GHz. If neglected this effect is clearly going to influence the outcome of a performance evaluation of the guard-ring. The crosstalk reduction resulting from the use of a guard-ring is going to appear much larger than it is. Based on these results the isolation performance presented in Figure 7 is chosen as basis for the development of a lumped element equivalent coupling model. The model parameter is fitted to the measurements and

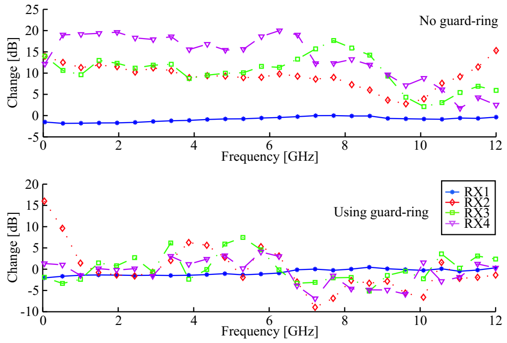

Fig. 8. Measured increase in isolation performance due to laser cut of ground ring with (bottom) and without (top) guard-rings.

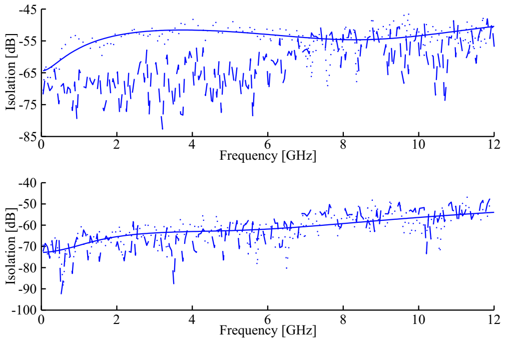

Fig. 10. Isolation performance for RX3 (top) and RX4 (bottom). Results are for structures without guard-ring (dotted), with guard-ring (dashed), and prediction based on lumped component model (solid).

the resulting performance of the developed model is shown in Figures 9 and 10 together with measurement for both structures with and without the use of guard-rings. From these results the model is seen to fit measured data very nicely which speaks in favour of the extended model.

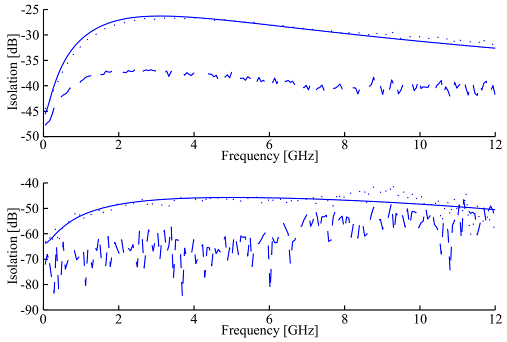

Fig. 9. Isolation performance for RX1 (top) and RX2 (bottom). Results are for structures without guard-ring (dotted), with guard-ring (dashed), and prediction based on lumped component model (solid).

Figures 9 and 10 also reveal the effect of using guard-rings. From Figure 9 the guard-ring is found to provide an almost constant 10-12dB of crosstalk attenuation over the entire frequency range for RX1. When the distance is increased by a factor 2.5 (RX2), the guard-ring is found to have a reduced effect from 7GHz and above. Below this frequency the attenuation is around 10-15dB while it is reduced to less than 5dB for higher frequencies. Furthermore, by comparing the results for RX1 and RX2 distance is found to play an important role. For closely spaced inductors a doubling (factor 2.5) of the distance is found to decrease crosstalk by more than 20dB depending on frequency. Looking at Figure 10 the guard-ring is seen have an attenuation around 10dB for frequencies up to 7GHz for RX3. At higher frequencies the guard-ring is found to provide no attenuation on average. For RX4 the distance is increased even further and here the guard-ring is found to have practically no effect.

V. CONCLUSION

Different coupling effects for CMOS on-chip co-planar spiral inductors are presented. An extended lumped element model is used for the modeling of crosstalk between inductors. Based on simulations and measurements the test fixture is shown to have a significant impact on coupling measurements. Taking the test fixture into account, the suggested model is found to fit very well with measurements. Further, simple guard-rings are shown to improve isolation between closely spaced adjacent inductors by approximately 10-15dB. At larger distances the gain of having a guard-ring reduces and is eventually found to be zero at a distance of 1000μm. For closely spaced devices a doubling of distance is found to provide an additional 20dB attenuation of crosstalk. Finally, 3D simulation proves to be a helpful tool in characterizing and understanding coupling effects in complicated test set-ups.

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