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Analysis of linear Phase-Locked Loops in Grid-Connected Power Converters

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Keywords

≪Converter control≫, ≪Non-linear control≫, ≪Alternative energy≫, ≪Fault ride-through≫, ≪Vector control≫

Abstract

Fast and accurate synchronization capability of grid-connected converters is becoming more and more important to ensure proper performance during transient events, such as grid faults. The higher requirements during the operation, as Fault-Ride-Through with reactive current injection, cause higher requirements on the operation during severe system conditions. This paper analyzes an addition to Synchronous-Reference-Frame Phase-Locked Loops for power electronic converters, that is linearizing the input signal. This enhances the tracking capabilities during abnormal transient events in the power grid. The improved control is analyzed and its increased performance is validated through simulations and experimental results.

Introduction

Due to the high penetration of renewables into the power system, Transmission System Operators (TSOs) have issued grid codes requiring e.g. wind farms to stay connected during fault events and perform voltage support through reactive current injection [1]. However, a fast inner current loop in a vector controlled converter is not alone responsible for such behavior, since its performance is also determined by the synchronization unit of the converter (as shown in Fig. 1), which is often a Synchronous-Reference-Frame Phase-Locked-Loop (SRF-PLL) [2, 3].

Extensive studies have been conducted for the SRF-PLL to investigate its influence on controller performance and on the converter stability [4, 5]. This investigation uses the small signal model of the control to verify the performance and stability. This model linearizes the SRF-PLL during low error values during steady-state operation. But the control, used in the converters is non-linear. This paper analyzes a linear SRF-PLL, that has been recently proposed for the usage in grid connected power electronic converters [6], which linearizes the control behavior. A linear SRF-PLL allows a reliable synchronization in all different phases of the operation, not only in the steady-state, but also during abnormal grid events, such as faults or during fault recovery. The time to synchronize during transient events is analyzed with

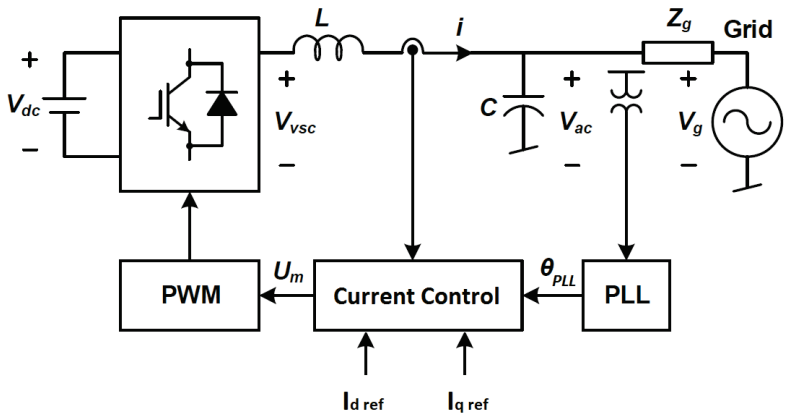


Fig. 1. Power Converter Scheme with Control Structure.

simulations and verified with experimental results. It is also determined, if this control change has to be taken into account in the converter stability analysis methods, such as the impedance-based approach [7].

SRF-PLL

The SRF-PLL is a well established control algorithm which is used to estimate the phase angle θ_G of the grid voltage vector. If the current control is done with a stationary reference frame, then the angle is used to construct a desired current reference value in a grid connected power converter. When the current control is done in a rotating reference frame, then the measured and reference currents are calculated with the estimated grid angle and are then controlled to maintain the converter output currents at the desired operating point.

The synchronization is done, by controlling the q-axis voltage component V_q in the Synchronous-Reference-Frame to zero, as shown in Fig. 2.

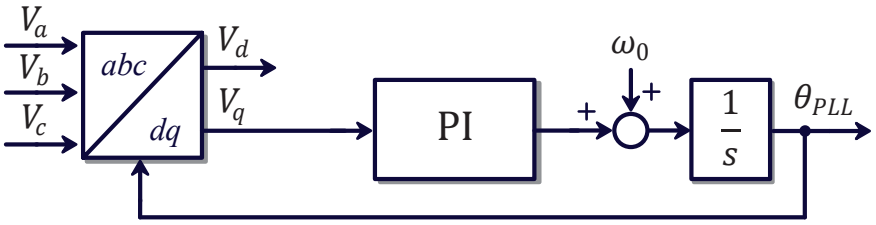


Fig. 2. Control Structure of a SRF-PLL.

Any deviation in V_q from zero is corrected by the proportional-integral (PI) controller by adjusting the internal frequency value, which is then integrated in order to obtain the synchronous angle θ_{PLL}. To get V_q, the Clark transformation is first used to calculate the grid voltage in the stationary reference frame.

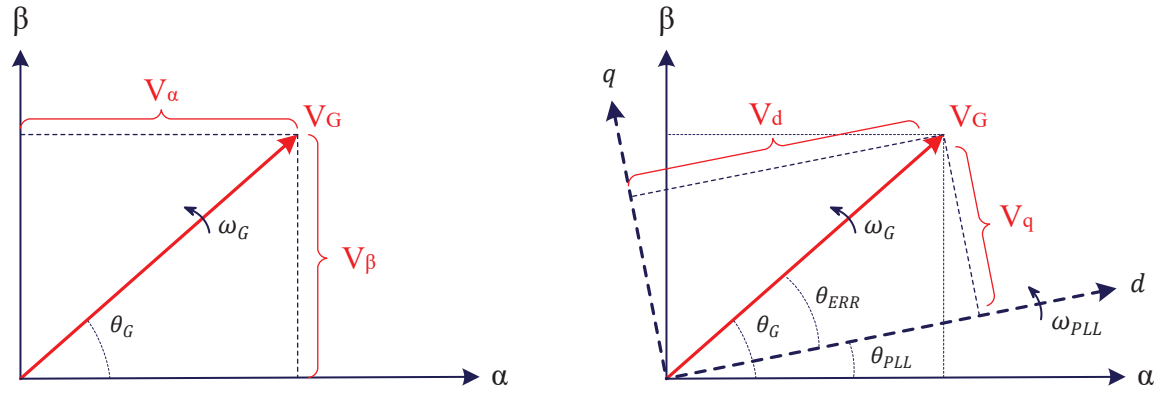
$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{1}$$

This is illustrated in the vector diagram in Fig. 3(a).

The angle of the grid voltage vector is represented with (2).

$$\tan(\theta_G) = \frac{V_\beta}{V_\alpha} \tag{2}$$

A positive sequence filter can be used afterwards for better performance during unbalanced conditions,



(a) Grid Voltage in the Stationary Reference Frame.

(b) Grid Voltage in the Synchronous-Reference-Frame.

Fig. 3. Grid voltage Vector Diagrams in the different Reference Frames.

which is not analyzed in this paper, because only balanced voltages are considered. For the SRF-PLL, the Park-Transformation with an estimated grid voltage angle θ_{PLL} is done, as it is given by (3).

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos(\theta_{PLL}) & \sin(\theta_{PLL}) \\ -\sin(\theta_{PLL}) & \cos(\theta_{PLL}) \end{bmatrix} \cdot \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{3}$$

Solving this results in the voltage components in the synchronous reference frame. This is illustrated in the vector diagram in Fig. 3(b) and also shown in (4) and (5).

$$V_d = |V_G| \cdot \cos(\theta_G - \theta_{PLL}) \tag{4}$$

$$V_q = |V_G| \cdot \sin(\theta_G - \theta_{PLL}) \tag{5}$$

Analysis of SRF-PLL

As shown in (5), V_q is dependent on the voltage magnitude and on the angle deviation. To compensate the dependancy on the voltage magnitude, V_q can be normalized with the measured voltage magnitude to only rely on the phase difference [8]. For the small signal analysis, it is assumed that the angle difference is small, which simplifies (5) to a direct representation of the angle error.

$$V_q \approx \theta_G - \theta_{PLL} = \theta_{ERR} \tag{6}$$

The open loop transfer function of the SRF-PLL is then

$$G_{ol}(s) = \left(K_p + K_i \cdot \frac{1}{s}\right) \cdot \frac{1}{s} \tag{7}$$

The closed-loop transfer function of the SRF-PLL can be developed as

$$G_{cl}(s) = \frac{G_{ol}(s)}{1 + G_{ol}(s)} = \frac{K_p s + K_i}{s^2 + K_p s + K_i} \tag{8}$$

This (second order) closed loop transfer function can be tuned by changing the control parameters K_p and K_i. The parameters are typically chosen with respect to the inner current control in such a way, that the synchronization bandwidth is much smaller than the current controller bandwidth to avoid instabilities and with a sufficient damping coefficient.

Non-Linearity of SRF-PLL

Notably, the above mentioned small signal simplification is only valid if the angle deviation is within the linear range. This non-linearity of the SRF-PLL can be best visualized with some examples. When the

angle difference doubles, V_q, as the input signal to the proportional-integral (PI) controller is not directly doubled. This is shown in (9), where the error angle signal is doubled from 45° to 90°, but $\sin(\theta_{ERR})$, is only multiplied with the square root of two.

$$\sin(\theta_{ERR}) = \begin{cases} \frac{\sqrt{2}}{2} \approx 0.707 & ,\theta_{ERR} = 45^\circ \\ 1 & ,\theta_{ERR} = 90^\circ \end{cases} \tag{9}$$

Further, the SRF-PLL can not appropriately track the grid voltage phase when the angle difference value exceeds 90°. An example of this behavior is given in (10). Here, the same value is used as controller input, with the error angles of 45° as well as 135°.

$$\sin(\theta_{ERR}) = \begin{cases} \frac{\sqrt{2}}{2} & ,\theta_{ERR} = 45^\circ \\ \frac{\sqrt{2}}{2} & ,\theta_{ERR} = 135^\circ \end{cases} \tag{10}$$

This behavior can also be seen in Fig. 4. The figure shows the positive angle range, hence the mathematical representation can be used for positive as well as negative inputs. It shows a comparison between the error angle value and the sinus of the angle difference value, represented by V_q.

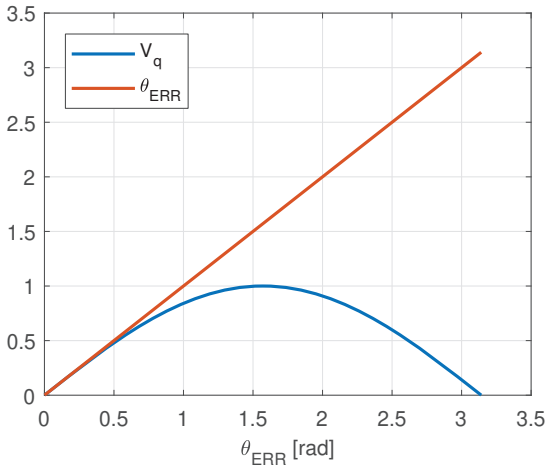


Fig. 4. Comparison of V_q and the voltage phase angle error.

The figure proves the correct simplification for low angle difference values (up to ca. 0.5 rad). In this condition both lines match up with each other, thus there is no difference in the control behavior, no matter which signal is used. Nevertheless, when the linear region is left, the error signal that is processed in a SRF-PLL (the normalized V_q) is smaller than in a linear system. This implies a slower response of the control system for high angle difference values than originally set with the control parameters.

Linear PLL

Linear phase-locked-loops are well established techniques in communication systems [9]. Lately, they have also been proposed for converter controls to enhance the performance of the synchronization [10]. This is done by calculating the angle difference as the control input, instead of the sinusoidal value of it. The angle difference can be calculated with a combination of V_q and V_d as described in (11).

$$\frac{V_q}{V_d} = \frac{|V_G| \cdot \sin(\theta_G - \theta_{PLL})}{|V_G| \cdot \cos(\theta_G - \theta_{PLL})} = \tan(\theta_G - \theta_{PLL}) \tag{11}$$

The phase angle difference is then calculated with the inverse tangent function. This can also be concluded from Fig. 3(b).

$$\theta_{ERR} = \theta_G - \theta_{PLL} = \tan^{-1}\left(\frac{V_q}{V_d}\right) \tag{12}$$

The signs of V_d and V_q can be used to determine the exact value of the angle error. It has also been proposed to control angle errors higher than 180° by comparing the error angle from the current and the last computational cycle [6]. The SRF-PLL control scheme can now be redrawn with the linearization as shown in Fig. 5.

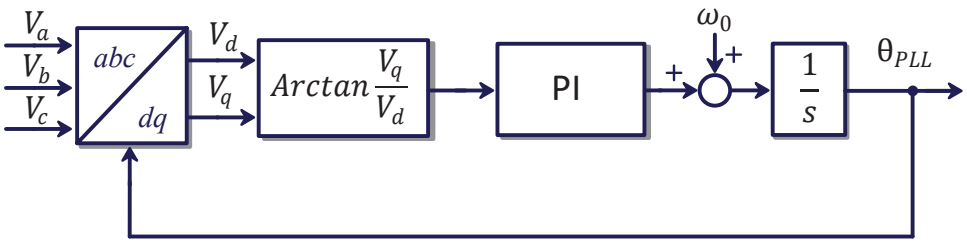


Fig. 5. Control Structure of a linear SRF-PLL.

This linear SRF-PLL is able to control angle deviations with the same response time, no matter how high the magnitude of the error signal is.

Stability Analysis with linear SRF-PLL

The open-loop and the closed-loop transfer functions are still the same as described above in (7) and (8), as the controller is behaving as before with the small-angle simplification now being implicit in the model. The linearization has not included any filtering or delay to the system behavior. To analyze the converter stability one can use the impedance based approach [7]. There, the SRF-PLL transfer function is determined with

$$\Delta\theta = \Delta V_q \cdot G_{cl}(s) \tag{13}$$

With G_{cl} being the closed-loop transfer function of the SRF-PLL. In order to determine the small signal model for the linear SRF-PLL, the following approximation is used.

$$\Delta\theta = \tan^{-1}\left(\frac{V_q}{V_d}\right) \approx \frac{V_q}{V_d} = \frac{\Delta V_q + V_{1q}}{\Delta V_d + V_{1d}} \tag{14}$$

The steady-state value V_{1q} is assumed to be zero. With this, the equation for a small signal deviation is rewritten to

$$\Delta\theta = \frac{\Delta V_q}{V_{1d} + \Delta V_d} \cdot G_{cl}(s) \tag{15}$$

This means, the ratio between the small signal changes in ΔV_q and the steady state voltage V_{1d} are mainly influencing the control behavior. ΔV_d is ignored for the further stability analysis, because it is rather small, compared to the steady state voltage V_{1d}. The control change is therefore not influencing the small signal behavior and the well-known analysis for controller stability is still valid.

Simulations

In the simulations, various phase jumps with different amplitudes are simulated and the time to control the error angle back to a certain threshold is compared. Phase jumps in the grid voltage mainly occur during grid faults, especially with reactive power injection [11]. The phase change is affected by the fault location and the system impedance. The angle steps that are performed in the simulations are performed

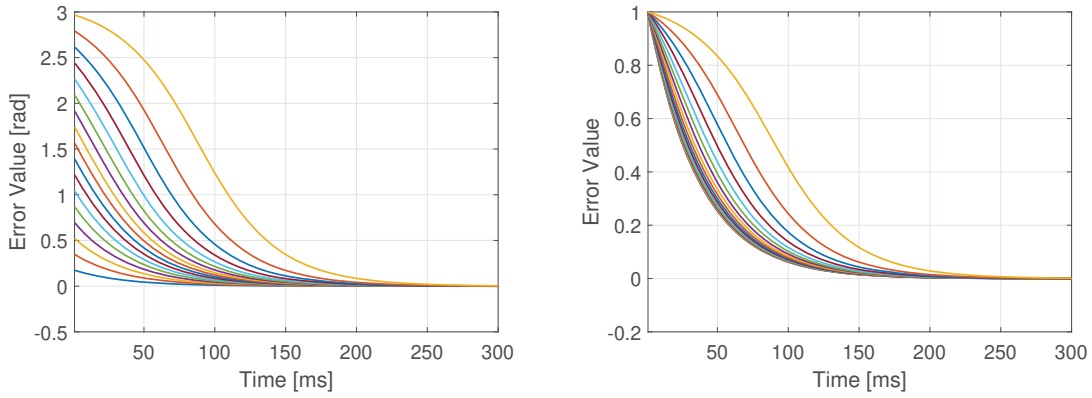
from 10° to 170° in 10° steps. The parameters for the simulation of the SRF-PLL are given in Table I.

Table I
SRF-PLL Control Parameters

K_p	36
K_i	5
nominal Grid frequency	50 Hz

Simulation of SRF-PLL

First, the standard control with V_q as the PI-controller input is analyzed. Afterwards, the linear SRF-PLL is tested to verify the control performance changes.



(a) Phase angle difference between θ_G and θ_{PLL} after applying Steps in the Grid Voltage Phase from 10° to 170° with SRF-PLL.

(b) Normalized Phase angle difference to compare the Control Performance.

Fig. 6. Simulation results of Phase Tracking Performance with SRF-PLL.

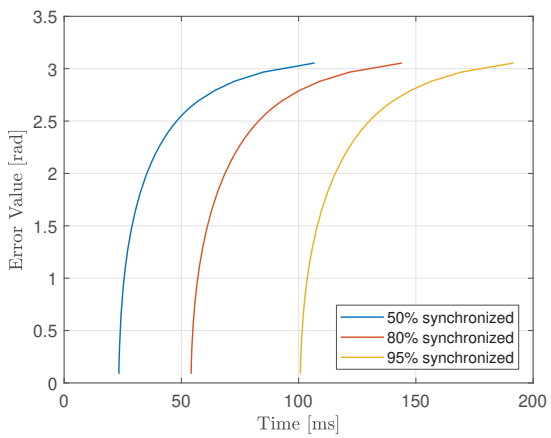
Fig. 6 shows the simulation results of symmetrical grid voltage phase jumps. The reduction of the error signal is performed by the PI controller. At low initial angle deviations, the error signal is reduced in a nearly exponentially decreasing curve. But high initial phase jump magnitudes in the grid voltage cause a flat curve, meaning a slower response, at the beginning of the synchronization. This causes a longer time to synchronize after a phase disturbance.

To better illustrate the dynamic performance, the results are also shown normalized with the applied initial grid voltage phase angle step in Fig. 6(b). With low starting deviations, the control is synchronized in ca. 100 ms. Higher starting values cause, that this time increases up to approximately 200 ms. This behavior is also verified with different control parameters.

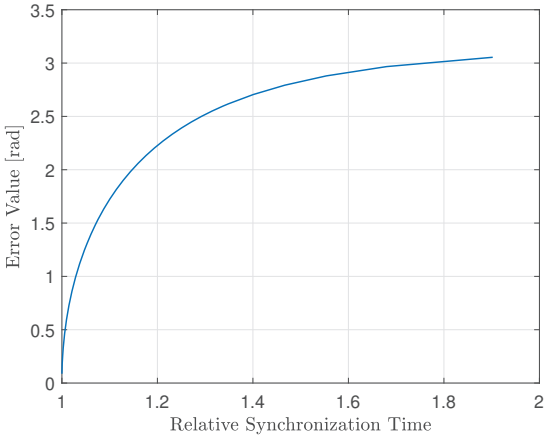
The delay in the synchronization is further analyzed in Fig. 7(a). The graphs show the time until the error angle has been reduced by 50 %, 80 % and 95 % by the PI controller. This is done in order to evaluate, how much time the synchronization takes (rise time to remaining 5 % error signal of the initial error angle).

This illustrates how much and when the delay happens. The delay is already taking place in the first 50 % of the synchronization process. After this returned the angle value back to the linear range. The time to control 50 % of the error value changes from 25 ms to 100 ms, so the time increase is approximately 75 ms. The time to be synchronized 95 % increases approximately 85 ms from 100 ms to 185 ms. Different controller parameters will change these times, but the time delay is proportional to the presented results.

Therefore, the synchronization time is set into relation to the fastest rise time in Fig. 7(b). This illustrates the increased time compared with the expected synchronization, defined by the control parameters. One



(a) Time to Synchronize to a certain degree.



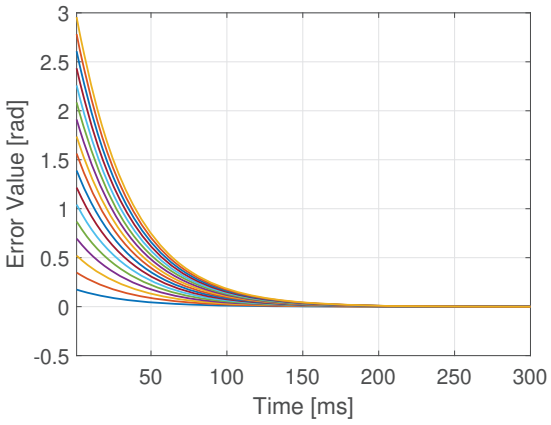
(b) Proportional Time Duration Increase due to non-linearity.

Fig. 7. Analysis of increased Synchronization time.

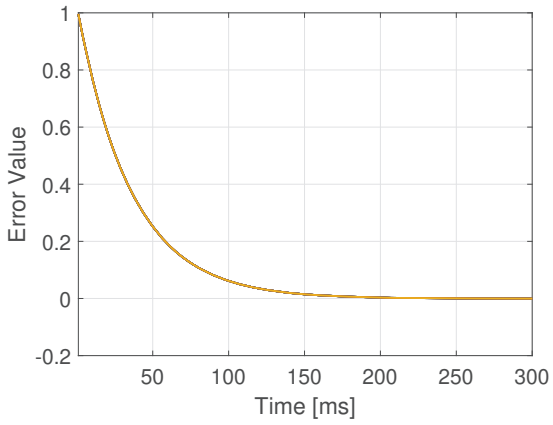
can see that the time to synchronize is increased less than 10 % below an initial angle error value of 90°. The time to synchronize 170° is almost doubled. This means that the current control can fulfill its purpose for this longer time. This increased synchronization time, presented in Fig. 7(b) is valid for other control parameters, hence the delay comes from the controller input reduction.

Simulation of linear SRF-PLL

Now, the control has been extended with the linearization block as shown in Fig. 5. The simulation results with the linear SRF-PLL are shown in Fig. 8.



(a) Phase angle difference between θ_G and θ_{PLL} after applying Steps in the Grid Voltage Phase from 10° to 170° with linear SRF-PLL.



(b) Normalized Simulation Results to compare the Control Performance.

Fig. 8. Simulation results of Phase Tracking Performance with linear SRF-PLL.

Fig. 8(a) shows the error signal in the control loop to verify the behavior due to the different grid voltage phase jumps. These graphs also shown normalized with respect to the applied step size in Fig. 8(b). With the linear SRF-PLL it can be seen, that the rise time is constant, hence all lines are on top of each other in this graph. There is no impact of the different starting error angle values. This illustrates the enhanced control performance, without any severe drawbacks. The linearization can be computed fast and with only a minor impact on the controller complexity.

Experiment

The experiments to verify the control behavior with and without linearization are shown in this section. A grid simulator is used to produce the three-phase grid voltages. The parameters are the same as in Table I. The currents and grid voltages during a grid voltage phase jump of 90° are shown in Fig. 9.

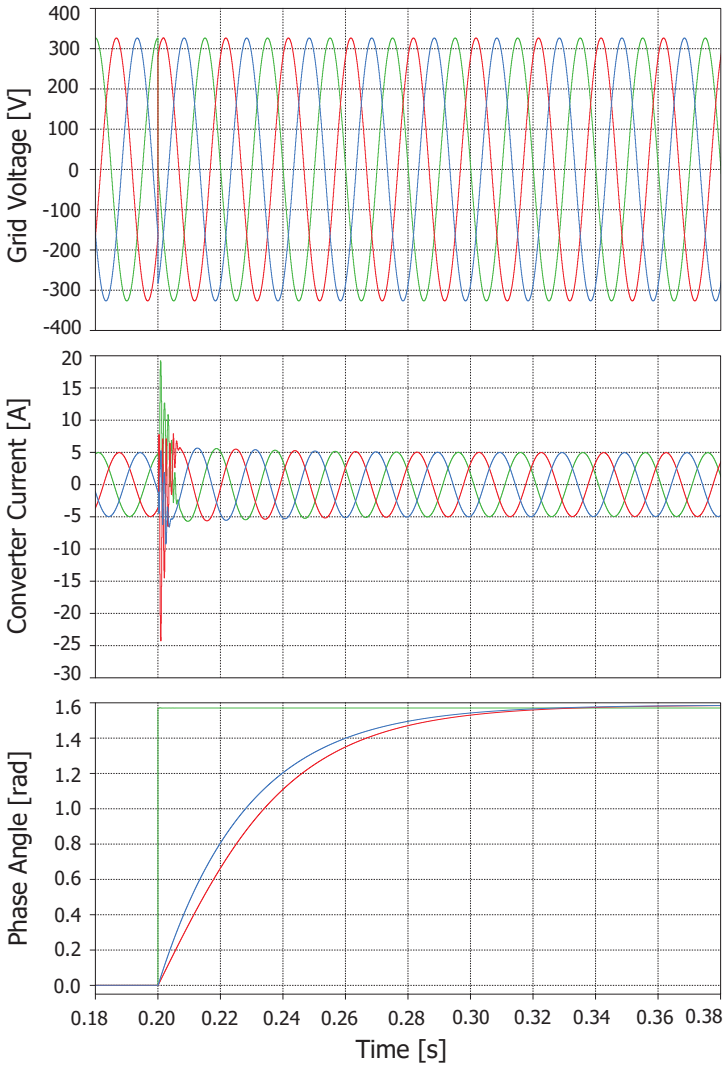
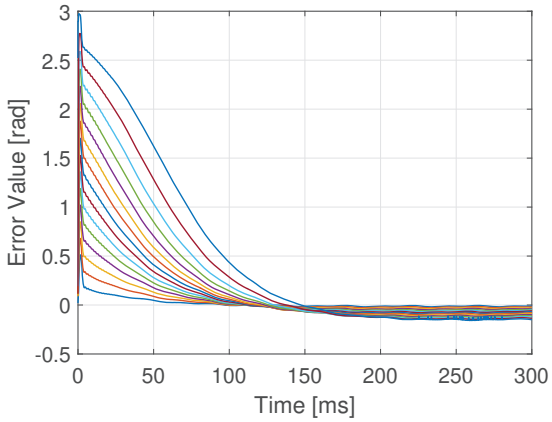


Fig. 9. Measurement during a phase jump of 90° at 0.2 sec.
Upper Graph: Grid Voltage [V].
Middle Graph: Converter Output Currents [A].
Lower Graph: Phase jump (Green), Phase tracking with SRF-PLL (RED) and linear SRF-PLL (BLUE).

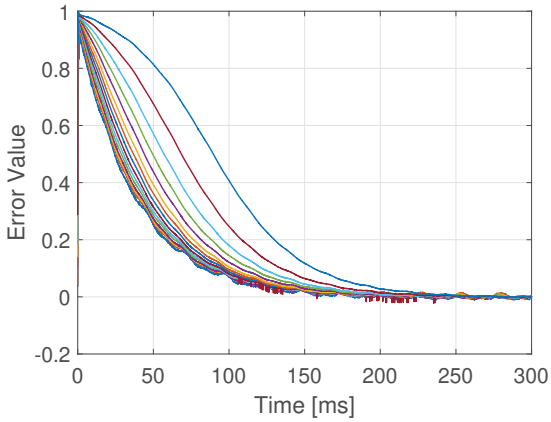
The experimental results for the different phase jumps are shown in Fig. 10. The phase error signal with different grid phase voltage jumps is shown in Fig. 10(a) and the same signals are normalized in Fig. 10(b).

These results verify the increased time to a synchronization with the usage of a conventional SRF-PLL. Small oscillations occur due to a small imbalance in the grid voltages. This can be avoided with positive sequence filters, which would add an additional control delay. Therefore, this has not been done in this comparison to achieve the same dynamics as in the simulations. The value of V_q in the SRF-PLL during the experiment is shown in Fig. 11. The lower values of V_q at higher error angles, as the PI controller input, cause the slow controller response at the beginning of the synchronization.

A linear SRF-PLL can calculate the angle difference, not only relying on this V_q signal. This has been validated with experiments.



(a) Phase angle difference between θ_G and θ_{PLL} after applying Steps in the Grid Voltage Phase from 10° to 170° with SRF-PLL.



(b) Normalized Experimental Results to compare the Control Performance.

Fig. 10. Experimental results of Phase Tracking Performance with SRF-PLL.

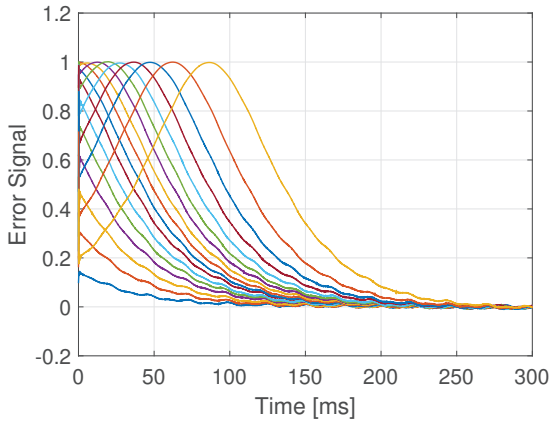
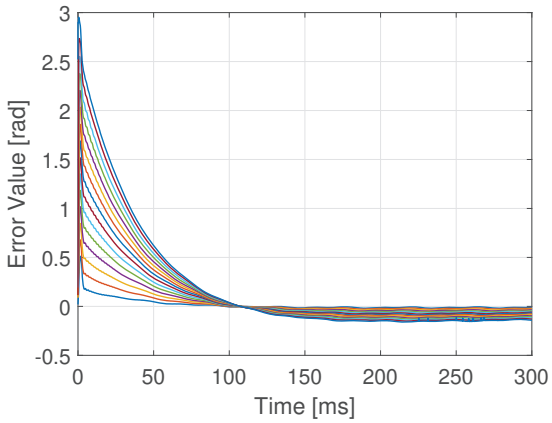
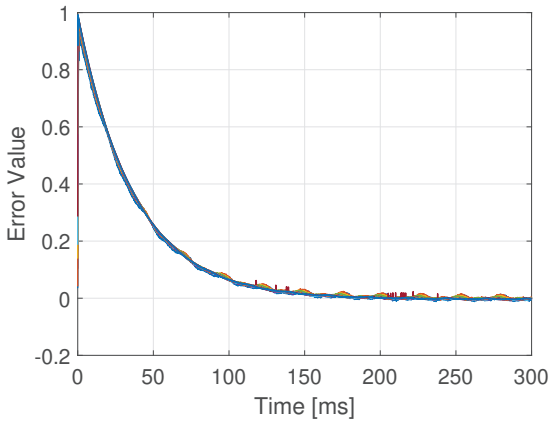


Fig. 11. Error Signal V_q inside the SRF-PLL during the grid voltage phase jumps in the experiment.



(a) Phase angle difference between θ_G and θ_{PLL} after applying Steps in the Grid Voltage Phase from 10° to 170° with linear SRF-PLL.



(b) Normalized Experimental Results to compare the Control Performance.

Fig. 12. Experimental results of Phase Tracking Performance with linear SRF-PLL.

The results of the experiments with linear SRF-PLL are shown in Fig. 12 prove the constant synchronization time and verify therefore the enhanced dynamics of the control system with a linear SRF-PLL.

The performed experiments have validated the simulation results and prove the behavior. The slowed synchronization severely affects the controller during transients in the power grid. A linear SRF-PLL can correct this, which makes the control predictable.

Conclusion

In this paper, a synchronization method which significantly improves the dynamic performance of the phase tracking capability of the SRF-PLL during high magnitude phase jumps is analyzed. It is verified with analysis, simulations and experiments, that this control adaption is beneficial for a reliable control in power electronic converters. With this control is it possible to achieve a constant and predictable control behavior even during severe grid events.

SRF-PLLs have a slower response when it comes to higher phase deviations. With a phase deviation of 170° takes it almost double the time to synchronize, than with the linear SRF-PLL.

- The linear SRF-PLL can be tuned with a fixed bandwidth that is not dependent on the magnitude of the angle difference.
- This control change does not affect the well-known tuning techniques and stability analysis.
- This technique can easily be applied in more advanced PLLs, such as D-SOGI PLLs, and also for single-phase systems.

As long as the phase jump is smaller than 90°, the synchronization time is not significantly affected. The influence on impedance based stability analysis can be neglected, because it had the linearization already as a simplification inside. But for the safe operation during transient events, such as grid faults, is it necessary to guarantee the linear behavior of a SRF-PLL to achieve a control that can fulfill the operational requirements, such as fault-ride-through. Control interactions between the synchronization and the outer control loops (reactive power, active power) can be analyzed in future research.

References

[1] E. Afshari, G. R. Moradi, R. Rahimi, B. Farhangi, Y. Yang, F. Blaabjerg, and S. Farhangi, "Control Strategy for Three-Phase Grid-Connected PV Inverters Enabling Current Limitation Under Unbalanced Faults," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8908-8918, Nov. 2017.

[2] R. Teodorescu, M. Liserre, and P. Rodriguez, *Grid Converters for Photovoltaic and Wind Power Systems*. John Wiley & Sons, 2011, vol. 29.

[3] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1398-1409, Oct. 2006.

[4] D. Dong, B. Wen, D. Boroyevich, P. Mattavelli, and Y. Xue, "Analysis of Phase-Locked Loop Low-Frequency Stability in Three-Phase Grid-Connected Power Converters Considering Impedance Interactions," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 310-321, Jan. 2015.

[5] H. Wu and X. Wang, "Transient Stability Impact of the Phase-Locked Loop on Grid-Connected Voltage Source Converters," *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, pp. 2673-2680, May 2018.

[6] V. Miskovic, V. Blasko, T. M. Jahns, R. D. Lorenz and P. M. Jorgensen, "Linear Phase-Locked Loop," *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, 2018, pp. 5677-5683.

[7] X. Wang, L. Harnefors and F. Blaabjerg, "Unified Impedance Model of Grid-Connected Voltage-Source Converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1775-1787, Feb. 2018.

[8] R. Teodorescu and F. Blaabjerg, "Flexible Control of Small Wind Turbines With Grid Failure Detection Operating in Stand-Alone and Grid-Connected Mode," *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1323-1332, Sept. 2004.

[9] J. Lee and C. Un, "Performance Analysis of Digital Tanlock Loop," *IEEE Transactions on Communications*, vol. 30, no. 10, pp. 2398-2411, Oct. 1982.

[10] I. Serban and C. Marinescu, "Control Strategy of Three-Phase Battery Energy Storage Systems for Frequency Support in Microgrids and with Uninterrupted Supply of Local Loads," *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 5010-5020, Sept. 2014.

[11] M. H. Bollen, "Understanding Power Quality Problems: Voltage Sags and Interruptions," *IEEE Press*, 2000.