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Published in:
IEEE Transactions on Power Electronics

DOI (link to publication from Publisher):
10.1109/TPEL.2017.2756626

Publication date:
2018

Document Version
Accepted author manuscript, peer reviewed version

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2756626, IEEE Transactions on Power Electronics

Steady-State and Small-Signal Analysis of A-Source Converter

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***Abstract*— This paper presents a detailed steady-state analysis and ac small-signal modeling of the power stage of pulse-width modulated A-source converter. The voltage and current waveforms along with their corresponding expressions describing the converter operation are presented in detail. The input-to-output and input-to-capacitor dc voltage transfer functions are determined. The minimum inductance required to ensure continuous-conduction mode is derived. The expressions for the semiconductor devices stresses are also presented. The dc, averaged equivalent circuit is derived using the circuit averaging technique. A complete derivation of the small-signal model including the converter parasitic resistances are presented followed by the power stage transfer functions relevant to the capacitor voltage loop, such as: (a) duty cycle-to-capacitor voltage and (b) input-to-capacitor voltage. In addition, the expressions for the network input impedance and output impedance are derived. Finally, experimental validations of the derived small-signal models are performed, both in frequency and time domain for a laboratory prototype of an A-source converter. The theoretical predictions were in good agreement with the experimental results over a wide range of frequencies.**

***Index Terms*— A-source converter, circuit averaging technique, high step up, small-signal model, steady-state, minimum inductance, stress, transfer functions, impedances.**

I. Introduction

IMPEDANCE-SOURCE converter topologies are becoming attractive in many areas including renewable energy, distributed generation, electric vehicle charging, and battery operation. It has unique properties such as wide voltage conversion, load short-circuit protection, and most importantly, its capability to operate as a voltage source or current source based on the load profile.

Manuscript received April 20, 2017; revised June 09, 2017; accepted September 11, 2017. (*Corresponding author: Agasthya Ayachit*)

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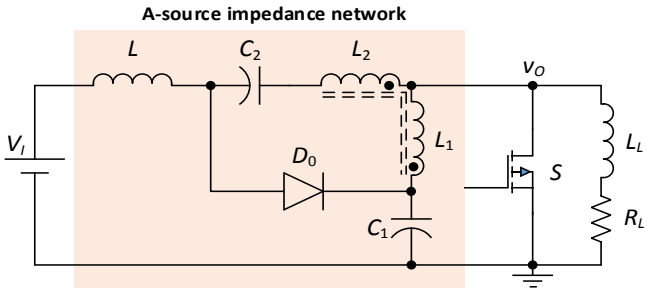

Fig. 1. Circuit of the A-source converter.

This buck/boost ability with high immunity to disturbances and simple seamless control may improve the reliability and performance of the complete power electronic system.

Since the publication of Z-source network in the year 2002, various impedance networks have been developed to provide an efficient means of converting power with a wide range of voltage gain. Improvements to the impedance networks by introducing coupled magnetics have also been lately proposed for achieving even higher voltage boosting, while using a shorter shoot-through time [1]-[3]. They include the Γ-source [4], T-source [5], trans-Z-source [6], TZ-source [7], LCCT-Z-source [8], high-frequency-transformer-isolated [9], and Y-source [10] networks. The voltage gain of Γ-source increases by a decrease in the turns ratio [4], on the other hand, the voltage gain of T-source increases by increasing of the turns ratio [5], different from both, the voltage gain of the Y-source increases by both increasing and decreasing its turns ratios [10].

In addition to boost capability, current ripple magnitude of an impedance source converter is the next factor to consider especially for distributed power generation. In general, pulsed current drawn by the converter is non-preferred since it penalizes the input source with increased high frequency rms current that may cause higher losses. For example, the pulsating input current may periodically shift operating point of the converter, making it difficult to track Maximum Power Point (MPP) of PV generation. The high current ripple drawn may also degrade the fuel cell stack, reducing its power production and life time [12]. An input filter is therefore needed for smoothing the discontinuous current at the expense of higher component count and losses.

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To address these issues, A-source impedance network was proposed in [13]. The network utilizes a minimal turns ratio in its coupled magnetics compared to other Magnetically Coupled Impedance Source (MCIS) networks and have proven to deliver a high voltage step up at low duty cycles and power density compared to the other impedance source counterparts. However, a comprehensive modeling and analysis of dynamic and stability behavior of A-source converter are still missing in the literature. The dynamic behavior modeling is essential to characterize the nature of the A-source converter for closed-loop control design. Two popular techniques used to determine the small-signal models are: (a) state-space averaging [14]-[18] and (b) circuit averaging [19]-[22]. The state-space averaging technique, although is computationally efficient, it is relatively challenging to extract the state matrices for higher order systems including the effect of parasitic resistance of the passive components. Therefore, considering the significance of control aspects of the A-source network, this paper uses the circuit averaging technique to transform the nonlinear, disjoint network of MOSFET and diode into a linear, two-port network of dependent current and dependent voltage sources, respectively. The relevant transfer functions relevant to the voltage loop are derived including the equivalent series resistances of the passive components. The major contributions of this paper are summarized as follows:

a) Derivations of the steady-state current and voltage waveforms of the A-source converter in continuous-conduction mode (CCM).
b) Derivations of the expressions for the dc transfer functions, minimum inductance for CCM operation, current and voltage stresses, and average switch current and diode voltage waveforms.
c) Derivations of the average large-signal, dc, and ac small-signal linear time-invariant model of the PWM A-source converter in continuous conduction mode by the circuit averaging technique.
d) Derivations of the small-signal duty-cycle-to-capacitor voltage and input-to-capacitor voltage transfer functions.
e) Derivations of the expressions for the input and the output impedances.
f) Experimental validation of the predicted analytical results.

This helps readers to understand the insights of various MCIS networks better for control and system design. In the following sections, a detailed small signal model for A-source converter operating in continuous conduction mode (CCM) is presented by means of the averaged switch PWM modeling approach. In Section II, steady state analysis of A-source converter is presented in details with emphasis on CCM and DCM mode. The derivation of averaged and small signal linear model of the converter is developed in Section III. The power stage transfer functions in open loop, such as control-to-capacitor voltage, input-to-capacitor voltage, input and output impedances are presented in Section IV followed by parameter selection in Section V. Section VI provides experimental and theoretical comparison of the average model and the derived transfer functions for all studied MCIS converters, while Section VII brings the conclusions.

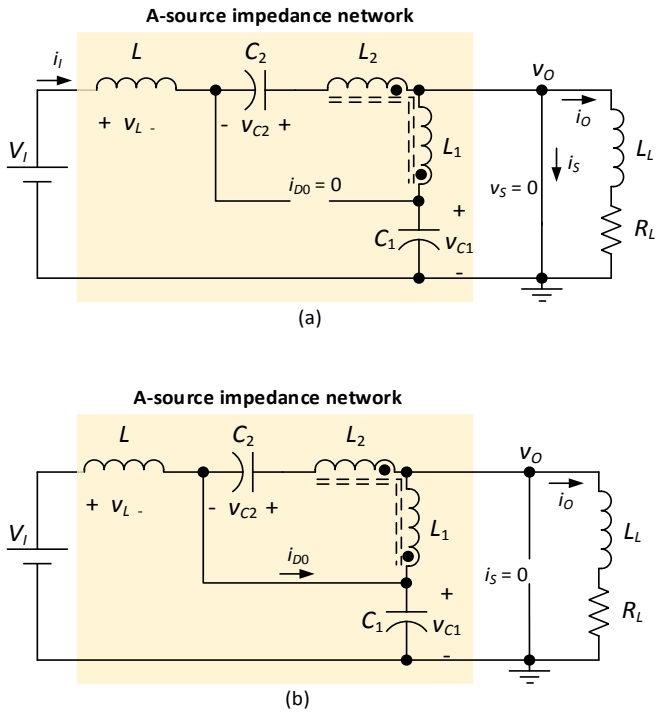

Fig. 2. Sub-circuits of the A-source converter during shoot-through and non-shoot through time intervals. (a) Shoot-through state $0 < t \leq D_{st}T$. (b) Non-shoot-through state $D_{st}T < t \leq T$.

II. Steady-State Analysis of A-Source Converter

Fig. 1 shows the circuit of a single-phase A-source converter. The circuit consists of a dc voltage source V_I, inductor L, capacitors C_1 and C_2, an auto-transformer with turns ratio N_1:N_2, a diode D_0, transistor S, and an impedance load with resistance R_L and inductance L_L. The time-varying output voltage is v_o, whose amplitude is V_{Om}. The amplitude of the output voltage V_{Om} is equal to the maximum voltage across the transistor S. The impedance load can be replaced by a second-order low-pass filter or a diode rectifier circuit to obtain a dc-dc converter with A-source impedance network. In principle, the A-source network can be utilized for dc-ac, dc-dc, ac-dc, or ac-ac energy conversion. The active transistor S, typically a MOSFET is switched at a switching frequency f_s and $T = 1/f_s$ is the switching time period. The duty cycle of the transistor is D_{st}. The duty cycle recreates the shoot-through state of the A-source converter similar to that in the other impedance source converter counterparts [1]. The steady-state analysis is based on the following assumptions:

a) The auto-transformer is ideal, i.e., its magnetizing inductance is infinite, the leakage inductances are zero, and the stray capacitances are ignored.
b) The transistor is ideal, i.e., its rise time, fall time, and ON-state voltage are zero and their parasitic inductances and capacitances are ignored.
c) The diode is ideal, i.e., its junction capacitance is ignored and its ON-state resistance and forward voltage drop are zero.
d) The load impedance can be modeled as a current sink.

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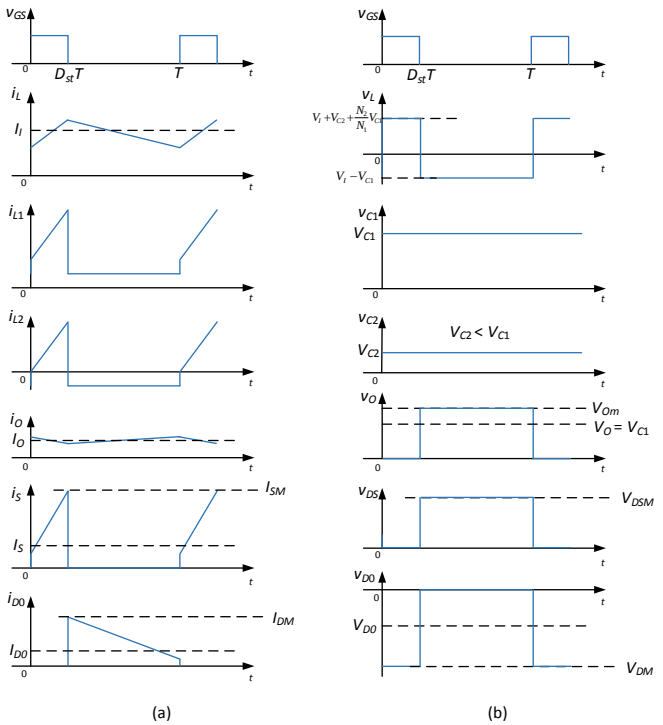

Fig. 3. Key current and voltage waveforms of the A-source converter shown in Fig. 1. (a) Current waveforms. (b) Voltage waveforms.

e) The converter operates in steady state.
f) The inductors, capacitors, and resistors are linear, time invariant, and frequency independent.
g) The capacitors C_1 and C_2 are large enough such that voltages across them are constant.

The sub-circuits of the A-source converter are shown in Fig. 2(a) and (b). The idealized current and voltage waveforms of the converter during the two switching intervals are illustrated in Fig. 3.

A. *Shoot-Through Sub-Interval* $0 < t \le D_{st}T$

The sub-circuit corresponding to this interval is shown in Fig. 2(a). In this time interval, the transistor is ON and the diode is OFF; hence, $i_{D0} = 0$ and $v_S = 0$. The voltage across the inductor L is [13]

$$v_L = V_I + V_{C2} + \frac{N_2}{N_1}V_{C1} = L\frac{di_L}{dt}. \quad (1)$$

The inductor current i_L is

$$i_L = \frac{1}{L}\int_0^t v_L dt + i_L(0) = \frac{1}{L}\left(V_I + V_{C2} + \frac{N_2}{N_1}V_{C1}\right)t + i_L(0). \quad (2)$$

The peak inductor current occurs at $t = D_{st}T$ to give [13]

$$i_L(D_{st}T) = \frac{D_{st}T}{L}\left(V_I + V_{C2} + \frac{N_2}{N_1}V_{C1}\right) + i_L(0). \quad (3)$$

Thus, the peak-to-peak value of the inductor current is

$$\Delta i_L = i_L(D_{st}T) - i_L(0) = \frac{D_{st}}{f_s L}\left(V_I + V_{C2} + \frac{N_2}{N_1}V_{C1}\right). \quad (4)$$

B. *Non-Shoot-Through Sub-Interval* $D_{st}T < t \le T$

The sub-circuit corresponding to this interval is shown in Fig. 2(b). In this time interval, the transistor is OFF and the diode of ON; hence, $v_{D0} = 0$ and $i_S = 0$. The voltage across the inductor L is [13]

$$v_L = V_I - V_{C1} = L\frac{di_L}{dt}. \quad (5)$$

The inductor current i_L is

$$i_L = \frac{1}{L}\int_0^t v_L dt + i_L(D_{st}T) = \frac{1}{L}(V_I - V_{C1})t + i_L(D_{st}T). \quad (6)$$

The peak-to-peak inductor current between the instants $D_{st}T$ and T is

$$\Delta i_L = i_L(T) - i_L(D_{st}T) = \frac{1}{f_s L}(V_I - V_{C1}). \quad (7)$$

C. *DC Voltage Transfer Ratio for Continuous-Conduction Mode*

The ratio of the voltage across the two capacitors is [13]

$$\frac{V_{C1}}{V_{C2}} = \frac{1 - D_{st}}{\left(1 + \frac{N_2}{N_1}\right)D_{st}}. \quad (8)$$

Applying the principle of voltage-second balance to the inductor L, we obtain

$$\int_0^{D_{st}T} v_L dt + \int_{D_{st}T}^{T} v_L dt = 0. \quad (9)$$

Substituting (1) and (5) into (9) and using (8) in (9), we get the dc voltage transfer ratio between the voltage supply V_I and the capacitor C_1 as

$$M_{C1} = \frac{V_{C1}}{V_I} = \frac{1 - D_{st}}{1 - \left(2 + \frac{N_2}{N_1}\right)D_{st}} = \frac{1 - D_{st}}{1 - (1 + N)D_{st}}, \quad (10)$$

where $N = 1 + (N_2/N_1)$. Similarly, the dc voltage transfer ratio from the input to the capacitor voltage C_2 is

$$M_{C2} = \frac{V_{C2}}{V_I} = \frac{\left(\frac{N_2}{N_1} + 1\right)D_{st}}{1 - \left(2 + \frac{N_2}{N_1}\right)D_{st}} = \frac{ND_{st}}{1 - (1 + N)D_{st}}. \quad (11)$$

During the non-shoot-through period, the transistor is OFF and the maximum voltage across the transistor is equal to the output voltage V_{Om} expressed as [3]

$$V_{Om} = V_{C1} - v_{L1} = V_{C1} - \frac{V_{C2}}{N}. \quad (12)$$

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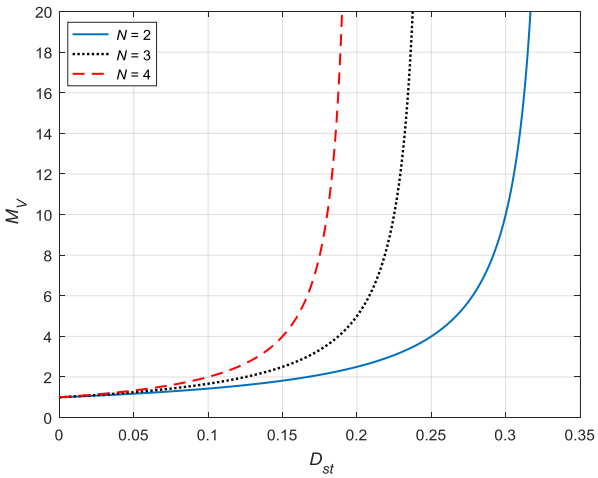

Fig. 4. DC voltage transfer ratio M_V as a function of the shoot-through duty cycle D_{st} for the A-source converter.

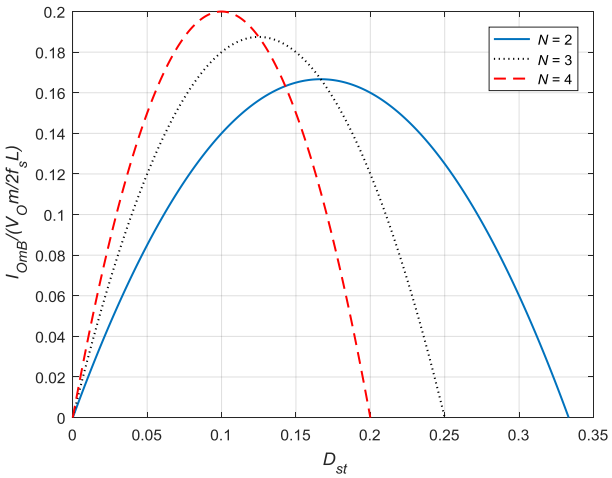

Fig. 5. Normalized load current $I_{om}/2f_sL$ as a function of shoot-through duty cycle D_{st} at the CCM/DCM boundary for A-source converter.

Using (8), (10), and (11) in (12) results in the voltage transfer ratio of the A-source converter for the non-shoot-through period as [13]

$$M_V = \frac{V_{Om}}{V_I} = \frac{1}{1-(1+N)D_{st}}. \tag{13}$$

It must be noted that $M_V > M_{C1} > M_{C2}$. The transfer ratios M_{C1} and M_{C2} are valid for the complete switching period, while M_V is valid only for the non-shoot-through period, which is required to determine the maximum achievable output voltage. Fig. 4 shows the plot of the voltage transfer ratio M_V as a function of shoot-through duty ratio D_{st} at selected values of auto-transformer turns ratio N. A high voltage gain can be achieved at low duty ratio at high turns ratio. Assuming that the converter is ideal, then the current transfer ratio for the non-shoot period is

$$M_I = \frac{I_{Om}}{I_{Im}} = \frac{1}{M_V} = 1-(1+N)D_{st}, \tag{14}$$

where I_{Om} is the peak current through the load for the non-shoot-through period. The average output voltage V_O is

$$V_O = V_{C1} = \frac{1}{T}\int_0^t v_o\,dt = \frac{1}{T}\int_{D_{st}T}^{T} V_{Om}\,dt = (1-D_{st})V_{Om}. \tag{15}$$

Substituting (13) into (15) results in the average output voltage as [13]

$$V_O = \frac{1-D_{st}}{1-(1+N)D_{st}}V_I. \tag{16}$$

Thus, comparing (10) and (16), the average output voltage V_O is equal to the voltage across the capacitor C_1, i.e., $V_O = V_{C1}$ to yield the dc voltage transfer ratio for the total switching period as derived in [13]

$$M_{C1} = \frac{V_O}{V_I} = \frac{V_{C1}}{V_I} = \frac{1-D_{st}}{1-(1+N)D_{st}}. \tag{17}$$

The average current through the load resistance is proportional to the average output voltage of the converter, i.e., $I_O = V_O/R_L$. Therefore, the dc current transfer ratio M_{IAV} for the average currents is

$$M_{IAV} = \frac{I_O}{I_I} = \frac{1}{M_{C1}} = \frac{1-(1+N)D_{st}}{1-D_{st}}. \tag{18}$$

D. Minimum Inductance for CCM

Using (8), (10), and (11) in (7), the peak-to-peak inductor current assuming the current $i_L(T) = 0$ at the boundary between the continuous conduction mode (CCM) and discontinuous conduction mode (DCM) is

$$\Delta i_L = i_L(T) - i_L(D_{st}T) = \frac{D_{st}NM_VV_I}{f_sL}. \tag{19}$$

Moreover, the dc inductor current is equal to the dc input current at the boundary to give

$$I_{IB} = I_{LB} = \frac{\Delta i_L}{2} = \frac{D_{st}NM_VV_I}{2f_sL}. \tag{20}$$

Using (14) and (15), the maximum output current at the boundary between the two modes is

$$I_{OmB} = \frac{D_{st}NV_I}{2f_sL} = \frac{D_{st}NV_{Om}}{2f_sLM_V} = \frac{D_{st}NV_{Om}}{2f_sL}[1-(1+N)D_{st}]. \tag{21}$$

The normalized output current at boundary $I_{OmB}/(V_{Om}/2f_sL)$ as a function of the shoot-through duty ratio D_{st} at selected values of the transformer turns ratio is shown in Fig. 5. The DCM region is enclosed within each curve. The maximum output

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current can be determined by taking the derivative of the current with respect to the duty ratio and equating the results to zero to get

$$\frac{dI_{OmB}}{dD_{st}} = \frac{d}{dD_{st}}\left\{\frac{D_{st}NV_{Om}}{2f_sL}[1-(1+N)D_{st}]\right\} = 0 \qquad (22)$$

to yield the duty ratio at the boundary as

$$D_{stB} = \frac{1}{2(1+N)}. \qquad (23)$$

Substituting (23) into (21) results in the minimum inductance for CCM operation as

$$L_{min} = \frac{NV_{Om}}{4(1+N)f_sI_{OmB}} = \frac{NR_{Lmax}}{4(1+N)f_s}. \qquad (24)$$

Thus, an inductance $L > L_{min}$ should be chosen to ensure CCM condition.

E. Expressions for Average Switch Current and Diode Voltage

From Fig. 3, the average switch current is

$$I_S = \frac{1}{T}\int_0^t i_S dt = \frac{1}{T}\int_0^{D_{st}T} i_S dt = I_I - I_O. \qquad (25)$$

The expression for I_O can be determined using (18). Substituting the result into (25) yields the average switch current as a function of the input current and duty cycle as

$$I_S = NI_I\frac{D_{st}}{D'_{st}} = a_3I_I, \qquad (26)$$

where $D_{st}' = 1 - D_{st}$ is the duty ratio of non-shoot-through period and $a_3 = ND_{st}/(1-D_{st})$. The average diode voltage is

$$V_D = \frac{1}{T}\int_0^t v_D dt = \frac{1}{T}\int_0^{D_{st}T}(V_L - V_{C1})dt = D_{st}(V_L - V_{C1}). \qquad (27)$$

Substituting (1), (8), and (10) into (25) results in the average voltage across the diode as

$$V_D = NV_{C1}\frac{D_{st}}{D'_{st}} = NV_I\frac{D_{st}}{1-(1+N)D_{st}} = a_2V_I, \qquad (28)$$

where the coefficient $a_2 = ND_{st}/[1-(1+N)D_{st}]$. Constants a_2 and a_3 are derived in subsequent sections.

F. Voltage and Current Stresses of Semiconductor Components

The maximum current and voltage stresses of the transistor *S*

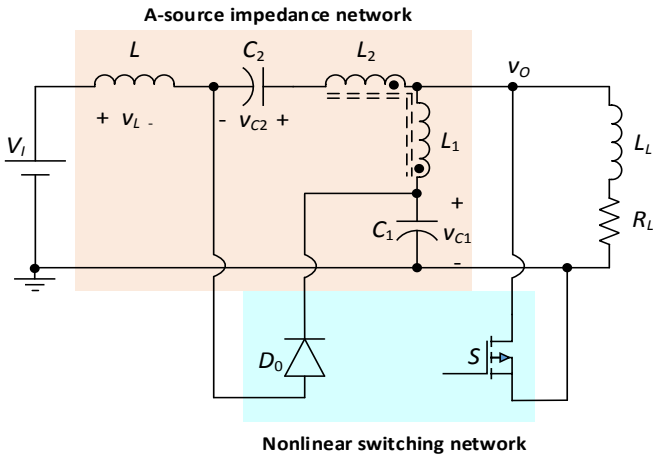

Fig. 6. . Circuit of the A-source converter with the nonlinear switching network as a two-port network.

and the diode D_0 are determined as follows. The maximum voltage stress V_{SM} of the transistor *S* is

$$V_{SM} = V_{Om}. \qquad (29)$$

The maximum current stress I_{SM} is

$$I_{SM} = I_S + \frac{\Delta i_L}{2}. \qquad (30)$$

Using (4) and (25) in (30) results in

$$I_{SM} = \frac{D_{st}}{D_{st}'}NI_I + \frac{DD'V_I}{2f_sL}\left[\frac{N}{1-(1+N)D_{st}}\right]. \qquad (31)$$

The maximum voltage stress V_{DM} across the diode D_0 is

$$V_{DM} = NV_{Om}. \qquad (32)$$

The maximum current stress I_{DM} of D_0 is

$$I_{DM} = D_{st}I_I - I_{L2} + \frac{\Delta i_L}{2}$$

$$= \frac{D_{st}[1-(1+N)D_{st}]}{N}I_I + \frac{D_{st}D_{st}'V_I}{2f_sL}\left[\frac{N}{1-(1+N)D_{st}}\right]. \qquad (33)$$

III. Derivation of Averaged and Small-Signal Linear Models

The circuit averaged dc and low-frequency ac models of the A-source converter is developed using the circuit averaging technique [16]-[20]. The nonlinear switching network in the A-source converter is shown in the form of a two-port network in Fig. 6. The expressions for the average switch current and the average diode voltage are given in (26) and (28), respectively. It can be seen that the averaged switch current I_S is expressed

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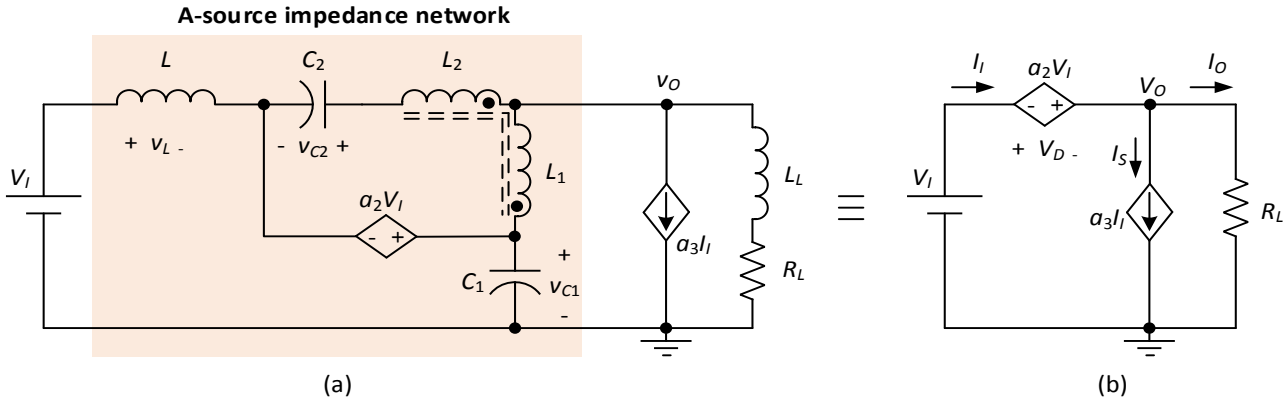

Fig. 7. DC model of the A-source converter obtained using circuit averaging technique. (a) Complete dc model. (b) Simplified dc model. Constants a_2 and a_3 are determined in (41).

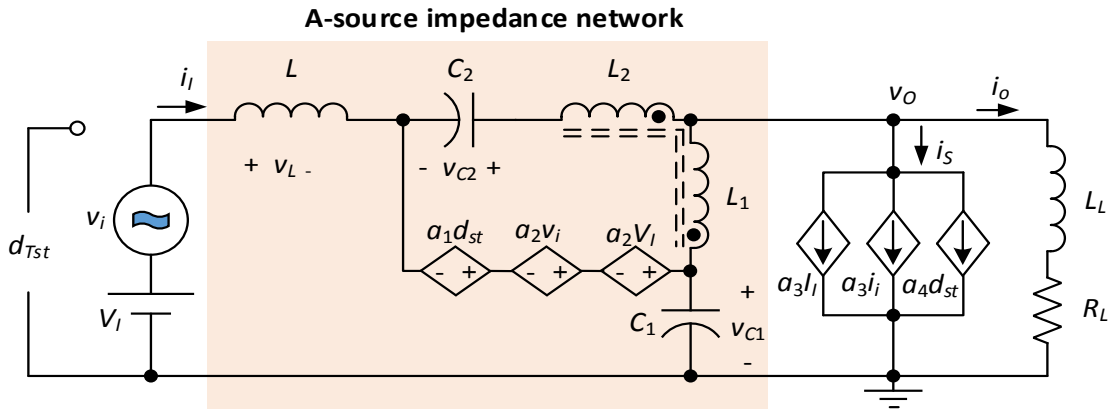

Fig. 8. Large-signal model of the A-source converter showing dc and ac small-signal components.

as a function of the input current I_I, while the averaged diode voltage V_D is expressed in terms of the input voltage V_I. Thus, the two-port switching network comprising the transistor and the diode can be replaced by controlled current and voltage sources, respectively. Fig. 7(a) shows the complete averaged model of the A-source converter. Using the circuit averaging technique, the transistor is replaced by a current-controlled current source a_3I_I and the diode by a voltage-controlled voltage source a_2V_I in accordance with (26) and (28), respectively. Fig. 7(b) shows the simplified dc model of the A-source converter, where the inductor is replaced by a short circuit and the capacitor is replaced by an open circuit. Subsequent analysis relevant to the development of the small-signal model makes the following assumptions:

a) Converter operates in continuous-conduction mode (CCM).
b) The auto-transformer is ideal, i.e., its magnetizing inductance is infinite, the leakage inductances are zero, and the stray capacitances are ignored.
c) The magnetizing inductance of the auto-transformer is infinite and does not store any energy. Therefore, the magnetizing inductance does not contribute to the order of the transfer functions.

The averaged model shown in Fig. 7(a) is perturbed by introducing small-signal perturbations superimposed on the dc currents, voltages, and duty cycle. The result is a large-signal nonlinear model. The perturbations in the duty cycle, input voltage, and input current are d_{st}, v_i, and i_i, respectively. Therefore, the large-signal duty cycle, input voltage, and input current are $d_{Tst} = D_{st} + d_{st}$, $v_I = V_I + v_i$, and $i_I = I_I + i_i$, respectively. Applying the perturbation to the switch current given in (26) results in its large-signal expression

$$i_S = I_S + i_s = Ni_I \frac{d_{Tst}}{d'_{Tst}} = Ni_I \frac{d_{Tst}}{D'_{st} - d_{st}}, \tag{34}$$

where $d_{Tst}' = 1 - (D_{st} + d_{st}) = D_{st}' - d_{st}$. The large-signal diode voltage is obtained by perturbing the input voltage and duty cycle in (28) to get

$$v_D = V_D + v_d = Nv_I \frac{d_{Tst}}{1 - (1+N)d_{Tst}}. \tag{35}$$

Manipulating (34) and (35) results in

$$D_{st}I_S + D'_{st}i_s - I_S d_{st} - di_s = DI_I N + I_I Nd + NDi_i + Ndi_i. \tag{36}$$

and

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$$V_D[1-(1+N)D_{st}] - V_D(1+N)d_{st} \quad + [1-(1+N)D_{st}]v_d + [1-(1+N)D_{st}]dv_d = NV_ID + NV_Id + NDv_i + Ndv_i. \tag{37}$$

The equations presented in (36) and (37) consist of dc terms, first-order ac terms, and high-order ac nonlinear terms. The principle of linearization can be applied to these equations by considering the following conditions:

$$\begin{aligned} D_{st} &\gg d_{st}, \\ I_I &\gg i_i, \\ V_I &\gg v_i. \end{aligned} \tag{38}$$

Thus, by applying the small-signality conditions in (38) to (36) and (37), i.e., equating $dv_d = dv_i = 0$ results in the linearized small-signal diode voltage and switch current as follows. The small-signal diode voltage is

$$v_d = \frac{NV_I}{[1-(1+N)D_{st}]^2}d_{st} + \frac{D_{st}N}{[1-(1+N)D_{st}]}v_i = a_1d_{st} + a_2v_i \tag{39}$$

and the small-signal switch current is

$$i_s = \frac{D_{st}N}{D'_{st}}i_i + \frac{NI_I}{D'^2_{st}}d_{st} = a_3i_i + a_4d_{st}, \tag{40}$$

where the coefficients a_1, a_2, a_3, and a_4 are

$$a_1 = \frac{NV_I}{[1-(1+N)D_{st}]^2}, \quad a_2 = \frac{D_{st}N}{[1-(1+N)D_{st}]}, \quad a_3 = \frac{D_{st}N}{D'_{st}}, \quad a_4 = \frac{NI_I}{D'^2_{st}}. \tag{41}$$

By applying the principle of superposition, the large-signal diode voltage and switch current expressions using the dc equations in (26) and (28) and small-signal linear equations in (39) and (40) are

$$v_D = V_D + v_d = a_1d_{st} + a_2v_i + a_2V_I \tag{42}$$

$$i_S = I_S + i_s = \mathrm{a}_3I_I + a_3i_i + a_4d_{st}. \tag{43}$$

Fig. 8 shows the large-signal model of the A-source converter representing the large-signal diode voltage and switch current equations given in (42) and (43), respectively. The complete small-signal linear model of the A-source converter obtained using the circuit averaging technique is shown in Fig. 8. For the sake of simplicity in deriving the transfer functions, the subsequent analysis considers lumped impedances and they are represented as follows:

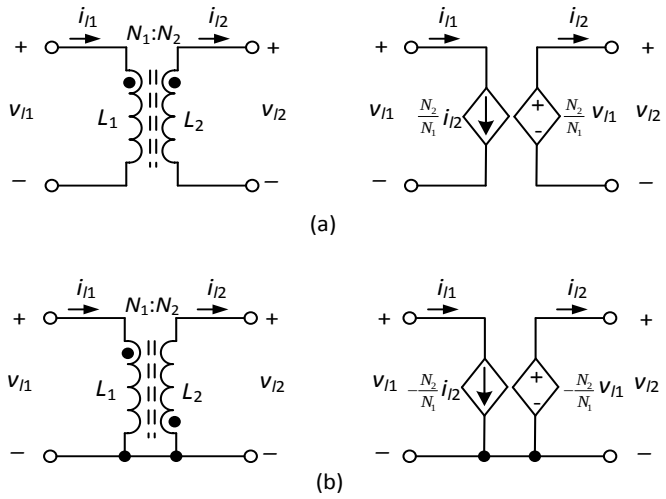

Fig. 9. Circuit and model of two-winding ideal transformer and auto-transformer. (a) Non-inverting transformer circuit and model. (b) Inverting auto-transformer circuit and model.

$$\begin{aligned} Z_L &= r_L + sL, \\ Z_{C1} &= r_{C1} + \frac{1}{sC_1}, \\ Z_{C2} &= r_{C2} + \frac{1}{sC_2}, \\ Z_x &= R_L + sL_L. \end{aligned} \tag{44}$$

In this work, an ideal auto-transformer is used. The following assumptions are made in the subsequent analysis:

a) In the A-source converter, the auto-transformer does not have to store energy during the switching intervals. Its magnetizing inductance is infinite, i.e., the auto-transformer does not possess a state variable. Therefore, the order of the transfer functions is unaffected by the auto-transformer.
b) The parasitic resistances and parasitic capacitances are negligible.
c) The primary and secondary windings are perfectly coupled.

The dependent voltage and current equations are

$$i_{l1} = \frac{N_2}{N_1}i_{l2}, \quad v_{l2} = \frac{N_2}{N_1}v_{l1}. \tag{45}$$

Using (45), a basic ideal two-winding transformer can be represented in terms of dependent current and voltage sources and it is shown in Fig. 9(a). Similar approach can be adopted

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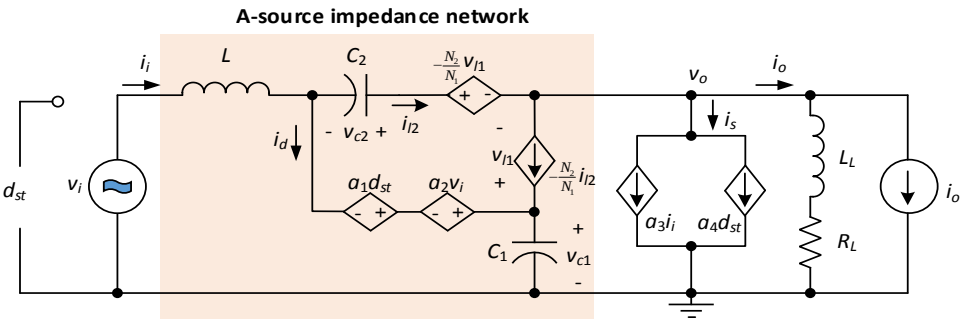

Fig. 10. Small-signal linear model of the A-source converter.

for an auto-transformer. An equivalent 2-port representation of a two-winding auto-transformer is shown in Fig. 9(b). The resulting small-signal linear model of the A-source converter with the switch *S*, diode D_0, and the auto-transformer represented by their equivalent models is as shown in Fig. 10.

IV. Power Stage Transfer Functions and Impedance Expressions

The small-signal model shown in Fig. 10 is used in the subsequent analysis to determine the power stage transfer functions. The four main power stage network functions relevant to the design of voltage control loop are: (a) control-to-capacitor voltage T_d, (b) input-to-capacitor voltage M_v, (c) input impedance Z_i, and (d) output impedance Z_o. The fundamental state equations, which are applicable to the complete small-signal model are as follows. Applying KCL at the node connecting the diode branch, capacitor C_1, and winding L_1 gives

$$i_d = \frac{v_{c1}}{Z_{C1}} + i_{l1} = \frac{v_{c1}}{Z_{C1}} + \frac{N_2}{N_1} i_{l2}, \tag{46}$$

Applying KCL at the node connecting the inductor L, diode branch, and the winding L_2 yields

$$i_i = i_d + i_{l2} = \frac{v_{c1}}{Z_{C1}} + N i_{l2}, \tag{47}$$

Using KCL at the node connecting the auto-transformer, transistor branch, and the load results in

$$i_{l2} + i_{l1} = N i_{l2} = a_3 i_i + a_4 d_{st} + \frac{v_o}{Z_x}. \tag{48}$$

Applying KVL to the loop comprising of the input voltage v_i, inductor L, diode branch, and capacitor C_1 yields

$$v_i = i_i Z_L - a_1 d_{st} - a_2 v_i + v_{c1}. \tag{49}$$

Applying KVL to the loop between the input voltage source and the load gives

$$v_i = i_i Z_L - i_{l2} Z_{C2} - v_{l2} + v_o. \tag{50}$$

Finally, applying KVL to the output loop comprising of the winding L_1, capacitor C_1, and the load is

$$-v_{l1} + v_{c1} = v_o. \tag{51}$$

The subsequent sections determine the closed-form expressions for the above-mentioned transfer functions.

A. Control-to-Capacitor Voltage Transfer Function T_d

Fig. 11(a) shows the small-signal model required to determine the control-to-capacitor voltage transfer function T_d. The model was obtained by letting the perturbations $v_i = 0$ and $i_o = 0$. The state equations provided in (46)-(51) are used and the condition $v_i = 0$ is substituted for the relevant terms. The control-to-capacitor voltage transfer function in the impedance form is expressed in (52). The constants a_1-a_4 are determined in (41) and the impedances are described in (44). Complete derivation of the transfer function in terms of components is cumbersome. Basic steps to derive are provided in Appendix.

B. Input-to-Capacitor Voltage Transfer Function M_v

Fig. 11(b) shows the small-signal linear model required to determine the input-to-capacitor voltage transfer function M_v. The model was obtained by letting the perturbations $d_{st} = 0$ and $i_o = 0$. The resulting state equations are obtained by substituting $d_{st} = 0$ into (46)-(51). The input-to-capacitor voltage transfer function in the impedance form is as given in (53). Similar to (52), one can derive the s-domain form of (53). The Bode magnitude and phase analysis for these high-order systems can be performed accurately using computation tools such as MATLAB.

C. Input Impedance Z_i

Fig. 11(b) shows the small-signal linear model required to determine the expression for the input impedance Z_i of the A-source converter. The model was obtained by letting the perturbations $d_{st} = 0$ and $i_o = 0$. By substituting $d_{st} = 0$ into (46)-(51), the input impedance is as given in (54).

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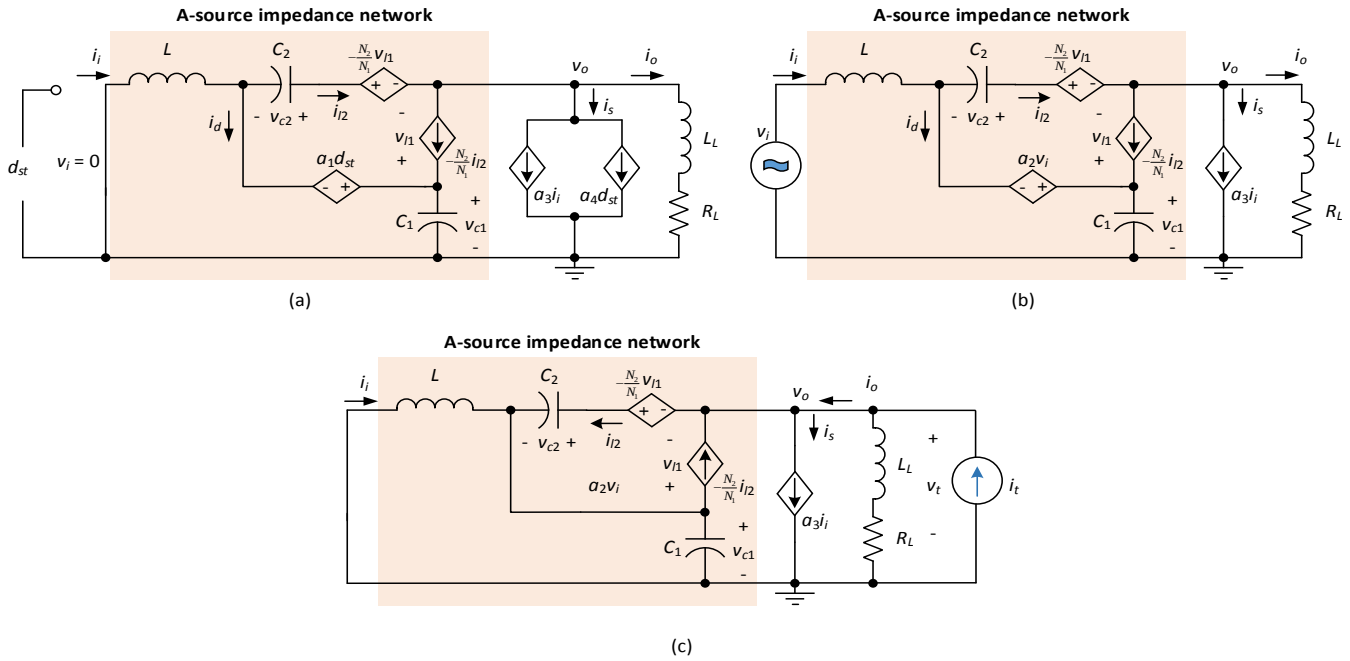

Fig. 11. Small-signal linear models required to determine (a) duty cycle-to-capacitor voltage transfer function T_d, (b) input-to-capacitor voltage transfer function M_v and input impedance Z_i, and (c) output impedance Z_o.

$$T_d = \frac{v_{c1}}{d_{st}} = \frac{[N^2 a_1(1-a_3)Z_x - a_1 Z_{C2} - a_1 N Z_L - a_4 N^2 Z_x Z_L]N_1 Z_{C1}}{N^2 N_1 Z_x[Z_L + (1-a_3)Z_{C1}] - N_1 Z_{C2}(Z_L + Z_{C1}) + N^2 N_1 Z_L Z_{C1}}. \tag{52}$$

$$M_v = \frac{v_{c1}}{v_i} = \frac{N_1 Z_{C1}[(1-a_3)N^2(1+a_2)Z_x - (1+a_2)Z_{C2} - NZ_L]}{N^2(1-a_3)Z_x[N_1 Z_{C1} + (1-a_3)N_1 Z_L] - N_1 Z_{C2}(Z_L + Z_{C1}) + N^3 Z_L(N_1 N a_3 Z_x - N_1 Z_L - N_2 Z_{C1})}. \tag{53}$$

$$Z_i = \frac{v_i}{i_i} = \frac{N^2 N_1[(1-a_3)Z_x Z_{C1} + Z_L(Z_x + Z_{C1})] - N_1 Z_{C2}(Z_L + Z_{C1}) + 2a_3 N_1 Z_{C1} Z_{C2}}{N_1(1+a_2)(N^2 Z_x - Z_{C2}) + N^2 N_1 Z_{C1} + N N_2 a_2 Z_{C1}}. \tag{54}$$

D. Output Impedance Z_o

Fig. 11(c) shows the model to determine the output impedance Z_o of the A-source converter. A sinusoidal test current source i_t is placed in parallel to the load branch. The perturbations d_{st} and v_i are equal to 0. Thus, the controlled voltage sources in the diode branch are treated as short circuits, while the controlled current source $a_1 d_{st}$ is treated as an open circuit. The equations required to determine the expression for the output impedance Z_o are as follows. Applying KCL at the the auto-transformer and switch node gives

$$i_a = i_{l2} + i_{l1} = i_{l2} + \frac{N_2}{N_1} i_{l2} = N i_{l2}. \tag{55}$$

Applying KCL at the output node yields

$$i_t = a_3 i_i + \frac{v_t}{Z_x} + i_a = a_3 i_i + \frac{v_t}{Z_x} + N i_{l2}. \tag{56}$$

The current through the secondary winding of the auto-transformer is

$$i_{l2} = \frac{1}{Z_{C2}}\left[v_t - v_{c1} - \frac{N_2}{N_1} v_{l1}\right]. \tag{57}$$

Applying KVL between the load and the capacitor C_1

$$v_{l1} = v_{c1} - v_t, \tag{58}$$

and the voltage across the capacitor C_1 is

$$v_{c1} = i_a Z_{eq}. \tag{59}$$

Using (55)–(59), the expression for the output impedance Z_o of the A-source converter is

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$$Z_o = \frac{v_t}{i_t} = \frac{Z_x(Z_{C1}Z_{C2} + Z_L Z_{C2} + N^2 Z_{C1} Z_L)}{N^2 Z_{C1}[Z_L + (1 - a_3)Z_x] + N^2 Z_L Z_x + Z_{C2}(Z_{C1} + Z_L)}. \quad (60)$$

V. Design and Selection of Components

This section presents the design of the A-source dc-ac converter. The minimum inductance, current and voltage stresses as well as the appropriate components are determined. The specifications of the A-source converter are as follows: input supply voltage V_I = 50 V, maximum output power during shoot-through P_O = 400 W, switching frequency f_s = 30 kHz, and desired maximum output voltage during shoot-through V_{Om} = 200 V. An auto-transformer with turns ratio N_1:N_2 = 1:1 was selected resulting in $N = 1 + N_2/N_1 = 2$. The load resistance is $R_L = V_{om}^2/P_O$ = 200 Ω and the maximum output current is I_{Om} = 1 A. The dc voltage ratio for the non-shoot-through period is $M_V = V_{Om}/V_I = 4$. The dc voltage transfer ratio for the complete switching period between the input and the capacitor C_1 is M_{C1} = 3. Therefore, from (13), the shoot-through duty cycle can be calculated as D_{st} = 0.25. Using (10) and (11), the dc voltages across the capacitor for the entire switching period is V_{C1} = 150 V and V_{C2} = 100 V. Using (24), the minimum inductance to establish continuous-conduction mode operation is

$$L_{min} = \frac{NR_L}{4(1+N)f_s} = \frac{2 \times 200}{4 \times (1+2) \times 30 \times 10^3} = 1.11 \text{ mH}. \quad (61)$$

An inductor with L = 1.2 mH was selected. The peak-to-peak inductor current ripple using (19) for L = 1.2 mH is Δi_L = 2.77 A. As the maximum output current is known, the maximum input current can be determined using (14) as $I_{Im} = M_V I_{Om}$ = 4 A. The average output current using (18) is $I_O = V_O/R_L = V_{C1}/R_L$ = 150/200 = 0.75 A. Therefore, using (18), the average input current is $I_I = M_{C1} I_O = 3 \times 0.75 = 2.25$ A. The average switch current using (26) is I_S = 1.5 A. The average diode voltage using (28) is V_D = 100 V. The voltage stress across the transistor using (29) is $V_{SM} = V_{Om}$ = 200 V. The maximum current stress of the transistor using (30) is I_{SM} = 2.885 A. The MOSFET chosen was IPW60R041C6 by Infineon Technologies with maximum drain-to-source voltage V_{DSmax} = 650 V, typical ON-state resistance R_{DSon} = 0.041 Ω, continuous drain current I_D = 77.5 A at 25ºC, pulse drain current I_{Dpeak} = 272 A at 25ºC, and output capacitance C_o = 235 pF [26]. The maximum voltage stress of the diode using (32) is $V_{DM} = NV_{Om}$ = 400 V. The maximum current stress of the diode using (33) is I_{DM} = 1.0729 A. The diode chosen was IDW40G65C5 by Infineon Technologies with maximum reverse voltage V_{RRmax} = 650 V, forward voltage V_F = 1.5 Ω, and continuous forward current I_F = 40 A at 25ºC [27].

The derivation of the expressions required to determine the capacitances C_1 and C_2 are identical to that for galvanically-isolated impedance source dc-dc converters and are derived in [3]. The capacitances can also be derived using the expression for the winding currents based on the techniques in [24], [25].

Table I. Specifications and Component Values Used for Theoretical and Experimental Analyses of a 400 W A-Source Inverter.

Parameter/Description		Value/Part Number
Power rating P_O		400 W
Input voltage V_I		50 V-150 V
Output voltage V_{Om}		200 V
Capacitor	C_1	100 µF, 400 V, 0.5 Ω Kemet
	C_2	220 µF, 400 V, 0.5 Ω Kemet
Inductor L		1.2 mH, 0.5 Ω
Load R_L		200 Ω
Turns ratio N_2: N_1		20:20 = 1:1 $N = 2$
Duty cycle D_{st}		0.1- 0.25
Switching frequency f_s		30 kHz
Switch S		IPW60R041C6
Diode D_0		IDW40G65C5

Using the results from [3], the following capacitors are selected C_1 = 100 µF and C_2 = 220 µF. Table I summarizes the specifications and components used in the experiments.

VI. Experimental Results

The A-source prototype was designed for the specifications provided in Table I, built, and tested to validate the theoretical predictions. The parasitic resistances of the passive components have been included in predicting the magnitude and phase of the network transfer functions T_d and M_v and the impedances Z_i and Z_o. The set-up used for measurements is shown in Fig. 12. Keysight 5061B network analyzer was used to capture the Bode magnitude and phase plots of the transfer functions and the impedances. A variable-frequency small-signal sinusoidal voltage was injected into the power stage through a Picotest 2101A Injection Transformer of a bandwidth 10 Hz – 45 MHz for control-to-capacitor voltage response. Similarly, Picotest 2120A Line Transformer was used to measure the input-to-output voltage response. A DC blocking capacitor was used to suppress the dc component from entering the power stage as well as the output probes while measuring the output impedance. An LM1630 op-amp was used to realize the op-amp analog pulse-width modulator. A measurement procedure similar to [28] was followed to capture the best frequency response from the test setup. The transfer functions were measured at the following dc operating conditions: dc supply voltage V_I = 50 V and shoot-through duty cycle D_{st} = 0.1.

The network required to measure the duty cycle-to-capacitor voltage transfer function T_d is shown in Fig. 12(a). Fig. 12(a) illustrates the predicted and measured Bode magnitude and phase plots of the transfer function T_d. The expression for the duty cycle-to-capacitor voltage transfer function was derived in (52). The modulator gain $T_m = 20\log(1/V_{Tm})$, where V_{Tm} is the peak value of the saw-tooth waveform was added to the

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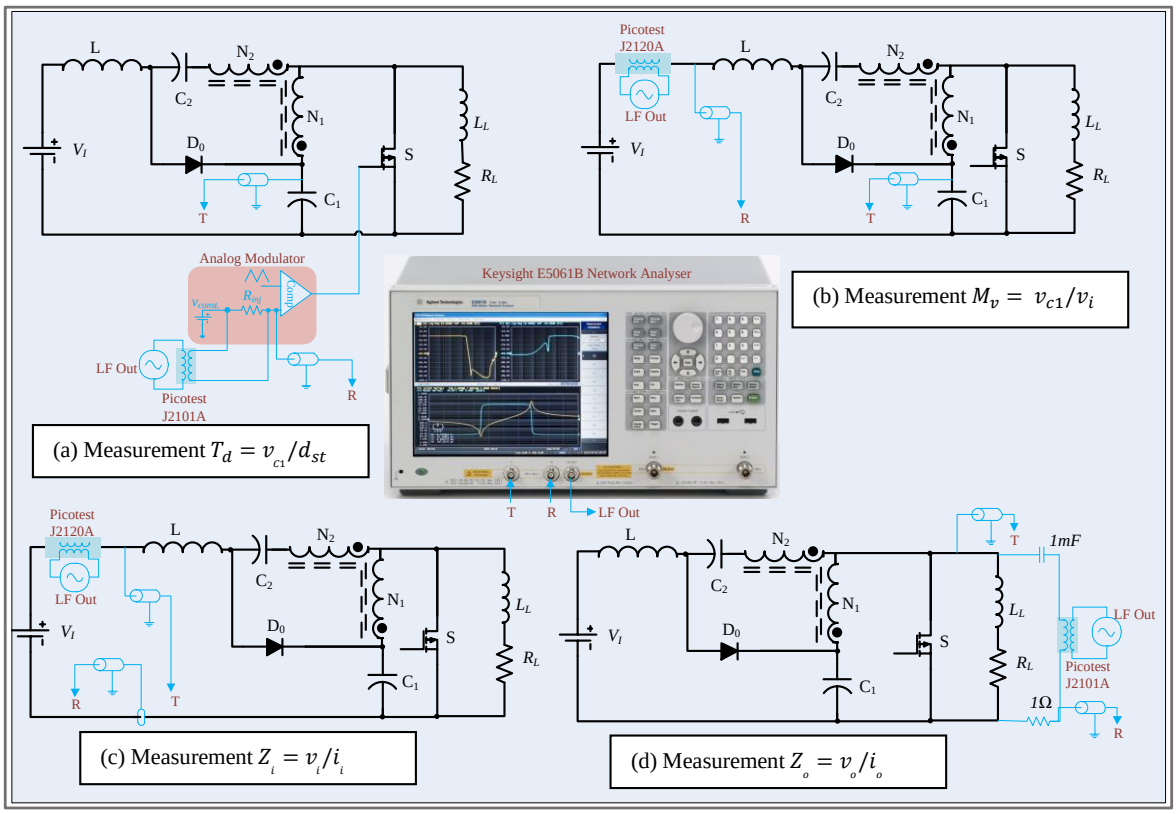

Fig. 12. Measurements set-up for capturing the frequency responses of (a) T_d , (b) M_v, (c) Z_i, and (d) Z_o.

theoretical transfer function to achieve good agreement between the predicted and measured results. The gain at dc was T_{d0} = 42.9 dB = 140 V/V. A pair of complex conjugate poles is located at 450 Hz. The phase crosses -180º at 1 kHz, drops to -220º and rises to -180º at high frequencies. Therefore, the A-source network is a non-minimum phase (NMP) system with a right-half plane zero in the duty cycle-to-capacitor voltage transfer function. The following was observed: the predicted transfer function T_d was of order 3. By inspection, one could state that the converter with four reactive elements must result in fourth-order transfer functions. However, from Figs. 2(a) and (b), it can be seen that the reactance to current flow is only by L, C_1, and C_2 during $0 < t \le D_{st}T$ and the reactance is due to L, C_2, L_L during the interval $D_{st}T < t \le T$.

Fig. 13(b) shows the predicted and measured frequency responses of the input voltage-to-capacitor voltage transfer function M_v. The network used to capture the measurement data is shown in Fig. 12(b). The expression for the input-to-capacitor voltage transfer function was derived in (53). The gain at dc is M_{v0} = 3.8 dB = 1.55 V/V. The phase tends to zero degrees at high frequencies due to the zero produced by the capacitance C_1 and its equivalent series resistance r_{C1}.

Fig. 14(a) shows the predicted and measured magnitude and phase plots of the input impedance as a function of frequency. The expression for the input impedance was derived in (54). The input impedance decreases from Z_{i0} = 86 Ω at 10 Hz to nearly 0.3 Ω at the corner frequency and increases with frequency, thereafter. The phase plot indicates that the converter is capacitive at low frequencies, nearly resistive at the corner frequency, and is inductive at high frequencies and are common features of boost-derived converters. Fig. 14(b) shows the predicted and measured magnitude and phase plots of the output impedance as a function of frequency. The expression for the output impedance was derived in (60). It can be seen that the output impedance decreases from Z_{o0} = 10 Ω at dc to nearly 1.8 Ω up to the corner frequency, then increases with increasing f to reach 9 Ω at the corner frequency, and decreases with an increase in frequency. These characteristics are typical for impedance source converters [1], [2].

Fig. 15 compares the predicted and measured responses of the capacitor voltage v_{C1} for a step change in the duty cycle by ΔD_{st} = 0.1 at V_I = 50 V and R_L = 120 Ω. The initial steady-state voltage was measured as V_{C1} = 77 V. The RHP-zero in the T_d transfer function results in undershoot in the voltage response at the instant of step change. The final steady-state voltage was nearly 140 V obtained for a settling time of 12 ms. Fig. 16 shows the predicted and measured responses of the capacitor voltage v_{C1} for a step change in the supply voltage from 35 V to 45 V.

VII. Conclusions

This paper has addressed a detailed steady-state analysis, design, and modeling of the A-source converter. The A-source converter can be classified as a high step-up, isolated, auto-transformer-based circuit topology. The analytical expressions for the key current and voltage waveforms have been derived.

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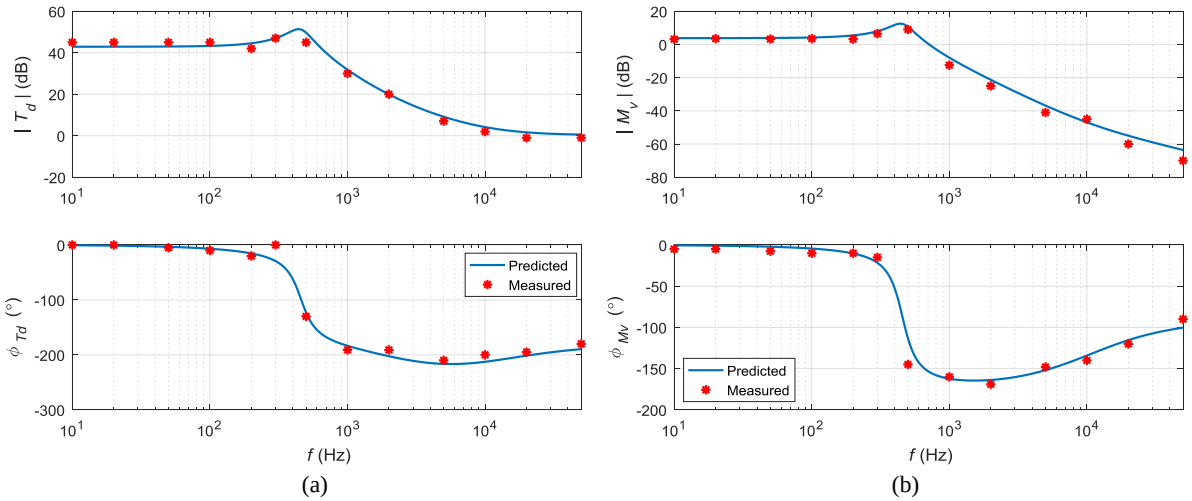

Fig. 13. Predicted and measured Bode magnitude and phase plots of (a) T_d and (b) M_v for the A-source converter.

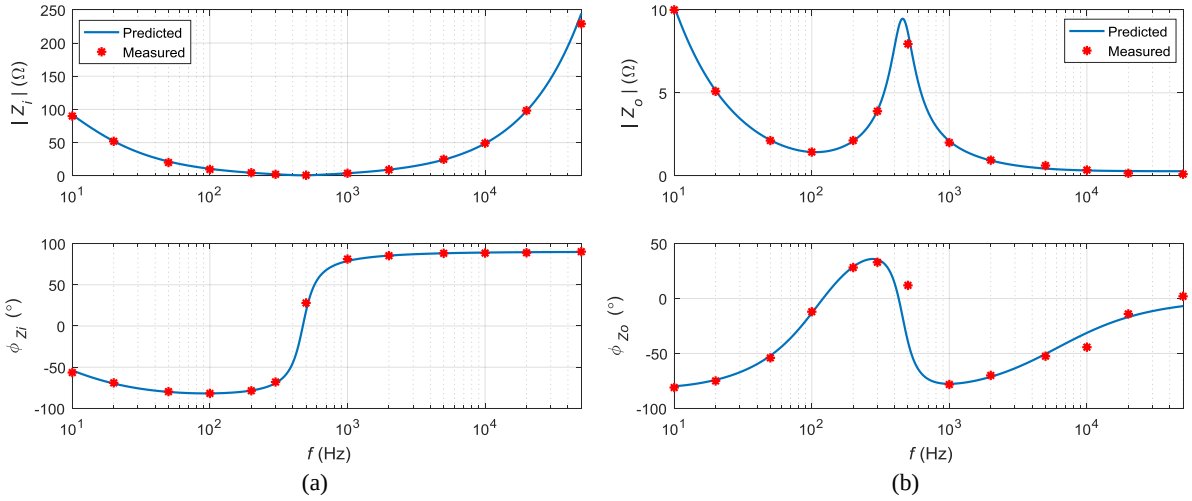

Fig. 14. Predicted and measured Bode magnitude and phase plots of (a) Z_i and (b) Z_o for the A-source converter.

The expressions for the dc voltage transfer functions between the supply voltage to the output voltage and the capacitor voltage for the converter operating in continuous-conduction mode (CCM) have been obtained. The minimum inductance required for the converter operation in CCM has been derived and the boundary conditions between continuous- and discontinuous-conduction modes have been analyzed. The voltage and current stresses of the semiconductor switches have been determined. The expressions for the average switch current and diode voltage required to establish a dc and low-frequency, averaged model of the A-source converter have also been derived. The nonlinear, disjoint PWM switch of the converter has been approximated by an averaged linear model by using circuit-averaging technique. The large-signal averaged model, dc, and ac small-signal linear model of the power stage of A-source converter operating in CCM have been developed. A method to model the auto-transformer in the form of dependent voltage and current sources has been shown. The power-stage duty cycle-to-capacitor voltage and input-to-capacitor voltage transfer functions and the network input and output impedances have been derived. The transfer functions take into account the equivalent series resistances of the passive components.

A-source converter prototype was designed, built, and tested. The following transfer functions were measured using the Agilent E5061B wide-bandwidth gain/phase network analyzer: duty cycle-to-capacitor voltage, input-to-capacitor voltage, input impedance, and output impedance. The response of the capacitor voltage for step changes in the control voltage and the supply voltage were predicted and obtained through experiments as well. The theoretically predicted step responses were found to be in good agreement with the experimental step responses. The theoretically predicted and the experimentally obtained Bode plots of the derived transfer functions were in

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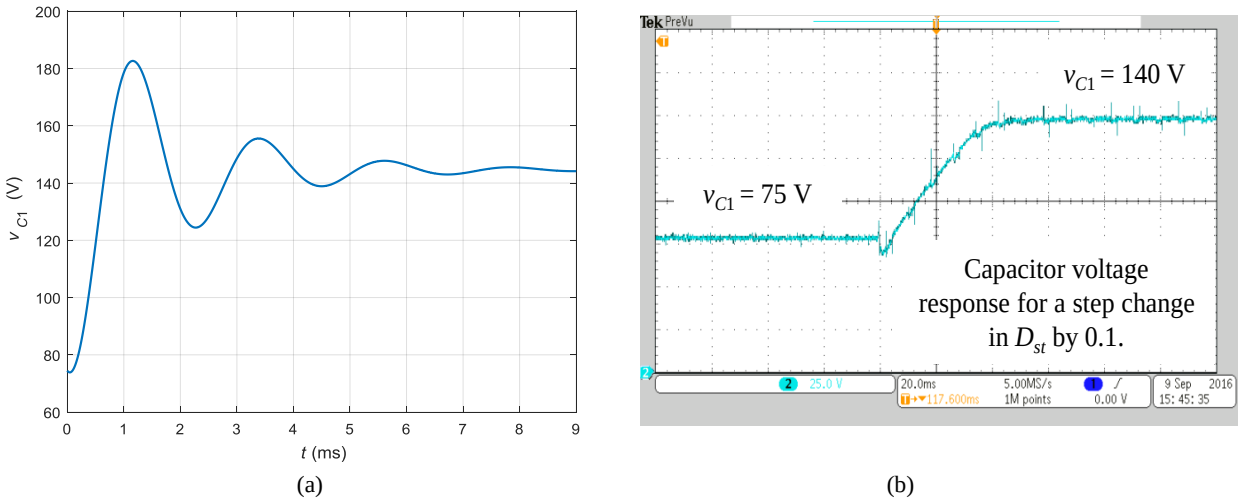
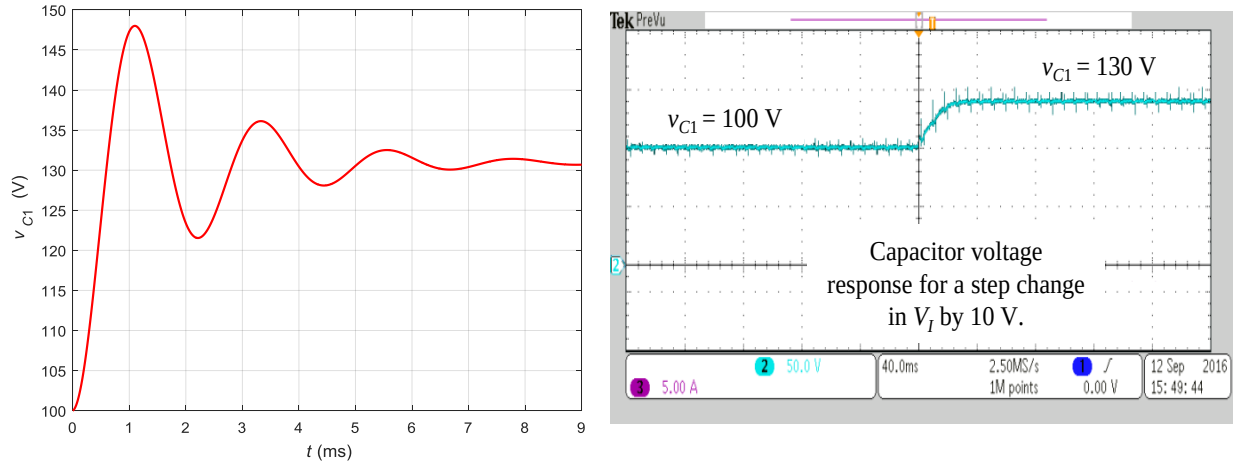


(a) (b)

Fig 15. Response of capacitor voltage v_{C1} for a step change in duty cycle by 0.1 at V_I = 50 V and R_L = 120 Ω. (a) Predicted. (b) Measured.



(a) (b)

Fig. 16. Response of capacitor voltage v_{C1} for a step change in input voltage by 10 V. (a) Predicted. (b) Measured.

good agreement up to half the switching frequency, thereby validating the derived small-signal models. The A-source converter is a non-minimum phase system and exhibits a zero in the right-half of the *s*-plane.

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2756626, IEEE Transactions on Power Electronics

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