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A Case Study of Bonaire Island Power System

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Article

The Impact of PLL Dynamics on the Low Inertia Power Grid: A Case Study of Bonaire Island Power System

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Abstract: To prepare for the future high penetration level of renewable energy sources, the power grid's technical boundaries/constraints for the correct operation of powerelectronics interfaced devices need to be further examined and defined. This paper investigates the challenge of integrating Voltage Source Converters (VSC) into low inertia power grids, where the system frequency can vary rapidly due to the low kinetic energy buffer available, which used to be provided by the rotational inertia of synchronous generators. The impact of rate of change of frequency (ROCOF) on the PLL dynamics and its subsequent influence on the VSC power stage output is explained. The Bonaire island network is presented as case study. The performance of the VSC is analyzed under a fast ROCOF event, which is triggered by a short circuit fault. A down-scaled experiment is used to validate the Bonaire island network simulation results. It shows that the phase angle error measured by the synchronous-reference frame phase-locked loop (SRF-PLL) is proportional to the slope of the ROCOF and inversely proportional to its controller integral gain constant.

Keywords: ROCOF; PLL; error; low inertia; VSC

1. Introduction

A weak grid is characterized as an AC power system with a low short-circuit ratio (SCR) and/or inadequate mechanical inertia (IEEE standard 1204-1997 [1]). Some recent studies [2–10] on the voltage-sourced converter (VSC) integration into a weak grid address only a weak grid with a high grid impedance, whilst the challenges associated with low inertia is seldom discussed. With the increase in renewable penetration in the AC power system, the system frequency stability margin decreases as the system inertia decreases. This leads to rapid frequency variations in low inertia power grids. Typically, for a large inter-connected power system, the total kinetic energy buffer provided by all the synchronous generators in the system is large. In this case, local disturbances (e.g., generator trip, load rejection, short circuit fault etc.) cause only mild frequency variation thanks to the total system mechanical inertia. However this is not the case with low inertia power grids, such as the Bonaire island grid. In Figure 1, a fault occurs in the 12 kV network and it is cleared after roughly 400 ms. From Figure 1, the frequency (red) plummets from 50 Hz to 46 Hz within 400 ms (i.e., ROCOF = 10 Hz/s) whilst the active (blue) and reactive power (green) consumption in the network jumped during the fault.

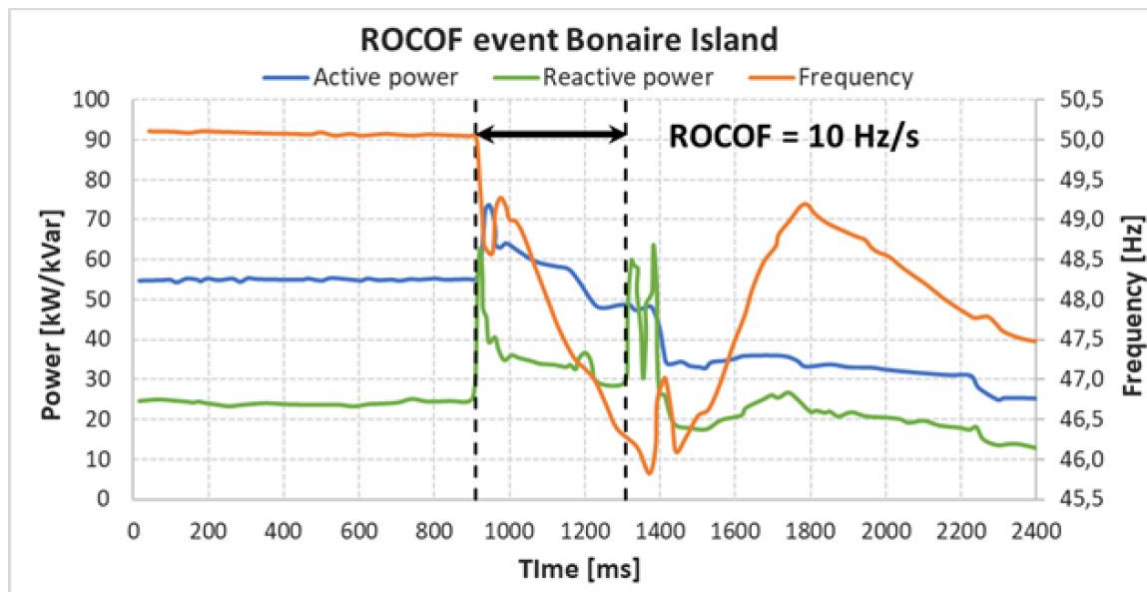


Figure 1. Fast rate of change of frequency (ROCOF) Event Triggered by a 12 kV short circuit fault on the Bonaire island grid—(red) system frequency y-axis on the right side, (blue) system active power consumption, (green) system reactive power consumption [11].

Inspired by this event and expected future challenges associated with battery storage, grid frequency support in a power grid with high penetration of renewable energy sources, this paper investigates the impact of fast rate of change of frequency (ROCOF) on the grid-connected VSC phase locked loop (PLL) dynamics. Although the ROCOF phenomena has already been mentioned in several papers concerning the design and analysis of the PLL alone for the anti-islanding detection [3,12,13] and the inertia emulation [14], the power grid mechanical inertia coupling is not considered. This paper explains the origin of the fault-induced fast ROCOF in the low inertia power grid. Thereafter, the mechanical inertia coupling is investigated using the case study of the Bonaire island, where the network model is validated and the mechanical inertia is represented by synchronous generator model in EMTDC/PSCAD. The case study results of the Bonaire island power grid is further verified by down-scaled experiments and the challenges associated with the fault-induced fast ROCOF on the grid-connected VSCs are discussed.

This paper is organized in four sections. Section 2 begins with the definition of the feedback control system error after which the PLL steady state error is derived. In Section 3, a detailed 850 kW VSC model created in EMTDC/PSCAD is introduced. Its stability is studied using a pole-zero diagram. In Section 4 the VSC dynamics under a fast ROCOF event is studied. First by considering the grid as a simple voltage source behind a given short circuit impedance. Then the VSC dynamic model is integrated into the validated Bonaire island power network model, where the mechanical inertia of diesel generators are also considered. With the coupling of the mechanical inertia, this case study investigates the VSC behavior under the fast ROCOF event triggered by a three-phase cable fault at the 12 kV level. A down-scaled experiment is performed to verify the EMTDC/PSCAD simulation results concerning the fault induced ROCOF in the Bonaire island power network. Finally, conclusions are drawn in Section 5.

2. PLL Modelling and Analysis

To understand the impact of fast ROCOF on the PLL dynamics, the definition of control system error is introduced first. Then the small signal dynamics of PLL is derived analytically with its steady state error expressed as a function of ROCOF frequency slew rate and PLL control integral gain constant (i.e., K_i). Despite the innovative concepts and implementations proposed in the literature,

the basic PLL structure remains largely unaltered [15,16] but enhanced with input signal filtering (e.g., bandpass filter realized by Second Order Generalized Integrator (SOGI)) and adaptive frequency tracking capability. In this section the PLL is implemented with the synchronous-reference frame (SRF) commonly used for the majority of three phase grid-connected applications.

2.1. Feedback Control System Error

For a typical three-phase SRF-PLL, its small signal transfer function is shown in Figure 2.

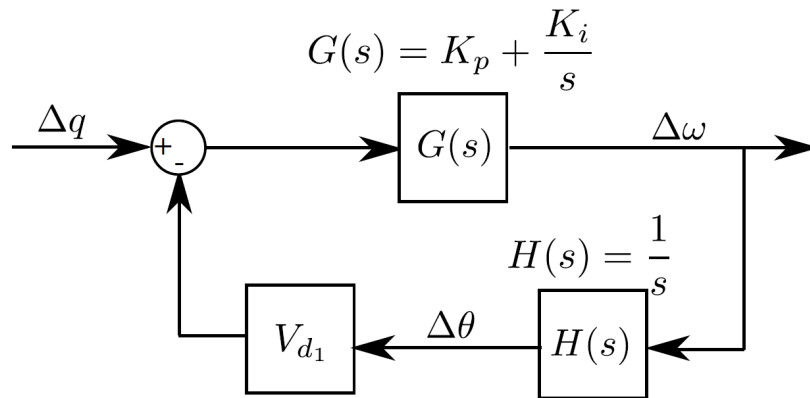


Figure 2. Phase locked loop (PLL) small signal closed loop transfer function diagram.

In Figure 2, Δq is the grid voltage space vector small perturbation projected on the q -axis of the SRF with respect to the steady-state operating point (i.e., q equals to zero), $\Delta\omega$ represents the PI controller output in rad/s, $\Delta\theta$ is the phase angle output, and V_{d1} is the grid voltage space vector projected on the d -axis of the SRF when the perturbation Δq is small. In the per unit system, V_{d1} can be normalized to 1, and Figure 2 can be simplified as shown in Figure 3.

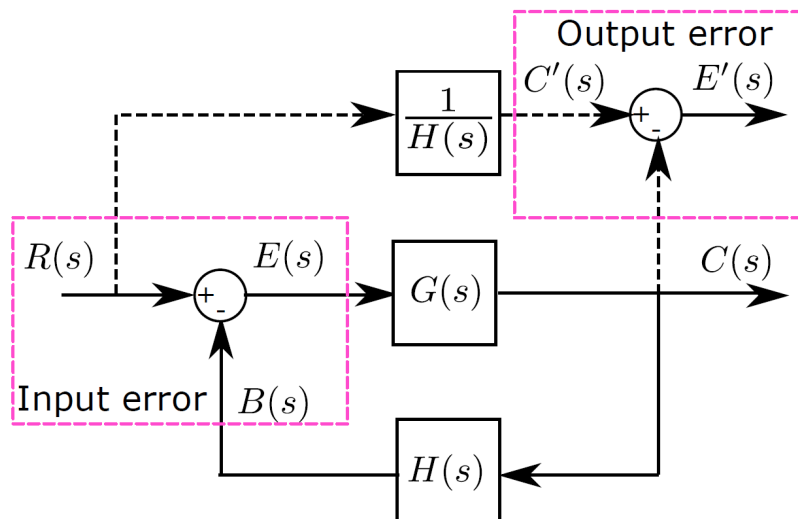


Figure 3. Feedback control system with input and output error definition.

To assess the small signal dynamic performance of a given feedback transfer function, the input error $E(s)$ is defined as the difference between input $R(s)$ and its closed loop feedback $B(s)$ i.e.,

$$E(s) = R(s) - B(s) = R(s) - C(s)H(s) \quad (1)$$

The relationship between input error and output error can be written as:

$$E'(s) = \frac{E(s)}{H(s)} \quad (2)$$

2.2. PLL Steady State Error

For the PLL feedback transfer function with $H(s) = \frac{1}{s}$, (2) provides the theoretical basis to explain the PLL steady-state frequency output error and phase angle output error. As the VSC power stage output depends on the accurate phase angle output from the PLL, we are thus interested in the phase angle output under the fast ROCOF event. When the system frequency is changing rapidly due to power system disturbances (e.g., generator trip, load change, faults etc.), the system frequency $f(t)$ and phase angle $\theta(t)$ deviation can be written as a function of time as follows:

$$f(t) = K_{ramp}t \quad (3)$$

$$\theta(t) = \frac{1}{2}K_{ramp}t^2 \quad (4)$$

where the $f(t)$ and $\theta(t)$ are the frequency and phase angle as function of time, t is the time, and K_{ramp} defines the ramp rate of frequency deviation. Following the input error definition (1), the steady-state phase angle error can be calculated by applying the final theorem and having $s \rightarrow 0$:

$$\begin{aligned} \lim_{s \rightarrow 0} sE(s) &= \lim_{s \rightarrow 0} sR(s) \frac{1}{1 + G_{open}(s)H(s)} \\ &= \lim_{s \rightarrow 0} \frac{K_{ramp}}{s^2} \frac{1}{1 + \frac{1}{s}(K_p + \frac{K_i}{s})} \\ &= \lim_{s \rightarrow 0} \frac{K_{ramp}}{K_i} \end{aligned} \quad (5)$$

Similarly the output frequency steady-state error can be calculated by inserting (5) into (2):

$$\lim_{s \rightarrow 0} sE'(s) = \lim_{s \rightarrow 0} s \frac{E(s)}{H(s)} = \lim_{s \rightarrow 0} \frac{sK_{ramp}}{K_i} = 0 \quad (6)$$

From (5), it can be seen that the phase angle will have a steady state error, which is a function of the ROCOF ramp rate K_{ramp} and PLL controller integral gain K_i . For a given ROCOF event, the K_{ramp} is largely fixed by the system inertia and the shortage/surplus of power caused by the transient event, hence the PLL output steady state phase angle error is determined by the integral gain K_i . To minimize the steady-state phase angle error during the fast ROCOF event, it is therefore beneficial to keep the PLL integral gain constant K_i high.

2.3. System Stability and PLL Controller Bandwidth

To allow for the rapid fundamental grid frequency tracking and phase angle determination, the PLL can be designed with a high control bandwidth. Yet, it is common practice to design the PLL with slow dynamics for stable operation. This is especially true under the high impedance power grid condition, where slower response of the PLL can filter out the terminal voltage variation caused by the active/reactive power injection [4] and limit the spurious harmonic current injection as a result of background voltage harmonics. Additionally, Wang et al. [17] points out that a high PLL control bandwidth could trigger harmonic instability of the VSC power stage output when the negative resistance region caused by the PLL impedance shaping effect intersects with the grid resonance point. Hence it is vital to design the PLL with slow dynamics in the high impedance grid for the overall VSC stable operation. Revisiting the conclusion from Section 2.2, one should opt to design the PLL with a high integral gain constant (K_i) yet low control bandwidth. From the control engineering

textbook [18], the controller bandwidth is defined as the frequency, where the close loop gain equals to -3 db. The closed loop transfer function of $\Delta\theta$ can be expressed as:

$$G_{PLLcl} = \frac{\Delta\theta}{\Delta q} = \frac{GH}{1 + GH} = \frac{K_p s + K_i}{s^2 + K_p s + K_i} \quad (7)$$

If the closed loop second order system (7) is represented in terms of its closed-loop roots natural damping frequency (ω_n) and damping factor (ξ) [19]:

$$G_{PLLcl} = \frac{K_p s + K_i}{s^2 + K_p s + K_i} = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (8)$$

where $\omega_n = \sqrt{K_i}$ and $\xi = \frac{K_p}{2\sqrt{K_i}}$. According to [18], when $\xi = 0.707$ (optimal damping) the closed-loop bandwidth (ω_{bw}) of the second order system depicted in (8) can be approximated by its closed-loop roots natural damping frequency (ω_n). Since $\omega_n = \sqrt{K_i}$, it is thus inevitable to have high steady-state phase angle output error under the fast ROCOF event when the PLL control bandwidth is kept low. Two sets of PLL parameters with 45 degree phase stability margin are proposed in Table 1. The PLL_{low} parameter set operates a PLL with low control bandwidth (i.e., $\omega_{bw} \approx 2.8$ Hz). PLL_{high} parameter set operates a PLL with high control bandwidth (i.e., $\omega_{bw} \approx 28$ Hz).

Table 1. PLL Parameters Selected for the Study.

Bandwidth (ω_{bw})	K_p	K_i
PLL_{low}	8.4	100
PLL_{high}	84	10,000

In the Section 4, the PLL parameters proposed in Table 1 and its influence on the VSC power stage output will be studies under a fast ROCOF event.

3. VSC Modelling and Analysis

To allow a holistic analysis of the impact of the ROCOF on the VSC power stage output considering the PLL dynamics, a generic switching VSC model of a 850 kW wind turbine is introduced in this section.

3.1. VSC Simulation Model

The main control system and the electrical parameters chosen for the 850 kW VSC are shown in Table 2. A typical cascaded control scheme is assigned to the 850 kW VSC simulation model as shown in Figure 4, where the outer loops are realized by two parallel PI controllers regulating the DC bus voltage and the reactive power output to a constant and inner-loop is realized by using proportional resonance (PR) controllers regulating the inverter side current dynamics. The reference value is indicated with * in their superscript. In Figure 4, v_c is the filter capacitor instantaneous phase to neutral voltage in the abc frame, i_1 is the inverter side instantaneous current in the abc frame, i_d^* and i_q^* are the current control loop references in-phase and quadrature with the grid voltage (i.e., v_c) in dq frame, P_1 and Q_1 are active and reactive power calculated at the filter capacitor side, v_{dc} and v_{dc}^* are the DC voltage and its reference setpoint respectively. K_p is the proportional gain of the PR controller and ω_0 is the frequency at which the PR controller resonant.

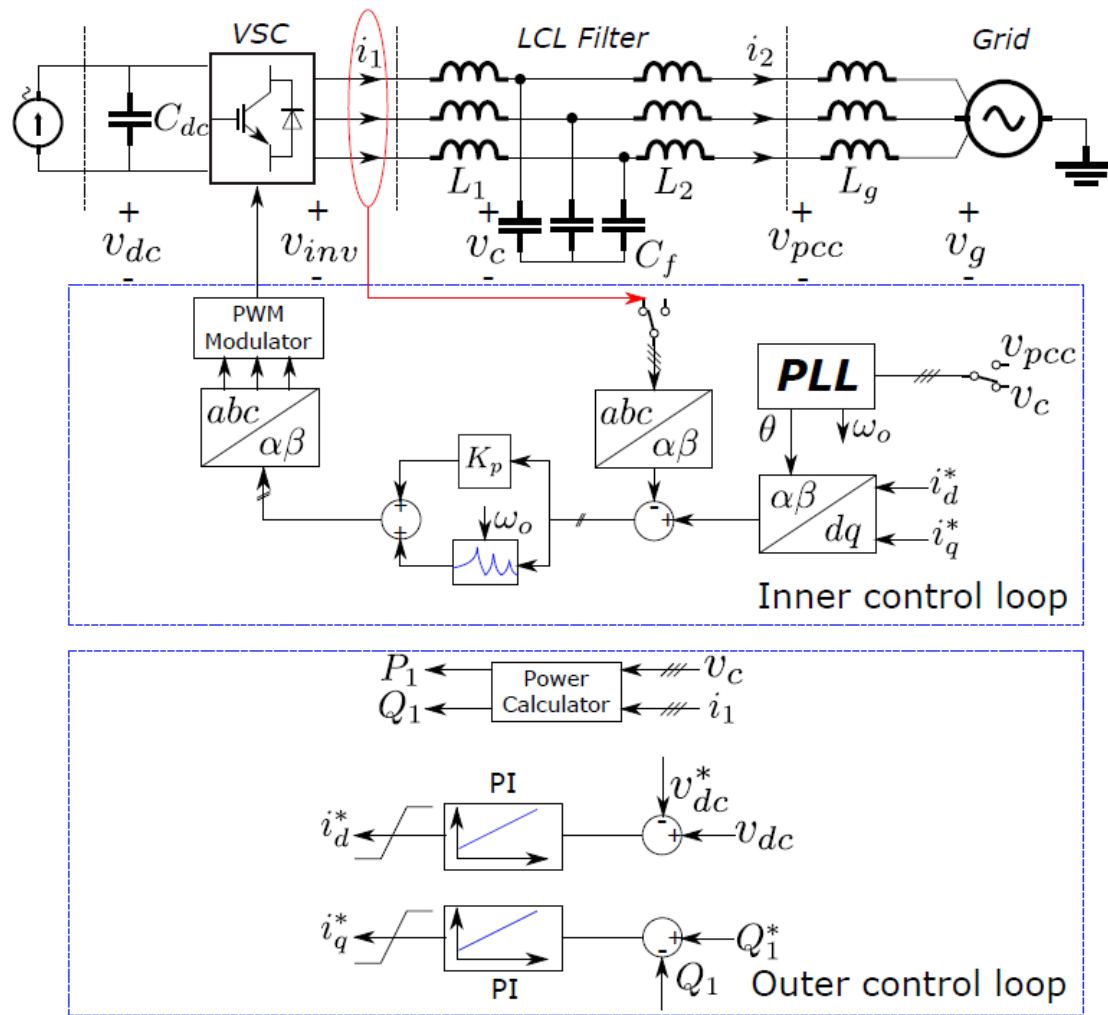


Figure 4. Voltage Source Converter (VSC) inner and outer control loop diagram for the study [20].

Table 2. VSC Main Parameters.

Parameter	Value	Unit
Rated Power	850	kW
DC Link Voltage V_{dc}	800	Volts
DC Link Capacitor C_{dc}	20	mF
AC Voltage V_{rms}	400	Volts
L_1 Inverter Side Inductor	80	μ H
R_1 Resistance of L_1	0.001	Ohm
L_2 Grid Side Inductor	80	μ H
R_2 Resistance of L_2	0.001	Ohm
C_f Filter Capacitor	425	μ F
R_f ESR of C_f	0.01	Ohm
Sampling Time T_s	100	μ s
Switching Frequency f_{sw}	5000	Hz
PR Proportional Gain K_p	1	p.u.
PR Integral Gain K_i	250	p.u.
PR Bandwidth ω_c	2	p.u.
DC Proportional Gain $K_{pv_{dc}}$	1	p.u.
DC Integral Gain $K_{iv_{dc}}$	100	p.u.
Q Proportional Gain K_{pQ}	1	p.u.
Q Integral Gain K_{iQ}	100	p.u.

3.2. VSC Stability Analysis

When the bandwidth of the inner and outer control loops are selected properly, then the inner loop and outer loop of the VSC control system can be considered as decoupled. From the VSC system stability point of view, the inner current control is directly interacting with the output filter circuit with a fixed operating point (i.e., reference signal received from outer control loop), hence the small-signal stability of VSC can be analyzed by deriving its closed-loop transfer function of current controller (Figure 5) and plotting it in a pole zero map (Figure 6). Figure 5, $G_{ic}(z)$ depicts the proportional resonance controller in Z domain with 10 kHz sampling time:

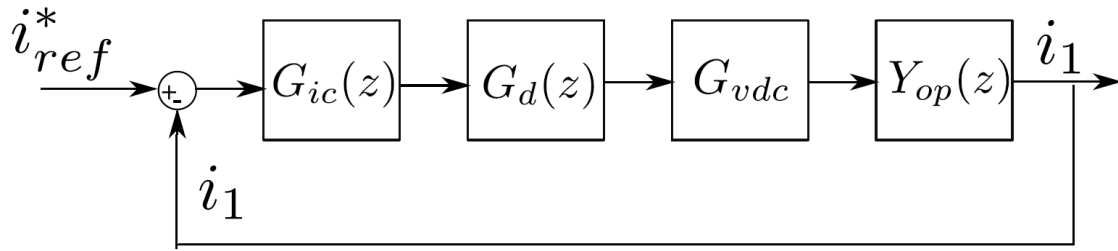


Figure 5. VSC Z Domain Current Control Loop Transfer Function Diagram.

$$G_{ic}(z) = \mathcal{Z} \left\{ K_p + \frac{2K_i\omega_c}{s^2 + 2\omega_c s + \omega_o^2} \right\} \Big|_{T_s=100 \mu s}^{Tustin} \quad (9)$$

where ω_o is the fundamental frequency output from the PLL, and ω_c is the bandwidth of the proportional resonance controller. $G_{vdc}(z)$ is half of the v_{dc} voltage (i.e., $800/2 = 400$ Volts) for a two-level VSC with bipolar switching:

$$G_{vdc}(z) = 400 \quad (10)$$

$G_d(z)$ indicates one sampling cycle digital computation delay:

$$G_d(z) = z^{-1} \quad (11)$$

The LCL filter transfer function block $Y_{op}(z)$ can be written as:

$$Y_{op}(z) = \mathcal{Z} \left\{ \frac{1}{L_f(s) + \frac{C_f(s)L_g(s)}{C_f(s)+L_g(s)}} \right\} \Big|_{T_s=100 \mu s}^{ZOH} \quad (12)$$

$$L_f(s) = L_1 s + R_1$$

$$C_f(s) = \frac{1}{C_f s + R_f} \quad (13)$$

$$L_g(s) = L_2 s + R_2$$

The parameters used in (9), (10), (12), (13) can be found in Table 2. In Figure 6, the proportional resonance controller parameters are calculated in proportion to the gain constant K ($K_p = 1 \cdot K$; $K_i = 250 \cdot K$), where K varies from $0 \rightarrow 2$ in step of 0.1. From the pole zero map, it indicates that when $K = 2$ the current controller is critically stable. When $K = 1$ is chosen, the dominant pole is approaching the optimal damping ($\xi = 0.707$) [18] and found the balance between the transient response speed and the overall system stability.

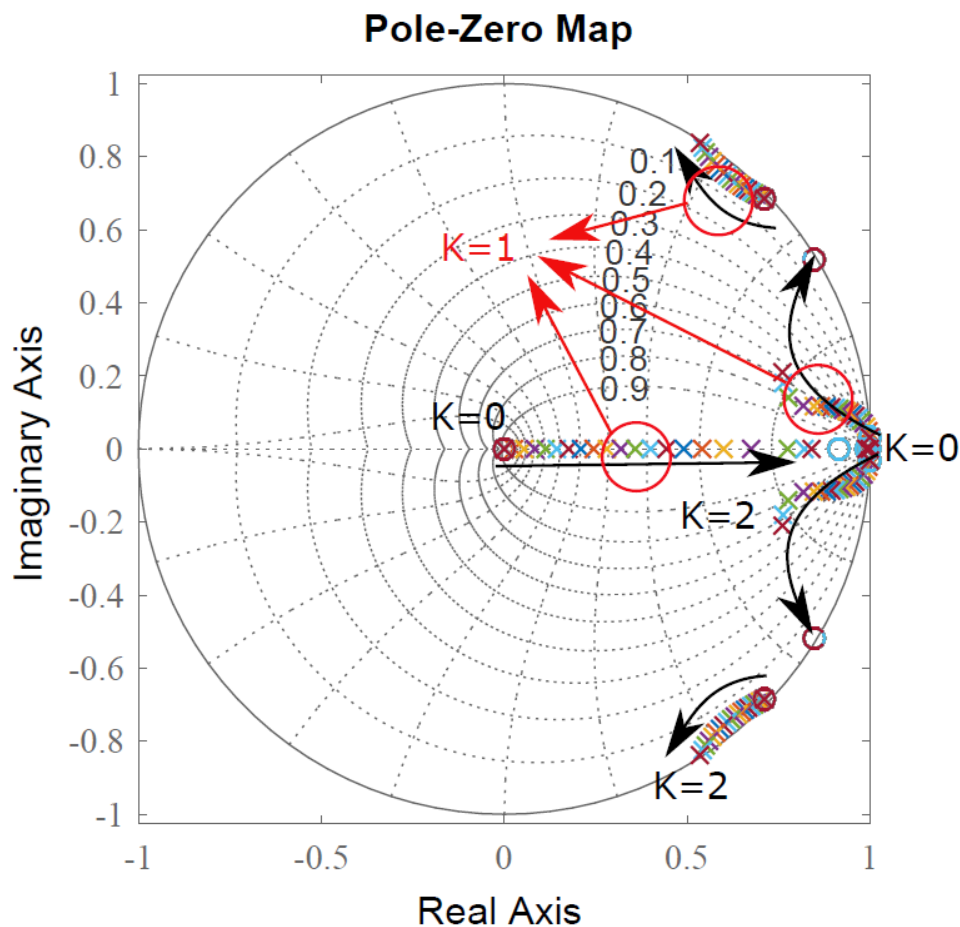


Figure 6. VSC Z-domain pole zero map of the inner current control loop.

4. Simulation and Experimental Results

This section presents the case study results of PLL dynamics under fast ROCOF. The detailed VSC model is firstly connected to a simple test network represented by an ideal voltage behind a short-circuit impedance, where the emulated fast ROCOF is triggered as a frequency ramp-down event. Next the VSC model is integrated with the validated Bonaire network model, and a fault-induced fast ROCOF event is triggered by applying a 400 ms three-phase fault on the 12 kV cable. Time domain simulation results under the fast ROCOF events are presented and a vector diagram based analysis is carried out to explain the phenomena. A down-scaled experiment is performed to verify the simulation results with Bonaire island power network.

4.1. Simulation Results—Simple Test Network

In this section, the detailed VSC electromagnetic transient model developed in Section 3.1 is connected to a simple test network model, where an ideal voltage source is connected in series behind a short-circuit impedance (Figure 7). To study the impact of a fast ROCOF on the PLL dynamics and the VSC power stage output, the ideal voltage source is triggered by a frequency ramp-down event (ROCOF = 10 Hz/s), where the mechanical inertia coupling is not considered.

Figure 8 presents the simulation results with a simple test network. The emulated frequency ramp-down event is shown by the green curve in Figure 8b, where system frequency starts to decline at 2 s and it settles at 46 Hz in 0.4 s (ROCOF = 10 Hz/s). Two sets of PLL parameters (see Table 1), namely the PLL with the high and low control bandwidth, are calculated on the same event. Looking at Figure 8b,c, the PLL with a high controller bandwidth (blue) tightly follow the frequency variation

(Figure 8b) with negligible phase error (Figure 8c) whilst the PLL with low controller bandwidth (red curves in Figure 8b,c respectively) exhibit inferior dynamic performance during the fast ROCOF event. Surprisingly the VSC power stage output (dashed line in Figure 8a) with low PLL bandwidth does not deviate significantly from its power set-point despite a significant phase angle error (red curve in Figure 8c).

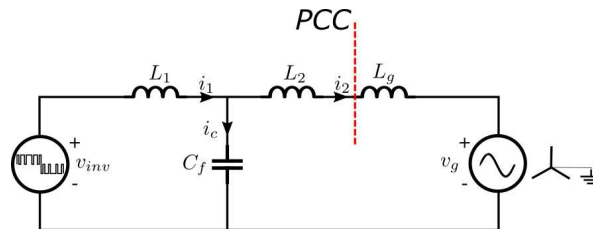


Figure 7. VSC dynamics under fast ROCOF connected to a simplified network.

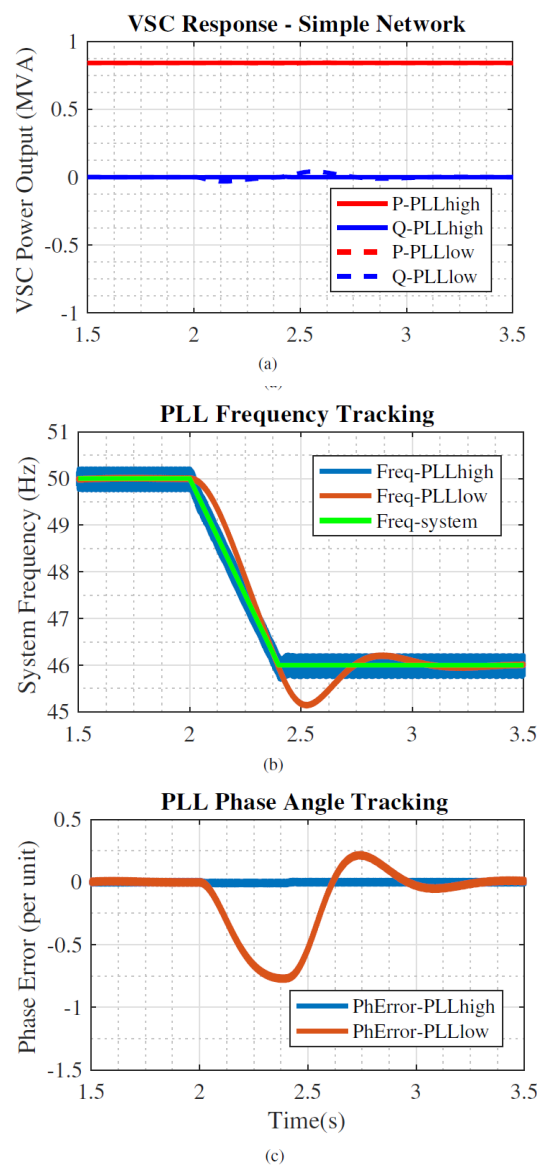


Figure 8. Simulation results with a simplified network and different PLL parameters (see Table 1)—(a) VSC output (b) PLL frequency tracking (c) PLL phase angle tracking.

In Figure 9, the direct (I_{dref}^*) and quadrature (I_{qref}^*) current reference is shown. For the case with a high PLL controller bandwidth, its current controller reference point is maintained the same during the fast ROCOF event (solid line in Figure 9). However, this is not the case when the PLL controller bandwidth is low. In order to maintain the VSC output power during the fast ROCOF event, the phase angle error introduced by the PLL will be counteracted by the outer controller loop which constantly regulates the direct (I_{dref}^*) and quadrature (I_{qref}^*) current reference (dotted and dashdotted line in Figure 9).

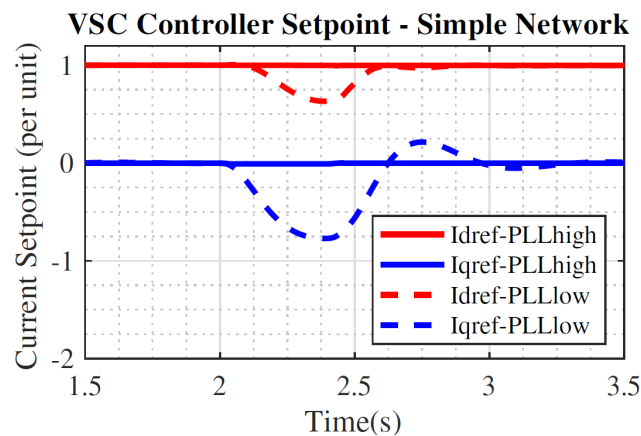


Figure 9. Current controller reference signal from dual outer loop controllers—PLL with low bandwidth (dash line), PLL with high bandwidth (solid line).

A detailed explanation of the fast ROCOF impact on the PLL dynamics and the subsequent VSC power stage output can be made by the vector diagram shown in Figure 10. Take the PLL with low controller bandwidth for example, when the fast ROCOF event initiates, a phase angle error (Δq) occurs between the actual grid voltage vector (U_{s1}) and the d-axis of rotating frame. Both i_d and i_q will project in phase and quadrature component on the actual grid voltage vector (U_{s1}). Effectively, this indicates the coupling of the active and reactive power in the control, and this can be compensated by the outer loop power flow controllers. In fact, the PI controller embedded in the outer loop controller increase the PLL controller from type II to type III making it capable of maintaining VSC power stage output despite the large phase angle error.

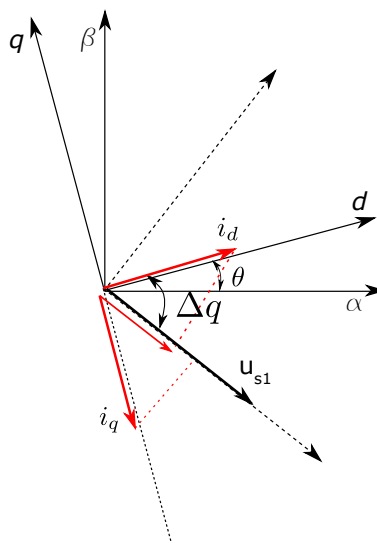


Figure 10. Vector diagram illustrating PLL dynamics under fast ROCOF.

4.2. Simulation Results—Bonaire Island Power System

In this section the simple test network is replaced by a simplified Bonaire island network (see Figure 11) with 5 diesel generators in service supplying a total system load of 12 MW/6 MVar lumped at the main 12 kV distribution substation, technical details related to the network structure, the dynamic diesel generator controllers, and the validation results are included in [21]. For the simplified Bonaire island network model, the inertia aspect is included in the PSCAD generator model. Similar to the actual fault record in Figure 1, where the fast ROCOF is induced by the 12 kV system fault, here for simplicity a balanced three-phase fault on the 12 kV system (400 ms fault clearing time, 20% voltage dip) and the dynamic behavior of a generic 850 kW wind turbines model is observed under a fault induced fast ROCOF event.

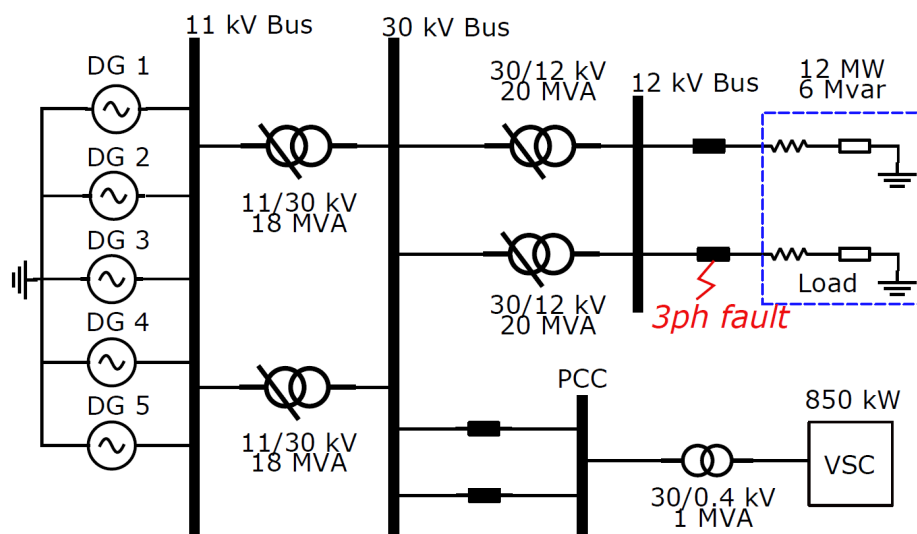


Figure 11. Single line diagram of Bonaire Island power system.

Figure 12 demonstrates the simulation results when the VSC is coupled to the simplified Bonaire island network. A simulated three phase 12 kV cable fault causes the total system consumption to increase (Figure 12b) and the system frequency decreases sharply from approximately 50 Hz to 47.5 Hz in 400 ms (Figure 12c). When the fault occurs in the network (for 20% voltage dip), the grid-connected VSC will run into the low voltage ride through (LVRT) mode and inject active/reactive power per grid code requirement. With reference to [7,22,23], anti-windup will freeze the outer loop controller integral input (i.e., set to 0) and the inner current controller current reference (I_{dcode}^* & I_{qcode}^*) is calculated according to the grid code requirement (see Figure 13). For this study, the LVRT strategy sets the $I_{dcode}^* = 1.0 pu$ and $I_{qcode}^* = 0.0 pu$ for the maximum active power delivery.

In the case of a fault induced fast ROCOF, the LVRT strategy will fix the current controller reference given by the grid code requirement. For the PLL with a low control bandwidth, the large phase angle error will effectively cause the coupling of active and reactive power control as explained in Section 4.1 with the vector diagram (Figure 10). For the LVRT strategy with maximized active power delivery, the results from Figure 12a indicates that the VSC output with a low PLL control bandwidth (dashed line in Figure 12a) delivers less active power and consumes additional reactive power from the grid during the fault induced fast ROCOF event.

4.3. Experimental Results

A down-scaled experimental setup is built to verify the analytical/simulation results concerning the fast ROCOF effect on the PLL dynamics. Chroma 61845 has been used to emulate the low inertia grid condition of Bonaire island power system. The VSC is implemented by a Danfoss FC103P11KT 11 converter and the control algorithms are programmed in dSPACE1007. The parameters of the inverter are summarized in Table 3 and the experimental setup is shown in Figure 14.

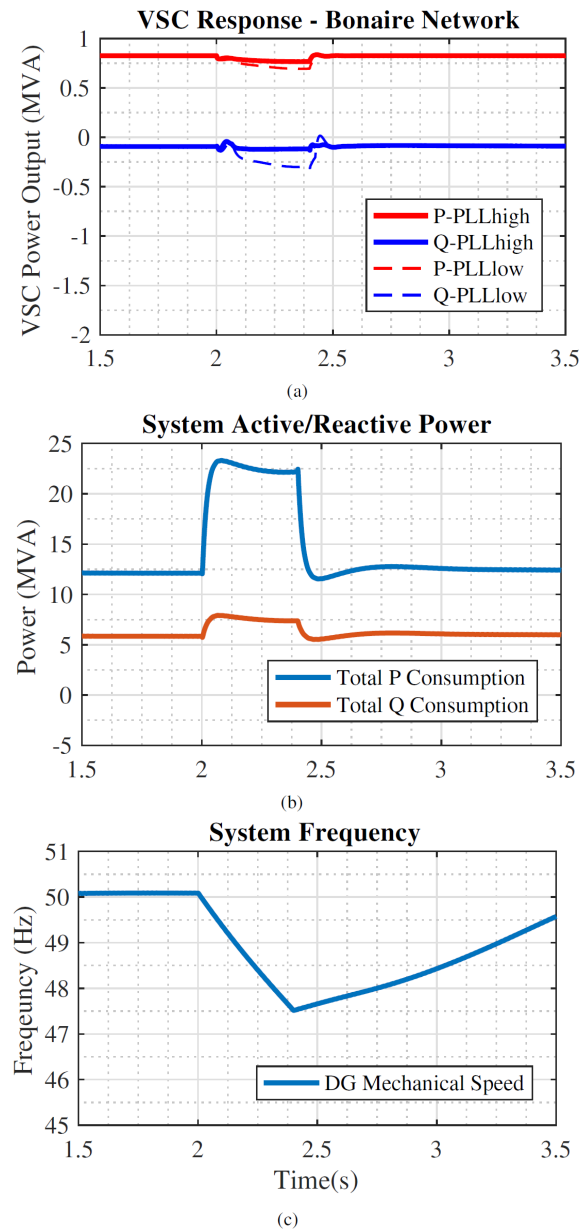


Figure 12. Simulation results with Bonaire island power network using different PLL control bandwidths—(a) VSC power output (b) Total active/reactive power consumption (c) System frequency measured by the diesel generator mechanical speed.

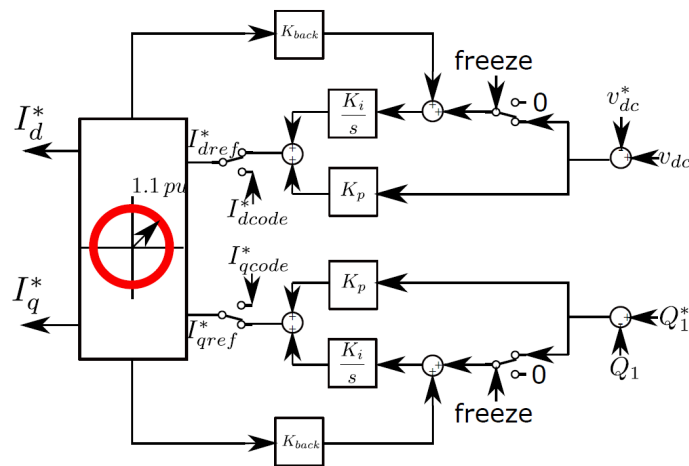


Figure 13. LVRT strategy for 850 kW voltage source converter.

Table 3. Parameters of inverter for experiment verification.

Parameter	Value	Unit
Rated Power	2	kW
Grid fundamental frequency	50	Hz
DC Link Voltage V_{dc}	730	Volts
DC Link Capacitor C_{dc}	1500	μF
AC Voltage V_{rms}	400	Volts
L_1 Inverter side inductor	1500	μH
L_t Equivalent grid-side inductor ($L_2 + L_g$)	1500	μH
C_f Filter capacitor	5	μF
Inverter control sampling frequency f_s	10	kHz
Inverter switching frequency f_{sw}	10	kHz

In this down-scaled experiment, a three-phase fault (20% voltage dip and 10 Hz/s ROCOF) is emulated by the regenerative grid simulator Chroma 61845 and cleared after 400 ms. Figure 15a demonstrates the experimental results when the inverter is operated with the low bandwidth PLL parameters (see Table 1). The inverter is firstly operated in normal operating condition with 2 kW active power output and 0 kVA reactive power output. Then the three-phase fault is initiated and cleared after 400 ms. During the fault, the frequency decreased from 50 Hz to 46 Hz (i.e., 10 Hz/s ROCOF), and the q-axis voltage deviated from zero indicating a large θ angle error.

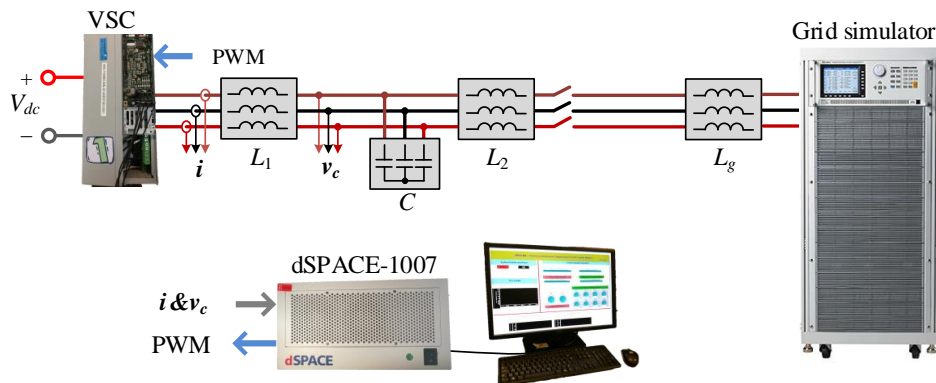
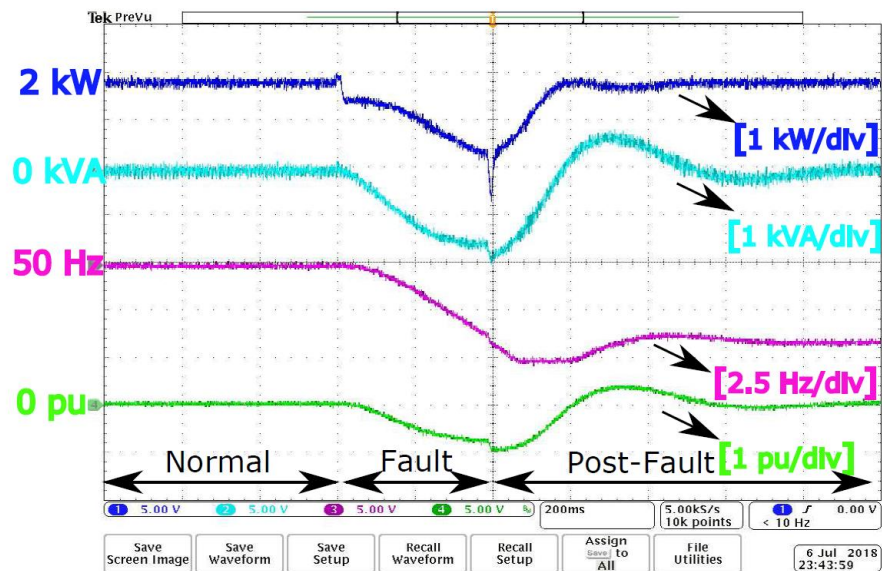


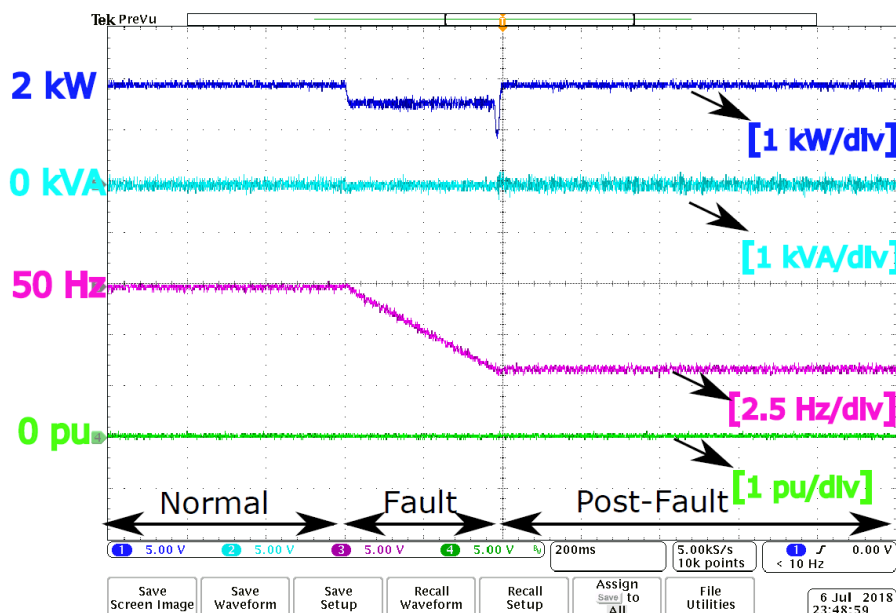
Figure 14. Single line diagram of bonaire island power system.

Figure 15b shows the experimental results when the inverter is operated with the high-bandwidth PLL parameters (see Table 1). For the LVRT strategy with maximized active power delivery,

experimental results confirm that the VSC output with a low PLL control bandwidth (Figure 15a) will deliver less active power and consumes additional reactive power from the grid. With increased renewable energy penetration, less active power delivery in the low inertia grid will not only threaten the frequency stability but also worsen the transient frequency nadir. Additionally, extra consumption of reactive power from the grid during the fault condition will hinder the voltage recovery following the fault clearance.



(a)



(b)

Figure 15. Experimental results with fault induced ROCOF of 10 Hz/s—(a) Inverter response during fault induced fast ROCOF with low bandwidth PLL parameters, (b) Inverter response during fault induced fast ROCOF with high bandwidth PLL parameters.

5. Conclusions

Based on the fault record in the Bonaire island grid, this paper investigates a low inertia power grid scenario, where the system frequency varies rapidly due to the low kinetic energy buffer provided by

the synchronous generator's mechanical inertia. For a PLL with low controller bandwidth, the phase angle error can effectively be counteracted by the outer loop PI controller regulation. However, for the fault induced fast ROCOF as recorded in the Bonaire island power grid, the existing LVRT strategy shown in the literature will freeze the outer loop PI controller and calculate the current controller reference directly according to the grid code requirement. Simulation results in a simplified Bonaire island network indicate that the VSC with a low PLL dynamics delivers less active power to the grid whilst it consumes additional reactive power during the fault induced fast ROCOF. A down-scaled experimental setup was used to verify the analysis/simulation results of the simplified Bonaire network.

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