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Finite-Time Large Signal Stabilization for High Power DC Microgrids with Exact Offsetting of Destabilizing Effects

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***Abstract*—The interleaved dual boost converter (IDBC) is a promising topology to interface high power solar PV generation or energy storage systems to DC microgrids (MGs). It provides a high boost ratio for voltage transformations and helps significantly to reduce ripples in the currents drawn from DC sources. However, the conventional control methods of IDBC cannot guarantee system stability in the presence of tightly regulated and rapidly varying power electronic loads which behave as constant power loads (CPLs). Moreover, the uncertainties of converter systems may further affect the stability of MGs. In this context, a large signal stabilization scheme, which comprises finite-time observers (FTOs) and a finite-time controller (FTC), is proposed. By considering CPLs and parameter dispersions as system disturbances, FTOs are able precisely observe the disturbances in finite time. Then the FTC exactly offsets the estimated values and stabilizes all system states at their designated points in finite time. By doing so, the finite-time large signal stability can be obtained and the corresponding results are proved with Lyapunov theorems. A detailed control parameter selection guideline is provided for practical applications. Simulations show that the proposed method gives a wider stability margin than the conventional PI (proportional-integral) control. Furthermore, experiments verify its effectiveness and feasibility.**

***Index Terms*—DC microgrid, nonlinear finite-time controls, large signal stabilization, interleaved dual boost converter.**

I. Introduction

In a DC microgrid (MG), distributed generators (DGs), energy storage systems (ESSs) and renewable energy sources (RESs) have their own terminal output voltages, which may be at low voltage levels [1]–[3]. It is not economically possible and also inconvenient to continuously stack up the DC sources to obtain high voltages. Furthermore, the unregulated source voltages may easily deviate from the required level with heavy loads, possibly damaging voltage-sensitive equipment. To overcome these difficulties, a widely accepted solution is use step-up converters to boost the source voltage to a wanted level. Conventional boost converters (CBCs) would be representatives. However, as highlighted in [4], CBCs have a limited boost ratio due to the existence of capacitor- and inductor-parasitic resistors. In addition, inductor current saturation problems also make CBCs not suitable for high power applications [5]. Although transformers can be used together with CBCs to accommodate high voltage AC applications, the configuration is not recommended for systems requiring high power density and low costs, as the transformers need additional capital investments and space. Moreover, when interfacing converters are linked to DC sources, current ripples should be suppressed within an acceptable range, to potentially prolong the source useful life.

To improve the voltage ratio and maintain small current ripples, an interleaved dual boost converter (IDBC) containing two mirrored interleaved boost converters (IBC) was proposed in [6]. Each IBC has N CBCs connected in parallel, and the complementary pair switches of CBCs are controlled by pulse-width modulation (PWM) signals with phase shifts. In this way, ripples in the current drawn from a DC source can be remarkably reduced. For IDBCs, the potential difference between the positive port of the upper IBC and the negative port of the lower is defined as the total output voltage. Therefore, IDBCs generally have much higher voltage ratios than CBCs, allowing for wider voltage operation ranges and more flexible selection of the rated bus voltage [6], [7].

For an IDBC-enabled high power DC MG, stable system operation is an important issue. However, many modern active loads, such as motor drives and power electronic loads when tightly regulated, behave as constant power loads (CPLs). These CPLs tend to draw constant power disregarding DC bus variations. From the small signal point of view, CPLs present incremental negative impedances that may interact with source converters posing threats to MG stability [8]–[10]. The DC MG stability can further deteriorate when CPLs vary rapidly in a wide range, introducing large signal disturbances to the system. Furthermore, when IDBC are working in a long run, converter parameters (e.g., capacitances and inductances) may drift away from their nominal and real values, causing parameter uncertainties, which will also aggravate the MG stability. To stabilize DC MGs, both linear and nonlinear approaches have been presented in the literature.

The simplest linear method is to add passive components (resistors) into DC networks to increase the system damping [11], [12]. However, the components will inevitably consume power, which downgrades the overall system efficiencies. Thus, in [13], active damping methods are proposed to modify the DC

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converter control loop to emulate resistances, but the methods may sacrifice CPL performances. In [14], diverse versions of virtual resistors are incorporated into DC MGs to revise system minor loop transfer functions. A frequency-adaptive low pass filter is reported in [15] to mitigate the destabilizing effects caused by the CPLs. A passivity-based control scheme is examined in [16] where the output and input impedances of source converters and CPLs are all shaped to have positive real parts. Then the entire DC MG is passive with a wide stability margin. Controller designs based on passivity rules can also be found in [17] and [18]. It should be mentioned that most linear stabilizations are derived based on small signal models which are merely effective around a particular equilibrium, and there is no indication of how far away from the equilibrium that the linearizations maintain valid.

In contrast, nonlinear approaches consider the converter intrinsic nonlinearities and are expected to attain the system stability in a full operating range. For example, a virtual capacitor controller is presented in [19], where the region of attraction can be estimated by fuzzy modeling and establishing linear matrix inequalities (LMIs). The LMI technique is further implemented in an AC system to predict the maximum apparent power of sources [20]. A shunt active damper derived from the LMI is also shown in [21] to reinforce the DC bus stability in the large signal sense. Yet, these LMI enabled controllers require an iterative evaluation of LMI tools, which would not be applicable for online operations. In [22], a model predictive control is designed to achieve an optimal trade-off between CPL impedance modification and DC voltage variation. However, similar to [17], the predictive controller assumes that the power quantity of the CPL is known and the desired stabilization may fail when there is a substantial CPL variation. In [23], a composite controller helps to realize the large signal stability of DC MG in a decentralized way. Follow-up efforts are made in [24], where a novel fine-tuning factor is introduced into the controller, helping to refine transient dynamics without affecting stability. It is worth mentioning that the controller designs in [23], [24] presume that the high order derivatives of CPL changes are bounded. DC power systems are input-to-state stable in theory, and only rough estimations are accomplished. In [25], a large signal stability criterion based on a complex mixed potential theory is proposed. However, the criterion is deduced based on a simplified linear system, which cannot be generalized to nonlinear converter models. In [26], a family of sliding mode controller is proposed to tailor the system convergence rate in either semiglobal/global finite-time or fixed-time. In [27], the system convergence and transient responses can be estimated by designing a quadratic Lyapunov function.

To resolve the problem recognized in the existing works and fill up the gap that rare studies focus on the stability of high power DC MG enabled by the IDBC, a finite-time large signal stabilization scheme is proposed in this paper. The scheme introduces a proper coordinate transformation to map the original states of IDBC into a new space. The dynamics of the newly-formulated states are disturbed by CPLs as well as system parameter uncertainties. Next, by means of premium finite-time observers (FTOs), unlike [23], [24] where observer gains are intentionally enlarged to suppress observing errors, system disturbances under the proposed scheme can be accurately tracked in finite time. Then a nonlinear finite-time control (FTC) law is designed to exactly offset the destabilizing effects imposed by CPLs and uncertain parameter variations, and the large signal

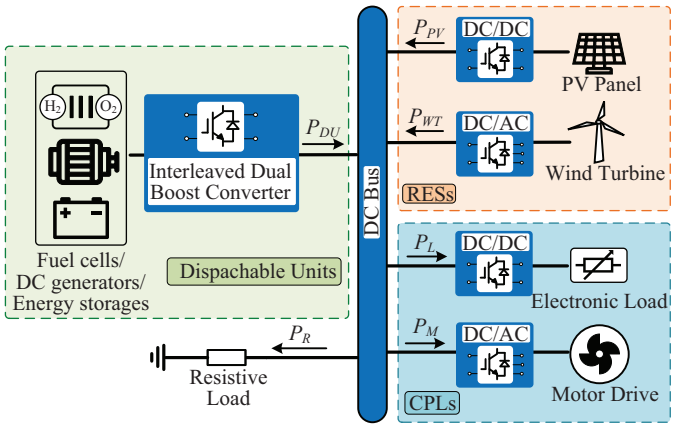

Fig. 1. A DC MG with dispatchable units (DUs), renewable energy sources (RESs), constant power loads (CPLs) and resistive load.

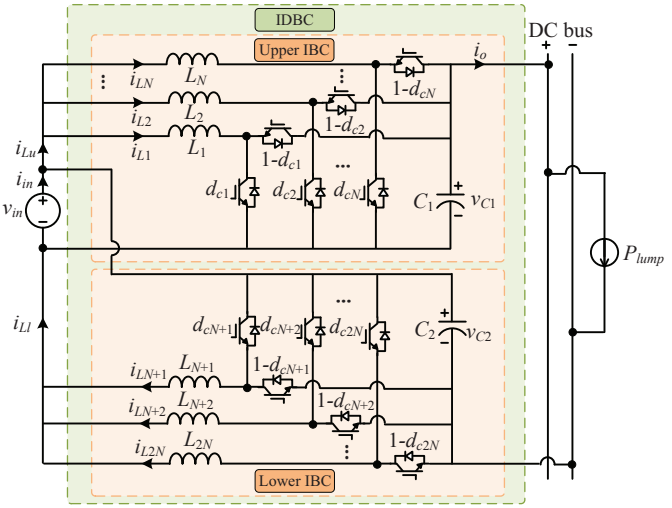

Fig. 2. A simplified high power DC MG with an interleaved dual boost converter (IDBC) feeding an equivalent lumped load (P_{lump}).

stabilization for the high power DC system can also be proved with Lyapunov theorems. Note that the stabilization scheme is arguably implemented in the IDBC based high power application for the first time. Its advantages can be summarized as follows:

- There is no requirement of using any specific stability criteria. The finite-time stabilization is autonomously guaranteed in the large signal sense under the proposed scheme.
- There is no local linearization around a specific equilibrium. The DC system can operate at any designated point as long as the point is in the range permitted by hardware.
- There are no destabilizing impacts of CPLs and parameter dispersions intruding into the closed-loop control system. System performances can be rapidly recovered even in the case of fierce loading changes.

The remaining of this paper is organized as follows. Section II describes the system layout and modeling. FTOs and FTC are designed in Section III, where large signal stability analyses are provided. Simulations and experimentations are provided in Sections IV and V. Finally, Section VI concludes the contributions.

II. System Description and Modeling

Fig. 1 shows a typical DC MG integrated with PV panels, wind turbines, electronic loads, motor drives and some other power sources. Maximum power point tracking algorithm should be applied to optimize the energy harvesting from PVs and

wind turbines. As explained in [28], electronic loads and motor drives can be modeled as CPLs. Resistive loads are passive components that will contribute to the damping in the DC system. The electrical sources, e.g., fuel cells, DC generators and energy storages are defined as dispatchable units (DUs) since they can be scheduled to regulate the DC bus voltage. These DUs can be interfaced with IDBCs to be applied at higher power. According to Fig. 1, the power balancing equation can be expressed as

$$P_{DU} = P_{lump} = P_R + P_L + P_M - P_{PV} - P_{WT}. \quad (1)$$

where P_R, P_L, P_M stand for the powers consumed by resistive load, electronic load and motor drive. P_{PV} and P_{WT} represent the powers produced by PV panel and wind turbine.

To have a clear view on the implementation of the large signal stabilization scheme in the IDBC and to better illustrate the system modeling, an IDBC enabled high power DC MG is displayed in Fig. 2. As mentioned previously, there are two IBCs mirrored to each other. Each IBC has N bridges accepting PWM signals with shifted phases for a given duty ratio. In reality, the inductances of the upper or lower IBC are designed to be identical for system symmetry and the ease of converter controls. Then, as in [6], the reduced-order IDBC model can be given as

$$\begin{cases} L_u \dot{i}_{Lu} = v_{in} - (1-d_u)v_{C1}, & (2a) \\ C_1 \dot{v}_{C1} = (1-d_u)i_{Ll} - i_o, & (2b) \\ L_l \dot{i}_{Ll} = -(1-d_l)v_{C2} + v_{in}, & (2c) \\ C_2 \dot{v}_{C2} = -i_o + (1-d_l)i_{Ll}. & (2d) \end{cases}$$

where $i_{Lu} = \sum_{j=1}^{N} i_{Lj}$ and $i_{Ll} = \sum_{j=N+1}^{2N} i_{Lj}$ are the summed equivalent current of two IBCs, respectively. In the upper IBC, since N inductors are connected in parallel, the equivalent inductances are calculated as $L_u = (1/N)L'_u$ where L'_u is the nominal value of L_j $(j = 1, ..., N)$. Similarly, the equivalent inductance in the lower IBC can be written as $L_l = (1/N)L'_l$ with L'_l the nominal value of L_j $(j = N+1, ..., 2N)$. d_u and d_l are duty ratios that are uniformly applied to the N bridges in IBCs, which means $d_u = d_1 = ... = d_N$ and $d_l = d_{N+1} = ... = d_{2N}$ [6]. u_{C1} and u_{C2} represent the terminal voltages of IBCs. C_1 and C_2 are the output capacitors. $i_o = \frac{P_{lump}}{v_o}$ is the output current where v_o is instantaneous DC bus voltage. Applying Kirchoff's circuit laws to the IBFC topology, the equations describing the relation of v_{in} and v_o and the relation of i_{in} and i_o, can be given as follows,

$$v_o = v_{C1} + v_{C2} - v_{in} \quad (3)$$

$$i_o = i_{Lu} + i_{Ll} - i_{in} \quad (4)$$

By setting the left hand sides in (2a) and (2c) to be zeros while assuming that d_u and d_l have the same static value D, the voltage ratio of IDBC can be given in (5) with the consideration of (3),

$$\frac{V_o}{V_{in}} = \frac{1+D}{1-D} \quad (5)$$

where V_o and V_{in} are the steady state values of the bus voltage and input voltage, respectively.

III. Proposed Finite-time Large Signal Stabilization Scheme

For proper regulation of the system in (2), there are three challenges. Firstly, duty cycles (d_u and d_l) are entangled with state variables (i_{Lu}, i_{Ll}, v_{C1} and v_{C2}). These entanglements will incur nonlinear terms to the IDBC and cause difficulties for conventional linear controllers to stabilize the DC MG. Secondly, the output current i_o is de facto induced by the power profile of P_{lump}. Notice from Fig. 1 and (1) that P_{lump} inherently incorporates all possible nonlinear dynamics of both CPLs and RESs. In this sense, the nonlinearity of CPLs and RESs would be introduced into the IDBC, which unnecessarily complicates the original system. Thirdly, the reduced model (2) merely utilizes nominal inductances and capacitances. However, for N bridges in the upper and lower IBCs in Fig. 2, there do exist differences among inductances, and inductances/capacitances would also deviate from their nominal values along with the aging of devices. These parameters uncertainties, if not treated properly, will impair control system stability.

To address the above challenges in the IDBC, a finite-time large signal stabilization is presented in this section. Coordinate transformations are performed to express (2) into a canonical system coupled with disturbances. Then, FTOs and a FTC are designed to completely cancel the underlying destabilizing effects, and also ensure large signal stability under Lyapunov framework.

A. System States Mapping

For the IDBC model in (2), system state vector [i_{Lu}, v_{C1}, i_{Ll}, v_{C2}]$^\top$ is in a four dimensional Euclidean space. To facilitate large signal stabilization, these states can be mapped into a new space and expressed as [29],

$$\begin{cases} z_1 = 0.5L_u i_{Lu}^2 + 0.5C_1 v_{C1}^2, & (6a) \\ z_2 = v_{in} i_{Lu}, & (6b) \\ z_3 = 0.5L_l i_{Ll}^2 + 0.5C_2 v_{C2}^2, & (6c) \\ z_4 = v_{in} i_{Ll}. & (6d) \end{cases}$$

Taking the differentiations of z_1, z_2, z_3 and z_4 results in,

$$\begin{cases} \dot{z}_1 = v_{in} i_{Lu} - v_{C1} i_o = z_2 + d_1, & (7a) \\ \dot{z}_2 = u_u + d_2, & (7b) \\ \dot{z}_3 = v_{in} i_{Ll} - v_{C2} i_o = z_3 + d_3, & (7c) \\ \dot{z}_4 = u_l + d_4, & (7d) \end{cases}$$

where $d_1 = -v_{C1} i_o + \tilde{d}_1$ and $d_3 = -v_{C2} i_o + \tilde{d}_3$ are the disturbances induced by the lumped DC load, $\tilde{d}_1$, d_2, $\tilde{d}_3$ and d_4 represent the disturbances caused by the possible parameter uncertainties and unmodeled dynamics, u_u and u_l are the equivalent control inputs which can be transformed into original duty cycles by the following equations:

$$u_u = v_{in} \dot{i}_{Lu} = \frac{v_{in}^2 - (1-d_u)v_{in}v_{C1}}{L_u}, \quad (8)$$

$$u_l = v_{in} \dot{i}_{Ll} = \frac{v_{in}^2 - (1-d_l)v_{in}v_{C2}}{L_l}. \quad (9)$$

After several mathematical manipulations on (8) and (9), d_u and d_l can be expressed in terms of u_u and u_l, respectively,

$$d_u = \frac{v_{in}(v_{C1-v_{in}}) + u_u L_u}{v_{C1} v_{in}}, \quad (10)$$

$$d_l = \frac{v_{in}(v_{C2-v_{in}}) + u_l L_l}{v_{C2} v_{in}}. \quad (11)$$

B. Finite-time Observer Design

It can be seen from (7) that the bilinear items in the rudimentary IDBC model have been subtly avoided in the new state dynamics. That is, the first challenge has been tackled. As for the other two challenges due to nonlinear lumped load and converter internal parameter uncertainties, they are detached from the state variables and collectively expressed as d_j $(j = 1, 2, 3, 4)$. To neutralize the destabilizing effects imposed by the disturbances, FTOs are designed that can exactly estimate the disturbances in finite time.

It is assumed that the disturbances d_js are continuously differentiable and their high order derivatives are bounded, i.e., $d_j \in L_\infty$ and $\max_{j,r}\{\sup|d_j^{(r)}|\} \leqslant D$ $(r = 1, 2, 3)$. The assumption is reasonable for most of the dynamic systems as all the disturbances have physical meanings.

For (7a) and (7b), the FTOs are given as [30].

$$\begin{cases} \dot{z}_{1,0} = z_2 + \kappa_{1,0},\ \dot{z}_{1,1} = \kappa_{1,1}, \\ \dot{z}_{1,2} = \kappa_{1,2},\ \dot{z}_{1,3} = \kappa_{1,3}, \\ \kappa_{1,0} = z_{1,1} - l_{1,0}\alpha^{\frac{1}{4}}\text{sig}^{\frac{3}{4}}(z_{1,0} - z_1), \\ \kappa_{1,1} = z_{1,2} - l_{1,1}\alpha^{\frac{1}{3}}\text{sig}^{\frac{2}{3}}(z_{1,1} - \kappa_{1,0}), \\ \kappa_{1,2} = z_{1,3} - l_{1,2}\alpha^{\frac{1}{2}}\text{sig}^{\frac{1}{2}}(z_{1,2} - \kappa_{1,1}), \\ \kappa_{1,3} = -l_{1,3}\alpha\text{sign}(z_{1,3} - \kappa_{1,2}); \end{cases} \tag{12}$$

$$\begin{cases} \dot{z}_{2,0} = u_u + \kappa_{2,0},\ \dot{z}_{2,1} = \kappa_{2,1},\ \dot{z}_{2,2} = \kappa_{2,2} \\ \kappa_{2,0} = z_{2,1} - l_{2,0}\alpha^{\frac{1}{3}}\text{sig}^{\frac{2}{3}}(z_{2,0} - z_2), \\ \kappa_{2,1} = z_{2,2} - l_{2,1}\alpha^{\frac{1}{2}}\text{sig}^{\frac{1}{2}}(z_{2,1} - \kappa_{2,0}), \\ \kappa_{2,2} = -l_{2,2}\alpha\text{sign}(z_{2,2} - \kappa_{2,1}). \end{cases} \tag{13}$$

where the denotation $\text{sig}^a(x)$ is defined as $\text{sign}(x)|x|^a$, two sets of parameters, $(l_{1,0},\ l_{1,1},\ l_{1,2},\ l_{1,3})$ and $(l_{2,0},\ l_{2,1},\ l_{2,2})$ respectively, correspond to Hurwitz polynomials, i.e., $L_1(s) = s^4 + l_{1,0}s^3 + l_{1,1}s^2 + l_{1,2}s + l_{1,3}$ and $L_2(s) = s^3 + l_{2,0}s^2 + l_{2,1}s + l_{2,2}$. $\alpha \geqslant 1$ is a scaling factor that can be utilized to adjust the observer dynamics. In (12), $z_{1,0}$, $z_{1,1}$, $z_{1,2}$ and $z_{1,3}$ are actually the estimations of z_1, d_1, $\dot{d}_1$ and $\ddot{d}_1$. Similarly, $z_{2,0}$, $z_{2,1}$ and $z_{2,2}$ in (13) estimate the values of z_2, d_2 and $\dot{d}_2$ in (7b). By denoting the observing errors of (12) as $e_{1,0} = z_{1,0} - z_1$, $e_{1,1} = z_{1,1} - d_1$, $e_{1,2} = z_{1,2} - \dot{d}_1$ and $e_{1,3} = z_{1,3} - \ddot{d}_1$, the error dynamics can be derived as,

$$\begin{cases} \dot{e}_{1,0} = e_{1,1} - l_{1,0}\alpha^{\frac{1}{4}}\text{sig}^{\frac{3}{4}}(e_{1,0}), \\ \dot{e}_{1,1} = e_{1,2} - l_{1,1}\alpha^{\frac{1}{3}}\text{sig}^{\frac{2}{3}}(e_{1,1} - \dot{e}_{1,0}), \\ \dot{e}_{1,2} = e_{1,3} - l_{1,2}\alpha^{\frac{1}{2}}\text{sig}^{\frac{1}{2}}(e_{1,2} - \dot{e}_{1,1}), \\ \dot{e}_{1,3} = -l_{1,3}\text{sign}(e_{1,3} - \dot{e}_{1,2}) + [-D, D]. \end{cases} \tag{14}$$

By the same token, the FTO (13) induces estimating errors as $e_{2,0} = z_{2,0} - z_2$, $e_{2,1} = z_{2,1} - d_2$ and $e_{2,2} = z_{2,2} - \dot{d}_2$, whose corresponding differentiations can be written as,

$$\begin{cases} \dot{e}_{2,0} = e_{2,1} - l_{2,0}\alpha^{\frac{1}{3}}\text{sig}^{\frac{2}{3}}(e_{2,0}), \\ \dot{e}_{2,1} = e_{2,2} - l_{2,1}\alpha^{\frac{1}{2}}\text{sig}^{\frac{1}{2}}(e_{2,1} - \dot{e}_{2,0}), \\ \dot{e}_{2,2} = -l_{2,2}\text{sign}(e_{2,2} - \dot{e}_{2,1}) + [-D, D]. \end{cases} \tag{15}$$

Following the results in [30], the error systems in (14) and (15) are finite-time stable, which means error dynamics will be forced to zeros in finite time T_o. When $t \geqslant T_o$, $z_{1,i}$ $(i = 0, 1, 2, 3)$ will accurately converge to z_1, d_1, $\dot{d}_1$ and $\ddot{d}_1$, individually, and $z_{2,k}, (k = 0, 1, 2)$ will also strictly track z_2, d_2 and $\dot{d}_2$ respectively. Note that (7c) and (7d) bear the identical formats with respect to (7a) and (7b). It is thus possible to construct the same observers as in (12) and (13) to estimate disturbance quantities. Specifically, $z_{3,i}$ $(i = 0, 1, 2, 3)$ and $z_{4,k}$ $(k = 0, 1, 2)$ will precisely approach z_3, d_3, $\dot{d}_3$, $\ddot{d}_3$, z_4, d_4 and $\dot{d}_4$ respectively, with $z_{3,i}$ and $z_{4,k}$ being the FTO states.

C. Finite-time Controller Design

After knowing the disturbance estimations given by the preceding FTOs, it is imperative to detach the impacts of these disturbances from the IDBC system regulation. To this end, a nonlinear finite time controller is designed and several intermediary error states are introduced in (16) to better illustrate the desired large signal stabilization scheme.

$$\begin{cases} \varepsilon_1 = z_1 - z_{1ref},\ \varepsilon_2 = (z_2 - z_{2ref})/\gamma, v_u = (u_u - u_{uref})/\gamma^2, \\ \varepsilon_3 = z_3 - z_{3ref},\ \varepsilon_4 = (z_4 - z_{4ref})/\gamma,\ v_l = (u_l - u_{lref})/\gamma^2, \end{cases} \tag{16}$$

where $\gamma \geqslant 1$ is a scaling gain that is similar to α in (12) and (13), z_{1ref}, z_{2ref}, z_{3ref} and z_{4ref} represent the reference signals of states in (7), whereas the references of control inputs of (7) are u_{uref} and u_{lref}, v_u and u_l denote the virtual control variables that are designed as follows,

$$\begin{cases} v_u = -k_1\text{sig}^{1+2\tau}(\varepsilon_1) - k_2\text{sig}^{\frac{1+2\tau}{1+\tau}}(\varepsilon_2), \\ v_l = -k_1\text{sig}^{1+2\tau}(\varepsilon_3) - k_2\text{sig}^{\frac{1+2\tau}{1+\tau}}(\varepsilon_4), \end{cases} \tag{17}$$

wherein τ is a homogeneous degree that resides in the range of $(-0.5, 0)$, as detailed in [31]. By varying τ, the dynamics of the control system with the finite-time stabilization can be modified, which will be detailed in the subsequent context. k_1 and k_2 are control parameters subjected to a Hurwitz polynomial, i.e., $K(s) = s^2 + k_2 s + k_1$. As per (16), u_u and u_l can be expressed in terms of v_u and v_l individually, i.e.,

$$\begin{cases} u_u = \gamma^2 v_u + u_{uref}, \\ u_l = \gamma^2 v_l + v_{lref}. \end{cases} \tag{18}$$

Then, the actual duty ratios d_u and d_l can be easily calculated by substituting u_u and u_l into (10) and (11).

Returning to the mathematical relation of the IDBC output voltage and input voltage as depicted in (3) and assuming that the terminal voltages of the two IBCs in Fig. 2 are the same, the references for v_{C1} and v_{C2} are given as

$$v_{C1ref} = v_{C2ref} = 0.5(V_{oref} + v_{in}), \tag{19}$$

where V_{oref} is the reference value of DC bus voltage. By virtue of (19), (6a) and (6c), z_{1ref} and z_{2ref} can be identified as

$$\begin{cases} z_{1ref} = 0.5L_u(\dfrac{v_{C1ref}i_o}{v_{in}})^2 + 0.5C_1 v_{C1ref}^2, \\ z_{2ref} = 0.5L_l(\dfrac{v_{C2ref}i_o}{v_{in}})^2 + 0.5C_2 v_{C2ref}^2. \end{cases} \tag{20}$$

Then, according to (7), z_{2ref}, z_{4ref}, u_{uref} and u_{lref} can be calculated as,

$$\begin{cases} z_{2ref} = \dot{z}_{1ref} - z_{1,1}, \\ u_{uref} = \dot{z}_{2ref} - z_{2,1} = \ddot{z}_{1ref} - z_{1,2} - z_{2,1}, \\ z_{4ref} = \dot{z}_{3ref} - z_{3,1}, \\ u_{lref} = \dot{z}_{3ref} - z_{4,1} = \ddot{z}_{3ref} - z_{3,2} - z_{4,1}. \end{cases} \tag{21}$$

Substituting (17) into (16), the closed-loop dynamic system comprising the intermediary error states can be deduced in the following compact form,

$$\dot{\bar{\varepsilon}} = \gamma[g_1\ g_2\ g_3\ g_4]^\top + [\varphi_1\ \varphi_2\ \varphi_3\ \varphi_4]^\top, \tag{22}$$

where $\bar{\varepsilon} = [\varepsilon_1\ \varepsilon_2\ \varepsilon_3\ \varepsilon_4]^\top$, $g_1 = \varepsilon_2$, $g_2 = -k_1\text{sig}^{1+2\tau}(\varepsilon_1) - k_2\text{sig}^{\frac{1+2\tau}{1+\tau}}(\varepsilon_2)$, $g_3 = \varepsilon_4$, $g_4 = -k_1\text{sig}^{1+2\tau}(\varepsilon_3) - k_2\text{sig}^{\frac{1+2\tau}{1+\tau}}(\varepsilon_4)$, $\varphi_1 = d_1 - z_{1,1}$, $\varphi_2 = \frac{1}{\gamma}(d_2 + \dot{z}_{1,1} - z_{1,2} - z_{2,1})$, $\varphi_3 = d_3 - z_{3,1}$, $\varphi_4 = \frac{1}{\gamma}(d_4 + \dot{z}_{3,1} - z_{3,2} - z_{4,1})$.

D. Finite-time Large Signal Stability Analysis

Based on (22), the intention hereby is to show that all components in $\bar{\varepsilon}$ can be rigorously regulated to zeros in a finite-time duration, which is proved as follows.

Stage 1 Trajectories of the state variables in (22) are uniformly bounded before T_o which is the convergence time of FTOs.

Construct a Lyapunov function for (22) as $V = V_1 + V_2 = \Xi_1^\top P\Xi_1 + \Xi_2^\top P\Xi_2$, where P is a positive definite matrix that satisfies $A^\top P + PA^\top = -I$ and $A = [0\ 1; -k_1\ \ -k_2]$. Ξ_1 and Ξ_2 are state vectors defined as

Performing differentiation on V along with time gives

$$\dot{V} = \gamma\sum_{j=1}^{2}\frac{\partial V_1}{\partial\varepsilon_j}g_j + \gamma\sum_{j=3}^{4}\frac{\partial V_2}{\partial\varepsilon_j}g_j + \sum_{j=1}^{2}\frac{\partial V_1}{\partial\varepsilon_j}\varphi_j + \sum_{j=3}^{4}\frac{\partial V_2}{\partial\varepsilon_j}\varphi_j. \tag{23}$$

Referring to the Homogeneity theory as in Lemmas 1-3 (see Appendix) from [31], V_1 and V_2 are inherently homogeneous of degree $2-\tau$, denoted as $V_1,\ V_2 \in \text{H}^{2-\tau}$. Additionally, it can also be recognized that $\partial V_1/\partial\varepsilon_1,\ \partial V_2/\partial\varepsilon_3 \in \text{H}^{1-\tau}$, $g_1,\ g_3 \in \text{H}^{1+\tau}$, $\partial V_1/\partial\varepsilon_2,\ \partial V_2/\partial\varepsilon_4 \in \text{H}^{1-2\tau}$ and $g_2,\ g_4 \in \text{H}^{1+2\tau}$. With these relations and based on [31], the following expression holds,

$$V' = (\sum_{j=1}^{2}\frac{\partial V_1}{\partial\varepsilon_j}g_j + \sum_{j=3}^{4}\frac{\partial V_2}{\partial\varepsilon_j}g_j) \in \text{H}^2. \tag{24}$$

which implies that V' is homogeneous of degree 2. In this sense, according to the operation fundamentals of the homogeneity theory, it is possible to make V comparable to V' by lifting V to the power of $\frac{2}{2-\tau}$, as in Lemma 3, and there is a constant c sufficing

$$V' \leqslant -cV^{\frac{2}{2-\tau}}. \tag{25}$$

As for the third item associated with φ_j in (23), it can be manipulated with Young's inequality (see Lemma 4) as [32]

$$\begin{aligned}\sum_{j=1}^{2}\frac{\partial V_1}{\partial\varepsilon_j}\varphi_j \leqslant& |\frac{\partial V_1}{\partial\varepsilon_1}|\varpi + |\frac{\partial V_1}{\partial\varepsilon_2}|\varpi\\ \leqslant& (|\frac{\partial V_1}{\partial\varepsilon_1}|^{\frac{2}{1-\tau}})^{\frac{1-\tau}{2}}(\varpi^{\frac{2}{1+\tau}})^{\frac{1+\tau}{2}}\\ &+ (|\frac{\partial V_1}{\partial\varepsilon_2}|^{\frac{2}{1-2\tau}})^{\frac{1-2\tau}{2}}(\varpi^{\frac{2}{1+2\tau}})^{\frac{1+2\tau}{2}}\\ \leqslant& \frac{1-\tau}{2}(|\frac{\partial V_1}{\partial\varepsilon_1}|^{\frac{2}{1-\tau}}) + \frac{1+\tau}{2}\varpi^{\frac{2}{1+\tau}}\\ &+ \frac{1-2\tau}{2}|\frac{\partial V_1}{\partial\varepsilon_2}|^{\frac{2}{1-2\tau}} + \frac{1+2\tau}{2}\varpi^{\frac{2}{1+2\tau}}\\ \leqslant& \frac{1}{2}c^*V^{\frac{2}{2-\tau}} + \frac{1}{2}\Delta,\end{aligned} \tag{26}$$

where $c^* \geqslant 2(1-2\tau)$, $\Delta \geqslant (1+\tau)\varpi^{\frac{2}{1+\tau}} + (1+2\tau)\varpi^{\frac{2}{1+2\tau}}$, and $\varpi = \sup|\varphi_j|$ for $j = 1, 2, 3, 4$. Similar to the deductions in (26), the fourth item in (23) can be extended as

$$\sum_{j=3}^{4}\frac{\partial V_2}{\partial\varepsilon_j}\varphi_j \leqslant \frac{1}{2}c^*V^{\frac{2}{2-\tau}} + \frac{1}{2}\Delta. \tag{27}$$

Substituting (25), (26) and (27) into (23) results in

$$\dot{V} \leqslant -(\gamma c - c^*)V^{\frac{2}{2-\tau}} + \Delta. \tag{28}$$

The inequality (28) holds in the case that the observing errors of FTOs have not been enforced to zeros before T_o. For a level set $\Omega_\delta = \{\bar{\varepsilon}|V^{\frac{2}{2-\tau}} \leqslant \delta\}$, since γ is only related to the control gain, it is always feasible to enlarge γ such that $\Delta < (\gamma c - c^*)\delta$. When $\bar{\varepsilon}$ is outside Ω_δ, the corresponding $V^{\frac{2}{2-\tau}}$ is no less than δ, it is easily inferred that $\dot{V} < 0$ meaning each elements in $\bar{\varepsilon}$, can always be captured by Ω_δ. In this sense, when the observing errors of FTOs have not been reduced to zeros before T_o, the control system given by (22) is uniformly bounded. More basic and professional knowledge regarding Lyapunov techniques can be found in [33].

Stage 2 Each components in $\bar{\varepsilon}$ can be stringently forced to the origin after T_o. As mentioned previously, FTOs can rigidly enforce the observing errors to zeros right after T_o, which has been endorsed by [30]. In view of this, φ_j $(j = 1, 2, 3, 4)$ which is closely related to observation errors, should be set as zeros, and there no longer exist c^* and Δ in (26) and (27). Afterwards, the overall Lyapunov function derivative of (28) can be degraded into

$$\dot{V} \leqslant -\gamma cV^{\frac{2}{2-\tau}}. \tag{29}$$

Separating variables and integrating (29) over the time t, it can be obtained that

$$V^{\frac{-\tau}{2-\tau}} \leqslant \frac{\tau}{2-\tau}\gamma ct + V_0^{\frac{-\tau}{2-\tau}}, \tag{30}$$

where V_0 represents the value of V at the time of T_o, and it actually equals δ, once the control gain γ is determined. Note that V is a function in terms of time t. Based on (30), the time T_c when V reaches zero can be easily obtained by setting t in (30) to zero,

$$T_c \leqslant \frac{\tau - 2}{\tau\gamma c}V_0^{\frac{-\tau}{2-\tau}}. \tag{31}$$

From (31), it is concluded that intermediary errors in (22) under the proposed large signal stabilization scheme can be regulated to zeros within T_c after T_o. Note that T_c is pertinent to V_0: a larger V_0 leads to longer T_c. The illustrative sketch is detailed in Fig. 3. For $t \in [T_o,\ T_o + T_c]$, disturbances in (7) have been precisely estimated. While for $t \in [T_o + T_c,\ +\infty]$, the destabilizing effects of disturbances have been exactly offset by the nonlinear controller, which also helps to realize large signal stability of the entire MG. The overall stabilization duration is $T_s = T_o + T_c$. After T_s, $\bar{\varepsilon}$ is limited at the original, and the mapped states z_j $(j = 1, 2, 3, 4)$ will accurately track their respective references given by (20) and (21). Consequently, the DC bus voltage and two capacitor voltages in the IDBC will approach to the individual desired values in (19), i.e., $v_o \to V_{oref}$, $v_{C1} \to v_{C1ref}$ and $v_{C2} \to v_{C2ref}$.

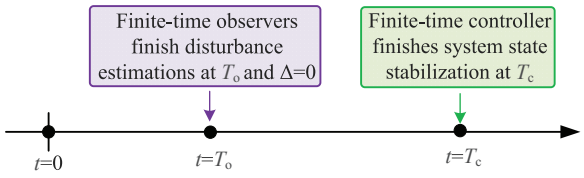

Fig. 3. The sketch of T_o and T_c.

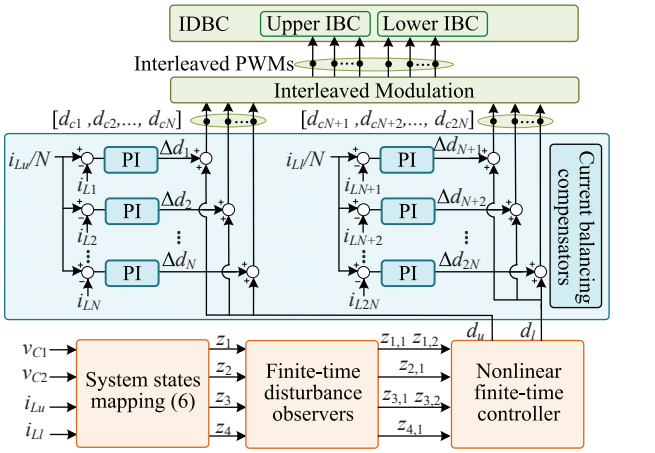

Fig. 4. Control diagram of the IDBC-enabled high power DC MG with the proposed large signal stabilization scheme, incorporated with current balancing modules.

E. Practical Implementation of Stabilization Scheme

The IDBC model includes the sum of inductor currents in the upper and lower IBCs. However, only regulating the total currents of the two IBCs may not be satisfactory as circulating currents may be induced due to the minor differences in real inductances and the executed duty ratios for multiples bridges. To solve this problem, typical current balancing compensators are integrated into the full IDBC model to generate compensation signals to correct duty ratios conveyed from the finite-time controller. Corresponding control diagram of the IDBC integrated with the compensators is shown in Fig. 4.

In Fig. 4, d_{cj} $(j = 1, 2, ..., N)$ and d_{cj} $(j = N+1, N+2, ..., 2N)$ are the practical duty ratios for all bridges of IDBC. These duty ratios are processed by interleaved modulations to produce PWMs such that the ripples in the output current of the DC source can be suppressed, thus potentially extending the source life time. Δd_j $(j = 1, 2, ..., 2N)$ are compensation signals given by proportional-integral (PI) controllers, i.e., $\Delta d_j = k_p e_j + k_i \int e_j \mathrm{d}t$, where k_p and k_i are PI parameters, and e_j is either $i_{Lu}/N - i_{Lj}$ for the upper IBC or $i_{Ll}/N - i_{Lj}$ for the lower IBC. On the other hand, small PI controller parameters in Fig. 4 can be selected so that the compensator dynamics are significantly slowed down and decoupled from the proposed FTC. In this way, Δd_j can be viewed as constants from the perspective of the FTC. Moreover, stability analysis in (24)-(31) does not involve Δd_j at all. Thus, the large signal stabilization endowed by FTOs and FTC still holds even in the presences of current compensators.

F. Discussions

1) Implementation logics in Fig. 4: It is obvious from Fig. 4 that the implementational logics of our proposed scheme are clear and can be divided into three steps. First step: The voltage values v_{C1} and v_{C2} and current values i_{Lu} and i_{Ll} should be collected via sensors. These electrical measurements are fed to coordinated transformations of (6) and obtain new states z_1, z_2, z_3 and z_4. Second step: Feed z_1, z_2, z_3 and z_4 to the observers as described in (12) and (13) which further gives the estimated values $z_{1,1}$, $z_{1,2}$, $z_{2,1}$, $z_{3,1}$, $z_{3,2}$, and $z_{4,1}$. Third step: The new state variables and the estimation values should be fed to the nonlinear controller (18) to attain equivalent control inputs. The inputs are processed by (10) and (11) to get real control inputs d_u and d_l. Then d_u and d_l are given to current balancing compensators to produce duty cycle for each bridge in the DC/DC converter.

2) Measurements required by the proposed large signal stabilizer: For the generic topology in Fig. 4, $2N$ currents and two capacitor voltages should be sensed and fed to the controller. In hardware experiments, totally six phases are used, and there are six currents and two voltages that should be measured by sensors.

3) Unnecessary to know the lumped load models.: The proposed finite time large signal control scheme has subtly expressed the dynamics of the lumped load into system disturbances. By using FTOs and FTC, the internal system states can be stabilized in the large signal sense, and the impacts of load models on DC system can be fully canceled. Therefore, it is unnecessary to know the exact lumped load models. This is an outstanding benefit offered by the proposed stabilizer.

4) Comparisons with other nonlinear methods: Sliding mode control (SMC) is normally designed based on a particular operating point [34]. Although the slide mode surface is constructed subjected to Lyapunov stability framework, the steady state performance of the DC converter under SMC would be not satisfiable if the real operating point differs from the nominal one. H_∞ control in [33] and the flatness-based control suffer from the similar difficulty that their control input is related to a certain loading condition. The adaptive passivity control in [29] could be extended to the IDBC topology. However, the passivity scheme encounters transient oscillations and have limited stability margin as in PI controls. Different from all these advanced methods, the proposed finite-time large signal scheme allows for infinity stability margin in theory. Moreover, as shown in Fig. 8, both transient dynamics and steady state regulations are smooth and stable.

5) DC bus voltage level selection: The standard bus voltage is set as 300 V in this paper. Nevertheless, the IDBC under the control of the finite-time large signal stabilizer can also used to escalate the bus voltage to higher bus voltages like 400 V for the integration with a single phase AC system or 700 V for the connection to an AC distribution system [35].

IV. Simulation Results

As understood from Section III, there are multiple control parameters in FTOs and FTC, which should be identified for system dynamic evaluations and performance verifications. However, unlike the classical PI controller design, no widely-received standards exist for the premium finite control. As such, an explicit parameter selection guideline for observers and the nonlinear controller is presented in this section, and current ripple mitigations enabled by the IDBC topology is also developed.

A. Control Parameter Selection Guideline

To properly configure control parameters in the FTOs and FTC, a representative IDBC with upper and lower IBCs having three bridges is utilized, which means N in the generic IDBC circuitry of Fig. 2 is 3. Main system parameters are listed in Table I.

TABLE I
SYSTEM PARAMETERS

Parameter	Description	Value
v_{in}	Input voltage	100 V
V_{oref}	Nominal DC bus voltage	300 V
L_j $(j = 1, 2, 3)$	Upper IBC inductance	3 mH
L_j $(j = 4, 5, 6)$	Lower IBC inductance	3 mH
C_j $(j = 1, 2)$	IBC capacitance	470 uF
f_{sw}	Switching frequency	10 kHz
f_{sa}	Sampling frequency	10 kHz
R_L	Resistive load	200 Ω
$k_p,\ k_i$	PI parameters in the current balancing compensators	0.2, 1

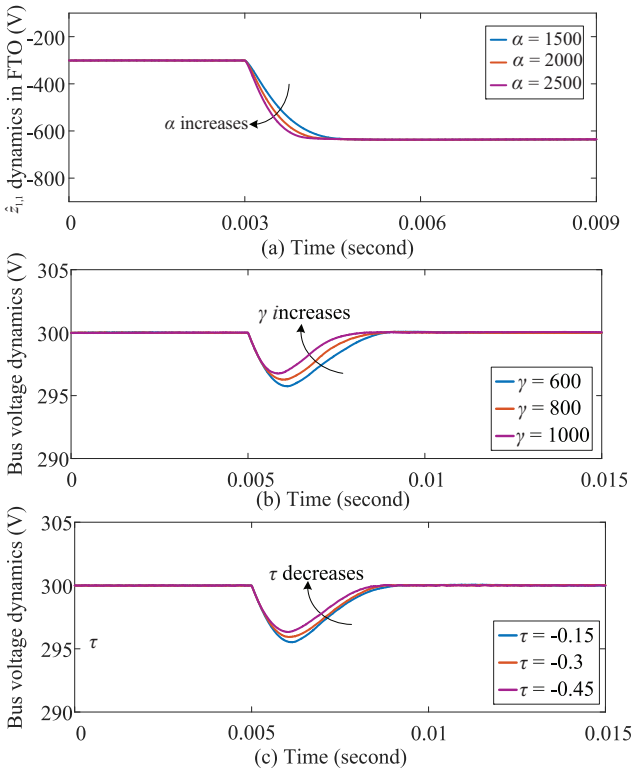

Fig. 5. Control parameter selection guideline for the FTOs and FTC. (a) $z_{1,1}$ dynamic responses in the FTO with $\gamma = 600, \tau = -0.15$ and various α; (b) DC bus voltage v_o dynamics with $\alpha = 2500, \tau = -0.15$ and various γ; (c) DC bus voltage v_o dynamics with $\alpha = 2500, \gamma = 600$ and various τ;

As explained in Section III *B-C*, $l_{1,j}$ $(j = 0, 1, 2, 3)$ and $l_{2,j}$ $(j = 0, 1, 2)$ in observers (12)-(13) are coefficients of Hurwitz polynomials $L_1(s)$ and $L_2(s)$, individually. Then, $l_{1,0}, l_{1,1}, l_{1,2}$ and $l_{1,3}$ can be identified as 8, 24, 32 and 16 by assigning four repeated poles of -2 to $L_1(s)$. Similarly, $l_{2,0}, l_{2,1}$ and $l_{2,2}$ are determined as 6, 12 and 8. For FTOs applicable to (7c) and (7d), the corresponding parameters $l_{3,j}$ $(j = 0, 1, 2, 3)$ and $l_{4,j}$ $(j = 0, 1, 2)$ can be chosen identical to $l_{1,j}$ and $l_{2,j}$, respectively, because (7c) and (7d) bear the same form as in (7a) and (7b). In (17), k_1 and k_2 denote the coefficients of $K(s)$; they can be given as 4, by placing the repeated poles of -2 to $K(s)$.

Based on the above configurations, the dynamics of the state $\hat{z}_{1,1}$ in (12) and DC bus voltage transients with respect to different settings of α, γ and τ are shown in Fig. IV-A. In Fig. IV-A(a), γ and τ are temporarily scheduled as 600 and -0.15. α in all FTOs is configured as 1500, 2000 and 2500 respectively, and the convergence time of $\hat{z}_{1,1}$ in (12) is estimated as 0.0018 s, 0.0015 s and 0.001 s. Notice that the FTC will stabilize the intermediary states in (22) at the origin in finite time only after the observers

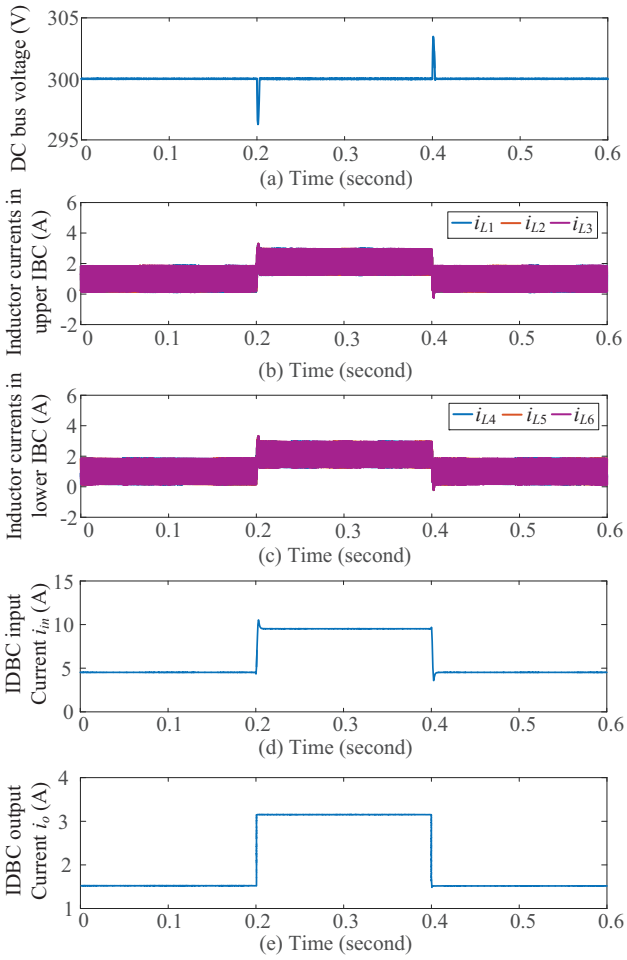

Fig. 6. System level simulations for IDBC enabled DC MG with a 500 W CPL plug-in and plug-out.

have finished their tracking transients. It is thus recommended to adjust the FTOs to be slightly faster than the controller dynamics. As such, α in the IDBC application should be selected as 2500 to obtain sufficiently rapid observers. Afterwards, the FTC dynamics are evaluated against different γ in Fig. IV-A(b) where α is fixed at 2500 and τ keeps unchanged. Initially, the IDBC is merely feeding the resistive load. When a CPL of 500 W is integrated to the DC bus at 0.005 s, it is apparent that larger γ results in a shorter bus voltage restoration and smaller voltage dip. In the case of $\gamma = 600$, the voltage restoration accounts for around 0.004 s which is four times of the converging duration (0.001 s) of the FTOs. This set of parameters ($\alpha = 2500, \gamma = 600$) allow for better dynamic coordination between the FTOs and FTC, and will be used in subsequent simulations and experiments. Proceeding to Fig. IV-A(c), bus voltage dynamics are displayed with τ being $-0.15, -0.3$ and -0.45, respectively. With the decrease of τ, the maximum voltage drop is reduced from about 4.5 V to 4 V and 3.5 V, while the voltage restoration time is almost not affected at 0.004 s. This observation indicates that the introduction of τ into the control system might help to modify the transient responses and improve voltage quality of the power DC MG. To fully benefit from τ, τ is hereby selected as -0.45. In fact, there are totally three parameters that need tuning, i.e., α, γ, and τ. Ideally, α and γ should be selected as large as possibly, and τ should be close to -0.5, to attain desired dynamics.

B. System Level Simulation

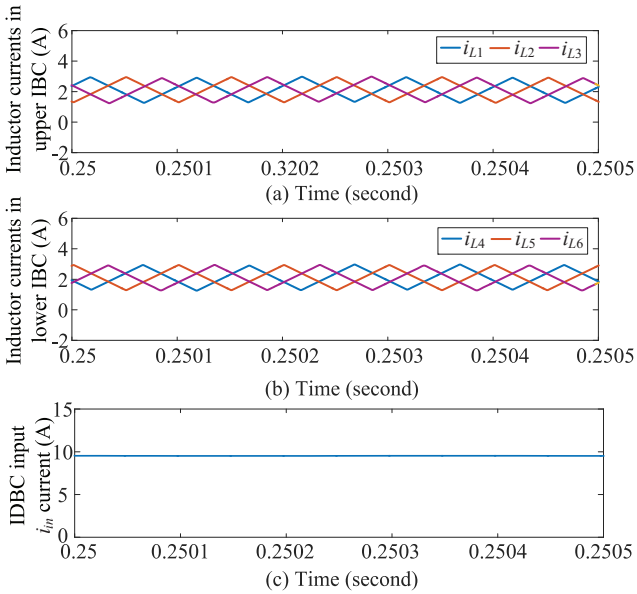

Fig. 7. Zoomed-in view of Fig. 6 from 0.25 s to 0.2505 s.

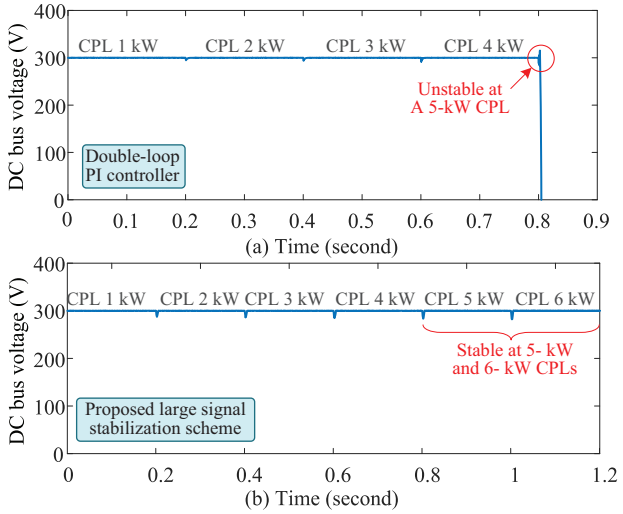

Fig. 8. Stability margin comparison between conventional PI controller designed according to [6] and the proposed large signal stabilization scheme. (a) PI controller in [6]; (b) Proposed large signal stabilization scheme.

Fig. 6 shows system level simulation results of the IDBC-based DC MG with new loading conditions. At the beginning, a resistive load of 200 Ω is integrated to the DC bus, which is rigorously regulated at 300 V. At the instances of 0.2 s and 0.4 s, a CPL of 500 W is plugged in and disconnected from the DC bus, and the overall system consistently works stably disregarding load changes. The six inductor currents i_{Lj} $(j = 1, 2, ..., 6)$ are detailed in Figs. 6(b) and (c). Clearly, there are current ripples of around 1.8 A in i_{Lj}. Revisiting (4), the output current of the DC power source equals the summation of these inductor currents with the subtraction of the load current i_o, i.e., $i_{in} = \sum_{j=1}^{6} i_{Lj} - i_o$. Due to the filtering effects of two capacitors in the IDBC, most of the high frequency components in i_o will be perfectly filtered and i_o is almost smoothened to be a constant. By using the interleaved modulations in Fig. 4, the total current that the IDBC draws from the DC source is exempted from any ripple contaminations, which helps to protect the DC source and extend its remaining useful life. This fact can also be justified by the zoomed-in view of the i_{Lj} and i_{in} in Fig. 7 where i_{in} is a purely DC signal of around 9.5 A.

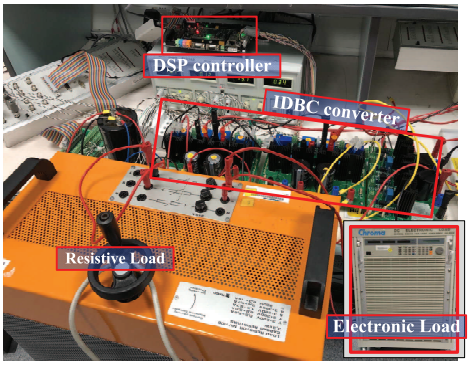

Fig. 9. Experimental platform to validate the proposed stabilization scheme.

C. Stability Margin Comparison

Stability margin comparisons between the proposed large signal stabilization scheme and the conventional double-loop PI controls in [6] are provided in Fig. 8. All control parameters for the FTOs and FTC have been determined by the design guideline in Section IV A. In contrast, for the work in [6], the two IBCs are respectively controlled by the double-loop PI controls. It should be noted that PI controllers are not empirically tuned but they are designed based on classical control mechanism as documented in [2], [29]. For each IBC, the current control loop is required to have a crossover frequency (f_{cr}) of 1000 Hz and a phase margin (PM) of 80°. The voltage control loop should have f_{cr} = 100 Hz and PM = 80°. Conforming to this requirement, the PI parameters for the IDBC configuration in this paper could be calculated, i.e., $k_p = 0.0309$, $k_i = 34.37$ for the current loop and $k_p = 0.58$, $k_i = 64.43$ for the voltage loop. Considering the worst case, only CPL is used in comparative simulations. Fig. 8(a) depicts the DC bus voltage profile with a CPL increasing from 1 kW under the traditional PI controls. It is conspicuous that the DC system is destabilized when the CPL rises to 5 kW. However, the IDBC equipped with the large signal stabilization scheme can still be well stabilized, even when the CPL surges to 6 kW, as seen from Fig. 8(b), which means the proposed method allows for a wider stability margin than the conventional PI control. In fact, the stability analyses in Section III D is irrelevant to load models, and hence, the stability margin endowed by the proposed large is infinite in theory.

V. Experiment Tests

To verify the effectiveness of the proposed large signal stabilization scheme, an experimental platform is built up, as shown in Fig. 9. The platform includes a six-bridge IDBC converter feeding a resistive load and a CPL emulated by a programmable electronic load. The electronic load is Chroma 63210 DC Electronic Load. When it is configured in constant resistance mode, the resistive load ranges from 3.3 Ω to 13200 Ω. When it is configured in constant current mode, the current ranges from 0 A to 150 A. When it is configured in constant power mode, the power ranges from 0 W to 14.5 kW. A controller board mounted with a DS38335 is adopted to collect current/voltage signals, execute FTOs/FTC algorithms and generate PWMs signal for the converter. The system parameters are the same as in simulations (see Table I). The entire finite-time control system follows the architecture given in Fig. 4.

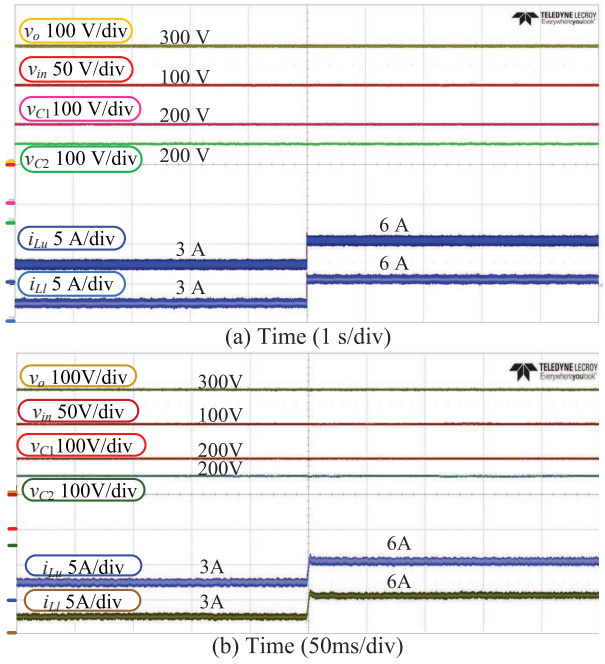

Fig. 10. (a) Experimental results with a resistive load changing from 200 Ω to 100 Ω and CPL being disabled; (b) Zoomed-in view of (a).

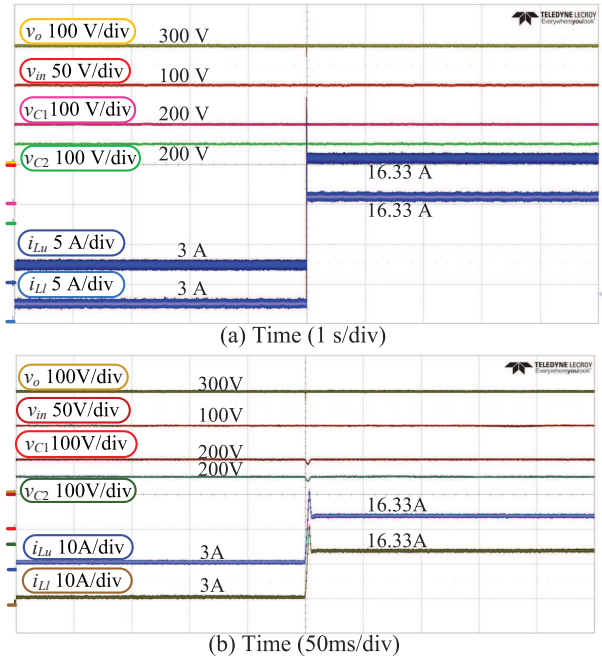

Fig. 11. (a) Experimental results with a large CPL step-up from 0 W to 2 kW and the resistive load is fixed at 200 Ω; (b) Zoomed-in view of (a).

A. Case 1: Loading Variations

Experimental results for the change of loading condition are presented in Figs. 10 and 11. In Fig. 10, the CPL is not enabled and the system is initially integrated with the resistive load of 200 Ω. Apparently, the DC bus voltage v_o is stably regulated at 300 V. The input voltage v_{in} of the IDBC is 100 V. The two capacitor voltages, v_{C1} and v_{C2} are read as 200 V. It can be verified that the mathematical relation of v_o, v_{in}, v_{C1} and v_{C2} is in perfectly agreement with the expression of (3), i.e., $v_o = 300\ \text{V} = v_{C1} + v_{C2} - v_{in} = 200\ \text{V} \times 2 - 100\ \text{V}$. The summed inductor currents of the upper and lower IBCs, i_{Lu} and i_{Ll} are identical as 3 A. When an other resistive load of 200

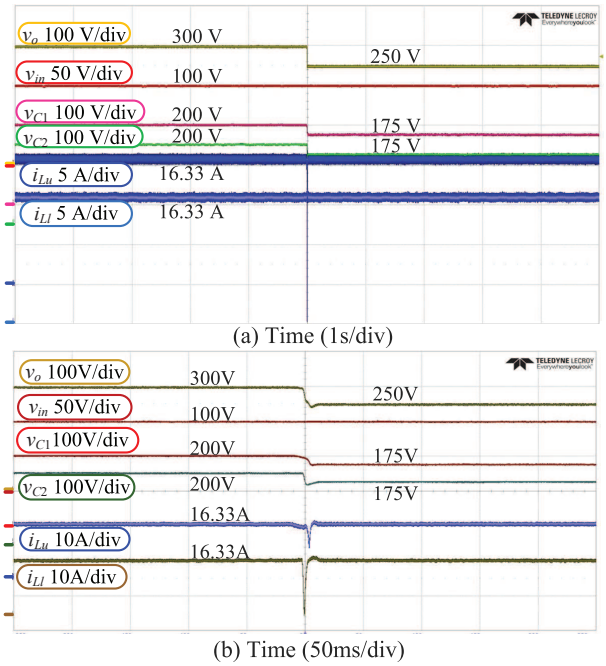

Fig. 12. (a) Experimental results with V_{oref} stepping down from 300 V to 250 V while the resistive load and CPL are fixed at 200 Ω and 2 kW, respectively; (b) Zoomed-in view of (a).

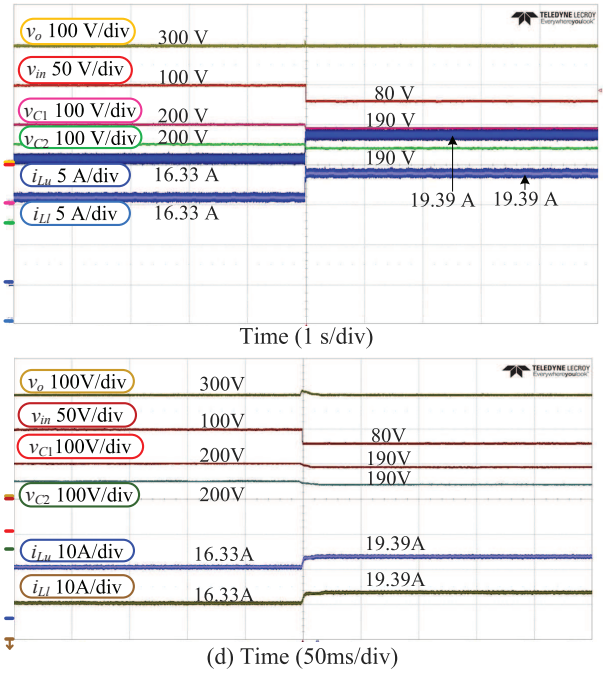

Fig. 13. (a) Experimental results with v_{in} deviating from 100 V to 80 V while the resistive load and CPL are fixed at 200 Ω and 2 kW, respectively; (b) Zoomed-in view of (a).

Ω is coupled to the DC bus, i_{Lu} and i_{Ll}, are doubled instantly and controlled at 6 A, whereas the DC bus voltage is stably maintained at the rated value of 300 V.

Fig. 11 shows the system dynamics when a harsh loading situation takes place. To start with, the resistive load is 200 Ω and the CPL is not in operation. In the case that the CPL increases from 0 W to 2 kW, as seen from Fig. 11, i_{Lu} and i_{Ll} are boosted to 16.33 A. Note that the CPL power is larger than the resistive load power, hence, CPL still dominates the total load [2]. Although there are overshoots in currents and undershoots in

voltages during transient state, the overall DC MG is favorably stabilized under such a large load change, which certainly attests to the effectiveness of the proposed method for attaining the large signal stability.

B. Case 2: V_{oref} and v_{in} Variations

Upon the operating point in Fig. 11, the 2 kW CPL and resistive load are all integrated into the system. This point means the DC system is heavily loaded. Given a certain power of the CPL, from the perspective of the small signal modeling, the lowered terminal voltage across the CPL results in the increased negative impedance which may more easily induce instability [2]. In this context, the voltage reference signal V_{oref} is deliberately truncated by 50 V decreasing to 250 V, and the pertinent experimental results are given in Fig. 12. From Fig. 12, it is seen that v_{C1} and v_{C2} concurrently fall to 175 V when v_o is driven to 250 V as it responds to the change of V_{oref}. Notice that v_{in}, v_o, v_{C1} and v_{C2} still satisfy the mathematical relation in (3). The currents i_{Lu} and i_{Ll} are well stabilized at 16.33 A. Fig. 13 shows the system dynamic performances when the input voltage v_{in} of the IDBC is reduced from original 100 V to 80 V. To maintain the relation in (3), v_{C1} and v_{C2} accordingly decrease to 190 V. i_{Lu} and i_{Ll} increase from 16.33 A to 19.39 A to ensure the balance between the power generation and load consumption. In spite of the sudden drop of v_{in}, the DC bus voltage can still be regulated at 300 V stably. Based on the above interpretations of Figs. 12 and 13, it can be concluded that the composition of the FTOs and FTC in the proposed large signal stabilization scheme can elegantly handle the destabilizing effects inured by variations of V_{oref} and v_{in}.

VI. Conclusion

This paper has proposed a large signal stabilization scheme that synthesizes the FTOs and FTC for the IDBC converter applied in high power DC MG. To analyze the destabilizing effects of CPL and internal parameter uncertainties, the effects have been expressed into system disturbances. FTOs can precisely estimate the disturbances and the estimated quantities are further exactly canceled in the proposed FTC controller. Besides, FTC also rigorously drives all states in the IDBC to stabilize at their expected values in finite time. Thanks to the large signal stabilization method, in theory, the DC system can operate at any equilibrium that is within hardware's limitation, which has been justified by using Lyapunov techniques. Simulation results have shown that the proposed approach endows a larger stability margin than the conventional PI control. The effectiveness of the FTOs and FTC are also verified by experiment tests. By means of the proposed approach, no specific stability criterion is needed, no localized linearization is used, and the destabilizing impacts of CPLs and parameter uncertainties are fully neutralized. Hence, the controller can stabilize the DC system in a very wide operating range.

Appendix

Some preliminaries regarding Homogeneity theory and Young's inequality are provided here to better understand the derivations in Section III.

Lemma 1 : For a continuous scalar function $V = f(x_1, \dots x_m, \dots, x_n)$, V is homogeneous of degree ζ, denoted by $V \in \mathrm{H}^{\zeta}$, if there exists a real number $\epsilon > 0$ such that

$$\epsilon^{\zeta} = f(\epsilon^{r_1} x_1, \dots \epsilon^{r_m} x_m, \dots, \epsilon^{r_n} x_n), \tag{A1}$$

where $r_m = 1 + (m-1)\tau$ and $\tau \in (-1/n,\ 0)$. $r = (r_1, \dots, r_m, \dots, r_n)$ is a dilation weighted vector.

Lemma 2 : If there are two scalar functions V_1 and V_2 which are homogeneous of degree ζ_1 and ζ_2 individually with respect to the dilation r, then the following inference holds,

$$V_1 \in \mathrm{H}^{\zeta_1},\ V_2 \in \mathrm{H}^{\zeta_2} \implies V_1 V_2 \in \mathrm{H}^{\zeta_1+\zeta_2} \tag{A2}$$

Lemma 3 : If both V_1 and V_2 are positive definite, it is possible to manipulate them to be comparable and there also exist two positive constants p_d and p_u such that

$$p_d V_1^{\zeta_2/\zeta_1} \le V_2 \le p_u V_1^{\zeta_2/\zeta_1} \tag{A3}$$

From (A3), it is easy to understand that the originally incomparable V_1 and V_2 are adapted to be comparable by simply raising the base V_1 to the power of ζ_2/ζ_1. An intuitive explanation is that the homogeneous degree of V_1 is lifted to V_2, which is exactly the homogeneous degree of V_2. Moreover, when touching on the homogeneous degree of derivative operations, according to the documentation from [31], $\partial V/\partial x_m$ is homogeneous of degree $\zeta - r_m$, i.e., $\partial V/\partial x_m \in \mathrm{H}^{\zeta - r_m}$.

Lemma 4 : Young's inequality is given as the following,

$$ab \le \frac{a^p}{p} + \frac{b^q}{q},\ \frac{1}{p} + \frac{1}{q} = 1, \tag{A4}$$

where a and b are nonnegative real numbers. p and q are real numbers greater than 1. Based on (A4), Young's inequality can be equivalently derived as,

$$a^{\alpha} b^{\beta} \le \alpha a + \beta b,\ \alpha + \beta = 1. \tag{A5}$$

Derivations from (8)-(9) to (10)-(11): Moving L_u, L_l, v_{in}^2, v_{in}, v_{C1}, and v_{C2} to the left-hand sides of (8)-(9) gives

$$\begin{cases} d_u = 1 - \frac{v_{in}^2 - u_u L_u}{v_{in} v_{C1}} = \frac{v_{in} v_{C1} - v_{in}^2 + u_u L_u}{v_{in} v_{C1}} \\ d_l = 1 - \frac{v_{in}^2 - u_l L_l}{v_{in} v_{C2}} = \frac{v_{in} v_{C2} - v_{in}^2 + u_l L_l}{v_{in} v_{C2}} \end{cases} \tag{A6}$$

Further manipulations on (A6) result in (10)-(11).

References

[1] W. Yuan, Y. Wang, D. Liu, F. Deng, and Z. Chen, "Efficiency-prioritized droop control strategy of ac microgrid," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2020.

[2] P. Lin, P. Wang, J. Xiao, J. Wang, C. Jin, and Y. Tang, "An integral droop for transient power allocation and output impedance shaping of hybrid energy storage system in dc microgrid," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 6262–6277, July 2018.

[3] Y. Qi, P. Lin, Y. Wang, and Y. Tang, "Two-dimensional impedance-shaping control with enhanced harmonic power sharing for inverter-based microgrids," *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 11 407–11 418, 2019.

[4] Y. Huangfu, S. Zhuo, F. Chen, S. Pang, D. Zhao, and F. Gao, "Robust voltage control of floating interleaved boost converter for fuel cell systems," *IEEE Transactions on Industry Applications*, vol. 54, no. 1, pp. 665–674, Jan 2018.

[5] Po-Wa Lee, Yim-Shu Lee, D. K. W. Cheng, and Xiu-Cheng Liu, "Steady-state analysis of an interleaved boost converter with coupled inductors," *IEEE Transactions on Industrial Electronics*, vol. 47, no. 4, pp. 787–795, Aug 2000.

[6] F. S. Garcia, J. A. Pomilio, and G. Spiazzi, "Modeling and control design of the interleaved double dual boost converter," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 8, pp. 3283–3290, Aug 2013.

[7] S. Choi, V. G. Agelidis, J. Yang, D. Coutellier, and P. Marabeas, "Analysis, design and experimental results of a floating-output interleaved-input boost-derived dc-dc high-gain transformer-less converter," *IET Power Electronics*, vol. 4, no. 1, pp. 168–180, Jan 2011.

[8] M. Su, Z. Liu, Y. Sun, H. Han, and X. Hou, "Stability analysis and stabilization methods of dc microgrid with multiple parallel-connected dc–dc converters loaded by cpls," *IEEE Transactions on Smart Grid*, vol. 9, no. 1, pp. 132–142, Jan 2018.

[9] Z. Liu, M. Su, Y. Sun, W. Yuan, H. Han, and J. Feng, "Existence and stability of equilibrium of dc microgrid with constant power loads," *IEEE Transactions on Power Systems*, vol. 33, no. 6, pp. 6999–7010, Nov 2018.
[10] P. Lin, W. Jiang, P. Tu, C. Jin, C. Zhang, and P. Wang, "Self-disciplined large signal stabilizer design for hybrid energy storage system in renewable dc power systems," *IEEE Transactions on Sustainable Energy*, pp. 1–1, 2019.
[11] W. Yuan, Y. Wang, D. Liu, F. Deng, and Z. Chen, "Impacts of inductor nonlinear characteristic in multi-converter microgrids: Modelling, analysis and mitigation," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2020.
[12] X. Li, X. Wu, Y. Geng, and Q. Zhang, "Existence and stability of equilibrium of dc microgrid with constant power loads," *Journal of Power Electronics*, vol. 13, no. 5, pp. 896–908, 2013.
[13] X. Zhang, X. Ruan, and Q. Zhong, "Improving the stability of cascaded dc/dc converter systems via shaping the input impedance of the load converter with a parallel or series virtual impedance," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 12, pp. 7499–7512, Dec 2015.
[14] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, "Dc microgrids—part i: A review of control strategies and stabilization techniques," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4876–4891, July 2016.
[15] L. Guo, S. Zhang, X. Li, Y. W. Li, C. Wang, and Y. Feng, "Stability analysis and damping enhancement based on frequency-dependent virtual impedance for dc microgrids," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 338–350, Mar 2017.
[16] J. Yu, J. Yu, Y. Wang, Y. Cao, X. Lu, and D. Zhao, "Passivity-based active stabilization for dc microgrid applications," *CSEE Journal of Power and Energy Systems*, vol. 4, no. 1, pp. 29–38, Mar 2018.
[17] J. Zeng, Z. Zhang, and W. Qiao, "An interconnection and damping assignment passivity-based controller for a dc–dc boost converter with a constant power load," *IEEE Transactions on Industry Applications*, vol. 50, no. 4, pp. 2314–2322, July 2014.
[18] M. A. Hassan, E. Li, X. Li, T. Li, C. Duan, and S. Chi, "Adaptive passivity-based control of dc–dc buck power converter with constant power load in dc microgrid systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 2029–2040, Sep 2019.
[19] P. Magne, D. Marx, B. Nahid-Mobarakeh, and S. Pierfederici, "Large-Signal Stabilization of a DC-Link Supplying a Constant Power Load Using a Virtual Capacitor: Impact on the Domain of Attraction," *IEEE Transactions on Industry Applications*, vol. 48, no. 3, pp. 878–887, May 2012.
[20] M. Kabalan, P. Singh, and D. Niebur, "A design and optimization tool for inverter-based microgrids using large-signal nonlinear analysis," *IEEE Transactions on Smart Grid*, vol. 10, no. 4, pp. 4566–4576, July 2019.
[21] H. Kim, S. Kang, G. Seo, P. Jang, and B. Cho, "Large-signal stability analysis of dc power system with shunt active damper," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 10, pp. 6270–6280, Oct 2016.
[22] X. Zhang, D. M. Vilathgamuwa, K. Tseng, B. S. Bhangu, and C. J. Gajanayake, "Power buffer with model predictive control for stability of vehicular power systems with constant power loads," *IEEE Transactions on Power Electronics*, vol. 28, no. 12, pp. 5804–5812, Dec 2013.
[23] P. Lin, C. Zhang, P. Wang, and J. Xiao, "A decentralized composite controller for unified voltage control with global system large-signal stability in dc microgrids," *IEEE Transactions on Smart Grid*, vol. 10, no. 5, pp. 5075–5091, Sep. 2019.
[24] P. Lin, C. Zhang, J. Wang, C. Jin, and P. Wang, "On autonomous large signal stabilization for islanded multi-bus dc microgrids: A uniform nonsmooth control scheme," *IEEE Transactions on Industrial Electronics*, 2019.
[25] D. Peng, M. Huang, J. Li, J. Sun, X. Zha, and C. Wang, "Large-signal stability criterion for parallel-connected dc-dc converters with current source equivalence," *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2019.
[26] A. Ibeas and M. de la Sen, "Exponential stability of simultaneously triangularizable switched systems with explicit calculation of a common lyapunov function," *Applied Mathematics Letters*, vol. 22, no. 10, pp. 1549 – 1555, 2009.
[27] E. Cruz-Zavala, J. A. Moreno, and L. Fridman, "Lyapunov-based design for a class of variable-gain 2nd-sliding controllers with the desired convergence rate," *International Journal of Robust and Nonlinear Control*, vol. 28, no. 17, pp. 5279–5296, 2018.
[28] P. Lin, T. Zhao, B. Wang, Y. Wang, and P. Wang, "A semi-consensus strategy toward multi-functional hybrid energy storage system in dc microgrids," *IEEE Transactions on Energy Conversion*, 2019.
[29] S. Bacha, I. Munteanu, and A. I. Bratcu, *Power Electronic Converters Modeling and Control*, ser. Advanced Textbooks in Control and Signal Processing. London: Springer London, 2014, vol. 454.
[30] A. Levant, "Higher-order sliding modes, differentiation and output-feedback control," *International Journal of Control*, vol. 76, no. 9-10, pp. 924–941, 2003.
[31] C. Zhang, J. Yang, Y. Yan, L. Fridman, and S. Li, "Semi-global finite-time trajectory tracking realization for disturbed nonlinear systems via higher-order sliding modes," *IEEE Transactions on Automatic Control*, 2019.
[32] W. H. Young, "On Classes of Summable Functions and their Fourier Series," *Proceedings of the Royal Society A: Mathematical, Physical and Engineering Sciences*, vol. 87, no. 594, pp. 225–229, aug 1912.
[33] H. K. Khalil and J. W. Grizzle, *Nonlinear systems*. Prentice hall Upper Saddle River, NJ, 2002, vol. 3.
[34] S.-C. Tan, Y.-M. Lai, and C.-K. Tse, *Sliding mode control of switching power converters: techniques and implementation*. CRC press, 2018.
[35] P. Lin, P. Wang, C. Jin, J. Xiao, X. Li, F. Guo, and C. Zhang, "A distributed power management strategy for multi-paralleled bidirectional interlinking converters in hybrid ac/dc microgrids," *IEEE Transactions on Smart Grid*, vol. 10, no. 5, pp. 5696–5711, Sep. 2019.

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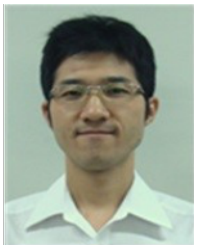

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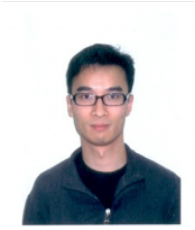

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