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ZVZCS Full-Bridge (FB) Three-Level DC/DC (TLDC) Converter with Reduced Device Count

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***Abstract*—This paper proposes a new zero-voltage and zero-current switching (ZVZCS) full-bridge (FB) three-level DC/DC converter (TLDC) with the reduced device count (RDC). The merits of the proposed converter with the corresponding modulation strategy are concluded as follows. In comparison with the zero-voltage-switching (ZVS) FB TLDC, 1) only one blocking capacitor is added to realize the ZVZCS strategy, 2) the primary circulating current and duty cycle loss can be effectively reduced. Also, the wide input voltage range can be satisfied because of having two working patterns. More significantly, the proposed converter with the corresponding modulation strategy can reduce the device count by removing the primary blocking diodes in comparison with other ZVZCS FB TLDCs, which would reduce the conduction losses of primary power devices and thus increase the converter's efficiency. Finally, experimental results are presented to verify the proposed converter with the corresponding modulation strategy.**

***Index Terms*—Full-bridge (FB), three-level DC/DC converter (TLDC), wide input voltage range, reduced device count (RDC), zero-voltage and zero-current switching (ZVZCS).**

I. Introduction

The three-level (TL) DC/DC converter (TLDC) is one of the most attractive candidates for the high voltage applications because the voltage stress on the primary power switches is only half of the input voltage (V_{in}/2) in the TLDC [1-3]. So far, many studies about the TLDC have been carried out. A novel four-switch TLDC with a compact circuit structure was proposed in [4]. Based on [4], new input-parallel output-parallel TLDCs with minimized and balanced currents on input capacitors were proposed in [5] and several new TLDCs were proposed in [6] with the major merits of extended zero-voltage-switching (ZVS) range and compact circuit structure for the industrial applications. Besides, the full-bridge (FB) TLDC with a balanced power device current based modulation strategy was proposed in [7].

The TLDCs mentioned above can all obtain ZVS, but they have some drawbacks including high duty cycle loss, high circulating current, and limited soft switching range. To solve these problems, some new TLDCs with zero-voltage and zero-current switching (ZVZCS) were proposed [8-13]. In [8], a ZVZCS half-bridge (HB) TLDC with a secondary active clamp circuit and a simple phase-shift control was proposed. Several ZVZCS TLDCs with simple circuit structures by removing clamping diodes were proposed in [6]. In [6], a phase-shift control is applied to these proposed ZVZCS TLDCs. In addition, reference [9] proposed a hybrid ZVZCS HB TLDC with two transformers and the resonant tank, in which the duty ratio control is used to adjust the output voltage. A new ZVZCS HB TLDC with a wide soft switching range and a compact structure was proposed in [10]. However, the HB converter is normally not suitable for higher power applications because of the high current stress on the primary power devices in comparison with the FB converter. A ZVZCS dual bridge TLDC with phase-shift control was proposed in [11], in which two four-switch ZVZCS HB TLDCs are connected in parallel. Besides, a hybrid ZVZCS FB TLDC with duty ratio control and a ZVZCS FB TLDC with phase-shift control were proposed in [12] and [13], respectively, for high power applications. Unfortunately, these ZVZCS FB TLDCs all need to add the blocking diodes for resetting the primary current and realizing zero-current-switching (ZCS), which would thus cause extra power losses. Consequently, it is still a valuable work to design a ZVZCS FB TLDC with a lower device count and higher efficiency.

In this paper, a new ZVZCS FB TLDC with the corresponding modulation strategy is proposed, which maintains the merits of the ZVZCS TLDC that reducing the primary circulating current and duty cycle loss. More significantly, compared with other ZVZCS FB TLDCs, the proposed converter can not only satisfy the wide input voltage range but also reduce conduction losses of the primary power devices due to the reduced device count (RDC) by removing the blocking diodes. The circuit structure, operation principles, and performances of the proposed converter are discussed. Finally, experimental results are presented to verify the proposed converter with the corresponding modulation strategy. The proposed converter can be applied to many industrial applications with the high input voltage, such as step-down stage DC/DC converter after 3ϕ power factor correction and

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DC interfaces for microgrids.

II. Circuit Structure and Operation Principle

Fig. 1 shows the circuit structure of the proposed converter. It needs to be mentioned that: in comparison with the conventional ZVS FB TLDC in [7], the proposed converter adds one more blocking capacitor C_b as marked in Fig. 1 and thus have a little more complex circuit structure. However, the proposed converter belongs to the ZVZCS converter, which means that it can solve the drawbacks of the conventional ZVS converter including the high duty cycle loss and high circulating current.

In Fig. 1, C_{i1} and C_{i2} are two input capacitors which split the input voltage V_{in} into two voltages (V_1 and V_2); S_1 - S_8 are primary power switches; D_1 - D_8 are body diodes of S_1 - S_8; C_1 - C_8 are parasitic capacitors of S_1 - S_8; C_{s1} and C_{s2} are two flying capacitors; D_9 - D_{12} are four clamping diodes; T_r is the isolation transformer; L_r is the leakage inductance of T_r; n is the turns ratio of T_r; D_{r1} - D_{r4} are output rectifier diodes; L_o and C_o are output filter inductor and capacitor, respectively. In addition, V_{in} is the input voltage; V_{ab} is the voltage between point a and b; i_p is the primary current of T_r; V_{cb} is the voltage on C_b; i_{Lo} is the current on L_o; V_o and I_o are the output voltage and current.

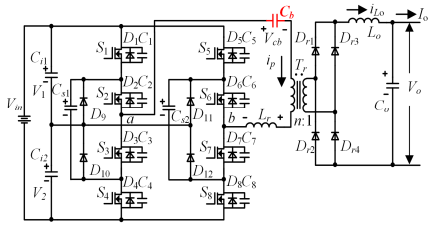
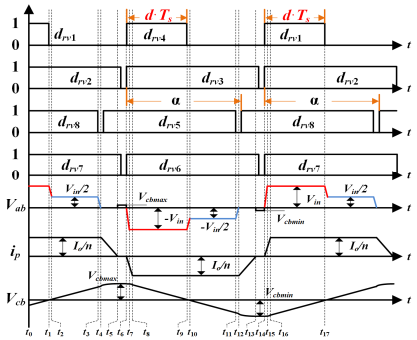


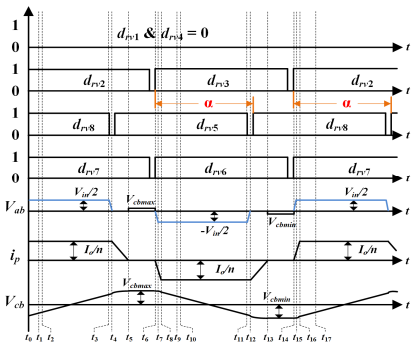
Fig. 1. Circuit Structure of proposed converter.

To simplify the following analysis, several assumptions are made as 1) all power switches and diodes are ideal; 2) C_{i1}, C_{i2} and C_{s1}, C_{s2} are large enough to be considered as the voltage sources with $V_{in}/2$; and 3) L_o is large enough to be considered as a constant current source.

Fig. 2 shows the proposed modulation strategy with converter's key waveforms, in which $d_{rv1} - d_{rv8}$ are the driving signals of S_1 - S_8; d is the duty ratio in one switching period T_s; α is the phase-shift time. The proposed modulation strategy is composed of two working patterns, which can thus satisfy the wide input voltage range.



(a)



(b)

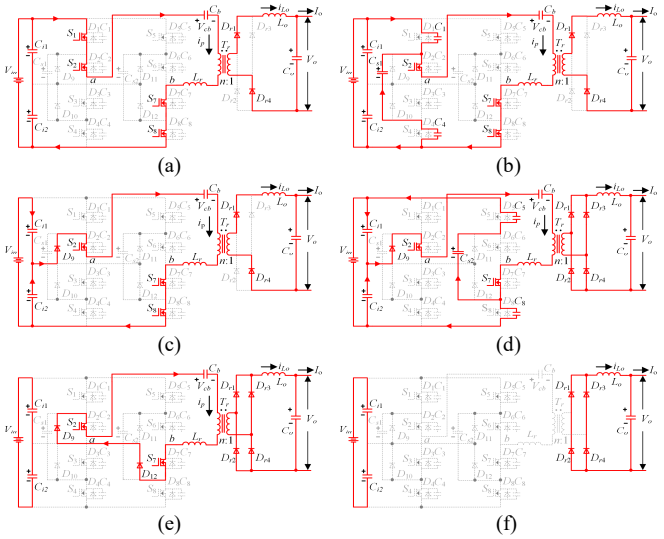
Fig. 2. Proposed corresponding modulation strategy. (a) Working pattern I. (b) Working pattern II.

*1) **Working pattern I*** is used for the low input voltage. In the working pattern I, α is kept at a constant value. By adjusting the value of the duty ratio d, the time length of the third-level voltages (V_{in} and $-V_{in}$) as marked by the red color in Fig. 2(a) can be changed, which would thus change the output voltage V_o. In practical applications, the duty cycle 0.5 minus the dead time divided by T_s is set for driving signals of power switches S_2, S_3, S_5, S_6, S_7, and S_8; the duty ratio d would be obtained by the calculation from the control loop and is set for driving signals of power switches S_1 and S_4.

*2) **Working pattern II*** is used for the high input voltage after the duty ratio d reduces to zero with the increasing of the input voltage. By adjusting the value of the phase-shift time α, the time length of the second-level voltages ($V_{in}/2$ and $-V_{in}/2$) as marked by the blue color in Fig. 2(b) can be changed, which would thus change the output voltage V_o. In practical applications, the duty ratio of d_{rv1} and d_{rv4} are set at zero; the duty cycle 0.5 minus the dead time divided by T_s is set for driving signals of power switches S_2, S_3, S_5, S_6, S_7, and S_8; the phase-shift time α would be obtained by the calculation from the control loop.

Fig. 3 presents equivalent circuits during the time period [t_0 - t_9] in the working pattern I shown in Fig. 2(a).

Stage 1 [$t_0 - t_1$]: During this stage, S_1, S_2, S_7, and S_8 are all in on-state, so V_{ab} equals to V_{in} and the input power transfers to the load through D_{r1} and D_{r4}. The primary current i_p is I_o/n and V_{cb} increases with the change rate given as (1).



(a) (b) (c) (d) (e) (f)

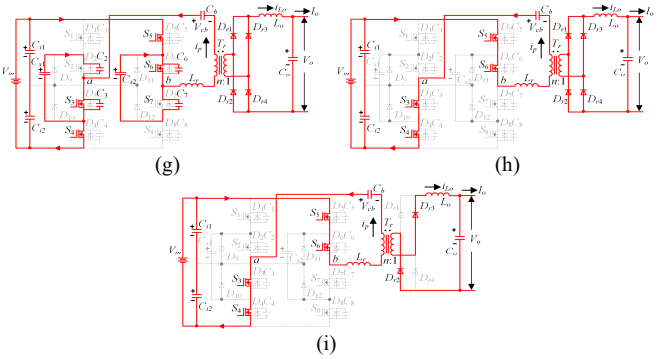


Fig. 3. Equivalent circuits in working pattern I. (a) [t_0-t_1]. (b) [t_1-t_2]. (c) [t_2-t_3]. (d) [t_3-t_4]. (e) [t_4-t_5]. (f) [t_5-t_6]. (g) [t_6-t_7]. (h) [t_7-t_8]. (i) [t_8-t_9].

$$\frac{dV_{cb}}{dt} = \frac{I_o}{n \cdot C_b} \tag{1}$$

Stage 2 [$t_1 - t_2$]: At t_1, S_1 is turned off, C_1 and C_4 start to be charged and discharged, respectively.

Stage 3 [$t_2 - t_3$]: At t_2, the voltage on C_4 decreases to 0 V and the voltage on C_1 increases to $V_{in}/2$. Therefore, D_9 conducts, which clamps the voltage on C_4 at 0 V. During this stage, V_{ab} is equal to $V_{in}/2$ and i_p remains I_o/n.

Stage 4 [$t_3 - t_4$]: At t_3, S_8 is turned off. C_5 and C_8 start to be discharged and charged. i_p is not enough to provide the output current I_o and starts to decrease. Accordingly, D_{r1}, D_{r2}, D_{r3}, and D_{r4} would conduct simultaneously, which clamps both the primary and secondary voltage of the transformer at 0 V.

Stage 5 [$t_4 - t_5$]: At t_4, the voltage on C_5 decreases to 0 V and the voltage on C_8 increases to $V_{in}/2$. Therefore, D_{12} conducts and clamps the voltage on C_5 at 0 V, which means S_5 can be turned on with ZVS. During this stage, the voltage on L_r is $-V_{cb}$, so i_p decreases with the change rate given as (2). The time period [$t_4 - t_5$] can be obtained by (3) approximately.

$$\frac{di_p}{dt} = -\frac{V_{cb}}{L_r} \tag{2}$$

$$t_5 - t_4 \approx \frac{L_r \cdot I_o}{n \cdot V_{cb\_max}} \tag{3}$$

Stage 6 [$t_5 - t_6$]: At t_5, the primary current i_p decreases to 0 A. Therefore, S_2 and S_7 can be turned off with ZCS during this stage.

Stage 7 [$t_6 - t_7$]: At t_6, S_3 S_4, S_6 are all turned on. S_4 can be turned on with ZVS. Then, C_3, C_6 are discharged and C_2, C_7 are charged. The primary current i_p starts to decrease.

Stage 8 [$t_7 - t_8$]: At t_7, the voltage of C_3, C_6 decrease to 0 V and the voltage of C_2, C_7 increase to $V_{in}/2$. During this stage, the primary current i_p decreases rapidly with the change rate given as (4).

$$\frac{di_p}{dt} = -\left(\frac{V_{in} + V_{cb}}{L_r}\right) \tag{4}$$

Stage 9 [$t_8 - t_9$]: At t_8, the primary current i_p decreases to the negative reflected output current $-I_o/n$. Then, D_{r1}, D_{r4} become off-state, the input power is transferred to the load through D_{r2}, D_{r3}.

At t_9, S_4 is turned off. The second half cycle [$t_9 - t_{17}$] starts. The analysis during [$t_9 - t_{17}$] is similar to that during [$t_1 - t_9$], which is not repeated here. The equivalent circuits and related analysis of the working pattern II are similar to that in the working pattern I as above, which is not repeated here.

III. Brief Discussion

A. Selection of Blocking Capacitor

The selection of the blocking capacitor is mainly decided by the primary current reset time and the leakage inductance of the transformer. According to the required maximum reset time named T_{reset_max}, the needed capacitance of the blocking capacitor can be approximately obtained by (5) if the energy stored in the blocking capacitor is much higher than the energy stored in the leakage inductance.

$$C_b < \frac{\alpha \cdot T_{reset\_max}}{2 \cdot L_r} \tag{5}$$

From equation (5), it can be also observed that the reset time is positively proportional to the transformer's leakage inductance and the blocking capacitor's capacitance. However, it needs to be mentioned that the voltage stress on the blocking capacitor is negatively proportional to the blocking capacitor's capacitance.

B. Soft Switching Performances

For the inner power switches S_2, S_3, S_6, S_7: 1) S_2, S_3, S_6, S_7 can be turned off after i_p is reset to 0 A. Therefore, with the proper design, S_2, S_3, S_6, S_7 can realize ZCS turn-off in a wide load range. 2) When S_2, S_3, S_6, and S_7 are turned on, the leakage inductance of the transformer L_r limits the change rate of i_p from 0 A, which would thus reduce the turn-on losses. However, the energy stored in the parasitic capacitors of S_2, S_3, S_6, S_7 would lose at the turn-on.

For the outer power switches S_1, S_4, S_5, S_8: 1) The maximum voltage on S_1, S_4 at the turn-on are $2*V_{cb}$ and V_{cb} is relatively small in comparison with $V_{in}/2$, so the switch-on loss of S_1, S_4 would be small and it can be said that S_1, S_4 can realize the virtual ZVS turn-on in a wide load range. 2) S_5, S_8 can also realize the ZVS turn-on. Although S_5, S_8 would lose the ZVS turn-on at the light load, only the energy stored in the parasitic capacitors of S_5 and S_8 would lose at the turn-on because the primary current i_p is reset to 0 A. 3) S_1, S_4, S_5, S_8 are turned off at the hard switching.

Table I presents a theoretical comparison of the ZVS range between other ZVZCS FB TLDCs and the proposed converter.

TABLE I. Comparison of ZVS Range

Item		Hybrid ZVZCS FB TLDC [12]	Conventional ZVZCS FB TLDC [13]	Proposed converter
ZVS Range	$I_o \geq$	$n \cdot V_{in} \cdot \sqrt{\frac{C_j}{2 \cdot L_r}}$	$n \cdot V_{in} \cdot \sqrt{\frac{C_j}{L_r}}$	$n \cdot V_{in} \cdot \sqrt{\frac{C_j}{2 \cdot L_r}}$

Note: C_j is the capacitance of the parasitic capacitors of low-voltage power switches.

C. Comparison with Other ZVZCS TLDCs

(1) Comparison of device counts of main primary power

devices

Table II presents comparison results about device counts of the main primary power devices between other ZVZCS TLDCs and the proposed converter. From Table II, the following points can be observed. 1) Although the hybrid ZVZCS FB TLDC has the lowest device count of main primary power devices, it needs two power switches with high voltage stress (V_{in}) as marked in Table II. The primary power switches in the conventional ZVZCS FB TLDC and proposed converter only needs to withstand half of the input voltage (V_{in}/2). 2) More importantly, by removing the blocking diodes, the proposed converter reduces the device count of primary power devices as marked in Table II and thus has a more compact circuit structure.

(2) Comparison of conduction power losses of primary power devices

Fig. 4 presents the equivalent circuits when resetting the primary current to 0 A in the positive side.

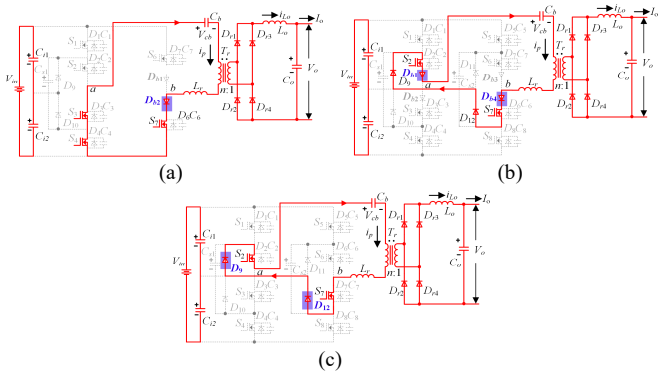


Fig. 4. Equivalent circuits during i_p reset. (a) Hybrid ZVZCS FB TLDC. (b) Conventional ZVZCS FB TLDC. (c) Proposed ZVZCS FB TLDC.

From Fig. 4, the following points can be observed. 1) In other ZVZCS FB TLDCs as highlighted in Figs. 4(a) and 4(b), the blocking diodes in series with the primary main power switches need to be added to reset the primary current, which would cause extra conduction losses because the primary current i_p would also go through these blocking diodes. However, 2) there is no need to add blocking diodes in the proposed converter with the corresponding modulation strategy because the clamping diodes can be also used as the blocking diodes as highlighted in Fig. 4(c). Therefore, the proposed converter can effectively reduce the conduction losses due to reduced device count and thus increase the converter's efficiency in comparison with other ZVZCS FB TLDCs.

Fig. 5 presents comparison results about calculated conduction losses of the main primary power devices based on the circuit parameters listed in Table II.

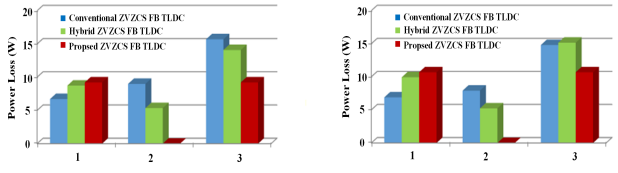


Fig. 5. Comparison results of calculated conduction losses of main primary power devices (V_o = 50 V, P_o = 1 kW). (a) V_{in} = 300 V. (b) V_{in} = 450 V.
Note: 1. Conduction losses of primary power switches and clamping diodes. 2. Conduction losses of blocking diodes. 3. Total conductions losses of main primary power devices (1+2).

IV. Experimental Verification

A 1 kW prototype of the proposed converter is established, whose circuit parameters are listed in Table III. Fig. 6 presents the photo of the experimental set-up and hardware of the proposed converter.

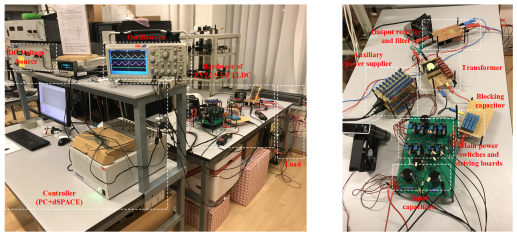


Fig. 6. (a) Experimental set-up. (b) Hardware of proposed converter.

Fig. 7 presents the diagram about the implementation of the proposed modulation strategy, in which the conventional proportional-integral PI control algorithm is utilized to calculate the duty ratio d and phase-shift time α. As shown in Fig. 7, the working pattern I is used for the low input voltage by adjusting the duty ration d from maximum value d_{max} to 0; when d decreases to 0 due to the increase of the input voltage, the working pattern II would be used for the higher input voltage by adjusting the phase-shift time α.

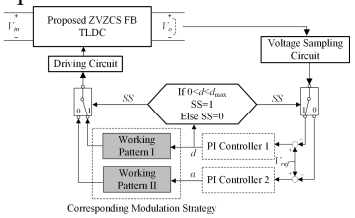
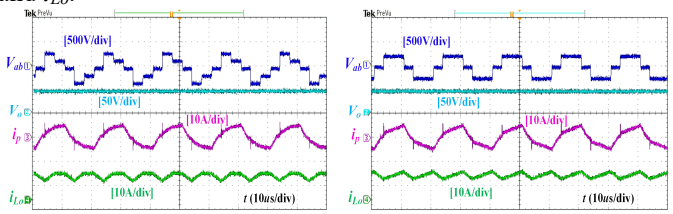


Fig. 7. Diagram about implementation of proposed modulation strategy.

TABLE II. Comparison Results of Device Counts

Item		Device Count of Half-bridge Structure		Device Count of Full-bridge Structure			
		Hybrid Resonant ZVZCS TLDC [9]	HB ZVZCS TLDC [10]	ZVZCS Dual Bridge TLDC [11]	Hybrid ZVZCS FB TLDC [12]	Conventional ZVZCS FB TLDC [13]	Proposed Converter
Power switch	V_{in}	**0**	**0**	**0**	**2**	**0**	**0**
	V_{in}/2	4	4	8	4	8	8
Blocking diode or switch		**2**	**2**	**4**	**2**	**4**	**0**
Clamping diode		2	0	0	2	4	4
Blocking capacitor		1	1	2	1	1	1
Flying capacitor		1	0	0	1	2	2
Transformer		2	1	2	1	1	1
Total device counts		**12**	**8**	**16**	**13**	**20**	**16**

Fig. 8 presents the experimental results including V_{ab}, V_o, i_p, and i_{Lo}.

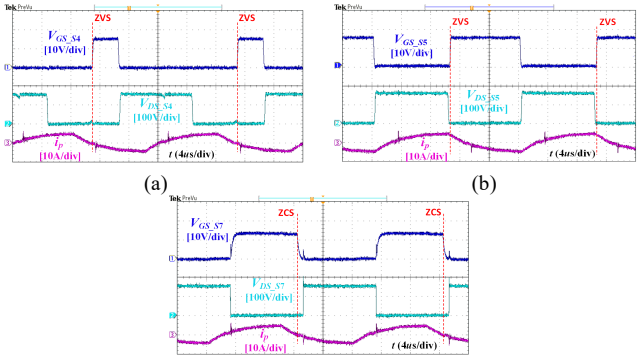


(a) (b)

Fig. 8. Experimental results including V_{ab}, V_o, i_p, and i_{Lo} (V_o = 50 V, P_o = 500 W). (a) Working pattern I (V_{in} = 300 V). (b) Working pattern II (V_{in} = 450 V).

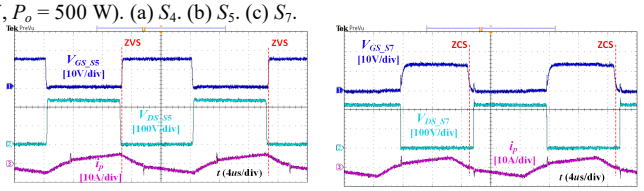
From Fig. 8, it can be observed that the primary current i_p can be reset to zero with no blocking diode in both two working patterns, which would thus reduce the primary circulating current and power losses.

Figs. 9 - 10 present soft switching performances in the working pattern I and II, respectively. In Figs 9 - 10, V_{GS_S4}, V_{GS_S5}, and V_{GS_S7} are driving signals of S_4, S_5, and S_7; V_{DS_S4}, V_{DS_S5}, and V_{DS_S7} are drain-source voltages of S_4, S_5, and S_7. From Figs. 9 - 10, it can be observed that: 1) S_4 can realize the virtual ZVS turn-on; 2) S_5 can realize the ZVS turn-on; 3) S_7 can realize the ZCS turn-off.



(a) (b) (c)

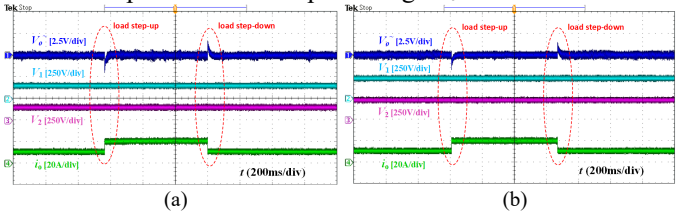
Fig. 9. Soft switching performances in working pattern I (V_{in} = 300 V, V_o = 50 V, P_o = 500 W). (a) S_4. (b) S_5. (c) S_7.



(a) (b)

Fig. 10. Soft switching performances in working pattern II (V_{in} = 450 V, V_o = 50 V, P_o = 500 W). (a) S_5. (b) S_7.

Fig. 11 presents the experimental results about transition performances of the proposed converter, which includes the input voltage (V_{in}), voltages on the two input capacitors (V_1, V_2), and ac component of the output voltage V_o~.



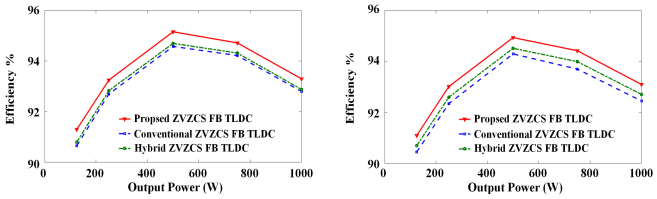
(a) (b)

Fig. 11. Experimental results about transition performances of proposed converter. (a) V_{in} = 300 V. (b) V_{in} = 450 V.

In Fig. 11, the output power steps up from 500 W to 1 kW and is finally set back to 500 W when the output voltage V_o is 50 V. From Fig. 11, it can be observed that 1) the voltages among the two input capacitors are balanced and 2) there is no abnormal voltage spike on the two input capacitors during the transitions.

Fig. 12 presents comparison results about efficiency curves among ZVZCS FB TLDCs. The related circuits parameters are listed in Table II. From Fig. 12, it can be concluded that the proposed converter with the corresponding strategy can effectively increase the efficiencies due to removing the blocking diodes in comparison with other ZVZCS FB TLDCs.

It needs to be mentioned that: 1) in order to further improve the efficiency of the proposed converter, the output rectifier diodes can be replaced by Si or even GaN power switches for the synchronous rectification when the input voltage is much higher than the output voltage and the input current is much lower than the output current; 2) SiC Schottky diode with higher rating voltage can be used when the input voltage is high.



(a) (b)

Fig. 12. Efficiency results (V_o = 50 V). (a) V_{in} = 300 V. (b) V_{in} = 450 V.

V. Conclusion

In this paper, a new zero-voltage and zero-current switching (ZVZCS) full-bridge (FB) three-level DC/DC converter (TLDC) with the RDC is proposed. The merits of the proposed converter with the corresponding modulation strategy include: 1) realizing the ZVZCS for the power switches; 2) reducing the primary circulating current and duty cycle loss in comparison with conventional ZVS FB TLDCs; 3) satisfying the wide input voltage range because of having two working patterns; and 4) having a more compact circuit structure by removing the primary blocking diodes, which would reduce conduction losses of the primary power devices and increase the converter's efficiency, in comparison with other ZVZCS FB TLDCs. Finally, the proposed converter with the corresponding modulation strategy is verified by the experimental results. It needs to be mentioned that the main disadvantages of the proposed converter are 1) high voltage stress on the output rectifier diodes; and 2) hard switching-on for the power switches S_2, S_3, S_6, and S_7.

Appendix

TABLE III. Main Circuit Parameters

Item		Hybrid ZVZCS FB TLDC [12]	ZVZCS FB TLDC [13]	Proposed converter
Power switches (voltage stress)	V_{in}	IPW90R120C3	/	/
	V_{in}/2	IPW65R045C7		
Blocking diodes		IDP30E60		/
Clamping diodes		IDP30E60		
Blocking capacitor (uF)		1		
Turns ratios of T_r		25/8		
Output rectifier diodes		FFA40UP35S		

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